Fossum insulted in his 2014 paper Sony and Hagiwara 1975 PPD invention.

Indeed, Hagiwara invented PPD with VOD and the virtual charge transfer in 1975 !!

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Sony HAD (PPD+VOD) does not use LOCOS !!!

A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

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False

Many people now said this is a fake paper !

C. Other Contributions to the PPD Invention

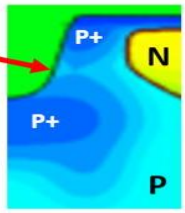
The PPD structure, while invented for low lag ILT CCD application, shares a strong resemblance to the Hynecek virtual-phase CCD structure, with the exception of the VOD. The two inventions were solving different problems with essentially the same device structure and operating principles.

In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a *pnp* vertical structure was disclosed, among several structures [24]. The top *p* layer was connected by metal to a bias used to control full-well capacity and the *n*-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1996, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called "Hole Accumulation Diode," or HAD structure [25]. However, the 1975 application did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the NEC paper was published. However, the "narrow-gate" CCD with an open *p*-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

The PPD, as it is most commonly used today, bears the strongest resemblance to the Teranishi et al. ILT CCD device. Thus, these days Teranishi is considered as the primary inventor of the modern PPD [29].

False

The surface P+ layer is NOT connected to the LOCOS P+ layer. The surface P+ layer may be floating and this photodiode may have serious image lag.



Serious Image Lag ?

NOT connected

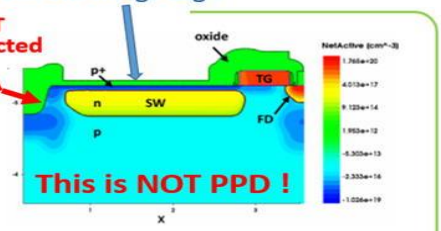


Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

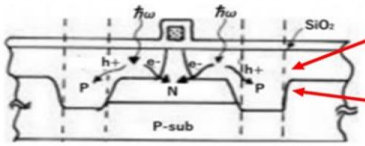
Hagiwara in 1975 invented PPD with VOD and the virtual charge transfer.
Study the Japanese Patents 1975-127646, 1975-127647 and 1975-134985.

True Historv of Photodiode

First Pinned Photodiode was invented by Hagiwara in 1975 and reported at SSDM1978 by Sony.

Sony never used LOCOS isolation nor Shallow Trench Isolation. Both suffer the yield problem of Dark Current and White Defects. Instead, Sony used high energy ion implantation to form the adjacent heavily doped P+ channel stops region with the Lamp Anneal Technology invented by Kazuo Nishiyama at Sony.

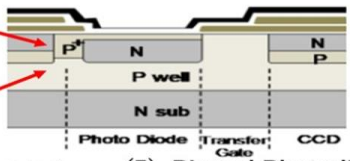
(1) The first Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation invented and reported at SSDM1978 by Hagiwara.



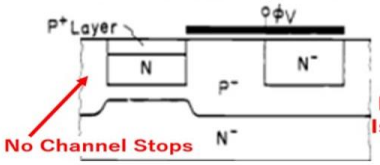
No LOCOS Isolation

No Shallow Trench Isolation

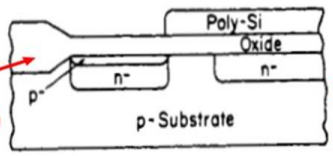
(2) Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation as explained by ssis.or.jp in the official Semiconductor History Museum WEB site.



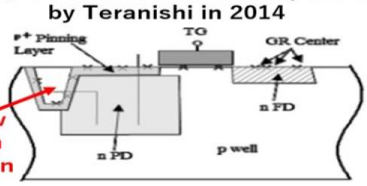
(3) Buried Photodiode reported at IEDM1982 by NEC



(4) Pinned Photodiode reported at IEDM1984 by KODAK



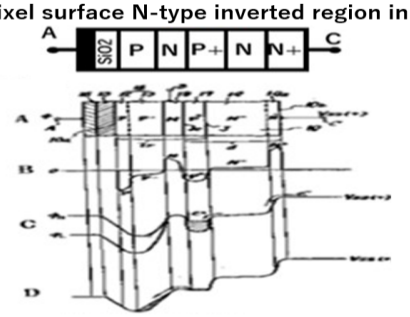
(5) Pinned Photodiode reported by Teranishi in 2014



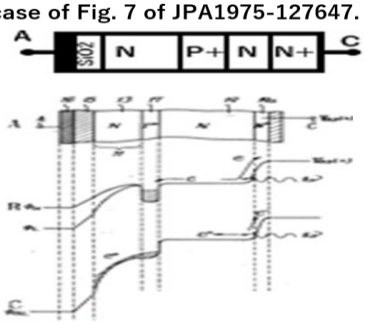
Sony Pinned Photodiode has the adjacent P+ heavily doped channel stops always directly grounded to the metal wire at the surface since 1978. Sony never used LOCOS isolation nor Shallow Trench Isolation.

Who invented Electric Shutter ?

Hagiwara at Sony invented Electric Shutter in October 23, 1975. The evidence is give and explained in Fig. 7 of the Japanese patent application, JPA1975-127646, in which the first Electric Shutter function was defined. The photo charge is transferred and drained to the in-pixel buried channel type vertical overflow drain (VOD) region, which is defined as the buried channel region of the buried channel type CCD/MOS buffer memory capacitor. The three-voltage-level clocking scheme (Clock C and D) of the first Electric Shutter Function mode was defined in Fig. 7 of JPA1975-127646, using the strong punch-thru action mode between the buried P type photo charge storage region and the P-type in-pixel vertical overflow drain (VOD) region. The strong draining gate clock D voltage as shown by creates the very deep potential well in the in-pixel P-type buried vertical overflow drain (VOD) region in case of Fig. 7 of JPA1975-127646 while the strong draining gate clock C voltage creates the very deep potential well in the in-pixel surface N-type inverted region in case of Fig. 7 of JPA1975-127647.



JPA1975-127646 Fig. 7



JPA1975-127647 Fig. 7

Hagiwara at Sony invented in 1975 the first Electric Shutter Function.

To achieve the complete Electric Shutter function, the surface of the photodiode must be pinned and fixed by the external constant voltage with the zero resistance.

The first Pinned Photodiode was invented by Hagiwara in 1975 to achieve the electric shutter function.