Dr. Yoshiaki Daimon Hagiwara Sept 25, 2021

BIOGRAPHY:

Hagiwara graduated Caltech with BS71 with honor, MS1972 and PhD1975. He joined Sony in 1975 and was engaged first in the early development of image sensors. Meanwhile, he was serving as a visiting professor in the electrical department and the applied physics at Caltech from 1998 to 1999. He was a visiting professor in the electrical department at Gunma University at Kiryu Japan from 2003 till 2006.

While working for Sony from 1975 to 2008, he was engaged in the early developments of image sensor and the digital camera chip set including the ADC, DRAM and high-speed Cache SRAM buffer memory chips and micro controller chips. Before retiring from Sony, he was engaged in the PS2 and PS3 chip set developments. He was invited to talk at CCD'79, ECS1980, ESSCIRC200, ESSICRC2008 and ISSCC2013 for his works at Sony from 1975 till 2008. Since 2009 till 2017, he taught graduate and undergraduate students as a full professor of the information science department at Sojo University.

In 1992 he also served as a member of JEDEC memory standardization committee and also as the IEC TC47 technical committee chair of the international standard committee (IEC). He also served as the international program chair and an operational committee member in IEEE EDS sponsored ICMTS conferences, IEEE ISSCC conferences for which he served as the ISSCC Asian Committee chair and also as the ISSCC international technical program (ITC) chair in series. He was also a member of the PC and OC and now advisory committee members of IEEE Cool Chips conferences in series. In 2008 he founded and worked as the president in the artificial intelligent partner system laboratory (AIPLAB consortium), a nonprofit research organization (NPO) registered by Kanagawa prefecture government in Japan in 2008. He is now completely retired but he is still serving as an operational committee member of the department of education in Society of Semiconductor Industry Specialists (ssis.or.jp).

Description of the main contributions:

Yoshiaki Daimon Hagiwara published his PhD work on the charge transfer of the buried channel CCD.at ISSCC1974 conference and after receiving PhD from Caltech and he joined Sony and was engaged in the early developments of image sensor. His important contributions to the image sensor world can also be evidenced by his 1975 inventions defined in his three Japanese patents JPA 1975-127646, JPA 1975-127647 and JPA 1975-134985 on the dynamic photo transistor structure now used widely. His 1975 invention (JPA1975-134985) on the new pnp and pnpn multi junction type dynamic photo transistor structures with the vertical overflow drain (VOD) function became later the basis of Pinned Photodiode and Hole Accumulation Diode (HAD).

His 1975 invention (JPA1975-127646 and JPA127647) of the back light illumination mode p+pnp dynamic photo transistor has the unique surface hole accumulation p+p barrier potential enhancing the short wave blue light sensitivity and in-pixel buffer memory for the global shutter operation which is now suitable for modern 3D multichip CMOS image sensor integration.

Hagiwara reported at SSDM1978 conference for the first time in the world the P+NP junction type photo transistor. The next year, he was invited and talked in the CCD79 conference in Edinburgh, Scotland UK and then in 1980 at the Electrochemical Society conference (ECS1980) at St. Luis, USA for his work.

And then he developed the digital camera chip set including ADC, DRAM and high-speed Cache SRAM buffer memory and micro controller chips. He then was engaged in the AIBO, PS2 and PS3 chip set developments. He was invited to talk at CCD'79, ECS1980, ESSCIRC200, ESSICRC2008 and ISSCC2013 for his achievements.

His life-long efforts were developing the various supporting consumer semiconductor chips, including ADC, DRAM, Cache SRAM and MCU controller chip set and PS2 and PS3 SOI cell processor to make AI vision chips.

His 1977 patent invention (JPA1977-1278885) of the all-solid state electronic shutter function of the Pinned Photodiode with the VOD function was the initiator for SONY, KODAK and many companies to develop all solid-state electronic eye with no mechanical parts which led our life style into a new era of the digital image sensing world of AI IoT Robotics and self-driving cars.

In 1992 he also served as a member of JEDEC memory standardization committee and also as the IEC TC47 technical committee chair of the international standard committee (IEC).

He also served as the international program chair and an operational committee member in IEEE EDS sponsored ICMTS conferences, IEEE ISSCC
conferences for which he served as the ISSCC Asian Committee chair and also as the ISSCC international technical program (ITC) chair in series. He was also a member of the PC and OC and now advisory committee members of IEEE Cool Chips conferences in series.

At Sojo University as a full professor of the information science department since 2009 till 2017, Prof. Hagiwara taught the various courses such as Engineering Mathematics, Numerical Computational Method, Semiconductor Device Physics, Digital Circuit and System Design and Artificial Intelligent Robotics.

He wrote a book entitled as "The world of Digital Circuits" for the Intelligent Partner System (AIPS) applications in 2016 which summarizes the most of the scopes of his class materials focused to the physics of semiconductor and AI LSI chip designs. He was also coauthor of the book titled as "Computer Engineering Handbook", CRC Press, in December 2003.

His most important contribution to the world is his 1975 inventions and his 1978 development efforts on the new image sensor structures, later called as Pinned Photodiode or Sony Hole Accumulation Diode (HAD), that initiated as a trigger for Sony, Kodak and other companies to develop all solid state, film free and high definition digital camera which transformed the world from the old analog world of the film camera life style to the digital information and communication world, that is, from the analog life style to the all solid state, semiconductor AI LSI chip, digital life style.

He is Caltech Distinguished Alumni and IEEE Life Fellow

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Yoshiaki Hagiwara wrote a book on "The World of Artificial Intelligent Digital Circuits", which is important and needed to build the intelligent image sensor systems. If you are interested in purchasing this book, please visit

https://www.seizansha.co.jp/ISBN/ISBN978-4-88359-339-2.html

https://www.seizansha.co.jp/

ISBM978-4-88359-339-2 ; Hard Cover, 460 page,¥ 9000 Japanese Yen + tax

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https://www.seizansha.co.jp/ISBN/ISBN978-4-88359-339-2.html

https://www.seizansha.co.jp/

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Publication List:

(1) April 1973

"The Influence of Interface States on Incomplete Charge Transfer

in Overlapping Gate Charge Coupled Devices"

IEEE Journal of Solid-State Circuits,

Vol. SC 8, No.2, April 1973

(2) February 1974

"Charge Transfer of Buried Channel Charge Coupled Devices"

Proceeding of International Solid State Circuit Conference

(ISSCC1974), San Francisco, February 1974.

(3) April 1974

"Final Stage of the Charge Transfer Process in Charge Coupled Devices"

IEEE Transactions on Electron Devices, Vol. ED-21, No.4, April 1974

(4) June 1975

Caltech_1975_PhD_Thesis_by_Yoshiaki_Daimon_Hagihara.pdf

in Electrical Engineering (major) and Physics(minor), June 1975,

California Institute of Technology, Pasadena, California USA.

(5) October 23,1975

Japanese Patent Application JPA1975-127646

on "Back-light Triple Junction Type Pinned Buried Photodiode

with Complete Charge Transfer Capability

and Global Shutter Function", Japanese Patent Application

written in Japanese, filed on Oct 23, 1975

(6) October 23,1975

Japanese Patent Application JPA1975-127647

on "Back-light Double Junction Type Pinned Buried Photodiode

with Complete Charge Transfer Capability and

Global Shutter Function", Japanese Patent Application

written in Japanese, filed on Oct 23, 1975

(7) November 10 1975

Japanese Patent Application JPA1975-134985

on "Triple Junction Type Pinned Buried Photodiode

with Complete Charge Transfer Capability and

Vertical Overflow Drain Function", Japanese Patent

Application written in Japanese, filed on Nov 10, 1975.

(8) September 1976

"128-Bit Multi Comparator"

IEEE Journal of Solid-State Circuits, VOL.SC11, No.4, October 1976

(9) September 1977

P1977_Narrow_Cahnnel_Transfer_Gate_CCD_SSDM1977_Paper_

by_Hagiwara.pdf" Proceeding of the 9th Conference

on Solid State Devices, Tokyo, September 1977

(10) September 1977

Japanese Patent Application JPA1977-126885

on "Electric Shutter Clocking and Gamma Control Scheme

using Overflow Drain (OFD) controlled

by Strong Punch Thru OFD Voltage Control",

Japanese Patent Application written in Japanese,

filed on Sep 29, 1977

(11) September 1978

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Proceeding of the 10th Conference on Solid State Devices,

Tokyo, September 1978

(12) September 1979

"ADVANCES in CCD Imager " Technical Digest of IEEE

International Conference of CCD Image Sensors (IEEE CCD'79),

Edinburgh, Scotland UK, September 1979

(13) May 1980

IEEE ECS1980 invited paper on "A CCD color imager

with narrow-channel transfer gates"

Proceeding of the 157th Electrochemical Society Meeting,

May 11-16, 1980, St. Luis, USA

(14) November 1980

Technology Book on "CCD Image Sensor and Applications",

Trickeps Press, November 1980

(15) October 1989

"A 25-ns 4-Mbit CMOS SRAM with Dynamic Bit-Line Loads"

IEEE Journal of Solid-State Circuits, vol.24, no.5, October 1989.

(16) December 1996

IEEE1996 Review Paper on Sony's 1980 One-Chip FT CCD Image Sensor

with Pinned Buried Photodiode

IEEE Transaction on electron Devices, VOl.43, No.12, Dec 1996.

(17) November 1997

"Sony Semiconductor History"

addressed at the 23th Research Seminar

in Tokyo Communication University, Nov 28, 1997

(18) November 1998

"DRAM/SRAM Technology and Problem.pdf"

Proceedings of the Institute of Electrostatics Japan,

127 Vol. 22 No. 6, 1998, pp.177-178

(19) September 2001

"Micro-Electronics for Home Entertainment"

an invited ESSCIRC2001 Plenary Talk, Technical Digest of

IEEE ESSCIRC2001 International Conference (ESSCIRC2001),

Villach, Austria, September, 2001

(20) December 2004

Tutorial Short Course on Image Sensors by Yoshiaki Hagiwara.pdf

IEEE IEDM2004 Conference Short Course

at IEDM2004 Short Course, December 2004

(21) September 2008

"SOI Design in Cell Processor and Beyond", an invited ESSCIRC2008 Plenary Talk,

Technical Digest of IEEE ESSCIRC2008, International Conference (ESSCIRC2008),

Edinburgh, Scotland UK, September 2008

(22) February 2013

Invited Plenary Panel Talk at ISSCCC2013 on Feb. 2013 on Image Sensors

(23) June 2013

"The p-n-p-n Diode in Future Linear Motor Cars and in Modern Imagers"

IEEE Journal of Solid-State Circuits, June issue, 2013.

(24) July 2014

Japanese Patent Application JPA2014_135497 on "Digital Transformation Matrix for Fast Image Recognition System", written in Japanese, filed on July 1, 2014.

(25) July 2014

"Design of Time to Frequency Domain Discrete Fourier Transfer Hardware Engine and its performance estimation" Digest of Technical Papers at the Japan Electron Society sponsored Integrated Circuit Workshop (IEEJ ECT) in Izumo, Japan, on July 4, 2014.

(26) June 2015

"Digital Frequency Transformation Circuit for Time-wise Unequally Sampled Data" The Institute of Electronics, Information and Communication Engineers (IEICE) Technical Paper on June 2015 in Kumamoto-city, Japan.

(27) April 2017

IEEE_CoolChips_2017_Conference_Invited_Panel_Talk_ on_Intelligent_Image_Sensor_Systems.pdf,
Yokohama, Japan, April 2017

(28) October 2019

"Multichip CMOS Image Sensor Structure for Flash Image Acquisition" IEEE International 3D Systems Integration Conference 2019 (3DIC2019), Digest of Technical Papers, Sendai, Japan, Paper4017, October 2019

(29) March 2020

"Simulation and Device Characterization of the P+PN+P Junction Type Pinned Photodiode and Schottky Barrier Photodiode" IEEE Electron Device and Manufacturing Technology Conference (EDTM2020),
Digest of Technical Papers, Penang Malaysia, Paper ID 3C4, March 2020.

(30) August 2020

Japanese Patent Application JPA2020-131313 on "Double Junction Pinned Buried Photodiode Type Solar Cell" written in Japanese, filed on August 1, 2020.

(31) June 2021

"Electrostatic and Dynamic Analysis of P+PNP Double Junction Type and

P+PNPN Triple Junction Type Pinned Photodiodes",

International Journal of Systems Science and Applied Mathematics, June 2, 2021.

doi: 10.11648/j.ijssam.20210602.13; ISSN: 2575-5838 (Print); ISSN: 2575-5803 (Online)

http://www.sciencepublishinggroup.com/journal/paperinfo?journalid=245&doi=10.11648/j.ijssam.20210602.13

Contributions to International Conferences and Organizations

(1) International Standardization Committee (1989-1992)
IEC TC47 Technical Committee Chair (1992)

(2) JEDEC Memory Chips Standardization Committee (2000-2004)

(3) IEEE EDS ICMTS International Program and Executive Committee (1991-2008)
General Chair (2003-2004); http://icmts.if.t.u-tokyo.ac.jp/home

(4) IEEE SSS ISSCC Asian Program Committee (2001-2007)
ISSCC Asian Chair (2006-2007); http://isscc.org/

(5) IEEE SSS ISSCC2008 International Program and Executive Committee (2007-2008)
International Program Chair (2007-2008); http://isscc.org/

(6) IEEE Computer Society Cool Chips Organization Committee (2001-2010)
https://www.coolchips.org/

(7) IEEE Computer Society Cool Chips Advisory Committee (2011-2021)
https://www.coolchips.org/

(8) Visiting Professorship in Electric Engineering Department and
Applied Physics Department at California Institute of Technology,
Pasadena, California, USA, 1998-1999; https://www.caltech.edu/

(9) Professorship in Electrical Engineering Department at Gunma University,
Kiryu-city, Gunma-ken, Japan, 2001-2008; https://www.gunma-u.ac.jp/

(10) Professorship in Information and Communication Technology Department
at Sojo University, Kumamoto-city, Japan, 2009-2017; https://www.sojo-u.ac.jp/

(11) Artificial Intelligent Partner System (AIPS) Consortium, Kanagawa-ken NPO, Japan,
President and CEO (2008-2017); http://www.aiplab.com//

(12) Society of Semiconductor Industry Experts of Japan:　http://www.ssis.or.jp/

currently also serving as the chairman of the SSIS Education Executive Committee.