Story of Pinned Photodiode

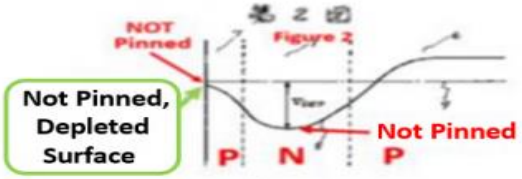
NEC_Teranishi_Patent_JPA1980-138026_is_NOT_Pinned_Photodiode.

JPA 1980-138026

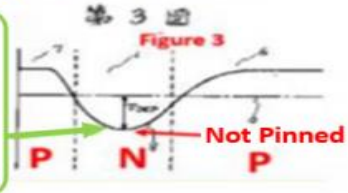
1980年10月2日出願

②特　　願　昭55—138026
②出　　願　昭55(1980)10月2日
②発 明 者　寺西信一
②発 明 者　石原保雄
②発 明 者　白木實光

第2図 Figure 2



第3図 Figure 3



The surface P region is not Pinned. The Buried N region is still floating.

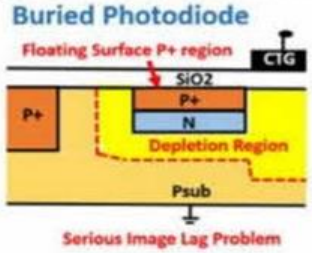
This patent is on the PNP junction type Buried Photodiode but NOT Pinned Photodiode. The surface P region is not pinned and grounded. The surface potential can be of any value depending on the floating buried N region potential, which is actually controlled by the substrate Psub potential which is grounded in this case, but in case of a built-in VOD function P+NPNsub junction photodiode, the P region potential is controlled by the Nsub VOD voltage and can be any value. The surface P region must be pinned by the adjacent P+ channel Stops region or the adjacent metal contact wiring.

NEC_Teranishi_Patent claimed that if the buried N charge storage region is completely depleted of the signal charge, there is no image lag problem. NEC_Teranishi_Patent claimed that both Figure 2 and 3 are possible in the NEC PNP double junction Buried Photodiode. If the surface P region was pinned, the case shown in Figure 2 would be impossible to be included in the NEC Teranishi Patent JPA1980-138026.

Difference of Buried Photodiode and Pinned Photodiode

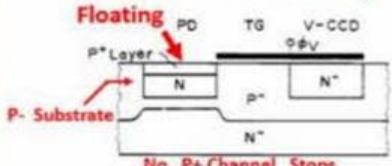
Figure 5 does not have the P+ channel stop nearby.

Buried Photodiode



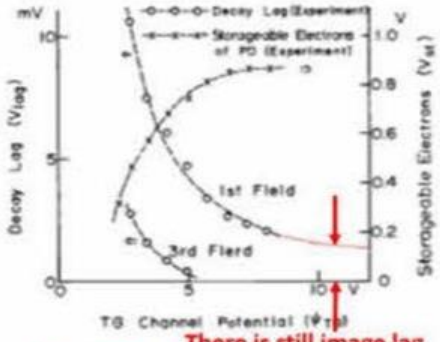
Serious Image Lag Problem

NEC IEDM1982 Paper



No P+ Channel Stops

Fig.5. P+NP+ structure photodiode
(a) Unit cell cross sectional view



There is still image lag at the CTD gate voltage more than 10 volt.

Fig.6. Storageable electrons vs. transfer gate channel potential, and decay lag vs. transfer gate channel potential in the P+NP+ structure photodiode

NEC IEDM1982 Paper reported Image Lag

Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 volt.

Apparently . the surface P region of the NEC PNP double junction Buried Photodiode is NOT pinned. The NEC Teranishi PNP double junction Buried Photodiode is NOT Pinned Photodiode. Surface potential Vs can be floating. This is the reason why Teranishi reported the serious image lag problem in the NEC IEDM1982 conference paper.