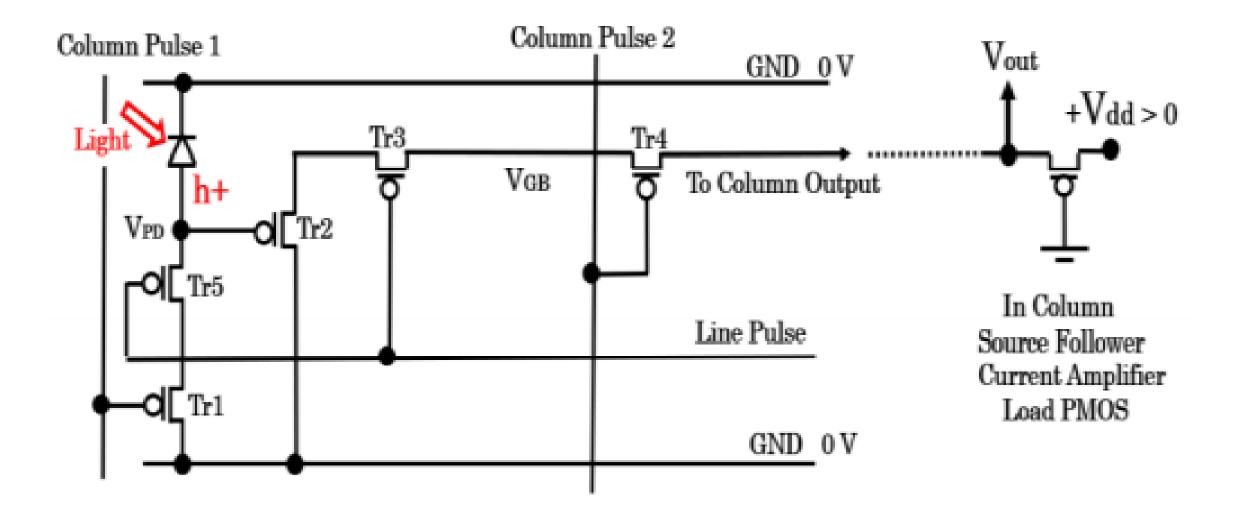


Active in-pixel AMP circuit invented by Peter Noble in 1968



Peter Nobel, IEEE Tran. of Electron Devices 15-4 (1968) pp. 202-209

Please see https://en.wikipedia.org/wiki/Photodiode#Pinned_photodiode,

which does not tell the real truth about the invention and the historical development efforts of Pinned Photodiode and the in-pixel active image sensors.

This documentation should be corrected and re-worded according to the true facts.

This document do not quote Peter Noble's 1968 work and Hagiwara's 1975 and 1978 works.

The truth is that Peter Noble is the inventor of in-pixel active image sensors in 1968.

The truth is that Yoshiaki Hagiwara is the inventor of Pinned Photodiode in 1975.

Fossum did not invent CMOS process technology.

Fossum did not invent the in-pixel image sensor.

The truth is that Ando Team at NHK developed the first active in-pixel image sensor in 1987.

Terniashi did not invent Pinned Photodiode.

Teranish reported in IEDM1978 Buried Photodiode which is not Pinned Photodiode because The Buried Photodiode reported by Teranishi in IEDM1982 had the serious image lag problem.

Please see https://en.wikipedia.org/wiki/Photodiode#Pinned_photodiode.

CCD does not have any image lag. The N+P floating photodiode had serious image Lag.

The pinned photodiode (PPD) has a shallow P+ implant in N type diffusion layer over a P-type epitaxial substrate layer. It is not to be confused with the PIN photodiode. The PPD is used in CMOS active-pixel sensors.^[21]

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- 27. ^ a b Fossum, Eric R. (12 July 1993). Blouke, Morley M. (ed.). "Active pixel sensors: are CCDs dinosaurs?". SPIE Proceedings Vol. 1900: Charge-Coupled Devices and Solid State Optical Sensors III. International Society for Optics and Photonics. 1900: 2-14. Bibcode:1993SPIE.1900....2F요. CiteSeerX 10.1.1.408.6558 a. doi:10.1117/12.148585요. S2CID 10556755요.

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Hagiwara invented Pinned Photodiode in 1975 with OFD function used in ILT CCD defined in 1975 patents.

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The photodiode with the serious image lag data reported by Teranishi in 1982 was NOT Pinned Photodiode.

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Sony in 1987 developed First Pinned Photodiode with the no-image-lag feature and the electric shutter function.

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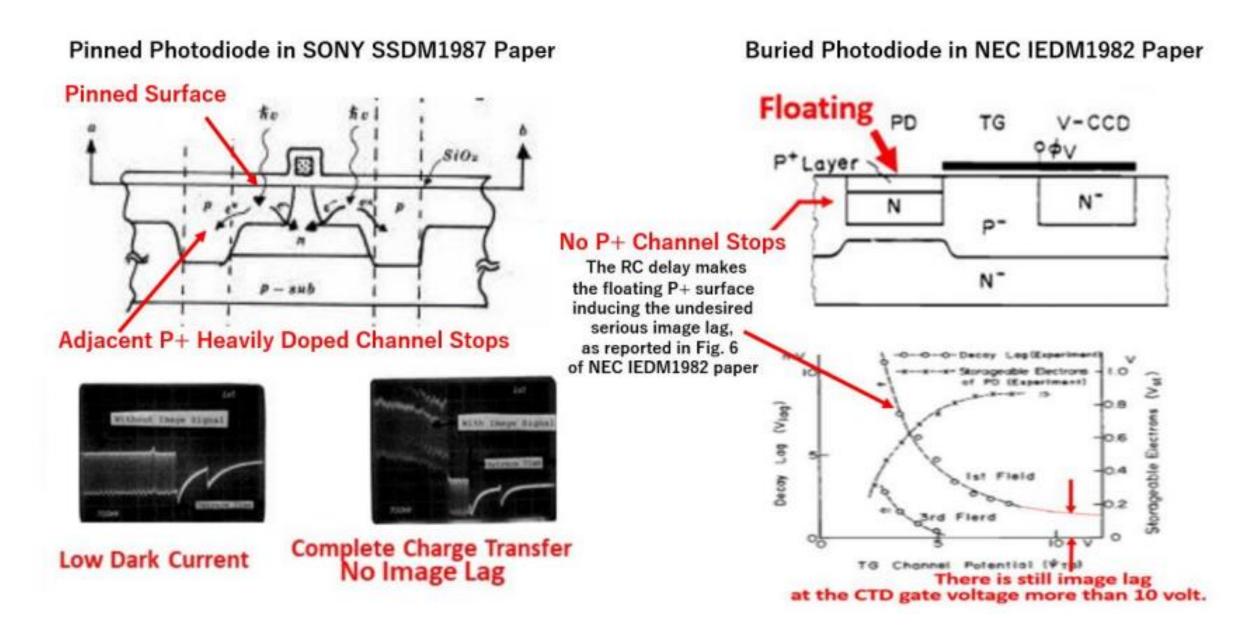
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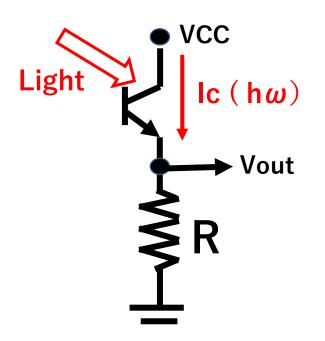
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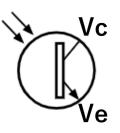
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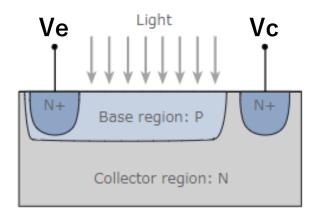


What is NPN Double Junction type Static Photo Transistor?





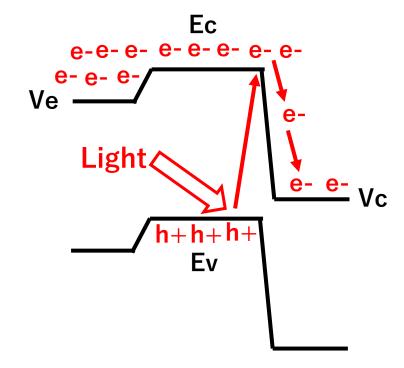
Phototransistor circuit symbol (for a device based around an NPN transistor)



Homojunction planar phototransistor structure

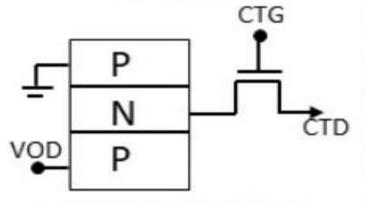
https://www.physlab.org/wp-content/uploads/2016/03/Photodiode_circuit.pdf

It is light-sensitive transistor and is similar to an ordinary bipolar junction transistor (BJT) except that it has no connection to the base terminal. Its operation is based on the photodiode that exists at the CB junction. Instead of the base current, the input to the transistor is provided in the form of light as shown in the schematic symbol



https://www.electronics-notes.com/articles/electronic_components/transistor/what-is-a-phototransistor-tutorial.php

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode



In 1975 the first PPD
was invented by
Hagiwara at Sony
and used in ILT CCD
PDs by Hamazaki
at Sony in 1987.

PPD must have the P+ channel stops nearby to pin the surface P+ layer. This is a commonly misunderstood misused set of terminologies.

First off these are not PIN Photodiodes - which stands for P - Intrinsic- N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though.

Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space.

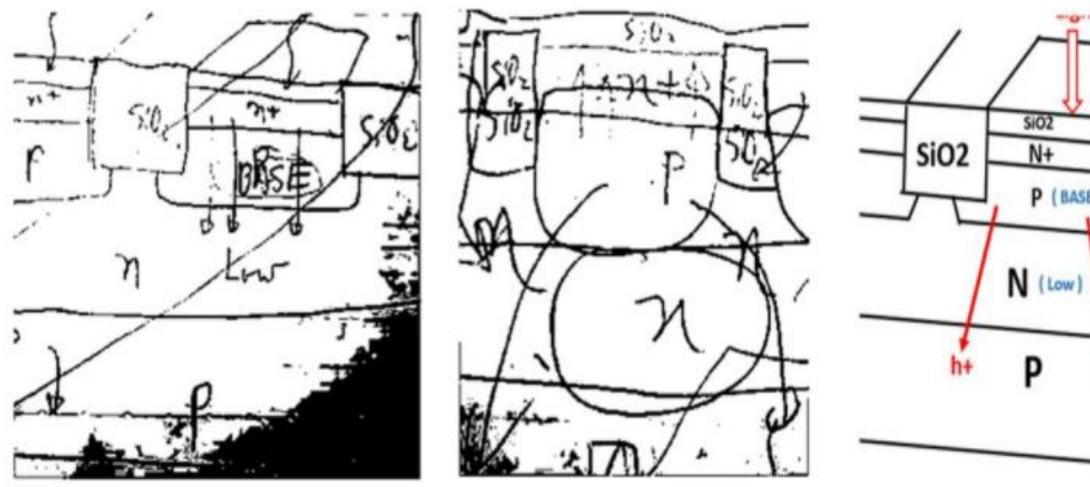
You can get surface state pinning from the dangling Si/SiO2 bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The Si/SiO2 surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface.

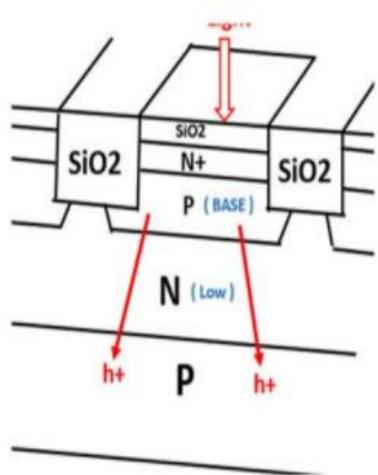
A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

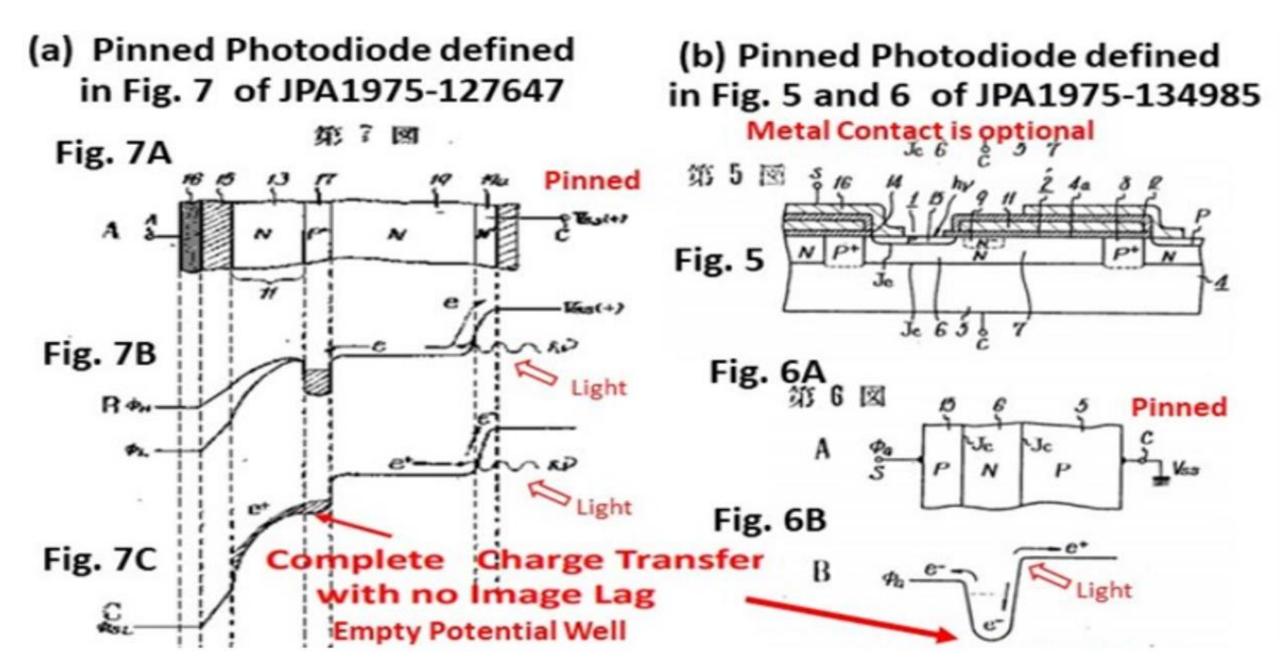
A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

The original 1975 invention of N+PNP junction type photodiode as sketched in the Sony Yokohama Research Cente Lab Note by Yoshiaki Hagiwara is the evidence that Hagiwara is the inventor of the Pinned Photodiode with the vertical overflow drain function with the lightly doped n base region by the thyristor punch thru action mode.







Four Types of Basic Photo Sensor Structures

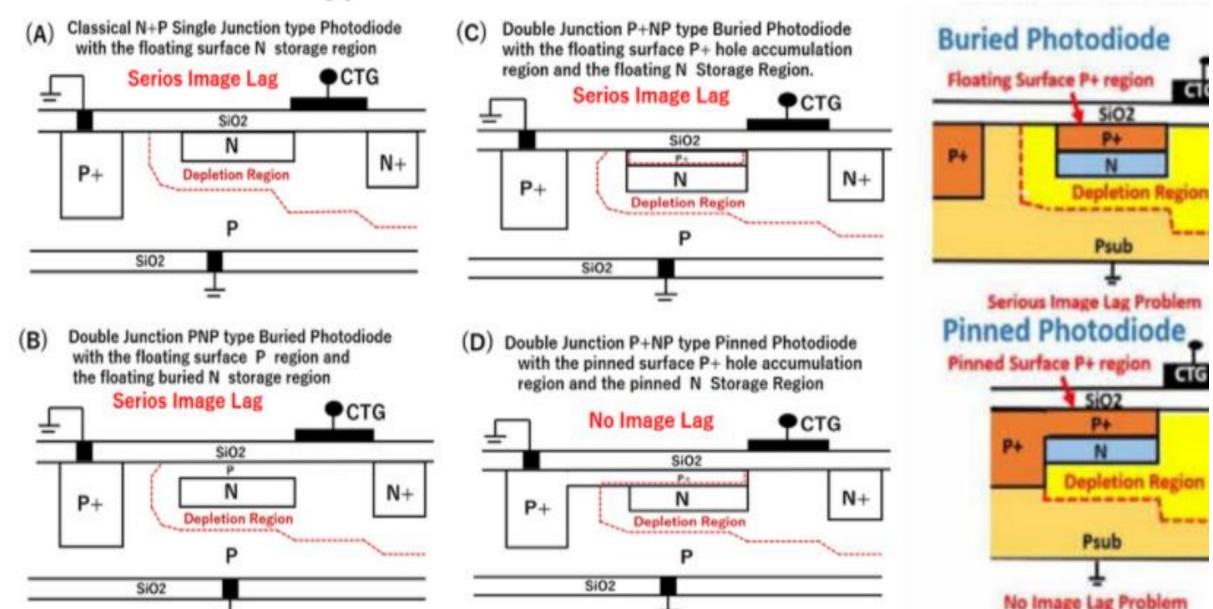
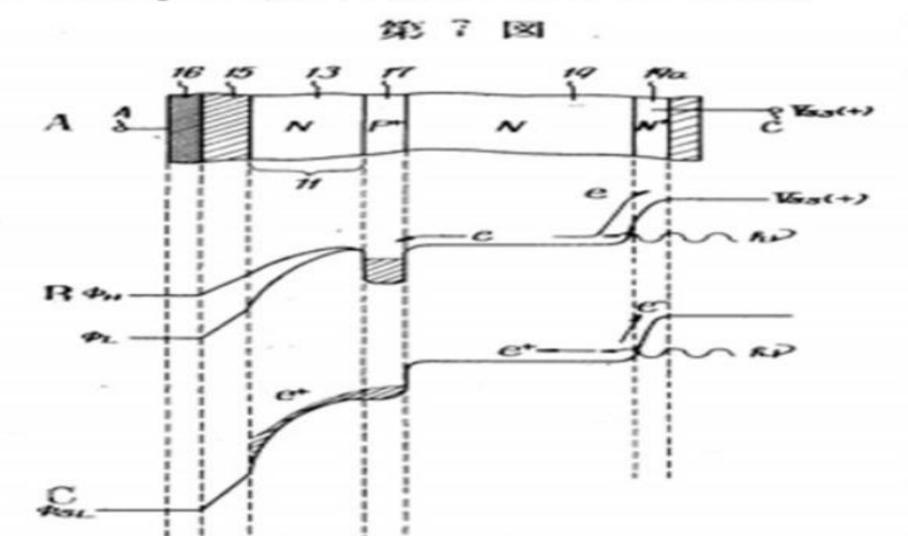


Figure 7 of Japanese Patent Application 1975-127647, applied Oct 23, 1975,

Public April 26, 1977 (Patent No. S52-51816)

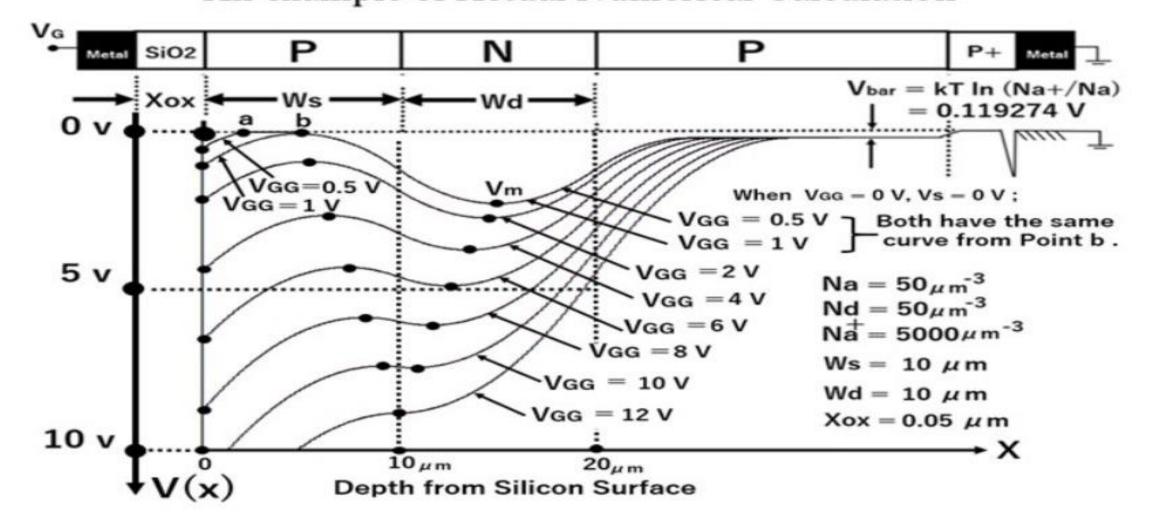


Yoshiaki Hagiwara invented it and applied for Japanese Patent on Oct 23, 1975.

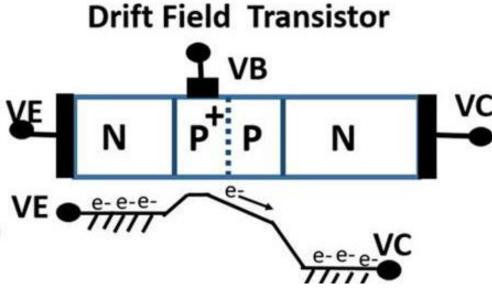
PNP Double Junction type Buried Channel Pinned Photodiode

with MOS Capacitor Buffer Memory for Built-in Global Shutter Function

An example of Actual Numerical Calculation←



What is Drift Field Transistor?



https://en.wikipedia.org/wiki/Drift-field_transistor

The drift-field transistor, also called the drift transistor or graded base transistor, is a type of high-speed bipolar junction transistor having a doping-engineered electric field in the base to reduce the charge carrier base transit time.

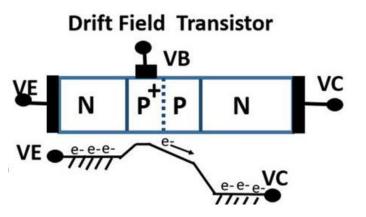
Invented by Herbert Kroemer at the Central Bureau of Telecommunications Technology of the German Postal Service, in 1953.

It continues to influence the design of modern high-speed bipolar junction transistors.

Early drift transistors were made by diffusing the base dopant in a way that caused a higher doping in a way that caused a higher doping concentration near the emitter reducing towards the collector.

Who invented the drift field Transistor?

Herbert Kroemer invented the drift field Transistor.





Herbert Kroemer in 2008

https://en.wikipedia.org/wiki/Herbert_Kroemer

Herbert Kroemer (born August 25, 1928) is a German-American physicist who, along with Zhores Alferov, received the Nobel Prize in Physics in 2000 for "developing semiconductor heterostructures used in high-speed- and opto-electronics". Kroemer is professor emeritus of electrical and computer engineering at the University of California, Santa Barbara, having received his Ph.D. in theoretical physics in 1952 from the University of Göttingen, Germany, with a dissertation on hot electron effects in the then-new transistor. His research into transistors was a stepping stone to the later development of mobile phone technologies.

August 25, 1928 (age 92) Born

Weimar, Germany

Nationality Germany

United States

Alma mater University of Jena

University of Göttingen

Known for Drift-field transistor

Double-heterostructure laser Heterojunction bipolar transistor

J J Ebers Award (1973) Awards

> Humboldt Research Award (1994) Nobel Prize in Physics (2000)

IEEE Medal of Honor[1](2002)

Scientific career

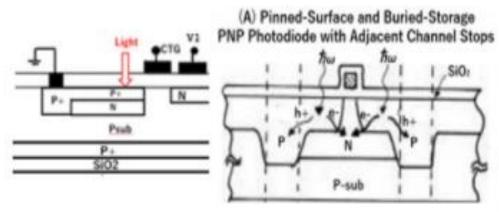
Electrical Engineering, Applied Fields

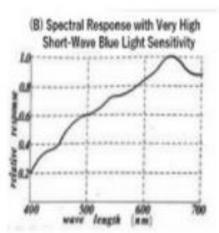
Physics

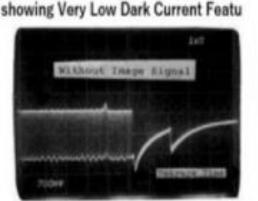
Sony developed in 1978 the P+NP double junction type Pinned Photodiode with the complete charge transfer capability to realize the excellent feature of no image lag for fast action pictures. The pinned surface P+ hole accumulation region was formed by self-aligned ion implantation. Total dark current was measured to be less than 5 nA/cm². And the dark current level was less than 3 % of the maximum signal level at room temperature of 20 °C. Very low surface dark current was observed since there is no electric field in the Pinned P+ surface region,

Yoshiaki Hagiwara, SSDM1978 'Paper and Japanese Patent No. 1215101 (Japanese Patent Application JPA 1975-134985)

Yoshiaki Hagiwara, Motoaki Abe and Chikara Okada, "A 380H x 488V CCD Imager with Narrow Channel Transfer Gates". Proceeding of the 10th Conference on Solid State Devices, Tokyo 1978; Japanese Journal of Applied Physics, Volume 18(1979) Supplement 18-1, pp. 335-340.







(C) Signal Output with No Light

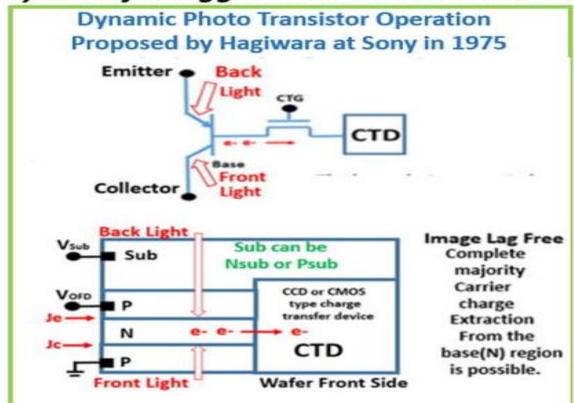


(D) Signal Output with Input Light

Finally the Sony-Fairchild Patent Wat(1991-2000) ended over the Sony HAD Sensor which is identical to the P+NPNsub junction type Pinned Photodiode with Vertical Overflow Drain, originally invented by Hagiwara at Sony in 1975.



And finally Hagiwara received for his 1975-134985 Japanese Patent officially, the First Patent Award from Mr. Ando, Sony president in April, 2001 after more 26 years of struggles since his invention.



Japanese Patent Application JPA 1975-134985

applied by Yoshiaki Hagiwara at Sony on November 10, 1975

Patent Claim in Original Japanese

- 半導体基体(N)に、
 第1導電型の第1半導体領域(P)と、 之の上に形成された第2導電型の 第2半導体領域(N)とが形成されて
- 2) 光感知部(NP)と之よりの電荷を転送する電荷転送部 (CTD)とが上記半導体基体の主面に沿う如く配置されて成る個体撮像装置に於いて
- 3)上記光感知部(NP)の上記第2半導体 領域(N)に整流性接合が形成され、 該接合をエミッタ接合(Je)とし、
- 4) 上記第1及び第2半導体領域間の接合 をコレクタ接合(Jc)とするトランジ スタ(PNP)を形成し、
- 5) 該トランジスタ(PNP)のベースとなる 上記第2半導体領域(N)に光学像に応 じた電荷を蓄積し
- 6) ここ(N) に蓄積された電荷を上記転送 部に移行させて、その転送を行うよう にしたことを特徴とする個体撮像装置

Patent Claim in English Translation

- In the semiconductor basic body (N), the first region (P) of the first impurity is formed, and on which the second region (N) of the second impurity type is formed.
- On The photo sensor (NP) so defined as a solid state image sensor with Charge Transfer Device (CTD) placed along the surface of the semiconductor basic body.
- a rectifying emitter junction (Je) is formed on the photo sensor (NP).
- The junction between the first region

 (P) and the second region (N), being as the collector junction (Jc) of the transistor (PNP),
- the second region (N) becomes the base region of the transistor (PNP) which stores the photo charge according to the photo image.
- And the charge stored in this region (N) is transferred to the Charge Transfer Device (CTD).

Filed 1975/11/10 File 1975-134985 Public 1977-058414 1977/05/13 Buried Pinned Photodiode Patent the PNP Double Junction type Dynamic Photo Transistor with the Vertical Overflow Drain (VOD) Function VOD N Si₀₂

CTG

Light

Patent Claim of JPA1975-134985 on the PNPN Pinned Photodiode

Please see https://en.wikipedia.org/wiki/Photodiode#Pinned_photodiode,

which does not tell the real truth about the invention and the historical development efforts of Pinned Photodiode and the in-pixel active image sensors.

This documentation should be corrected and re-worded according to the true facts.

This document do not quote Peter Noble's 1968 work and Hagiwara's 1975 and 1978 works.

The truth is that Peter Noble is the inventor of in-pixel active image sensors in 1968.

The truth is that Yoshiaki Hagiwara is the inventor of Pinned Photodiode in 1975.

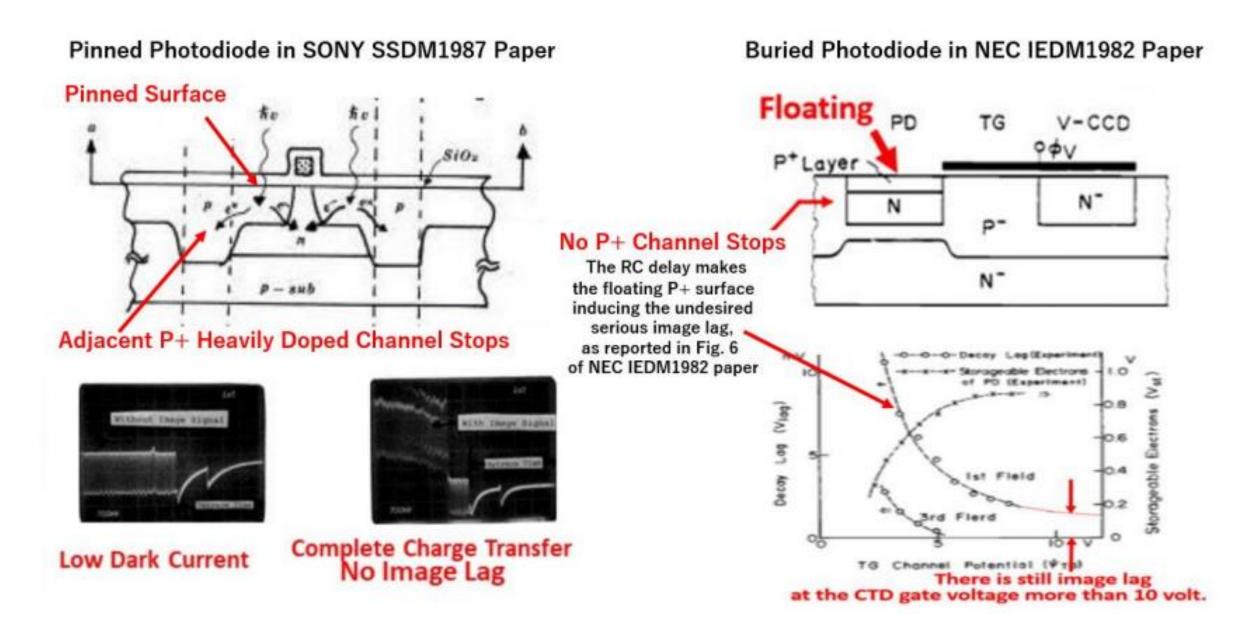
Fossum did not invent CMOS process technology.

Fossum did not invent the in-pixel image sensor.

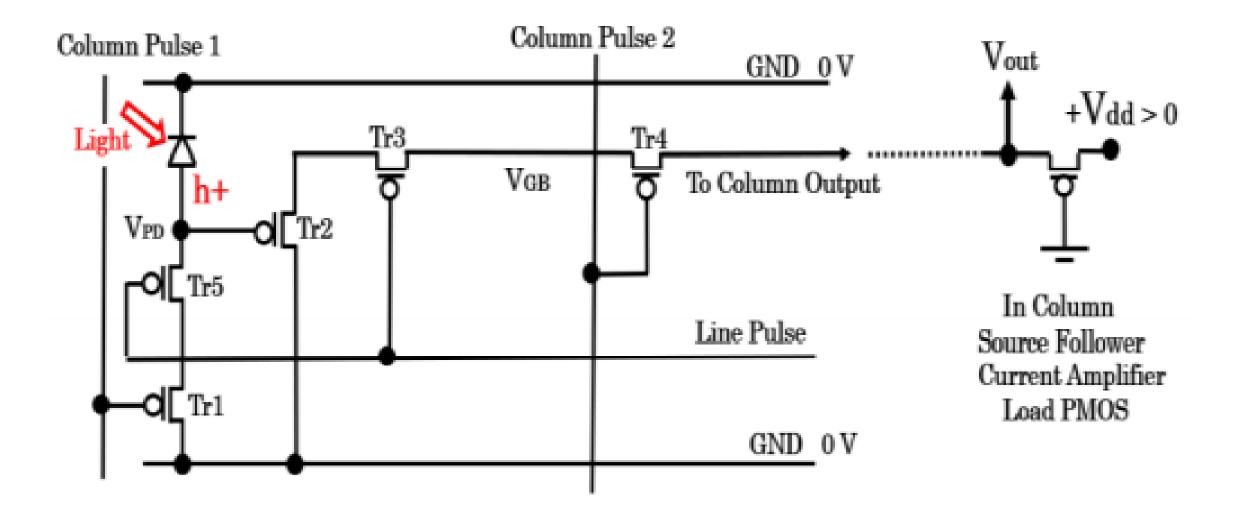
The truth is that Ando Team at NHK developed the first active in-pixel image sensor in 1987.

Terniashi did not invent Pinned Photodiode.

Teranish reported in IEDM1978 Buried Photodiode which is not Pinned Photodiode because The Buried Photodiode reported by Teranishi in IEDM1982 had the serious image lag problem.



Active in-pixel AMP circuit invented by Peter Noble in 1968



Peter Nobel, IEEE Tran. of Electron Devices 15-4 (1968) pp. 202-209

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