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イメージセンサー（CCD・CMOS）

概要 | イノベーションに至る経緯 | 発明技術開発の概要 | 主な受賞歴 | 参考文献等

概要

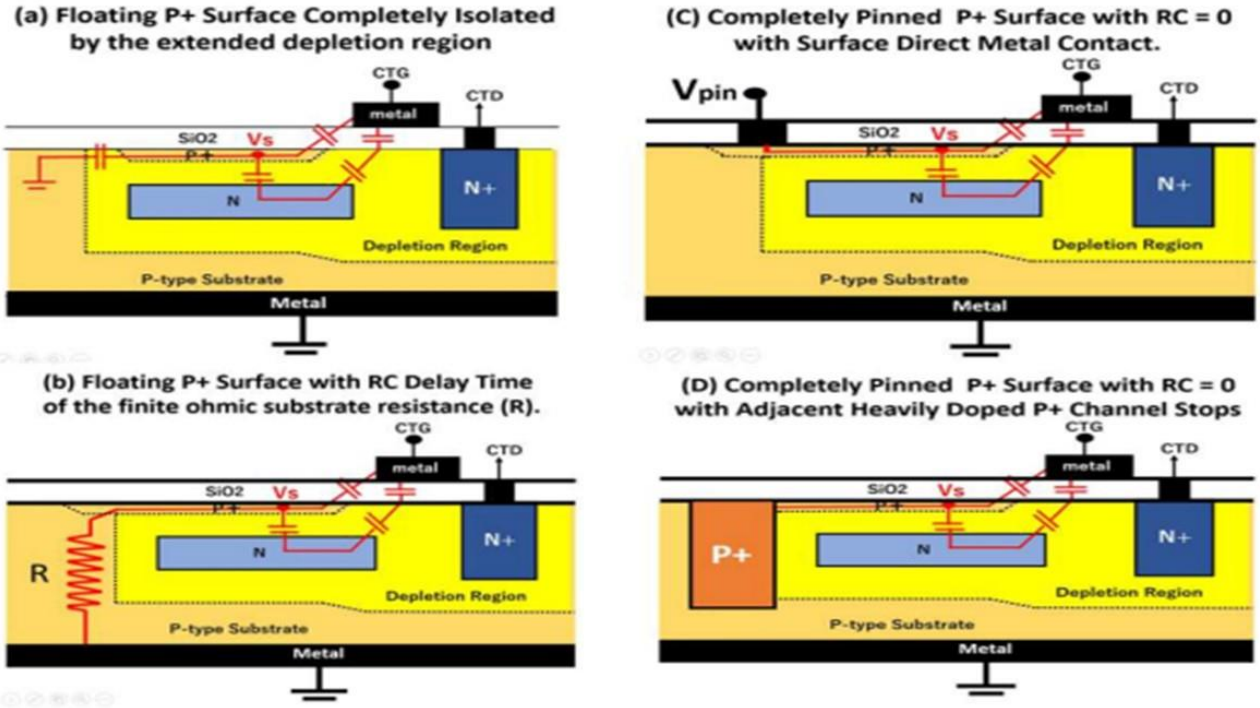
撮像デバイスの研究開発は、19世紀後期のテレビジョン研究がスタートである。機械式、撮像管、固体撮像素子（以下「イメージセンサー」と呼ぶ）と発展し、社会に大きなインパクトを与えつつ、大きく発展してきた。

真空管の一種である撮像管は、サイズが大きい、割れ物である、消費電力が大きい、画像にゆがみがある、高価である、などの欠点があり、固体化が望まれていた。1960年代半ばにイメージセンサーの開発がスタートした。そのときは、ＭＯＳ（Metal Oxide Semiconductor）型が中心であった。

1970年にBoyleとSmith（当時Bell研究所）がＣＣＤ（Charge-Coupled Device、電荷結合素子）を発表した[1]。構造が単純であり、イメージセンサーのような大規模なアレイ構造を製造するのに適していること、矢継ぎ早にＣＣＤに改善が加えられたことから、イメージセンサー開発の中心はＣＣＤになった。1970年後半からは開発の中心は日本に移った。1978年、山田哲生（当時 東芝）は、強い光が入射したときに縦線の偽信号を発生させるブルーミングを抑制する縦型オーバーフロードレイン構造を発明した[2]。1979年には寺西信一（当時 ＮＥＣ）が、白傷や暗電流を大幅に低減し、残像や転送ノイズを解消する埋込フォトダイオード（Pinned Photodiode）を発明した[3]。これらの結果、ＣＣＤはまずムービーを、引き続きコンパクトデジタルスチルカメラを主な市場として量産されていった。

事実誤認？

Difference of Floating Surface PNP Buried Photodiode and Pinned Photodiode



Fossum_insulted_Sony_and_Hagiwara_in_his_2014_paper

IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY, VOL. 2, NO. 3, MAY 2014

A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, *Fellow, IEEE,* and Donald B. Hondongwa, *Student Member, IEEE*

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[24] Y. Hagiwara, Japanese Patent App 50-134985, 1975.
[25] Y. Hagiwara, "High-density and high-quality frame transfer CCD imager with very low smear, low dark current and very high blue sensitivity," *IEEE Trans. Electron Devices*, vol. 43, no. 12, pp. 2122–2130, Dec. 1996.
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No reference on JPA1975-127646, JPA1975-127647 and JPA1977-126885

Completely misleading and false comments

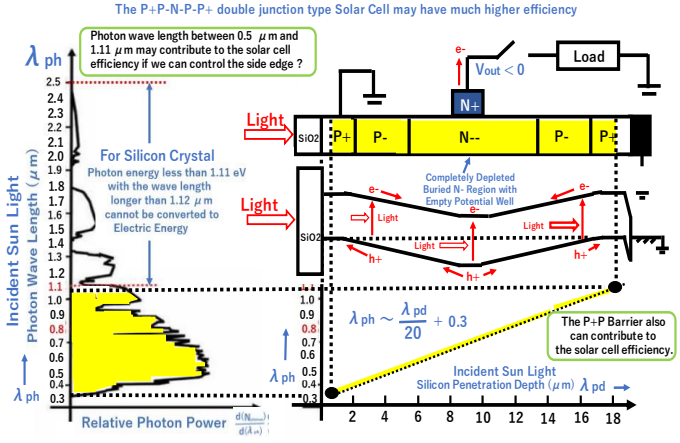
In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a *pnp* vertical structure was disclosed, among several structures [24]. The top *p* layer was connected by metal to a bias used to control full-well capacity and the *n*-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1996, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called "Hole Accumulation Diode," or HAD structure [25]. However, the 1975 application did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the NEC paper was published. However, the "narrow-gate" CCD with an open *p*-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28]. Yes, in 1983 !

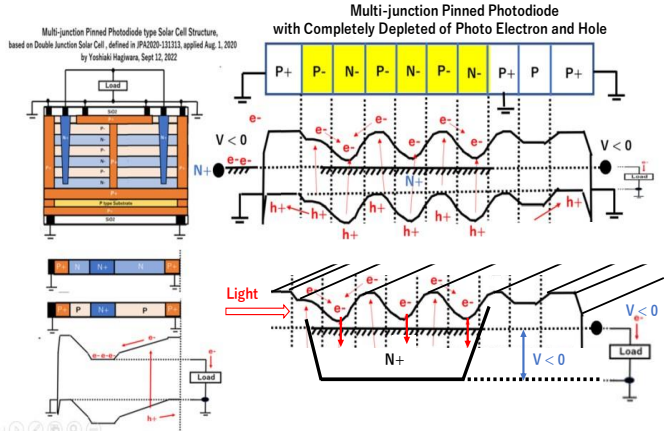
On Oct 23, 1975, Hagiwara at Sony filed a patent application on N+NPNP triple junction type dynamic photo thyristor structures with the CCDMOS capacitor type global shutter buffer memory, which is applicable both for Interline Transfer (ILT)CCD image sensors and the modern CMOS type image sensors in which a vertical overflow drain (VOD)structure was disclosed, among several structures. The top p layer was connected by metal to a bias used to control full-well capacity and the n-type completely buried base layer was proposed for carrier storage with the complete charge transfer capability and with the no image lag feature.

In a subsequent review paper, Hagiwara, in 1996, revisited the 1975 invention and explained it was essentially the invention of both the virtual phase CCD with the built-in narrow-channel type directionality and the no image lag feature, which became the basis of the Sony so-called "Hole Accumulation Diode," or HAD structure. The 1975 applications JPA1975-127646, JPA1975-127647 and JPA1975-134985 in the figures explained the complete charge transfer, lag or anti-blooming properties and the actual PNP junction type pinned photodiode device was developed and reported in his SSDM1977 conference paper and his SSDM1978 conference paper. Hagiwara explained that the built-in potential step and the directionality of charge transfer was created by the unique narrow-channel effect and realized complete charge transfer aspects of the virtual-phase CCD. Hagiwara explained also in a 2001 paper and shows a VOD structure that is found in the 1975 patent application JPA1975-134985.

Sony focused in developing the mass production and the yield enhancement technology for a long time and finally Ishikawa's team at Sony commercialized in 1987 the PNPN triple junction dynamic thyristor type Pinned Photodiode with the in-pixel vertical overflow drain (VOD) structure with anti-blooming function, the no image lag feature and the electric shutter function capability. Sony named the perfected structure as Hole Accumulation Diode (HAD) structure.

The “narrow-gate” CCD with an open p-type pinned surface region was reported in more detail by Hagiwara team at Sony in 1978, which showed the improved QE as proposed and explained by Hagiwara in the 1975 applications. A similar structure was used extensively by Philips in 1983. The PPD invented by Hagiwara at Sony in 1975 has improved QE, as it is most commonly used today, now has the potential application for the future solar cell.





This paper draft is based on my talk at Sony Kumamoto Tech Center on Sept 20, 2022.

Hagiwara_at_Sony_Kumamoto_Tech_Slides_2022_09_20.pdf(Japanese)

Hagiwara_at_Sony_Kumamoto_Tech_2022_09_20_MP4_Video_in_English

Hagiwara_at_Sony_Kumamoto_Tech_2022_09_20_MP4_Video_in_English_Part_Two

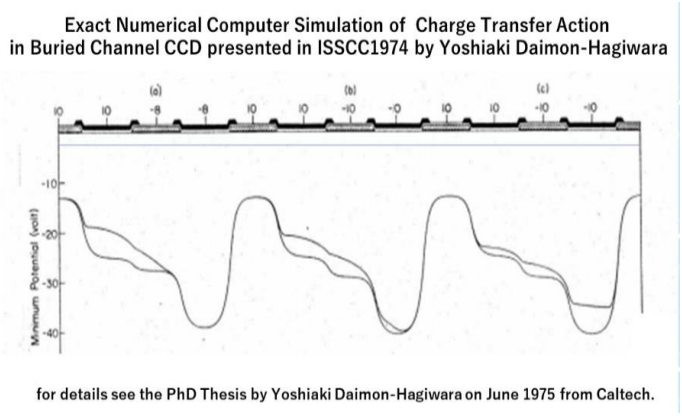
[IJSSM2021 e-Journal Paper on Pinned Photodiode.html]

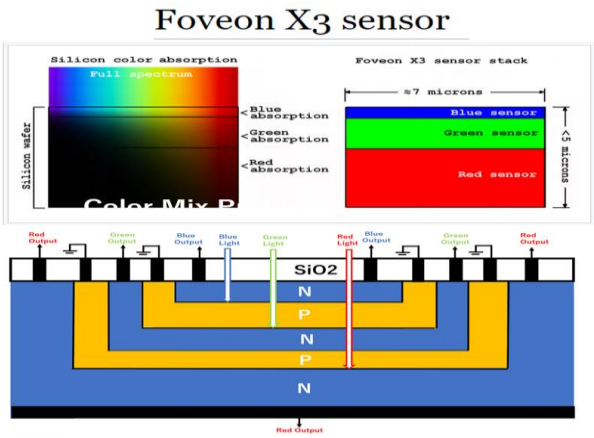
[ICECET2021_Paper61.html]

[ICECET2021_Paper75.html]

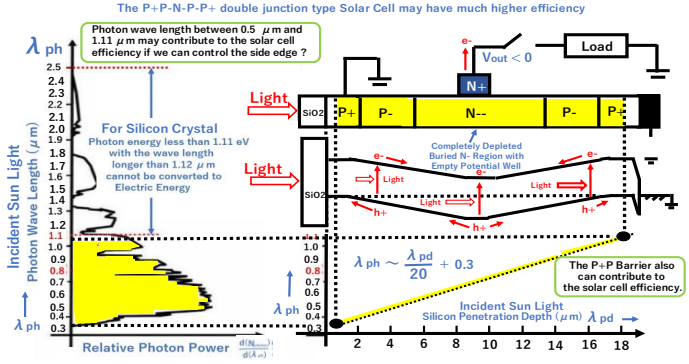
[P2020_EDTM2020_PaperID_3C4_by_Hagiwara_4_pages.pdf]

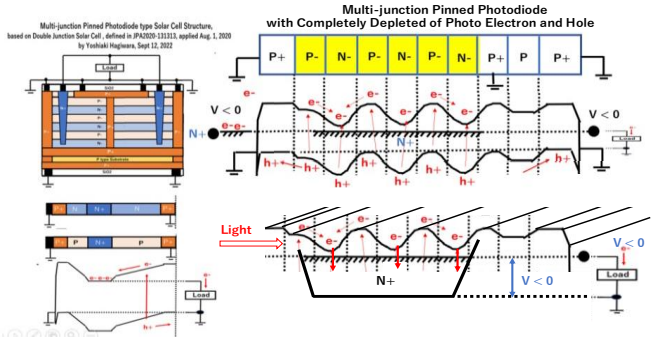
[P2019_3DIC2019_Paper_on_3D_Pinned_Photodiode_6_pages.pdf]





Hagiwara now proposing a new kind of the muti-junction type Solar Cell. See JPA2020-131313.





The 1975 applications JPA1975-127646, JPA1975-127647 and JPA1975-134985 in the figures explained complete charge transfer, lag or anti-blooming properties and the actual PNP junction type pinned photodiode device was developed and reported in his SSDM1977 conference paper and his SSDM1978 conference paper. Hagiwara explained that the built-in potential step and the directionality of charge transfer was created by the unique narrow-channel effect and realized complete charge transfer aspects of the virtual-phase CCD. Hagiwara explained also in a 2001 paper and shows a VOD structure that is found in the 1975 patent application JPA1975-134985.

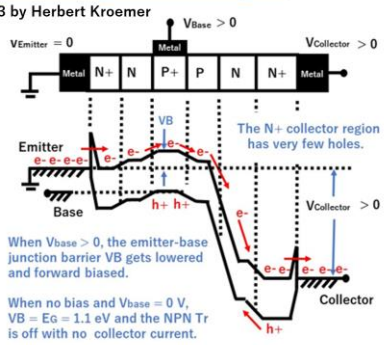
https://en.wikipedia.org/wiki/Drift-field_transistor- Wikipedia

Invented in 1953 by Herbert Kroemer

The drift-field transistor, also called the drift transistor or graded base transistor, is a type of high-speed bipolar junction transistor having a doping-engineered electric field in the base to reduce the charge carrier base transit time.

Invented by Herbert Kroemer at the Central Bureau of Telecommunications Technology of the German Postal Service, in 1953, it continues to influence the design of modern high-speed bipolar junction transistors.

Early drift transistors were made by diffusing the base dopant in a way that caused a higher doping concentration near the emitter reducing towards the collector.



Solid-State Electronics

Volume 24, Issue 12, December 1981, Pages 1161-1165

Theory of back surface field silicon solar cells

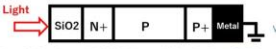
S.R. Dhariwal, Arun P. Kulshreshtha

Abstract

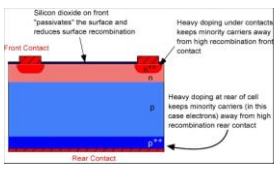
Back surface field silicon solar cells with n^+pp^+ (or sometimes p^+nn^+) structures are found to have better characteristics than the conventional solar cells. The existing theories have not been able to satisfactorily predict the experimentally observed parameters on these cells. A theory, based on the transport of both minority and majority carriers under the charge neutrality condition, has been developed in the present paper which explains the behavior of the back surface field solar cells. Good agreement is achieved between the results obtained by using this theory and the experimental observations of earlier workers.

Back Surface Field Silicon Solar Cell in vented by Wolf in 1963

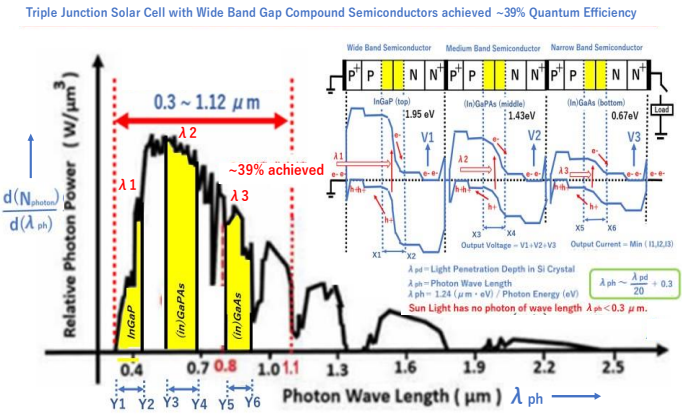
*M. Wolf, Proc. IEEE, 51 (1963) 674

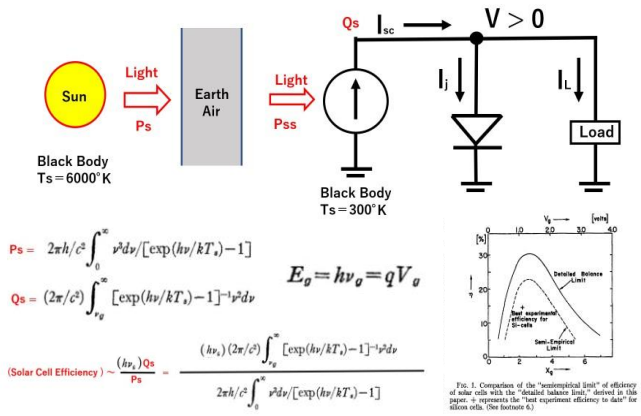


Conventional N++NPP++ type Solar Cell



https://www.sciencedirect.com/science/article/abs/pii/0038110181901854





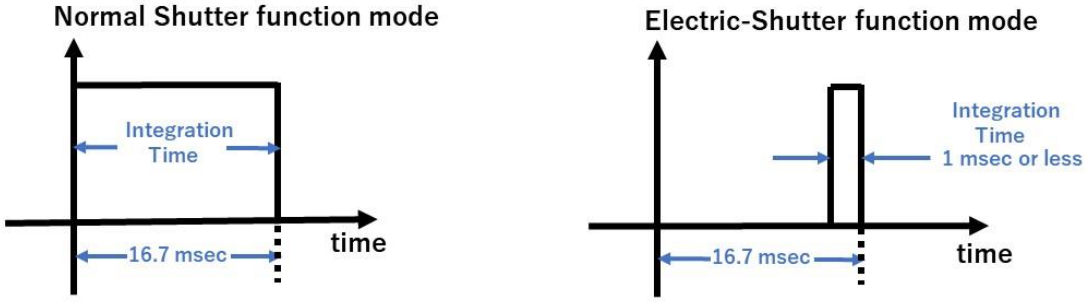
Sony focused in developing the mass production and the yield enhancement technology for a long time and finally Ishikawa's team at Sony commercialized in 1987 the PNPN triple junction dynamic thyristor type Pinned Photodiode with the in-pixel vertical overflow drain (VOD) structure with anti-blooming function, the no image lag feature and the electric shutter function capability. Sony named the perfected structure as Hole Accumulation Diode (HAD) structure.

Hagiwara team at Sony in 1977 introduced the concept of Electronic Shutter.

The difference between Global-Shutter function and Electric-Shutter function

For the NTSC interlace TV scanning system, the frame rate is 60 frames per second, and the light integration (exposure) time is 1000/60 = 16.7 msec for both odd and even picture fields.

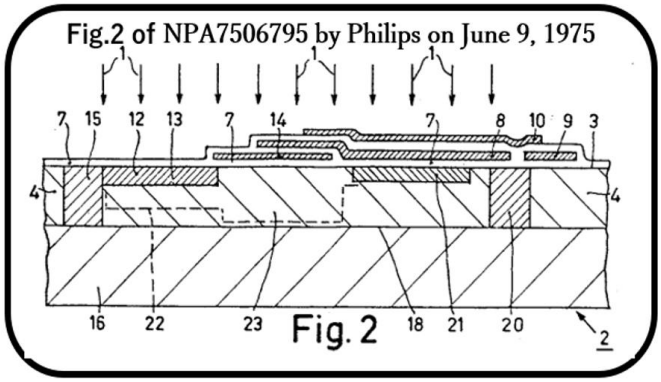
However, the 16.7 msec integration time may be too long for a fast moving action object, specially for digital still camera applications. In mechanical-shutter camera, the exposure time can be adjusted mechanically and freely by the user. The desired integration time can be made as shorter as 1 msec or less. The light in-take window must be opened and closed with a very short time duration. This can be achieved by shortening the effective integration (exposure) time electrically by controlling the in-pixel overflow drain (OFD) voltage in the CCD/MOS capacitor type sensor (JPA1977-126885) and also in the triple junction type Pinned Photodiode.

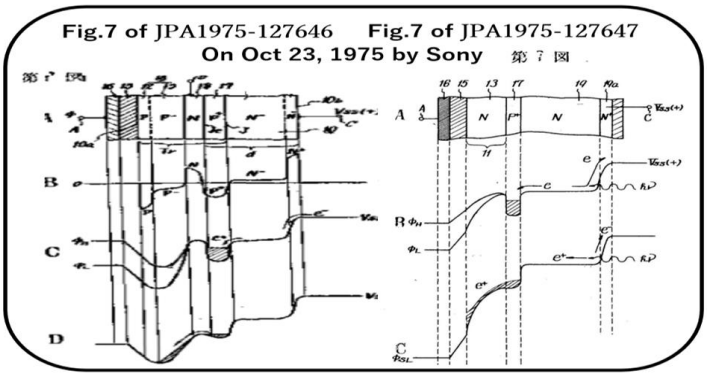


Electric-Shutter function mode is a special case of Normal Global Shutter function mode.

The world's first double junction type Buried Photodiode:

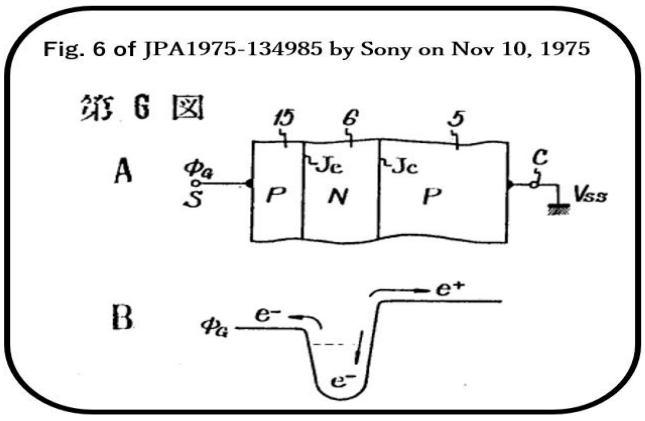
Philips invented the first double junction type Buried Photodiode on June 9, 1975. The evidence is given in the Netherland Patent Application (NPA7506795) applied by Philips for use in the interline transfer CCD image sensor. In Fig. 2 of the NPA7506795, a dashed potential profile (12) is drawn to show an empty potential well of complete charge transfer. And no image lag feature was expected. However, as shown in Fig. 2, the surface (P) region is connected to the (P) high resistivity substrate (16) by a resistive region (15). Evidently the surface (P) region (13) may have a large RC delay time constant, introducing a serious image lag problem. Since the surface (P) region is not completely pinned and being floating with RC delay, the structure cannot be Pinned Photodiode.

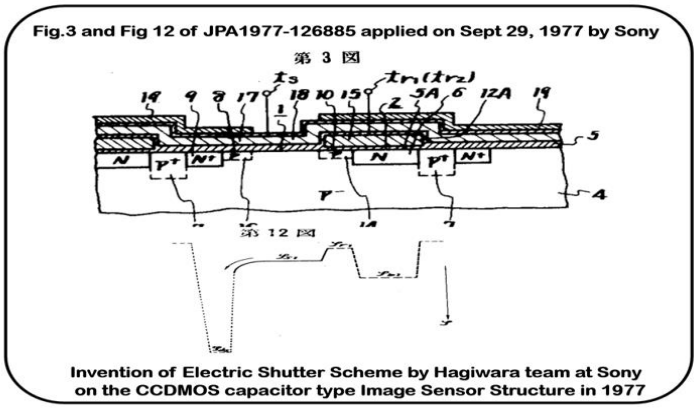




The world's first double junction type Pinned Photodiode with antiblooming and electronic shutter functions.

On October 23, 1975 Yoshiaki Hagiwara at Sony invented the double junction and triple junction type Pinned Photodiodes. (See Fig. 7 of JPA1975-127646 and JPA1975-127647). Seen in Fig.7, the surface is pinned by an external metal contact with zero RC delay time. This is the ideal Pinned Photodiode which has the potential application of the high frequency electric shutter function capability with zero RC delay time and the no image lag feature. Moreover, the structure also has the in-pixel CCDMOS capacitor type buffer memory needed as for the modern CMOS image sensor applications in order to suppress the rotary shutter effect that the conventional classical MOS image sensors suffered for a long time. The first Pinned Photodiode was invented in order to realize the high frequency global shutter function capability in this way.

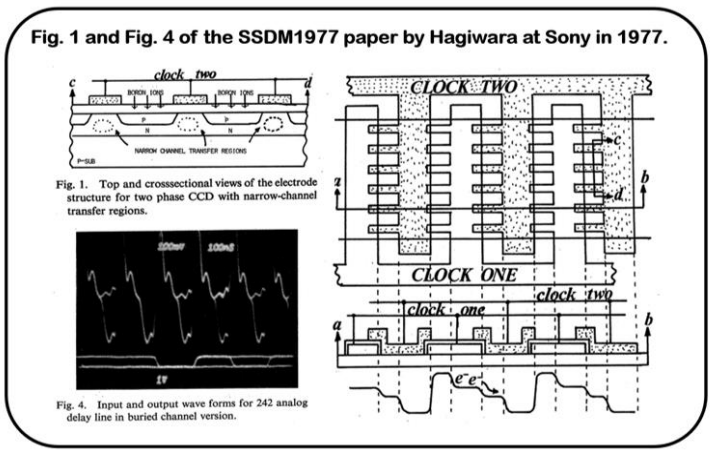


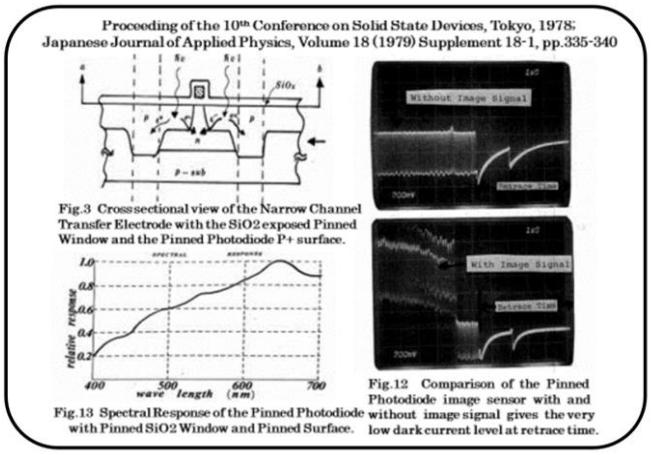


On November 10, 1975, Hagiwara at Sony also invented, (JPA1975-134985,) the PNP double junction type Pinned Photodiode with the in-pixel vertical overflow drain (VOD) structure with anti-blooming capability. In JPA1977-126885, Hagiwara at Sony also proposed the electronic shutter clocking scheme on CCDMOS capacitor type image sensor structure with the no image lag feature and the complete charge transfer capability.

The world's first frame transfer type CCD image sensor, using the double junction type Pinned Photodiode:

Hagiwara at Sony developed, and reported at the SSDM1977 conference in Tokyo, the first PNP junction type Pinned Photodiode in the analog delay line with the complete charge transfer capability, the no image lag feature and with the built-in potential step and the directionality for the complete signal charge transfer created by the unique narrow-channel charge-transfer gate structure. Hagiwara team at Sony also developed, and reported at the SSDM1978 conference in Tokyo, the frame transfer type CCD area image sensor using the PNP junction type Pinned Photodiode with the very low dark current, the complete charge transfer capability and the no image lag feature. The surface hole accumulation region is pinned by the adjacent heavily doped channel stops which is formed by the high energy ion implantation and the lamp anneal technology invented by Kazuo Nishiyama at Sony. Sony never used the LOCOS isolation nor the shallow trench isolation technology in the area image sensor productions because the LOCOS isolation and the shallow trench isolation technology invited the extra thermal stress and the undesired crystal damage, degrading chip yield.





The world's first interline transfer type CCD image sensor.

Hagiwara's team at Sony developed in 1980 and reported in Japanese conference the interline transfer (ILT) type CCD image sensor, using a thin polysilicon (SIPOS) gate type MOS photo capacitor photo sensor structure with the lateral overflow drain (OFD) for the anti-blooming and the electronic shutter function capability.

Teranishi's team at NEC developed and reported at the IEDM1982 conference the interline transfer (ILT) type CCD image sensor, using the PNP double junction type Buried Photodiode. The details of the image lag data were reported. No LOCOS isolation technology nor Shallow Trench isolation technology were reported.

KODAK developed and reported at the IEDM1984 conference the interline transfer (ILT) type CCD image sensor, using the PNP double junction type Pinned Photodiode. KODAK emphasized the importance of the pinned surface in order to achieve the complete image lag free feature. LOCOS isolation technology was used.

Ishikawa's team at Sony developed and reported at the SPIE1989 conference the inter transfer type CCD image sensor, using the PNPN triple junction type Pinned Photodiode with the anti-blooming and the electric shutter function capability. The pinned surface is the very important necessary condition to achieve the complete charge transfer capability, the no image lag feature and also the high frequency electric shutter function in order to achieve the completely mechanical-part-free solid state image sensors.

The lost invention of the Pinned Photodiode:

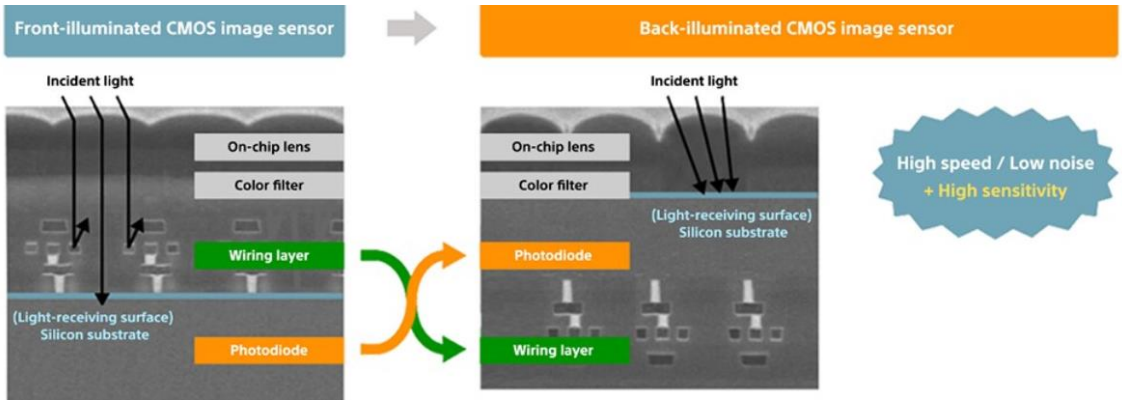
Sony applied three basic patents JPA1975-127646, JPA1975-127647 and JPA1975-134985 on Pinned Photodiode in Japanese Patent Office. However, Sony did not apply to any USP and other oversea patent offices. The invention was completely forgotten by the rest of the world until June 26, 2020 when Sony finally disclosed officially the Hagiwara 1975 patent applications and quoted Hagiwara 1978 effort of developing the first PNP junction type Pinned Photodiode.

https://www.sony.com/en/SonyInfo/News/notice/20200626/

Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.



https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

Semiconductor History Museum of Japan

1975-85

Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

~ Discrete Semiconductor/Others ~

Semiconductor History Museum of Japan says that Hagiwara invented Pinned Photodiode.

In 1975, Sony proposed using a PNP transistor as the photodetector [3]. By providing a P^+ layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated to improve the light sensitivity greatly. It was a basic proposal for a pinned photodiode with a P^+ layer on the surface of the light receiving part.

【3】Y. Hagiwara, Japanese Patent JP1975—134985

Next, proposals were made separately by Hitachi and Sony to use the P^+ layer as the substrate potential. In 1977, Hitachi presented a structure in which the high-concentration surface P^+ layer is connected to a P-type substrate (well) and pinned it to the same potential as the substrate to increase the charge storage capacity and widen the dynamic range of the photodiode [4].

【4】N. Koike, I. Takemoto. Japanese Patent JP1977—837

. In 1978, Sony announced an FT (Frame Transfer) -CCD image sensor, using the photodiode with the same structure [5]. Sony succeeded for the first time in the world in prototyping a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor that developed this technology, in 1981 [6].

【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

【6】I. Kajino, M. Shimada, Y. Nakada, Y. Hirata and Y. Hagiwara, "Single Chip Color Camera Using Narrow channel CCD Imager with Over Flow Drain"、Technical Report of The Institute of Image Information and Television Engineers、vol. 5, no. 29, pp. 32-3S, (1981)

NEC in 1982 and Kodak in 1984 developed Pinned Photodiode but they did not invent it.

In 1980, NEC analyzed in detail the relationship between the electric potential of the N layer of a photodiode in which the P layer was pinned to the substrate potential and the potential of the transfer gate to an external circuit. They then demonstrated a principle of operation that completely transfers the signal charges while keeping the potential of the depleted N layer higher than the channel potential of the transfer gate by a required value or higher, realizing image lag free operation [8][9]. The design methods based on this operation principle of the pinned photodiode focusing on this N-layer potential were widely studied and have been standardized as the Pinned Photodiode for today's CCD and CMOS image sensors.

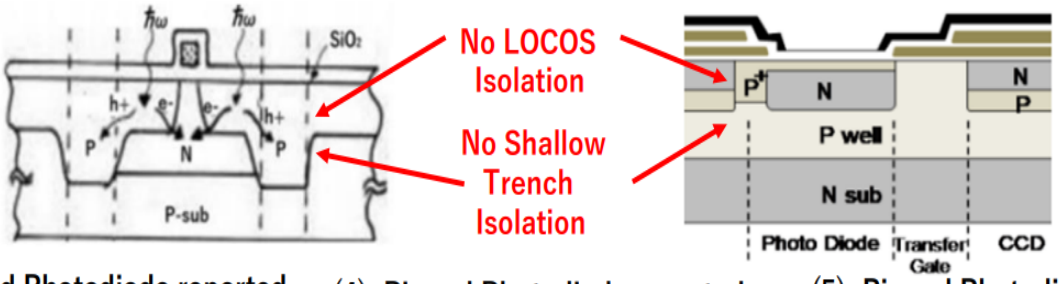
The Pinned Photodiode is a photodiode in which the entire N layer is covered with a P layer. The part of the P layer on the light incident surface is heavily doped P^+(Fig.1). Kodak named this structure Pinned Photodiode in 1984 because the P^+ surface of the light incident surface was pinned to the substrate potential. This device has features such as high light sensitivity, wide dynamic range, image lag free, much smaller dark current due to reduced influence of GR center on the light receiving surface, and no white scars.

First Pinned Photodiode was invented by Hagiwara in 1975 and reported at SSDM1978 by Sony.

Sony never used LOCOS isolation nor Shallow Trench Isolation. Both suffer the yield problem of dark Current and White Defects. Instead Sony used high energy ion implantation to form the adjacent heavily doped P+ channel stops region with the Lamp Anneal Technology invented by Kazuo Nishiyama at Sony.

(1) The first Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation invented and reported at SSDM1978 by Hagiwara.

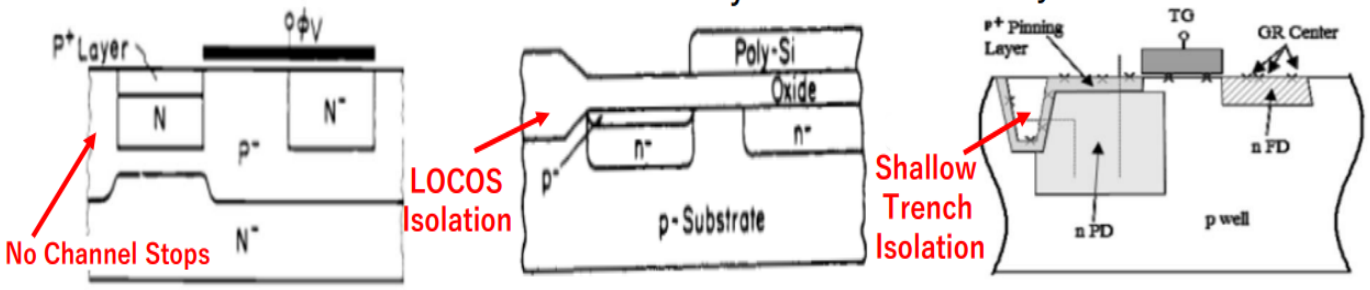
(2) Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation as explained by ssis.or.jp in the official Semiconductor History Museum WEB site.



(3) Buried Photodiode reported at IEDM1982 by NEC

(4) Pinned Photodiode reported at IEDM1984 by KODAK

(5) Pinned Photodiode reported by Teranishi in 2014



Hagiwara reported the first PNP junction type Pinned Photodiode in the SSDM1977 and SSDM1978 conferences in Tokyo which were sponsored by Japan Applied Physics Society. But the journal of Japan Applied Physics Society circulation was quite limited. Albert Theuwissen quoted finally in his IEDM conference paper on "Hole Role" Hagiwara 1978 SSDM1978 paper.

Albert J.P. Theuwissen, Jan T.J. Bosiers, Edwin Roks, " The Hole Role ", an invited paper at IEDM2005, Washington DC, Techn. Dig. , 2005.

But in the case that parts of the depleted n-type CCD channels are not covered by gate material, their surface potential is undefined ! Such a structure will suffer from charge transport issues during operation, because charge can be trapped in local potential pockets. The effect can be solved by defining the potential in the open areas through an extension of the p^+ channel stopper. A simple self-aligned implant of $2x10^{13}$ /cm^2 boron ions is sufficient to extend the channel stop areas to the gate edge and consequently fix the potential in the open areas [2]. The result after this self-aligned implant is shown in Figure 3. The presence of enough holes plays a crucial role in fixing the potential for the regions "beyond control" of the gates. (Is this structure the mother of the pinned-photodiode or buried diode or hole-accumulation device ?)

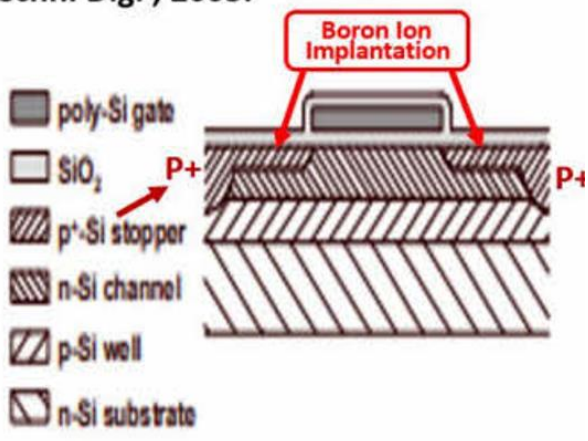


Figure 3. Cross section of a buried-channel CCD on n-Si substrate including light windows and pinned interface potential in the non-covered CCD channels (the cross section is made perpendicular to the CCD channel).

[2] Y. Daimon-Hagiwara et.al., Proc. 10th Conf. on Solid-State Devices, Tokyo, 1978, pp.335-340,

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

ELECTRICALENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

Asked 8 years, 10 months ago Modified 2 years, 8 months ago Viewed 6k times

6 What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

Fossum insulted in his 2014 paper Sony and Hagiwara 1975 PPD invention.

Indeed, Hagiwara invented PPD with VOD and the virtual charge transfer in 1975 !!

IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY, VOL. 2, NO. 3, MAY 2014 33

Sony HAD (PPD+VOD) does not use LOCOS !!!

A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, *Fellow, IEEE*, and Donald B. Hondongwa, *Student Member, IEEE*

False

Many people now said this is a fake paper !

C. Other Contributions to the PPD Invention

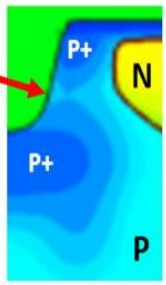
False

The PPD structure, while invented for low lag ILT CCD application, shares a strong resemblance to the Hynecek virtual-phase CCD structure, with the exception of the VOD. The two inventions were solving different problems with essentially the same device structure and operating principles.

In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a *pnp* vertical structure was disclosed, among several structures [24]. The top *p* layer was connected by metal to a bias used to control full-well capacity and the *n*-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1996, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called "Hole Accumulation Diode," or HAD structure [25]. However, the 1975 application did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the NEC paper was published. However, the "narrow-gate" CCD with an open *p*-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

The PPD, as it is most commonly used today, bears the strongest resemblance to the Teranishi et al. ILT CCD device. Thus, these days Teranishi is considered as the primary inventor of the modern PPD [29].

The surface P+ layer is NOT connected to the LOCOS P+ layer. The surface P+ layer may be floating and this photodiode may have serious image lag.



Serious Image Lag ?

NOT connected

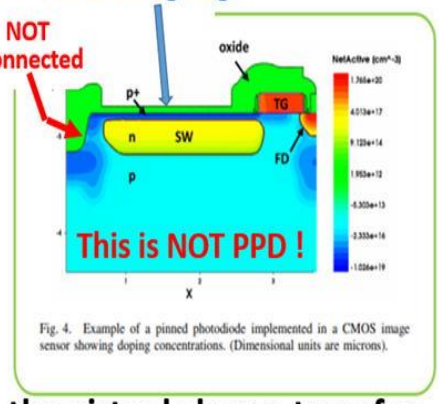


Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

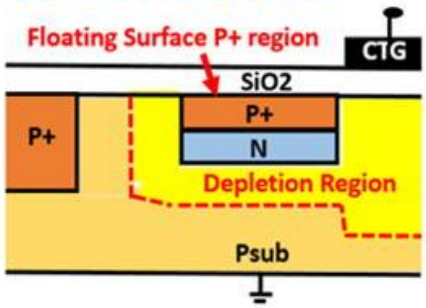
Hagiwara in 1975 invented PPD with VOD and the virtual charge transfer.

Study the Japanese Patents 1975-127646, 1975-127647 and 1975-134985.

Difference of Buried Photodiode and Pinned Photodiode

Figure 5 does not have the P+ channel stop nearby.

Buried Photodiode



Serious Image Lag Problem

NEC IEDM1982 Paper

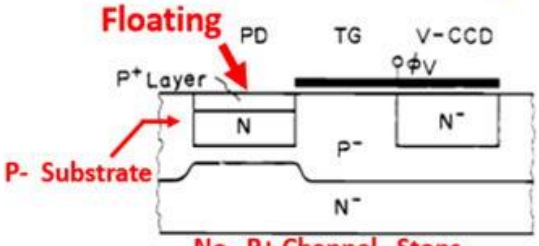
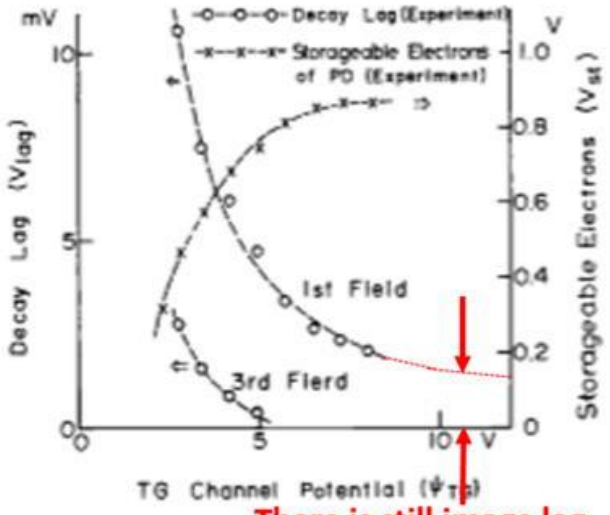


Fig.5. P⁺NP⁻ structure photodiode
(a) Unit cell cross sectional view



There is still image lag
at the CTD gate voltage more than 10 volt.

Fig.6. Storageable electrons vs. transfer gate channel potential, and decay lag vs. transfer gate channel potential in the P⁺NP⁻ structure photodiode

NEC IEDM1982 Paper reported Image Lag

Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 volt.

JPA 1980-138026

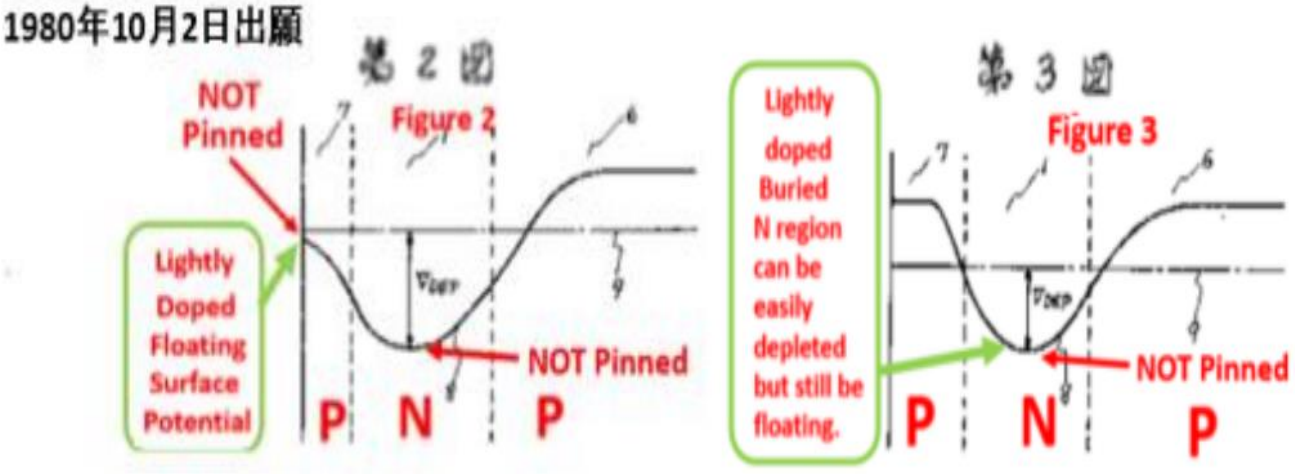
Japanese Patent on Buried Photodiode by Teranishi.

This is NOT a Pinned Photodiode Patent.

Buried Photodiode (BPD) is not always Pinned Photodiode (PPD).

This patent includes the Fig. 2 case of the completely depleted surface P region which is not by definition Pinned Photodiode (PPD).

1980年10月2日出願



SONY- Fairchild Patent War (1991-2000) on Pinned Photo Diode with Vertical OFD

CCD特許侵害訴訟

ソニー、逆転勝訴

NY東部地裁

日刊 7/16

電子機器の基幹部品である電荷結合素子（CCD）の特許侵害訴訟を係属していた米ニューヨーク東部地裁は、ソニー（社長出井伸之氏）を訴えていた米ローラル・フェアチャイルド社の主張を退け、ソニー勝訴の判決を下した。同訴訟はソニーが特許を侵害しているとの陪審員評決が二月に出ていたが、ソニーが逆転勝訴した。フェアチャイルドは日立製作所、東芝など日独の大手電機メーカー二十社以上を同様の趣旨で訴えており、ソニーの勝訴は他社の審理にも影響を与えそうだ。

ソニーが十五日明らかにしたところによると、ニューヨーク東部地裁は「ソニー製のCCDはローラル・フェアチャイルド社の二件の特許に抵触しない」との判決を下し、陪審員の評決を破棄した。フェアチャイルドは控訴するかどうかの態度をまだ表明していないという。

CCDはカメラ一体型VTRやファクスなどの電子機器に使われる光学部品で、「電子の目」と呼ばれる重要部品。フェアチャイルドは自社が保有するCCDの製造プロセスと構造に関する二件の特許を侵害しているとして九一年九月、ソニーのほか日立、東芝、神戸製鋼所、松下など日独の大手各社を訴えていた。ソニーは「当社のCCDはフェアチャイルドの特許とは異なる製造プロセスと構造を採用していると主張してきたが、その正当性が認められた」としている。ただフェアチャイルドが控訴すれば、裁判が再び長期化する可能性も残っている。

From Japanese News Paper, July 16, 1996.

1996 年 7 月　　日刊工業新聞記事から

（2000 年 1 月米国最高裁で最終決着ソニー勝訴）

In January 2000, the US supreme court made the final judgement favoring Sony claims. And the long SONY-Fairchild Patent War on the PDD with the built-in vertical overflow drain (VOD) ended.

Sony Chairman Ohga and Hagiwara
at Chairman Office in Sony Tokyo Headquarter, 1996