Story of Pinned Buried Photodiode

For details, please visit http://www.aiplab.com/Story_of_Pinned_Buried_Photodiode_2021

Artificial Intelligent Partner System(AIPS)
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by Yoshiaki (Daimon) Hagiwara
IEEE Life Fellow

Born on July 4, 1948 in Kyoto Japan. Moved to USA in 1965 for studying. Graduated Riverside Polytechnic High School, Calif USA in June, 1967. Graduated Caltech in Pasadena Calif. USA with the degrees of BS in 1971, MS in 1972 and PhD in 1975. Worked for Sony Tokyo Japan from Feb 1975 till July 2008. Worked as a professor at Sojo University in Kumamoto, Japan from April 2009 till March 2017. Currently serving as the chair of the Education Committee of Society of Semiconductor Industry Specialists (http://www.ssis.or.jp).

Story of Pinned Buried Photodiode

https://www.sony.com/en/SonyInfo/News/notice/20200626/

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Sony's Representative Inventions Supporting Stacked Multi-Functional CMOS Image Sensors

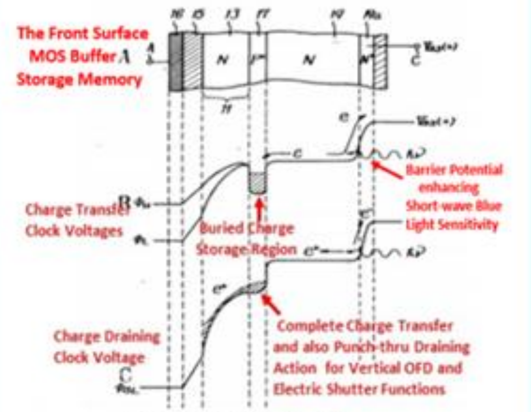
Sony Corporation
Sony Semiconductor Solutions Corporation

Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

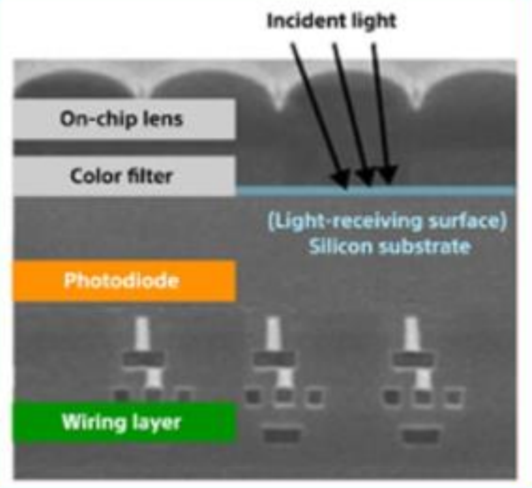
In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

Fig. 7 第7図



JPA1975-12767 with Global Shutter Function

Back-illuminated CMOS image sensor



Society of Semiconductor Industry Specialists (SSIS) Founded 1998

https://www.ssis.or.jp/en/index.html

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

Semiconductor History Museum of Japan

1975-85

Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

~ Discrete Semiconductor/Others ~

In 1975, Sony proposed using a PNP transistor as the photodetector [3]. By providing a P⁺ layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated to improve the light sensitivity greatly. It was a basic proposal for a pinned photodiode with a P⁺ layer on the surface of the light receiving part.

Next, proposals were made separately by Hitachi and Sony to use the P⁺ layer as the substrate potential. In 1977, Hitachi presented a structure in which the high-concentration surface P⁺ layer is connected to a P-type substrate (well) and pinned it to the same potential as the substrate to increase the charge storage capacity and widen the dynamic range of the photodiode [4]. In 1978, Sony announced an FT (Frame Transfer) -CCD image sensor, using the photodiode with the same structure [5]. Sony succeeded for the first time in the world in prototyping a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor that developed this technology, in 1981 [6].

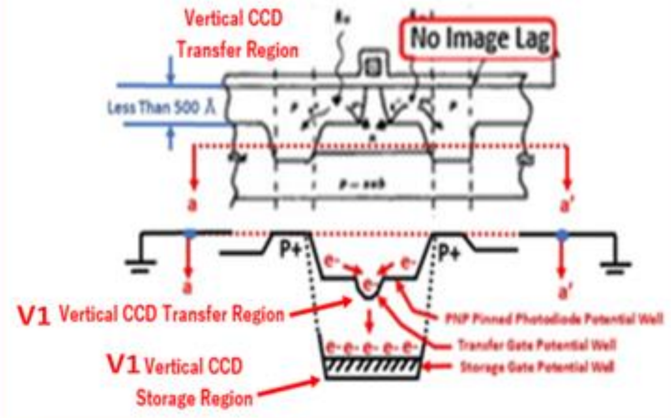
【3】Y. Hagiwara, Japanese Patent JP1975—134985

【4】N. Koike, I. Takemoto. Japanese Patent JP1977—837

【5】Y. Hagiwara, M. Abe, and C. Okada, “A 380H x 488V CCD imager with narrow channel transfer gates”, Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

Locos Free Process

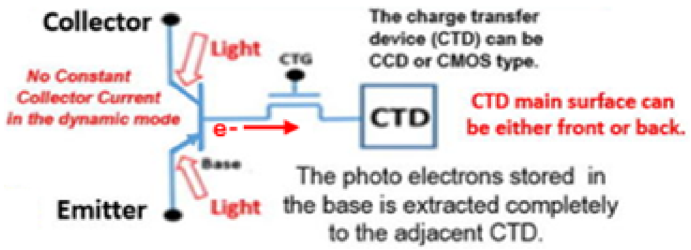
SSDM1978 Paper

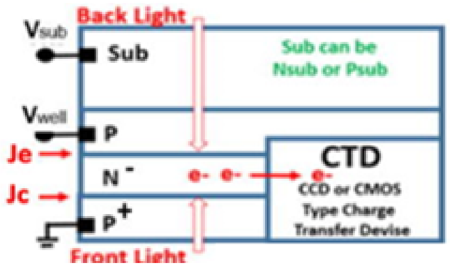


Sony 1980 Video Movie has in one body an 8 mm VTR and One Chip FT CCD Image Sensor with the PNP Double Junction type Pinned Photodiode developed by Hagiwara in 1978

Invention and Historical Development Efforts of Pinned Buried Photodiode.

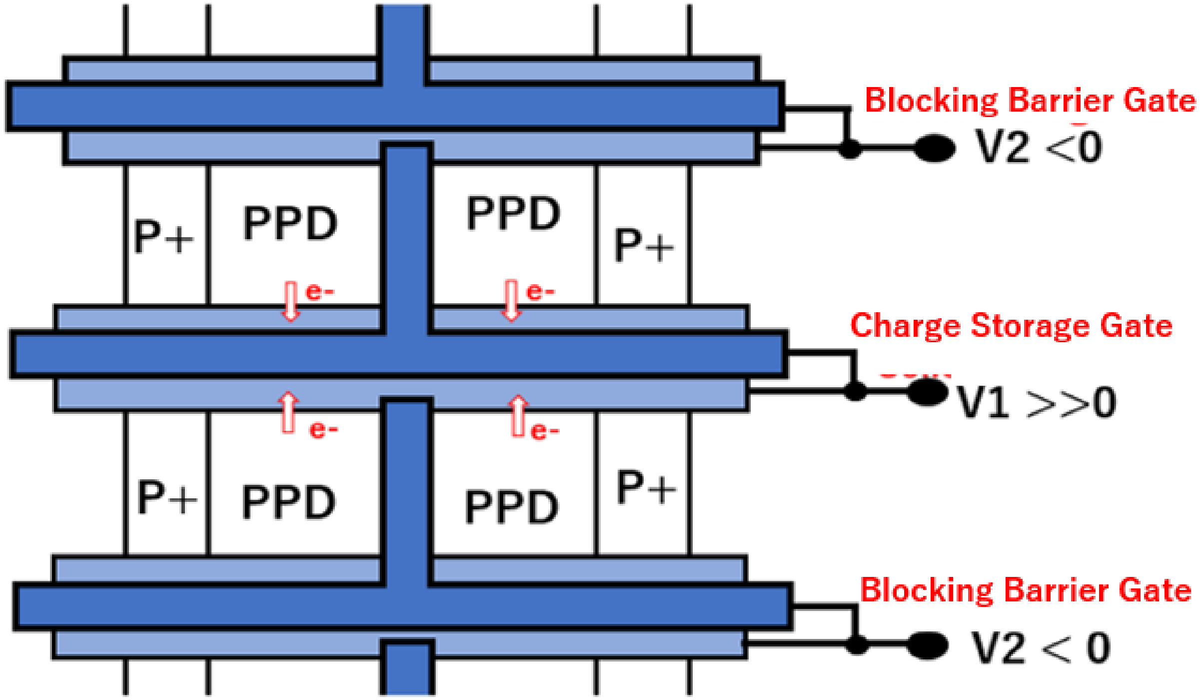
P+NP Double Junction Dynamic Photo Transistor type Pinned Buried Photodiode



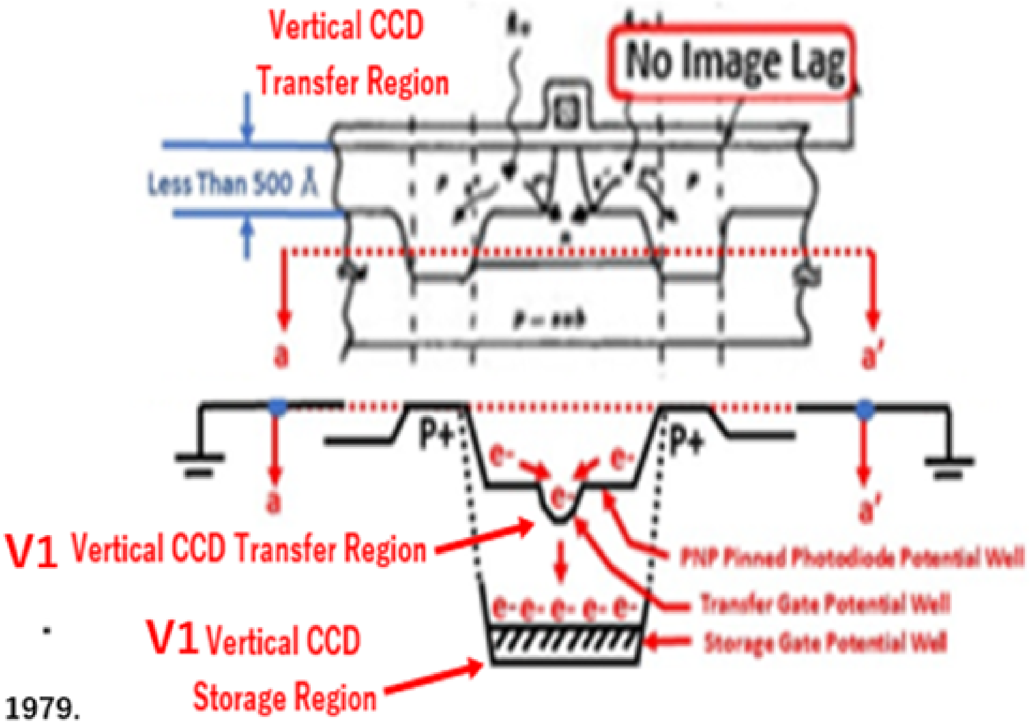


Electric Shutter Function Capability

Complete Charge Extraction from the N base region for low image lag and high speed high quality action pictures



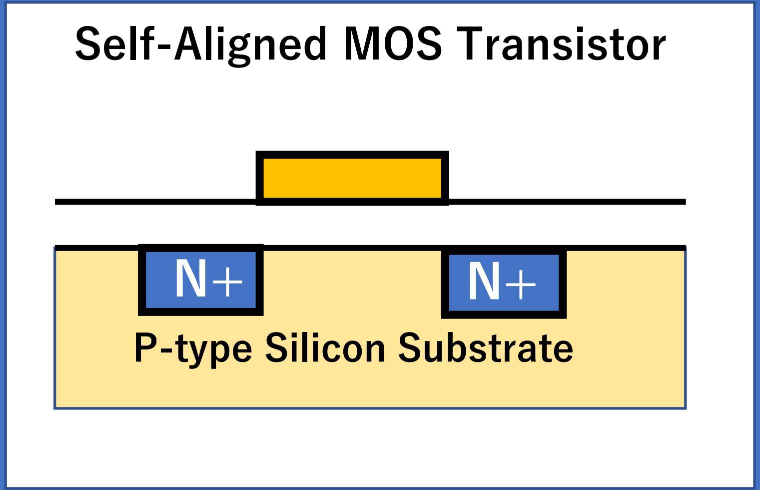
SSDM1978 Paper

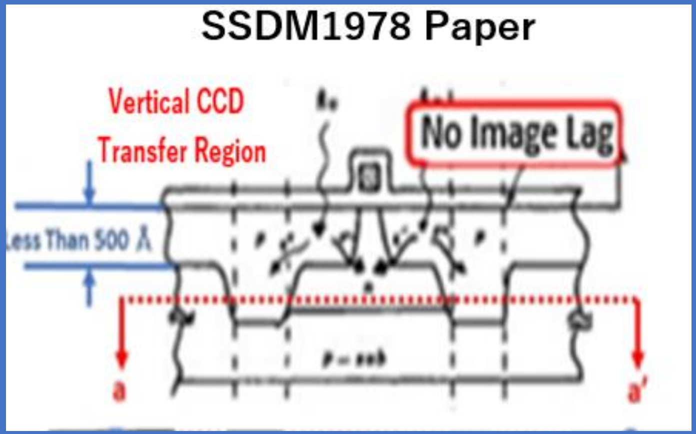


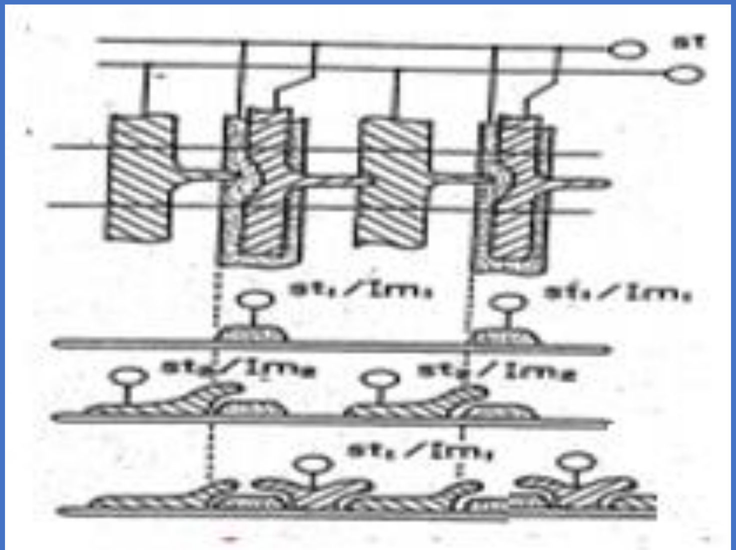
Yoshiaki Hagiwara, Motoaki Abe and Chikara Okada,
"A 380H X 488V CCD Imager with Narrow Channel Transfer Gates",
Proceeding of the 10th Conference on Solid State Devices, Tokyo 1978,
Japanese Journal of Applied Physics, Volume 18 Sup 18-1, pp. 335-340 November 1979.

The self-aligned ion implantation technology using the Polysilicon Gate Patterns as Masking invented by Dr. Robert. W. Bower in 1966.

USP3472712, Oct 17, 1966 and USP3615934, Oct 30, 1967



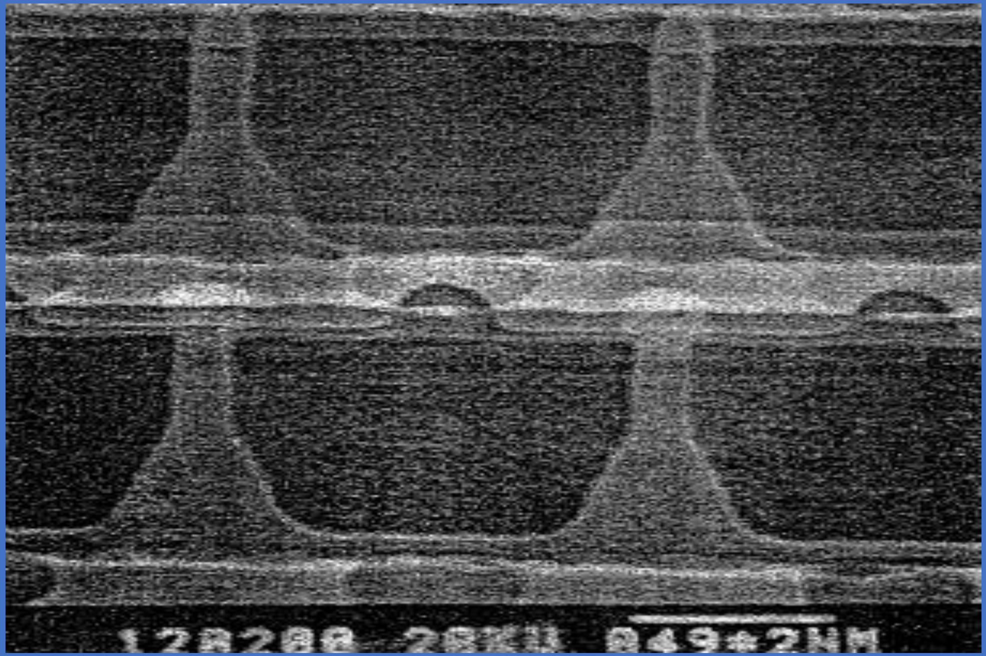




The cell size of the imaging area is 11 μm x 13 μm while the storage area has 11 μm x 13 μm cell size to keep the area occupation in the chip to the minimum.

The chip size of the device is 10.0 mm x 12.5 mm. The device is fabaricated in a buried-channel version of a-type (100) oriented 10-15Ω・cm silicon substrate with standard triple-layer overlapping-electrode-type polysilicon gate definition with the self-aligned boron atom ion implantation technology.

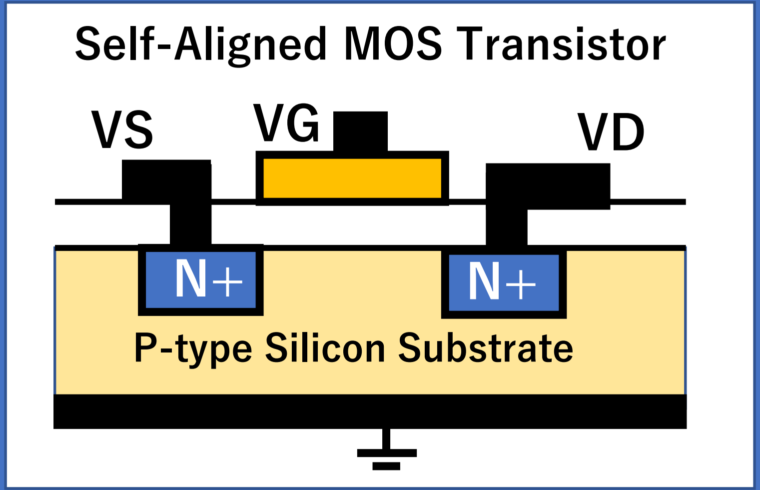
Using the polysiliocn patterning as an ion implantation mask, boron ions with a dose level of 7 x $10^{12}cm^{-2}$ were implanted into the silicon substrate throughout the exposed portions of the thermall grown oxide The step provides self-aligned channel stops which surround the narrow-channel transfer part of each electrode.

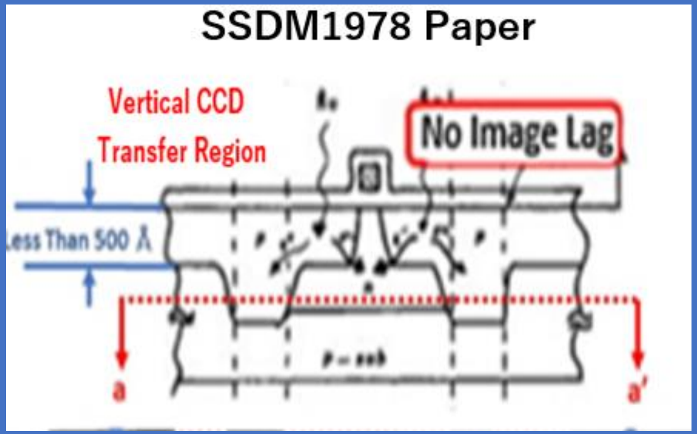


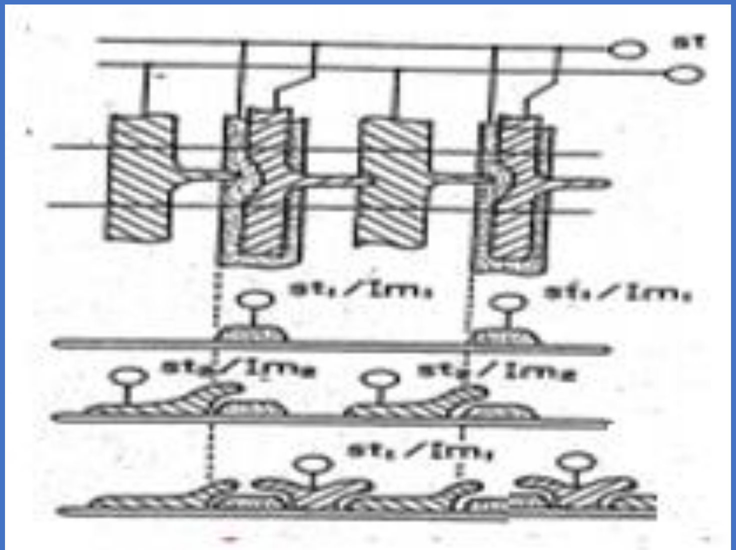
(a) SEM picture of storage area.
Cell size is 11 μmH x 9 μmV

The self-aligned ion implantation technology using the Polysilicon Gate Patterns as Masking invented by Dr. Robert. W. Bower in 1966.

USP3472712, Oct 17, 1966 and USP3615934, Oct 30, 1967



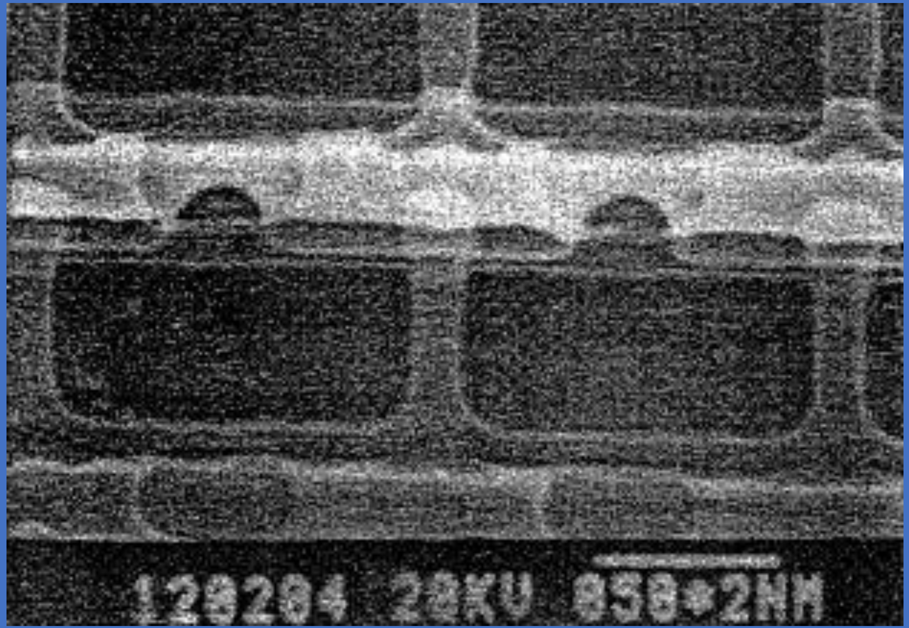




Since the early 1960's, this technique of ion implantation into the silicon substrate, has been known to produce many practical device structures.

The polysilicon patterns were used then for the masking of the ion implantation technology, as originally invented by Dr. Robert Bower in 1966. And it is now widely used to form the source and drain of self-aligned polysilicon gate CMOS transistors.

It is a very basic and practical technique. And it is now applied here to form the shallow junction layer at the Si-SiO2 interface of the image sensing element, which is now called as the hole accumulation diode (SONY HAD sensor), which is also identical to the widely known Pinned Buried Photodiode as invented in 1975 by Hagiwara at Sony and developed by Hagiwara Team at Sony in 1978.



(b) SEM picture of imaging area.
Cell size is 11 μmH x 13 μmV

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Semiconductor History Museum of Japan

1975-85

Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

~ Discrete Semiconductor/Others ~

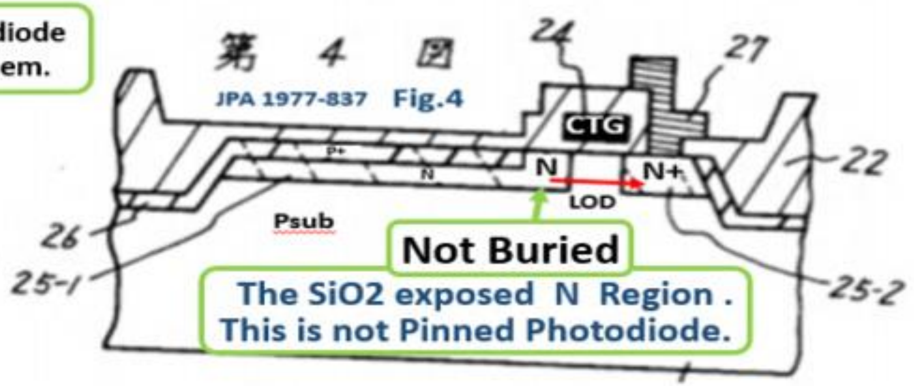
Japanese Patent JPA 1977-837

This patent is applied for the lateral overflow drain (LOD) function. The excess charge is drained to the N+ lateral output drain (LOD).

This SiO2 surface exposed photodiode has the serious Image lag problem.

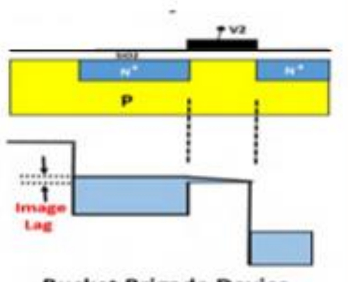
⑭固体撮像装置

㉑特　願　昭52—837
㉒出　願　昭52(1977) 1 月10日
㉗発　明　者　小池紀雄
①特許出願公開　昭53—86516



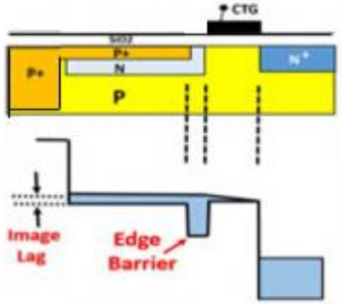
【3】Y. Hagiwara, Japanese Patent JP1975—134985
【4】N. Koike, I. Takemoto. Japanese Patent JP1977—837
【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

(1) Floating Surface N+P Single Junction type Photodiode with BBD Barrier causing the serious Image Lag problem



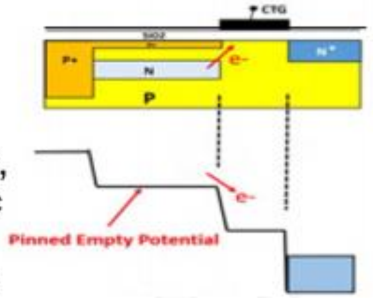
JPA1977-837

(2) Partially Pinned but Floating Surface and not Buried Photodiode with the BBD Barrier causing the serious Image Lag problem



SSDM1978

(3) Completely Pinned Buried Photodiode with no BBD barrier and the complete charge transfer capability of the no-image-lag feature, achieving the electric shutter function for the instant snapshot and fast motion pictures



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For details, please visit http://www.aiplab.com/Story_of_Pinned_Buried_Photodiode_2021

⑲日本国特許庁(JP) ⑪特許出願公開

⑫公開特許公報(A) 昭54—95116

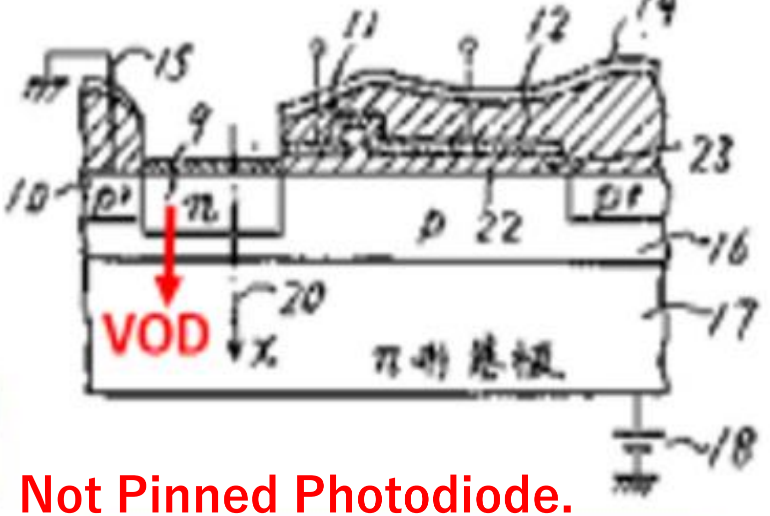
㊸公開 昭和54年(1979)7月27日

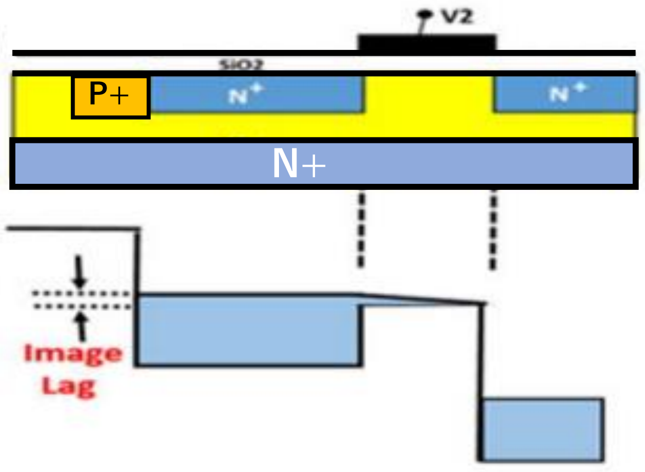
㉔固体撮像装置

㉑特 願 昭53—1971

㉒出 願 昭53(1978)1月13日

㉒発 明 者 山田哲生





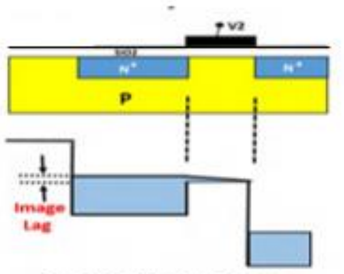
Bucket Brigade Device (BBD)

Not Pinned Photodiode.

This is a floating surface double junction photodiode with the vertical overflow drain (VOD) function with serious image lag problem.

Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

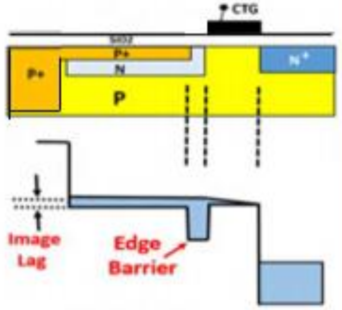
(1) Floating Surface N+P Single Junction type Photodiode with BBD Barrier causing the serious Image Lag problem



Bucket Brigade Device (BBD)

JPA1977-837

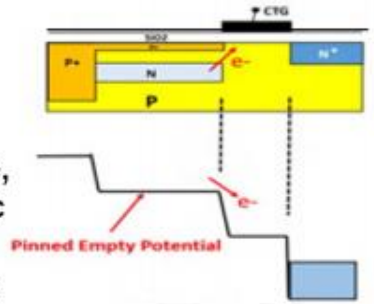
(2) Partially Pinned but Floating Surface and not Buried Photodiode with the BBD Barrier causing the serious Image Lag problem



Buried Photodiode with BBD Barrier

SSDM1978

(3) Completely Pinned Buried Photodiode with no BBD barrier and the complete charge transfer capability of the no-image-lag feature, achieving the electric shutter function for the instant snapshot and fast motion pictures



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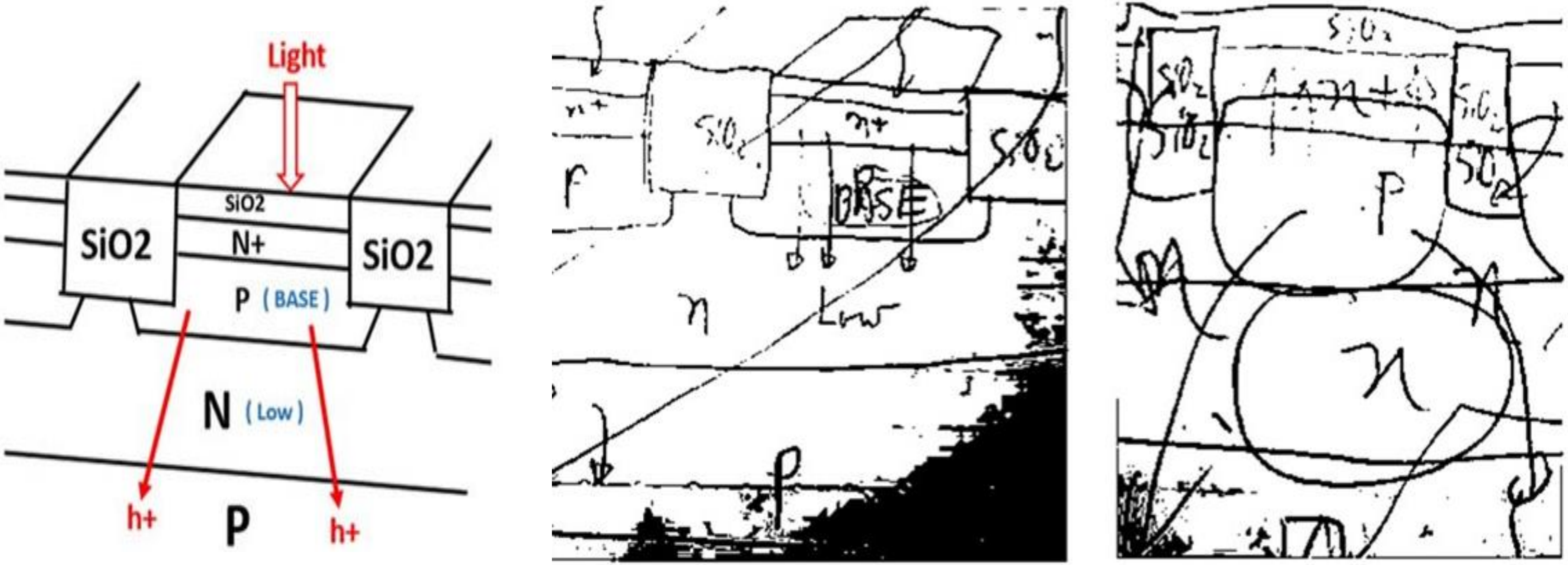


Hagiwara's Lab Note at Sony in February 1975

ELECTRICALENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

This is a commonly misunderstood misused set of terminologies.

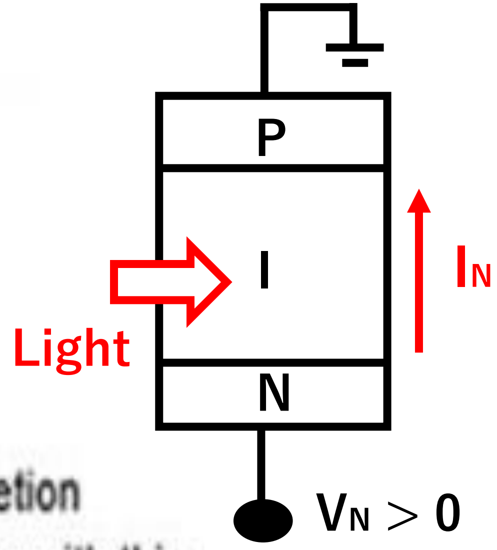
First off these are not PIN Photodiodes - which stands for P - Intrinsic- N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though.

Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space.

You can get surface state pinning from the dangling Si/SiO2 bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The

PIN Photodiode

Nishizawa, 1950



https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

ELECTRICALENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

(Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The Si/SiO2 surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface.

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

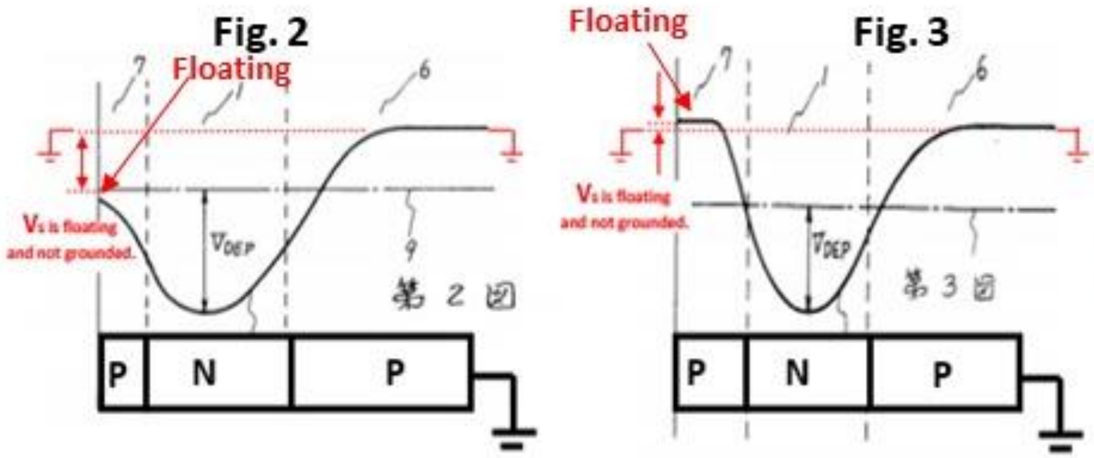
ELECTRICAL ENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

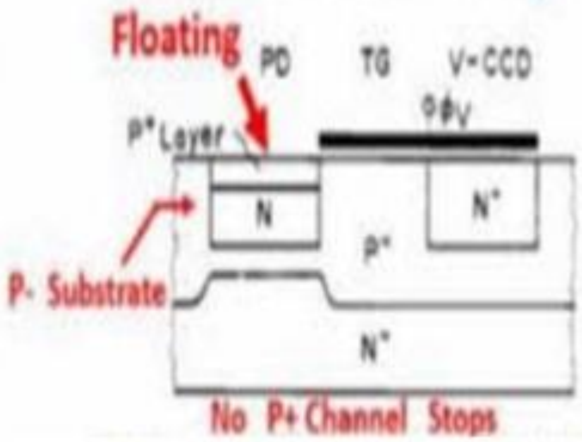
I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

"The first Pinned Photodiode was invented by Hagiwara at Sony."
"It has long been incorrectly attributed to Teranish and to Fossum."

Teranishi at NEC Patent filed Japanese Patent Application JPA 1980-138026 on Buried Photodiode with Fig. 2 and Fig.3 shown below. Observe that the surface potential in Fig.2 is not pinned. It has an undesired surface electric field which induces the serious surface dark current noise problem. Observe also that the surface potential in Fig.2 is not pinned to the substrate ground potential. This is NOT Pinned Photodiode.



The surface P region is NOT pinned. See Fig.2 of JPA1980-138026



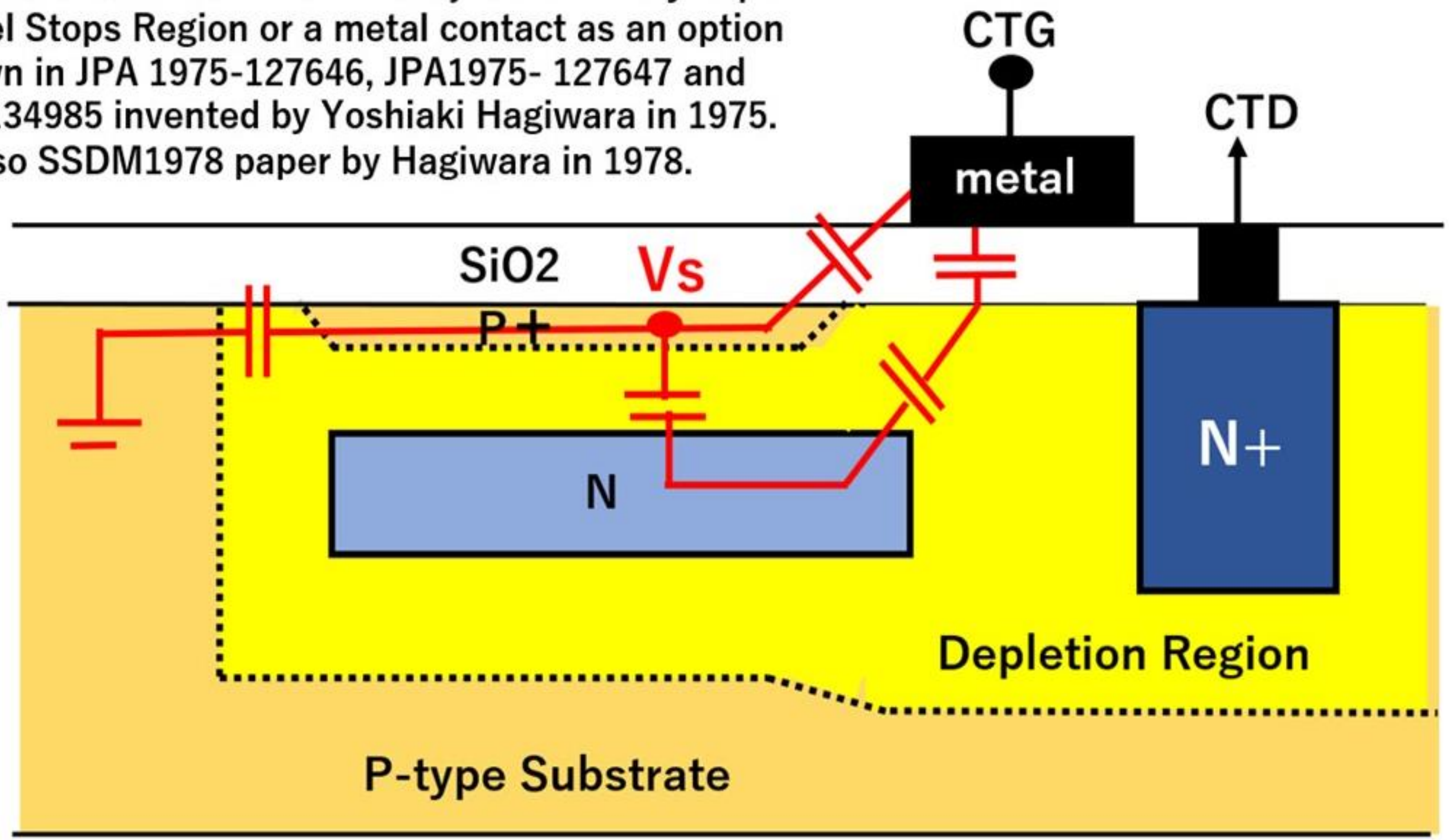
The Buried Photodiode reported in NEC IEDM1982 Paper

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

Buried Photodiode with Floating P+ Surface of Serious Image Lag Problem

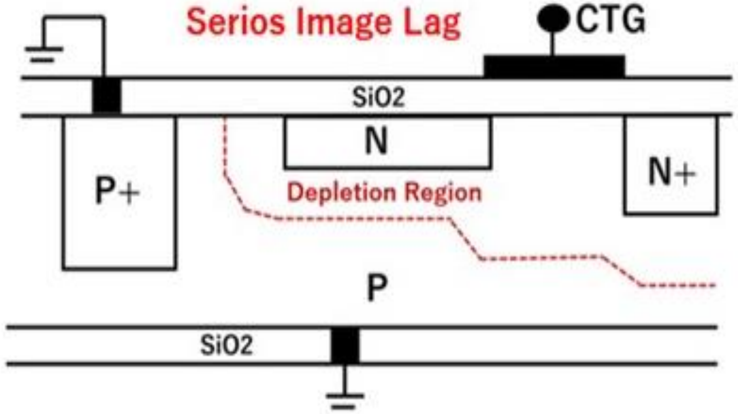
The parasitic capacitance coupling with the surrounding depletion region and the gate oxide.

Pinned Photodiode must have the adjacent heavily doped P+ Channel Stops Region or a metal contact as an option as shown in JPA 1975-127646, JPA1975- 127647 and JPA 1975-134985 invented by Yoshiaki Hagiwara in 1975. See also SSDM1978 paper by Hagiwara in 1978.

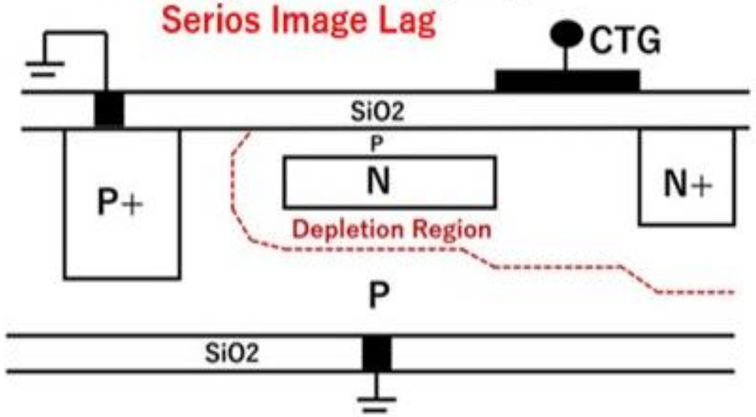


Four Types of Basic Photo Sensor Structures

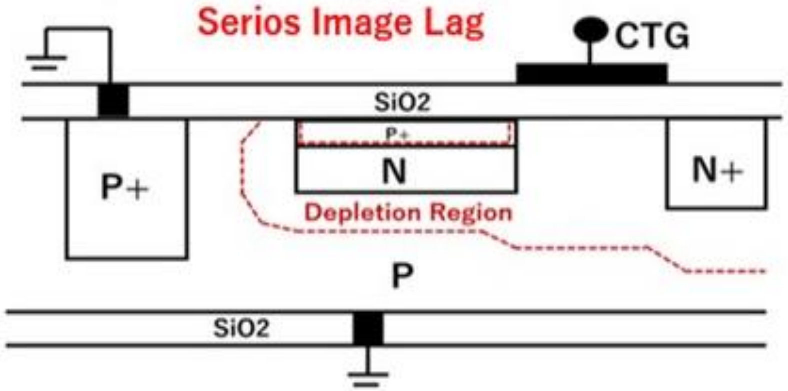
(A) Classical N+P Single Junction type Photodiode with the floating surface N storage region



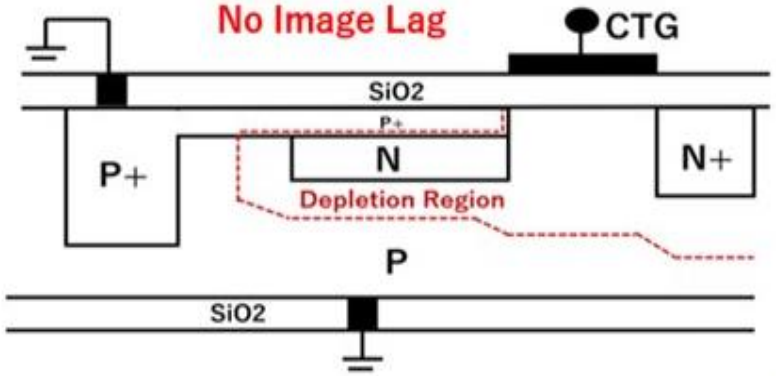
(B) Double Junction PNP type Buried Photodiode with the floating surface P region and the floating buried N storage region

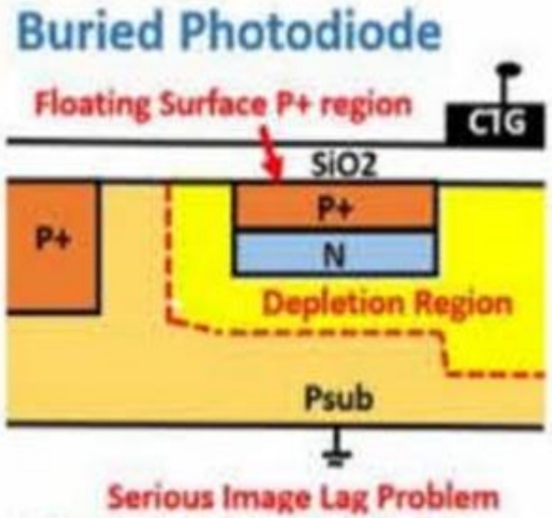


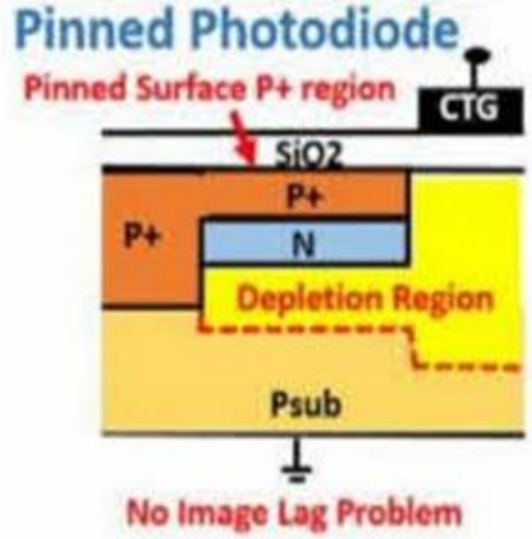
(C) Double Junction P+NP type Buried Photodiode with the floating surface P+ hole accumulation region and the floating N Storage Region.



(D) Double Junction P+NP type Pinned Photodiode with the pinned surface P+ hole accumulation region and the pinned N Storage Region



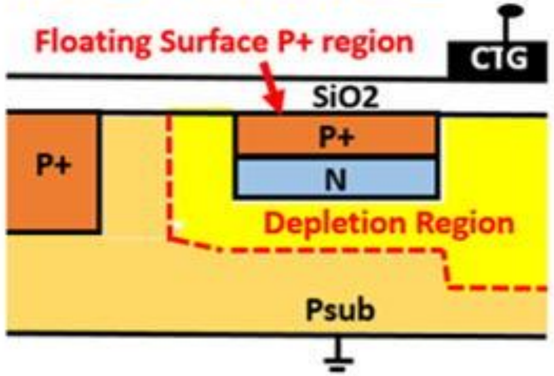




Difference of Buried Photodiode and Pinned Photodiode

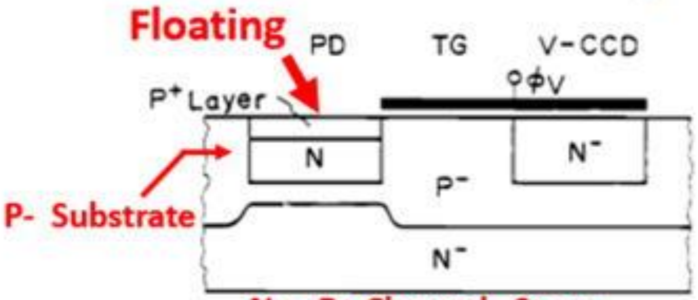
Figure 5 does not have the P+ channel stop nearby.

Buried Photodiode



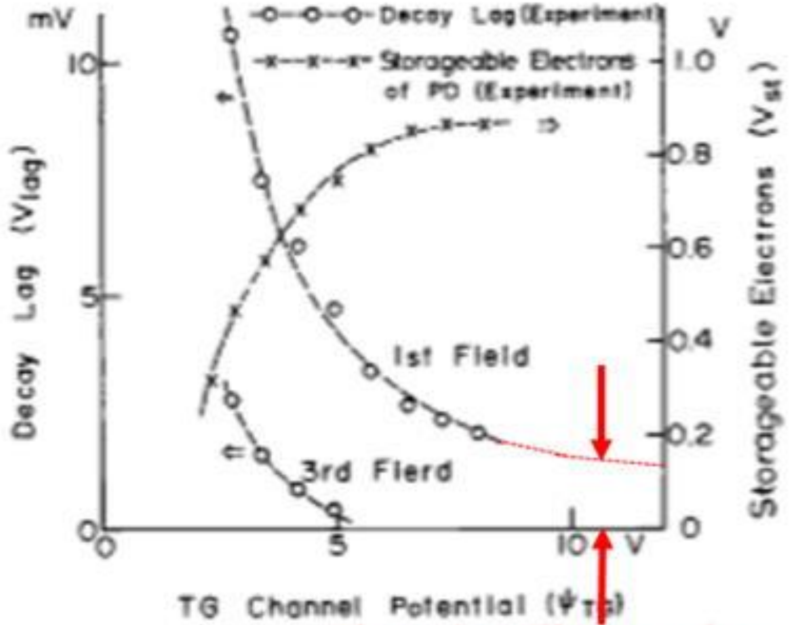
Serious Image Lag Problem

NEC IEDM1982 Paper



No P+ Channel Stops

Fig.5. P+NP- structure photodiode
(a) Unit cell cross sectional view



There is still image lag
at the CTD gate voltage more than 10 volt.

Fig.6. Storageable electrons vs. transfer gate channel potential, and decay lag vs. transfer gate channel potential in the P+NP- structure photodiode

NEC IEDM1982 Paper reported Image Lag

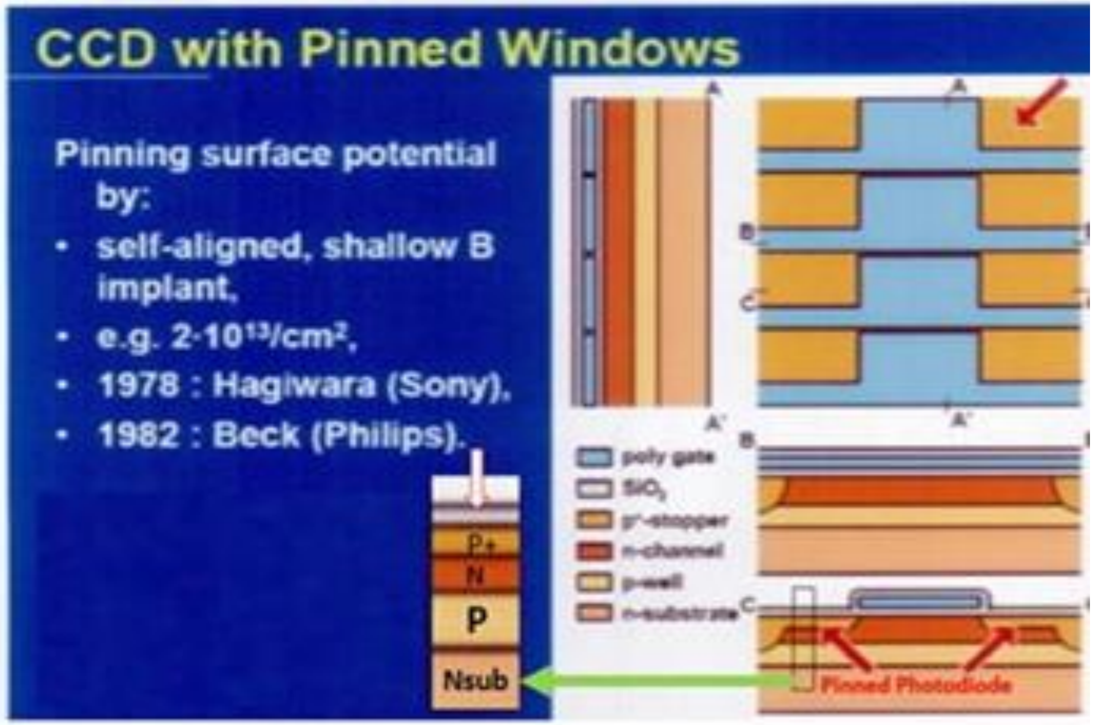
Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 volt.

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO. 12, DECEMBER 2006

The Hole Role in Solid-State Imagers

Albert J. P. Theuwissen, *Fellow, IEEE*

Despite these advantages, notice that parts of the depleted n-type CCD channels are not covered by gate material. In this way, their electrostatic potential is not defined! Such a structure will suffer from serious charge transport issues during its operation, because charge can and will be trapped in local potential pockets. The effect can simply be solved by defining the potential in the open areas through an extension of the p^+-channel stopper. A simple self-aligned p-implant of $2 \cdot 10^{13}/cm^2$ B-ions after the gate construction is sufficient to extend the channel stop area to the gate edge and, consequently, fix the potential in the open areas. The result after this self-aligned implant is shown in Fig. 4. The presence of enough holes plays a crucial role in fixing the potential for the regions normally "beyond control" of the gates. [Is this structure the mother of the PPD or buried diode or hole-accumulation device (HAD)?]



Albert Theuwissen quoted Hagiwara 1978 paper and explained the importance of hole role in image sensors @ Workshop on CMOS Imaging, Duisburg May 16, 2006

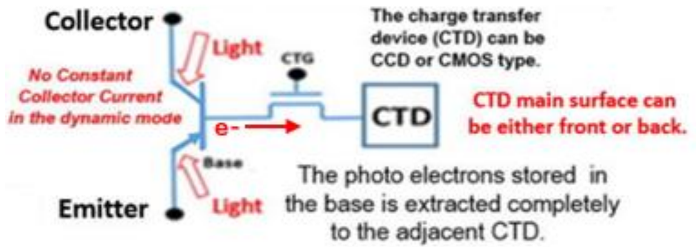
Direct Quotation

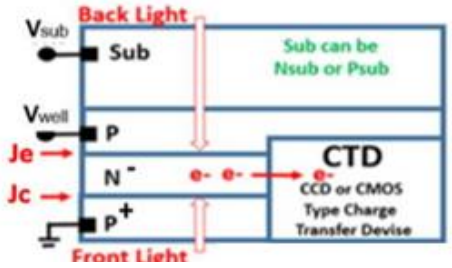
The presence of enough holes plays a crucial role in fixing the potential for the regions normally "beyond control" of the gates. [Is this structure the mother of the PPD or buried diode or hole-accumulation device (HAD)?]

Quoted directly from IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL.53, No.12, DEC 2006

Invention and Historical Development Efforts of Pinned Buried Photodiode.

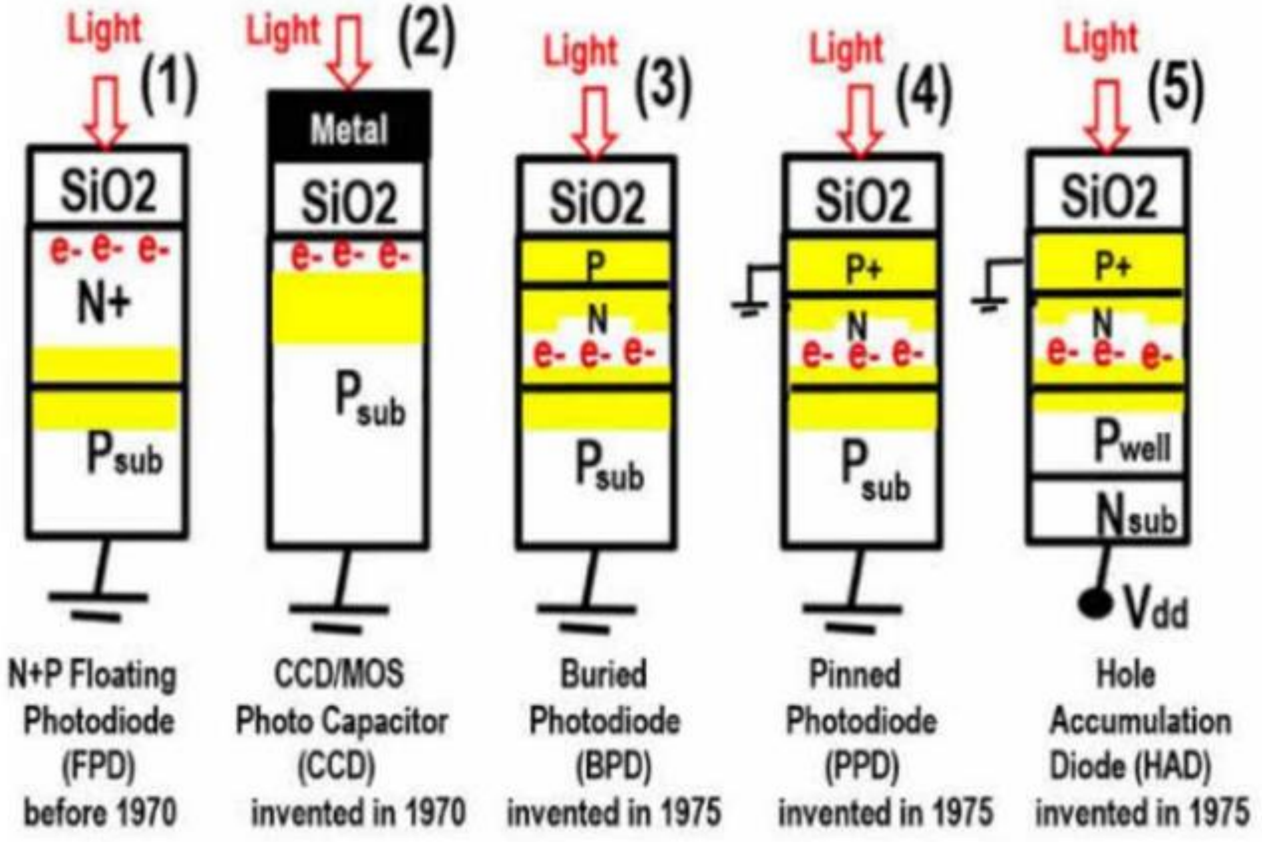
(3) P+NP Double Junction Dynamic Photo Transistor type Pinned Buried Photodiode



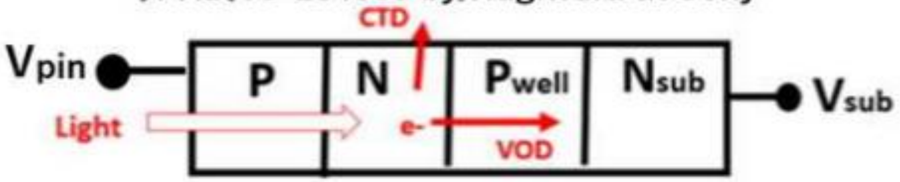


Electric Shutter Function Capability

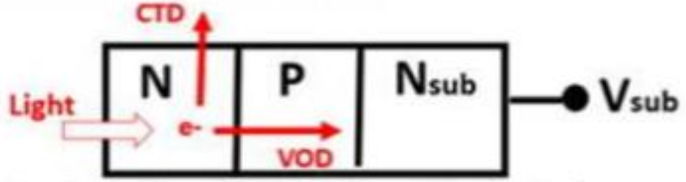
Complete Charge Extraction from the N base region for low image lag and high speed high quality action pictures



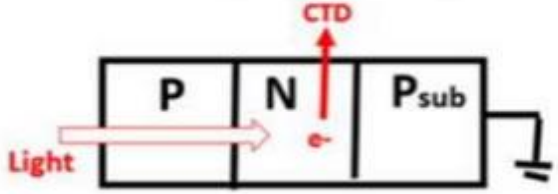
(5) Triple Junction Pinned Photodiode on Substrate
JPA1975-134985 by Hagiwara at Sony



(5a) Floating Surface Double Junction Photodiode
JPA1978-1971 by Yamada at Toshiba



(5b) Floating Surface Double Junction Photodiode
JPA1978-1971 by Teranishi et al at NEC

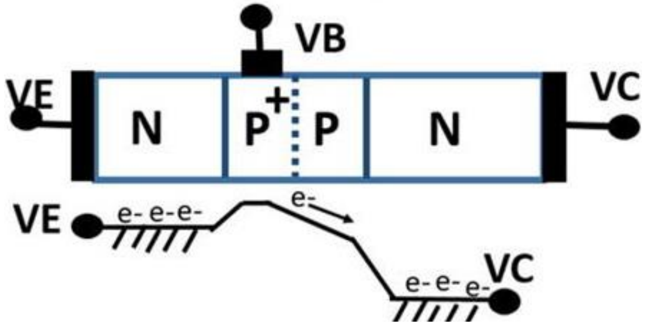


Historical Developments of Five types of Basic Photo Sensors Structures.

Invention and Historical Development Efforts of Pinned Buried Photodiode.

JPA1975-127646, JPA1975-127647 and JPA1975-134986 are the evidence that Yoshiaki Hagiwara at Sony is the inventor of Pinned Buried Photodiode and the SSDM1978 paper by Hagiwara team in Sony is the evidence that Hagiwara developed the first Pinned Buried Photodiode with the no-image-lag feature, the low surface dark current and the excellent short-wave blue-light sensitivity.

Drift Field Transistor



Herbert Kroemer,1953

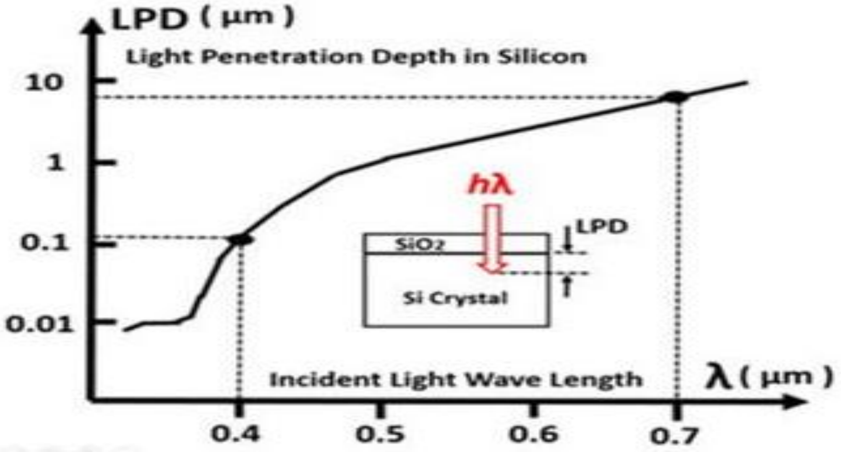
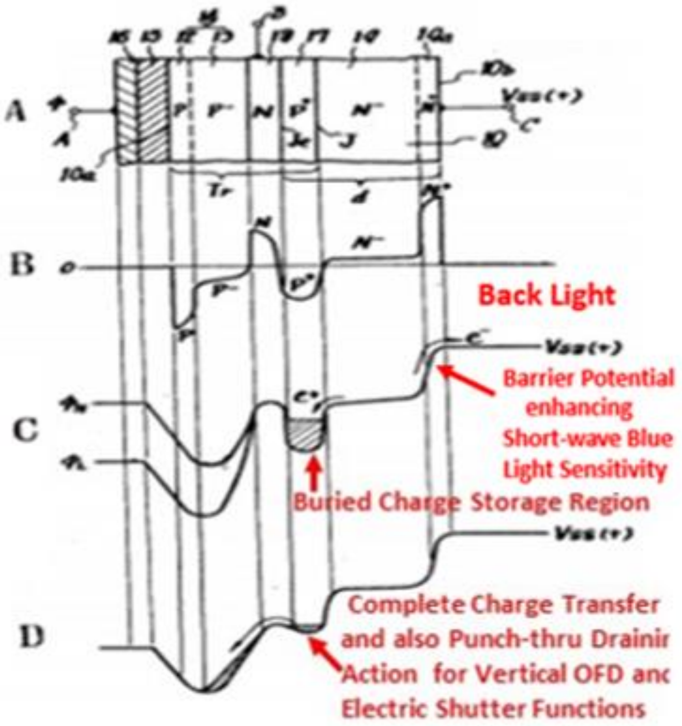


Fig. 7 第7図



JPA1975-127646 with Global Shutter Function

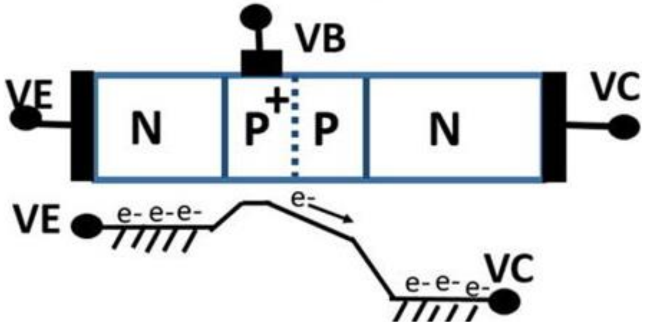
JPA1975-127646

N+N-P+NP-P Triple Junction Dynamic Photo Thyristor type Pinned Surface Buried Storage Photodiode
No Image Lag Problem
No Surface Dark Current Noise
Excellent Short-Wave Light Sensitivity

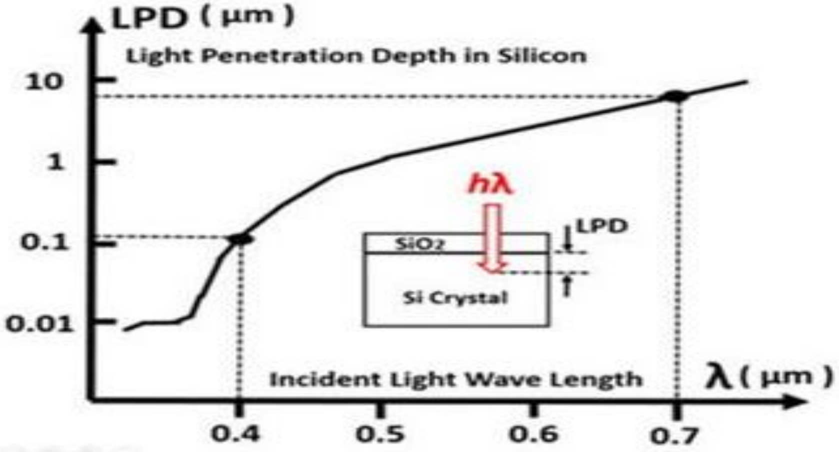
Invention and Historical Development Efforts of Pinned Buried Photodiode.

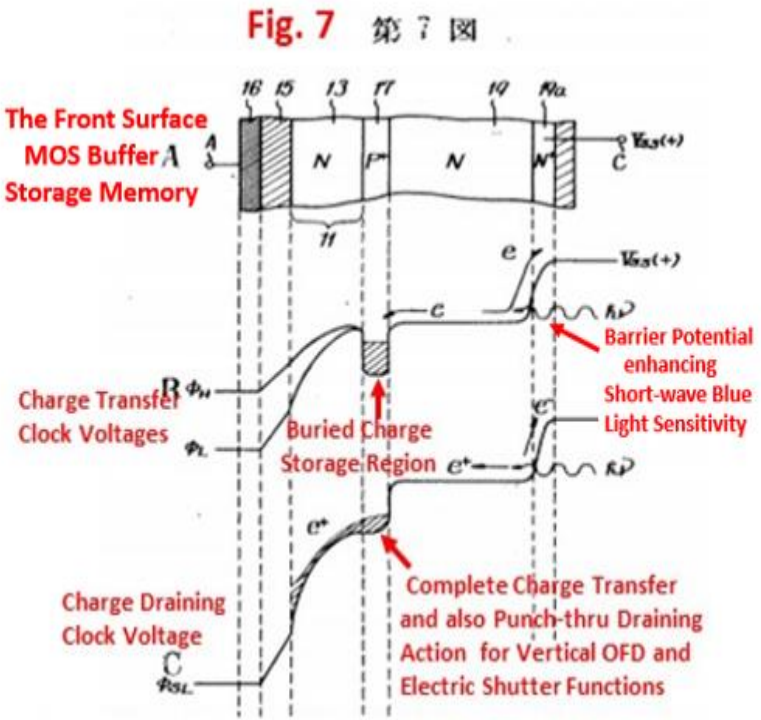
JPA1975-127646, JPA1975-127647 and JPA1975-134986 are the evidence that Yoshiaki Hagiwara at Sony is the inventor of Pinned Buried Photodiode and the SSDM1978 paper by Hagiwara team in Sony is the evidence that Hagiwara developed the first Pinned Buried Photodiode with the no-image-lag feature, the low surface dark current and the excellent short-wave blue-light sensitivity.

Drift Field Transistor



Herbert Kroemer,1953





JPA1975-127647 with Global Shutter Function

JPA1975-127647

N+NP+N Double Junction Dynamic Photo Transistor type Pinned Surface Buried Storage Photodiode
No Image Lag Problem
No Surface Dark Current Noise
Excellent Short-Wave Light Sensitivity

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JPA1975-134985

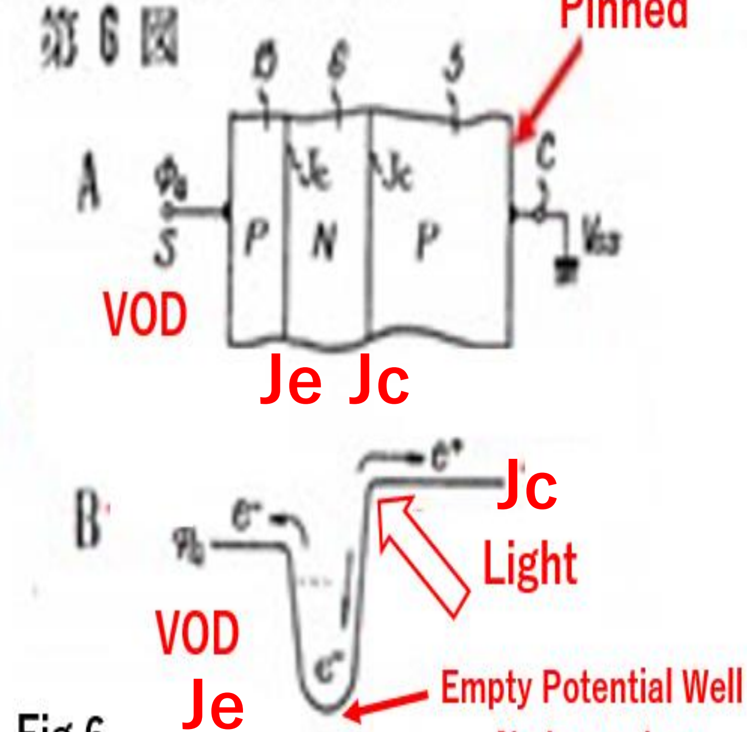
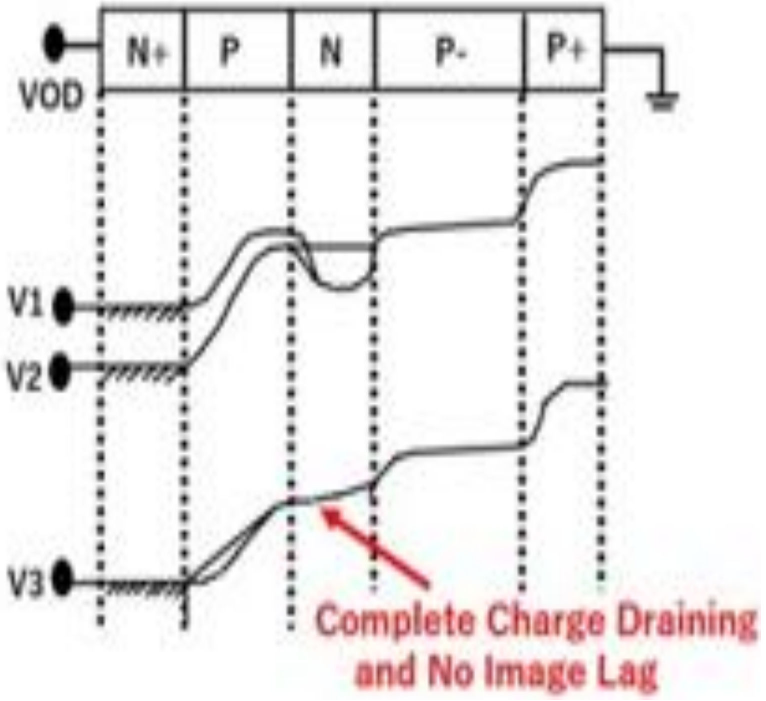


Fig.6

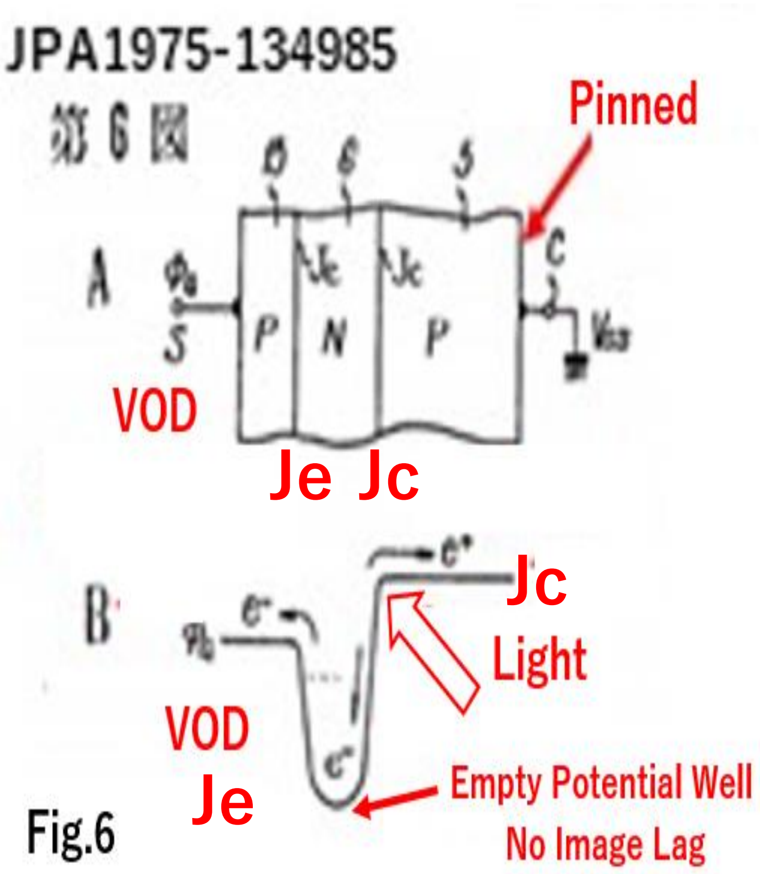


JPA1975-134985 with In-Pixel Vertical Overflow Drain (VOD)

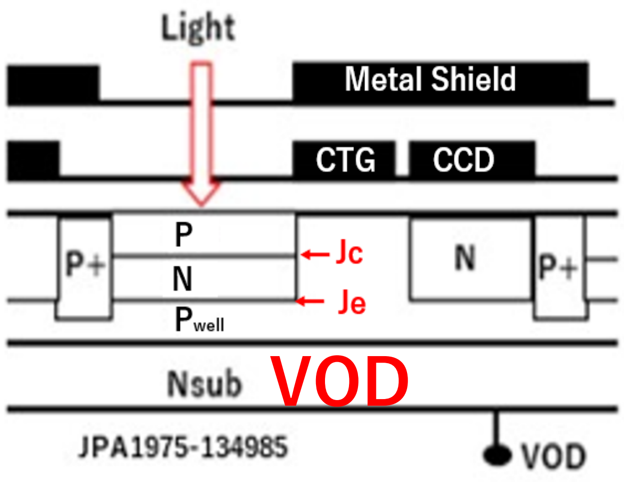
JPA1975-134985
PNP Double Junction Dynamic Photo Transistor type Pinned Surface Buried Storage Photodiode
No Image Lag Problem
No Surface Dark Current Noise
Excellent Short-Wave Light Sensitivity

Invention and Historical Development Efforts of Pinned Buried Photodiode.

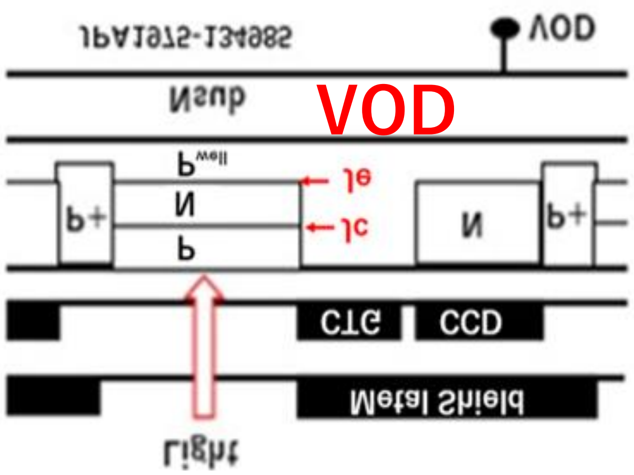
In Figure 6, Light is at Jc side VOD is at Je side



Unit Pixel of Interline CCD Image Sensor



Upside Down Mirror Image



Original Japanese Patent Claims

JPA1975-134985

特許請求の範囲

半導体基体に、第1導電型の第1半導体領域と、之の上に形成された第2導電型の第2半導体領域とが形成されて光感知部と之よりの電荷を転送する電荷転送部とが上記半導体基体の主面に沿り如く配置されて成る固体撮像装置に於いて、上記光感知部の上記第2半導体領域に整流性接合が形成され、該接合をエミッタ接合とし、上記第1及び第2半導体領域間の接合をコレクタ接合とするトランジスタを形成し、該トランジスタのベースとなる上記第2半導体領域に光学像に応じた電荷を蓄積し、ここに蓄積された電荷を上記転送部に移行させて、その転送を行うようにしたことを特徴とする固体撮像装置。

Invention and Historical Development Efforts of Pinned Buried Photodiode.

English Translation of JPA1975-134985

On a semiconcucntor substrate (Nsub), formig the first region (P) and also forming the second region (N) upon it, the photo detecting part is formed, from which the photo charge is tranfered to the charge transfer device placed along the semiconducor surface. On the second region a rectifying junction is formed and called as the emitter junction (Je). A transistor structure is formed then with the collector junction (Jc) between the first region (N) and the seoncd region (P). The base region (N) of the transistor structure stores the signal charge according to the illuminated light intensity, from which photo charge is tranfered to charge transfer device.

Original Japanese Patent Claims

JPA1975-134985

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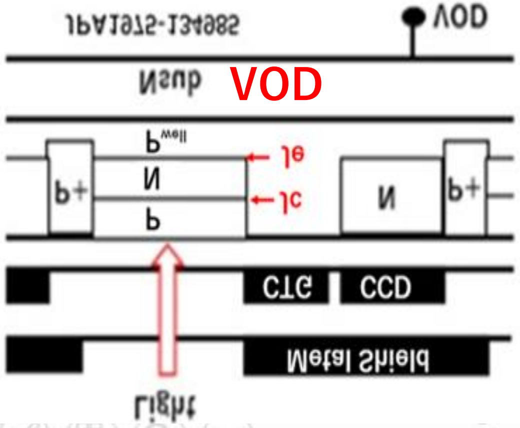
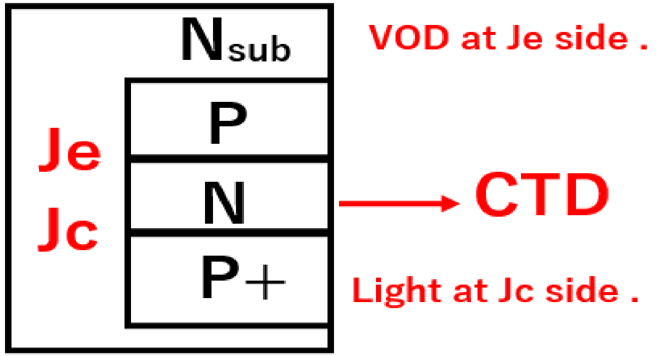
半導体基体に、第1導電型の第1半導体領域と、之の上に形成された第2導電型の第2半導体領域とが形成されて光感知部と之よりの電荷を転送する電荷転送部とが上記半導体基体の主面に沿う如く配置されて成る固体撮像装置に於いて、上記光感知部の上記第2半導体領域に整流性接合が形成され、該接合をエミッタ接合とし、上記第1及び第2半導体領域間の接合をコレクタ接合とするトランジスタを形成し、該トランジスタのベースとなる上記第2半導体領域に光学像に応じた電荷を蓄積し、ここに蓄積された電荷を上記転送部に移行させて、その転送を行うようにしたことを特徴とする固体撮像装置。

Upside Down Mirror Image



Structure defined in JPA1275-134985



Invention and Historical Development Efforts of Pinned Buried Photodiode.

English Translation of JPA1975-134985

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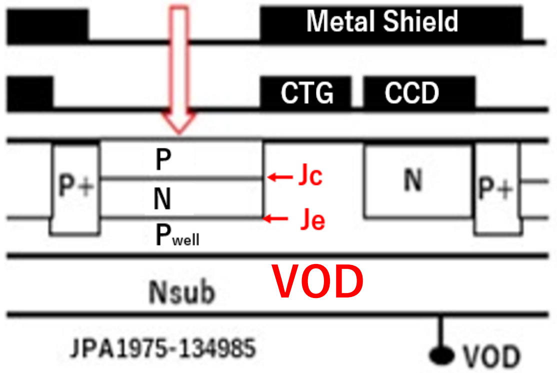
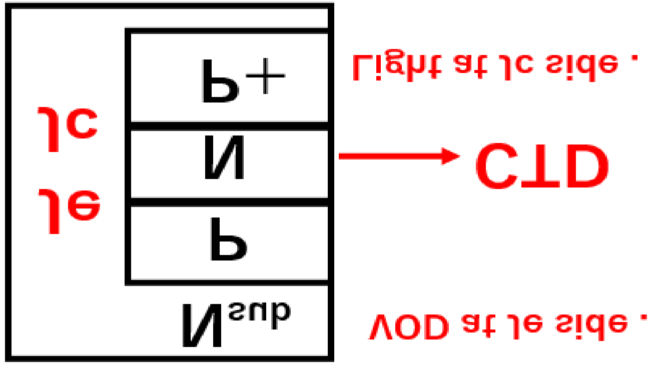
In Figure 6,
Light is at Jc side
VOD is at Je side

Original Sensor Structure



Upside Down Mirror Image of
Structure defined in JPA1275-134985



JPA1975-134985

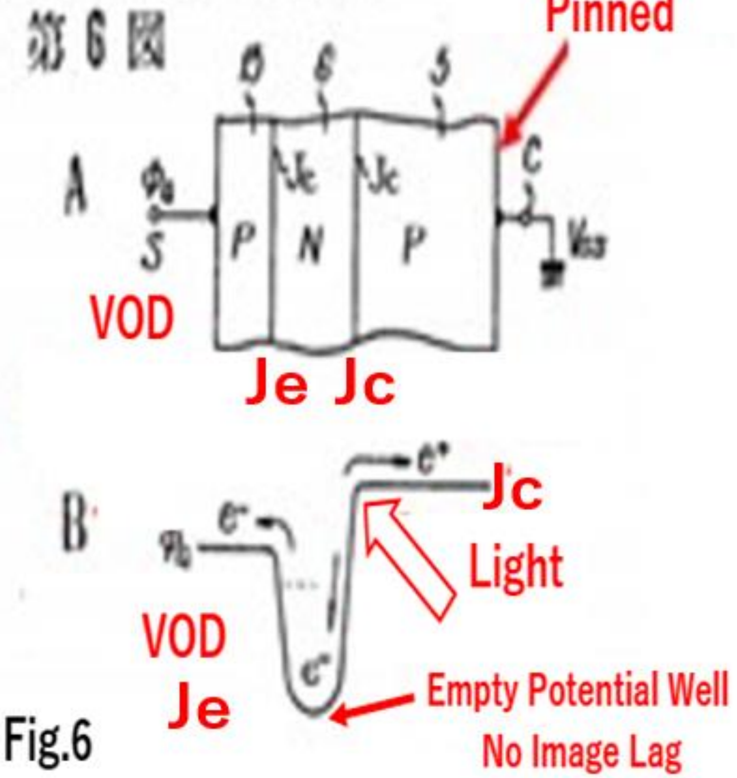
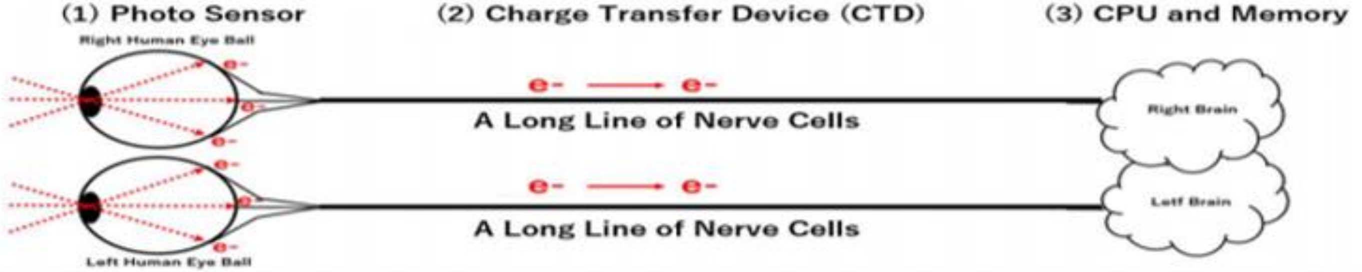


Fig.6

Invention and Historical Development Efforts of Pinned Buried Photodiode.

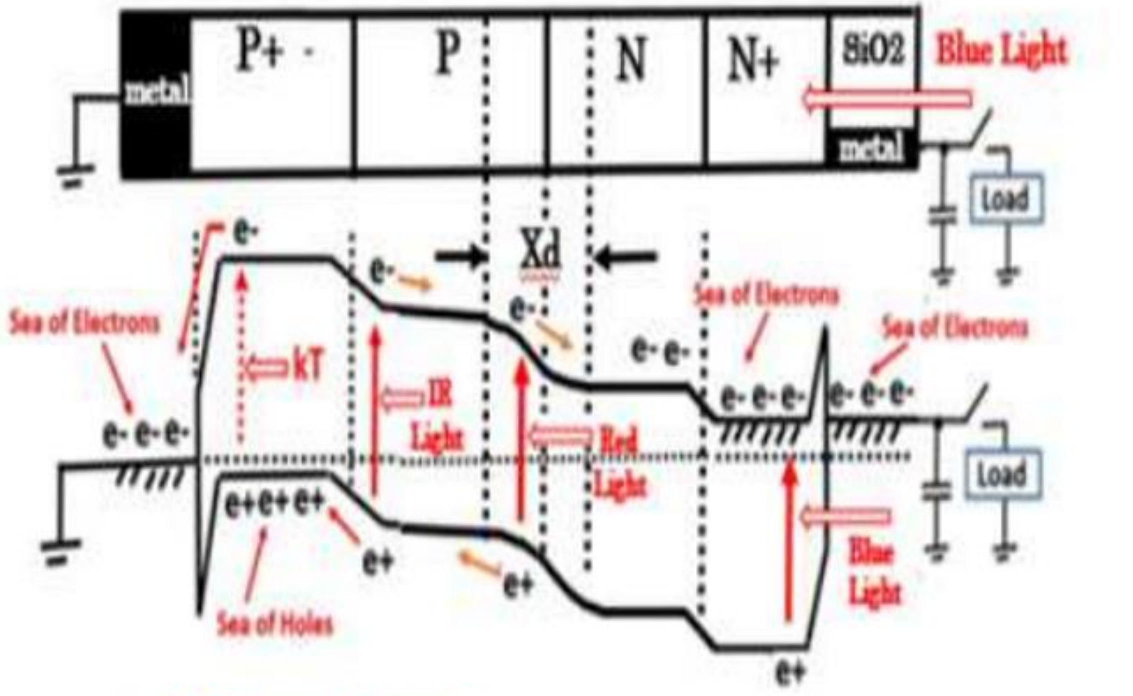
An image sensor is composed of three basic components, (1)Photo Sensor , (2)Charge Transfer Device (CTD) and (3)CPU and Memory



Three important Features \ Three types of Photo Sensing Devices	1	2	3
	N+P Single Junction Photodiode with Floating N+ Surface	Charge Couple Device CCD/MOS Dynamic Photo Capacitor	P+NP Double Junction Dynamic Photo Transistor Pinned Buried Photodiode
1 Image Lag Problem	Serious Image Lag Problem	No Image Lag Problem	No Image Lag Problem
2 Surface Dark Current Noise	No Surface Dark Current Noise	Serious Surface Dark Current Noise	No Surface Dark Current Noise
3 Short-Wave Light Sensitivity	Poor Short-Wave Light Sensitivity	Very Poor Short-Wave Light Sensitivity	Excellent Short-Wave Light Sensitivity

(1)	N+P Single Junction Photodiode with Floating N+ Surface	Serious Image Lag Problem	No Surface Dark Current Noise	Poor Short-Wave Light Sensitivity

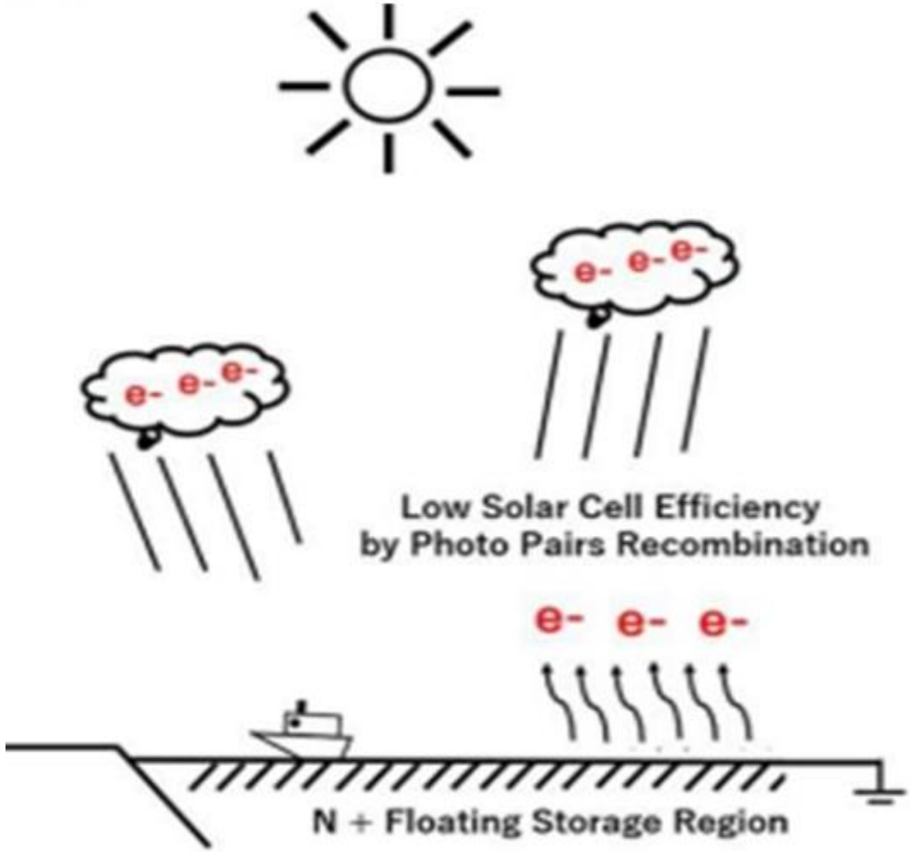
(1) Floating Surface N+NPP+ Single Junction Photodiode



Serious Image Lag Problem

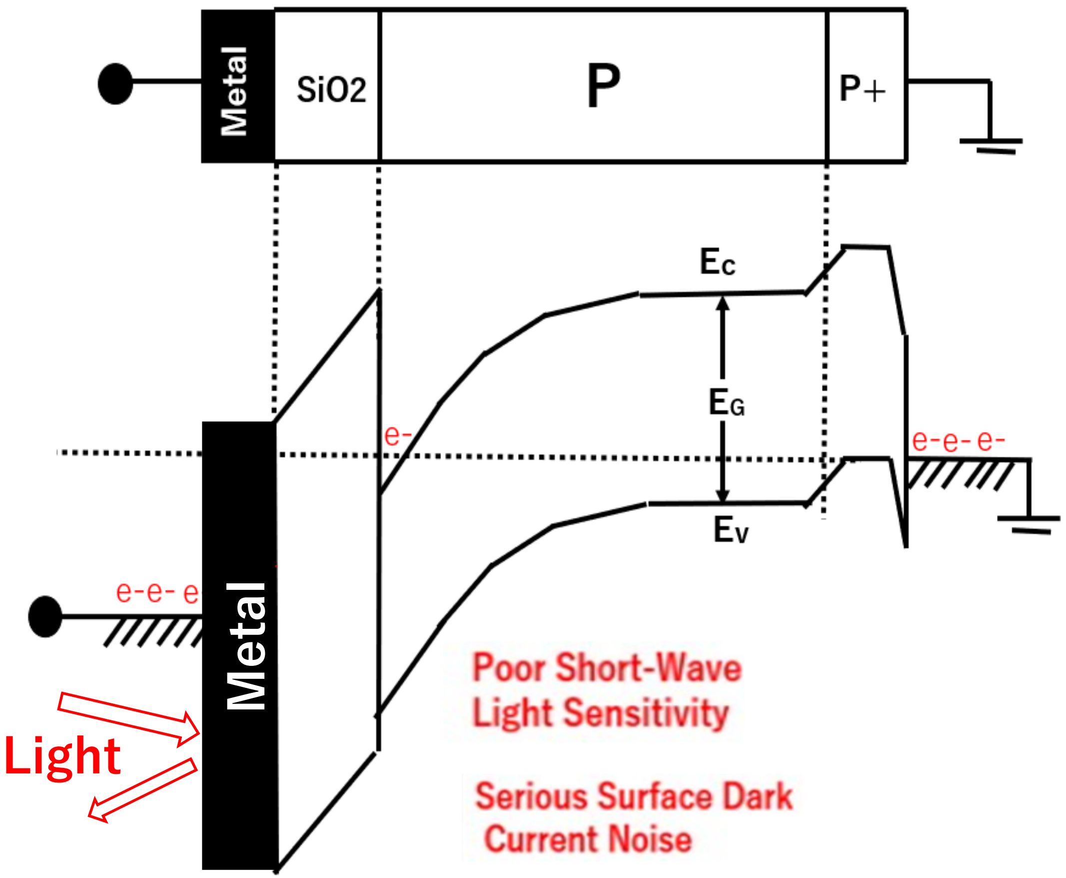
Poor Short-Wave Light Sensitivity

(1) N+P junction type Solar Cell

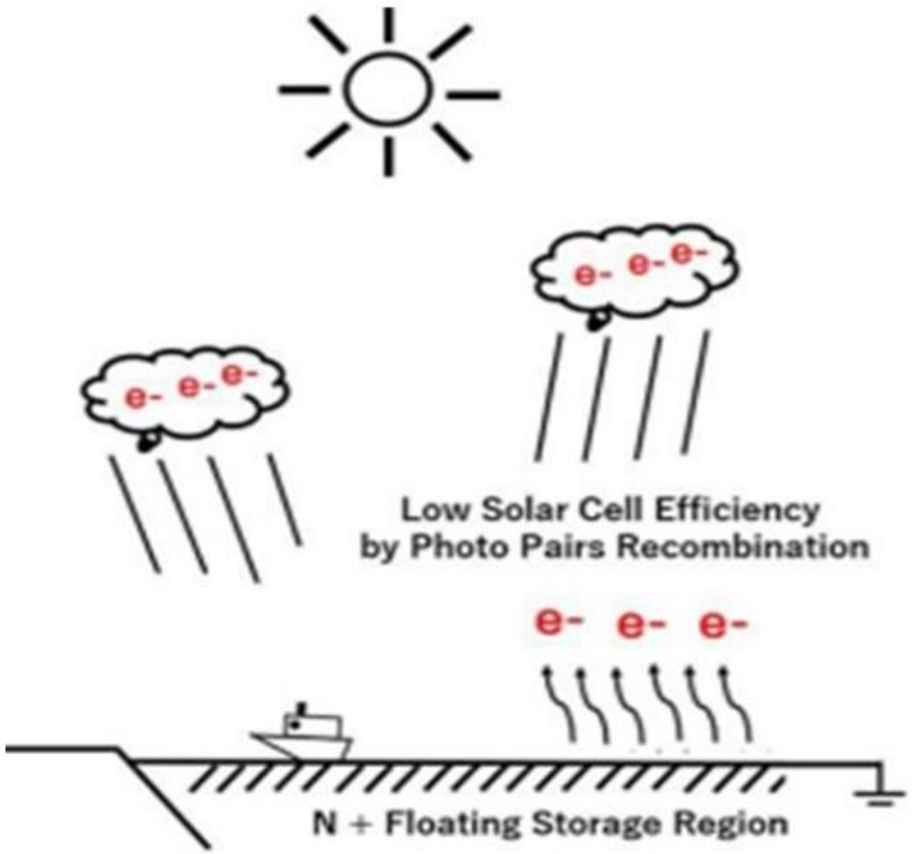


(2)	Charge Couple Device CCD/MOS Dynamic Photo Capacitor	No Image Lag Problem	Serious Surface Dark Current Noise	Poor Short-Wave Light Sensitivity

(2) CCD/MOS Dynamic Photo Capacitor type Photo Sensor



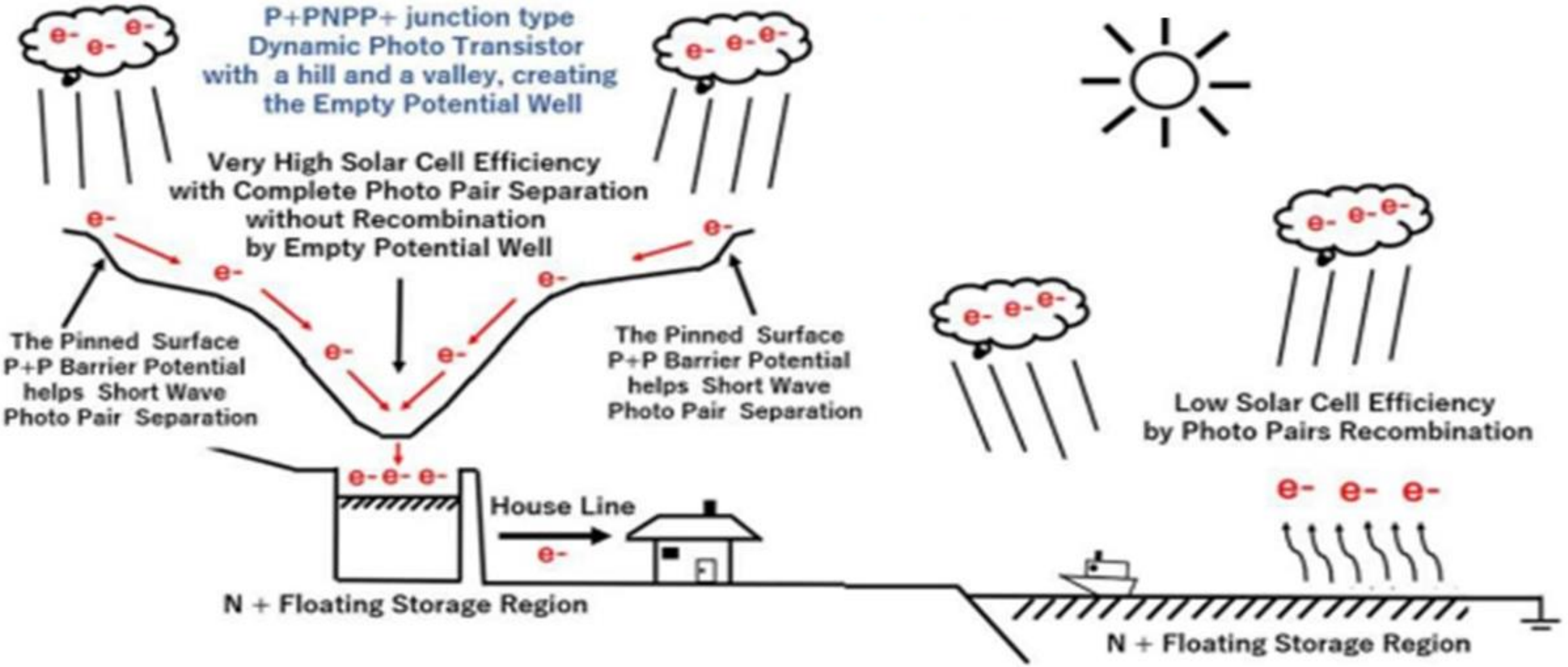
(1) Floating Surface N+P Single Junction Solar Cell



(3)	P+NP Double Junction Dynamic Photo Transistor Pinned Buried Photodiode	No Image Lag Problem	No Surface Dark Current Noise	Excellent Short-Wave Light Sensitivity

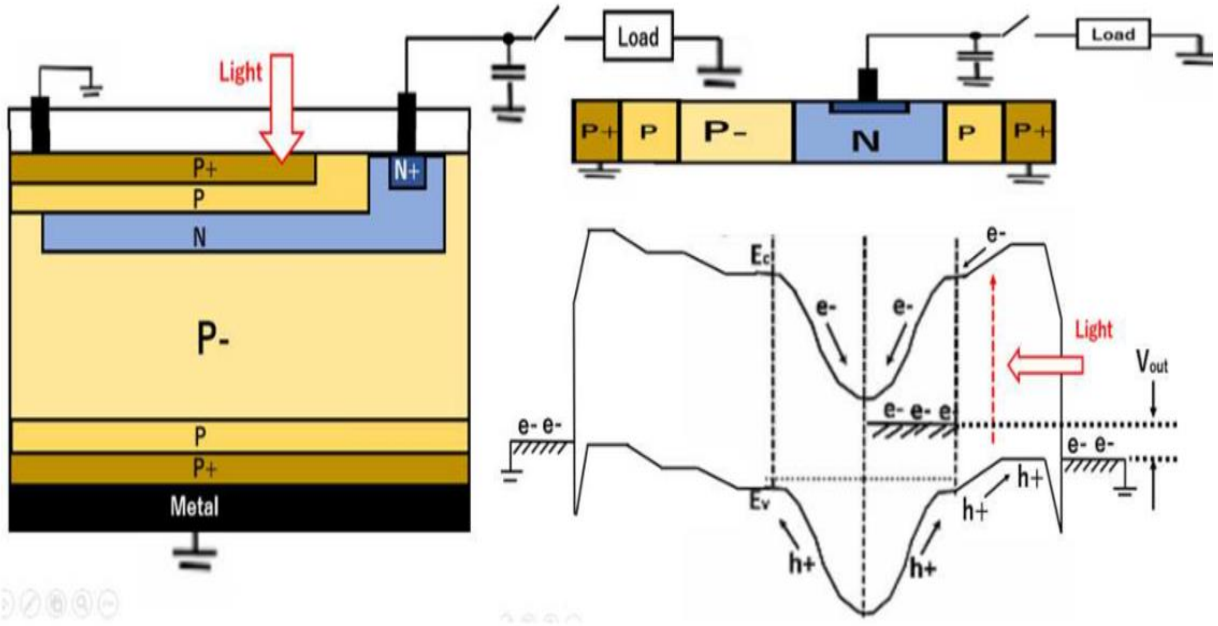
(3) Pinned Surface P+PNPP+ Double Junction Solar Cell

(1) Floating Surface N+P Single Junction Solar Cell



(3)	P+NP Double Junction Dynamic Photo Transistor Pinned Buried Photodiode	No Image Lag Problem	No Surface Dark Current Noise	Excellent Short-Wave Light Sensitivity

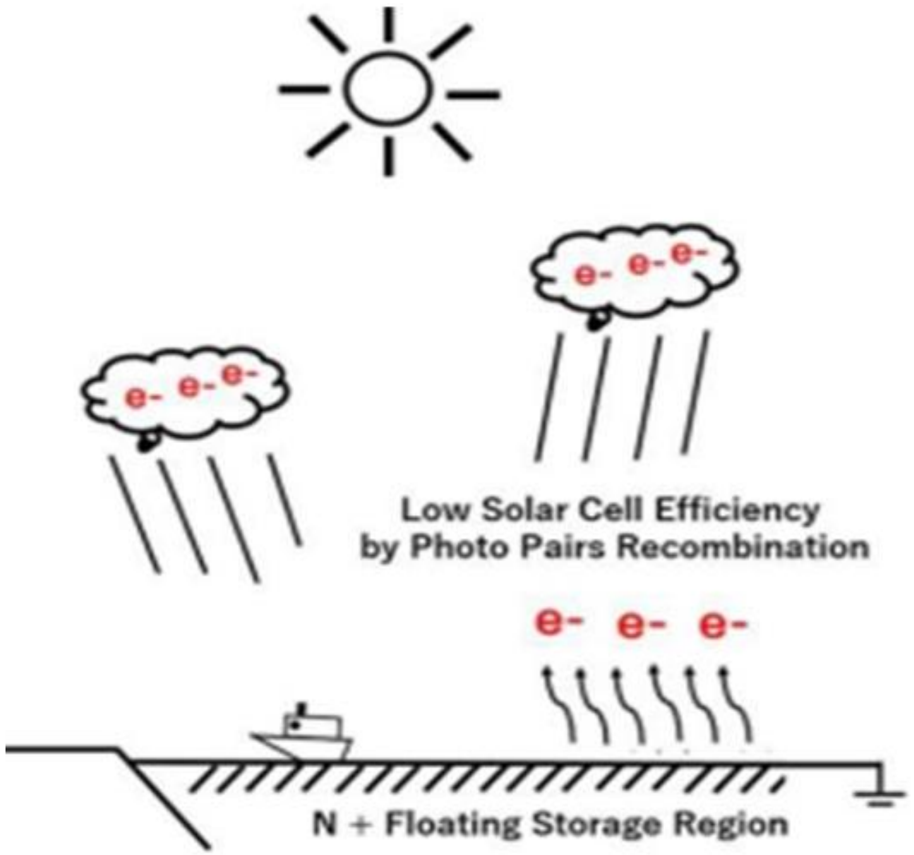
(3) Pinned Surface P+PNPP+ Double Junction Solar Cell



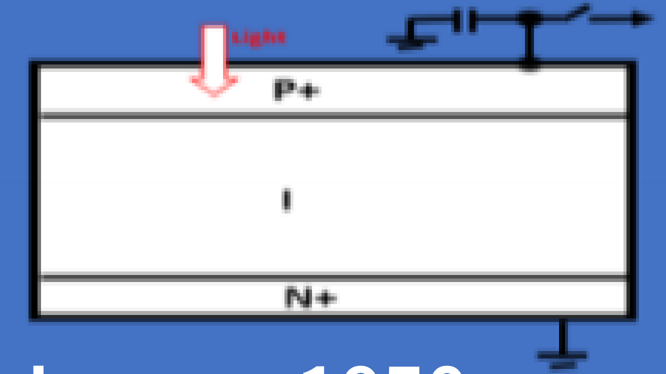
Band Diagram of P+PNPP+ Double Junction Type Photodiode Solar Cell.

See JPA2020-131313 invented by Hagiwara

(1) Floating Surface N+P Single Junction Solar Cell

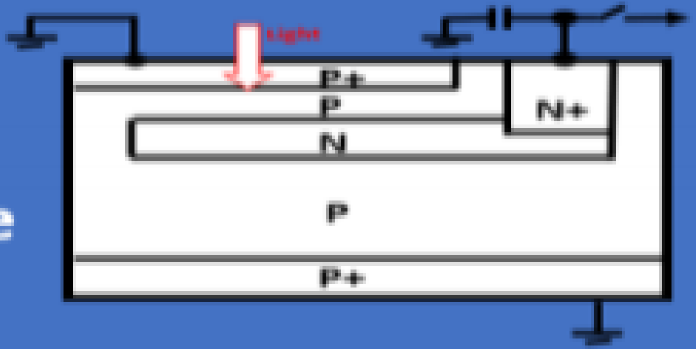


(1) PIN Diode



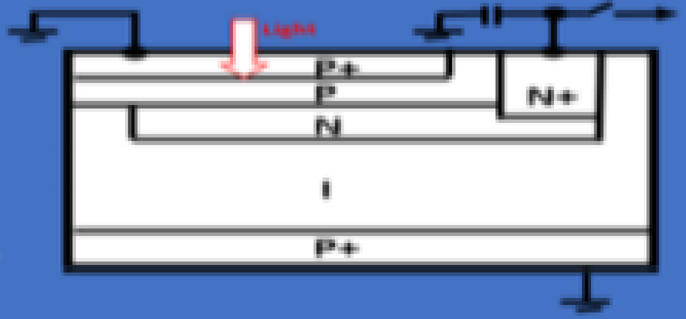
Jun-Ichi Nishizawa , 1950

(2) Pinned Buried Photodiode

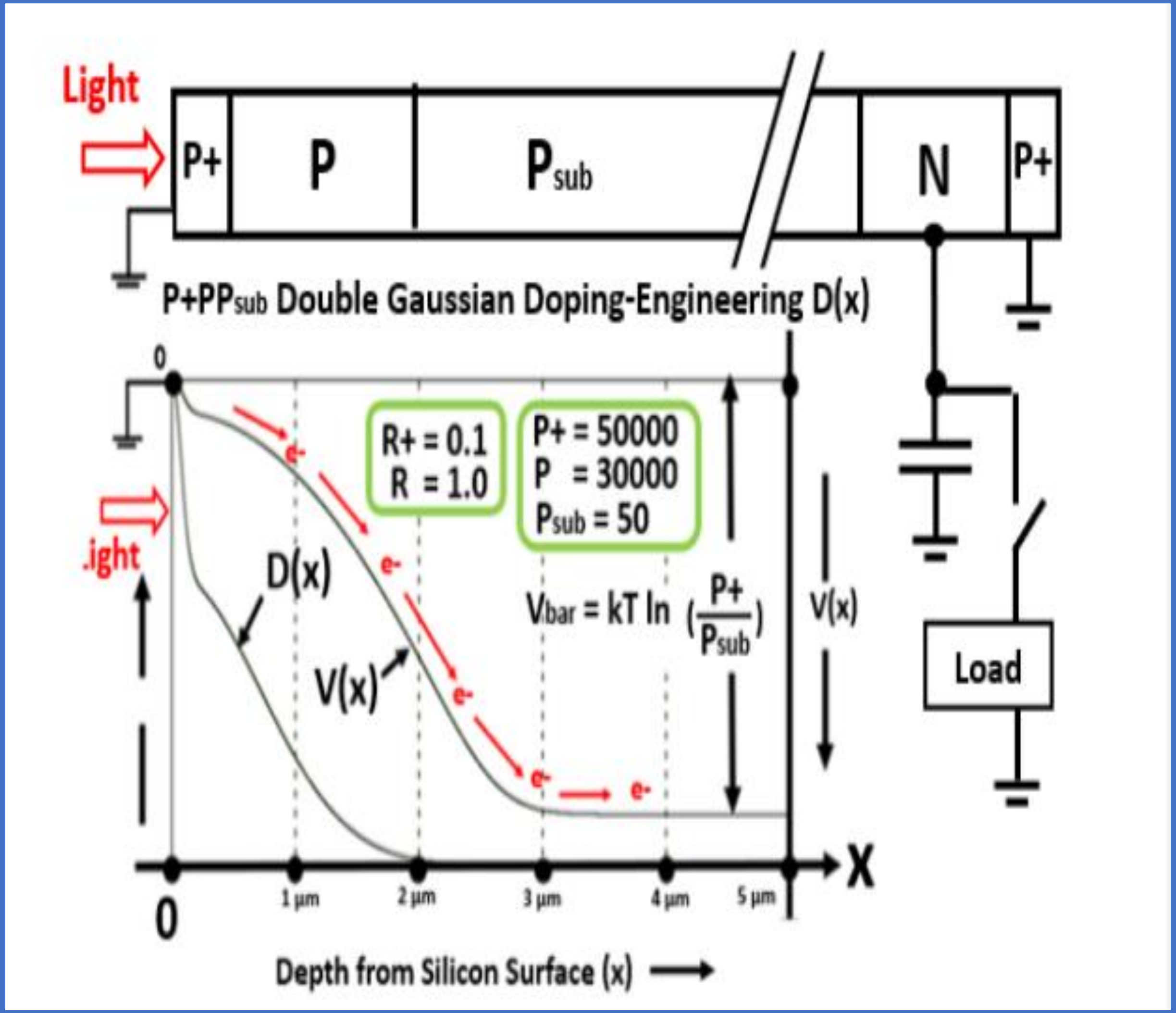


JPA2020-131313 by Hagiwara

(3) Pinned Buried PIN Photodiode

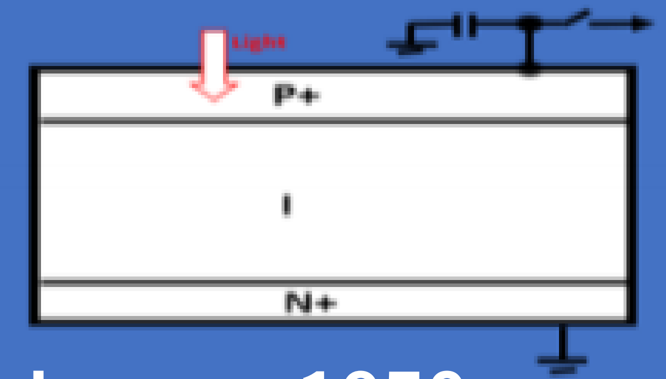


Yoshiaki Hagiwara, 2021



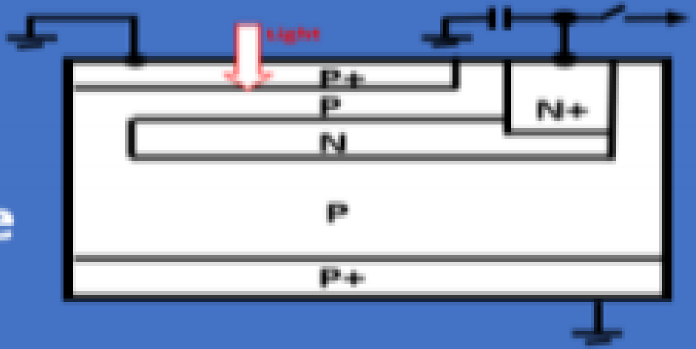
Exact Numerical Computation of the P+P Surface Barrier Potential V(x)

(1) PIN Diode



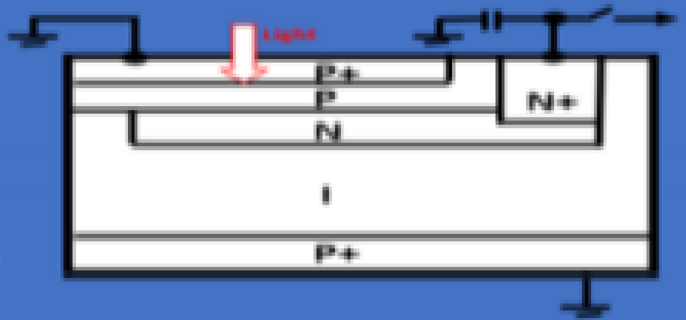
Jun-Ichi Nishizawa , 1950

(2) Pinned Buried Photodiode

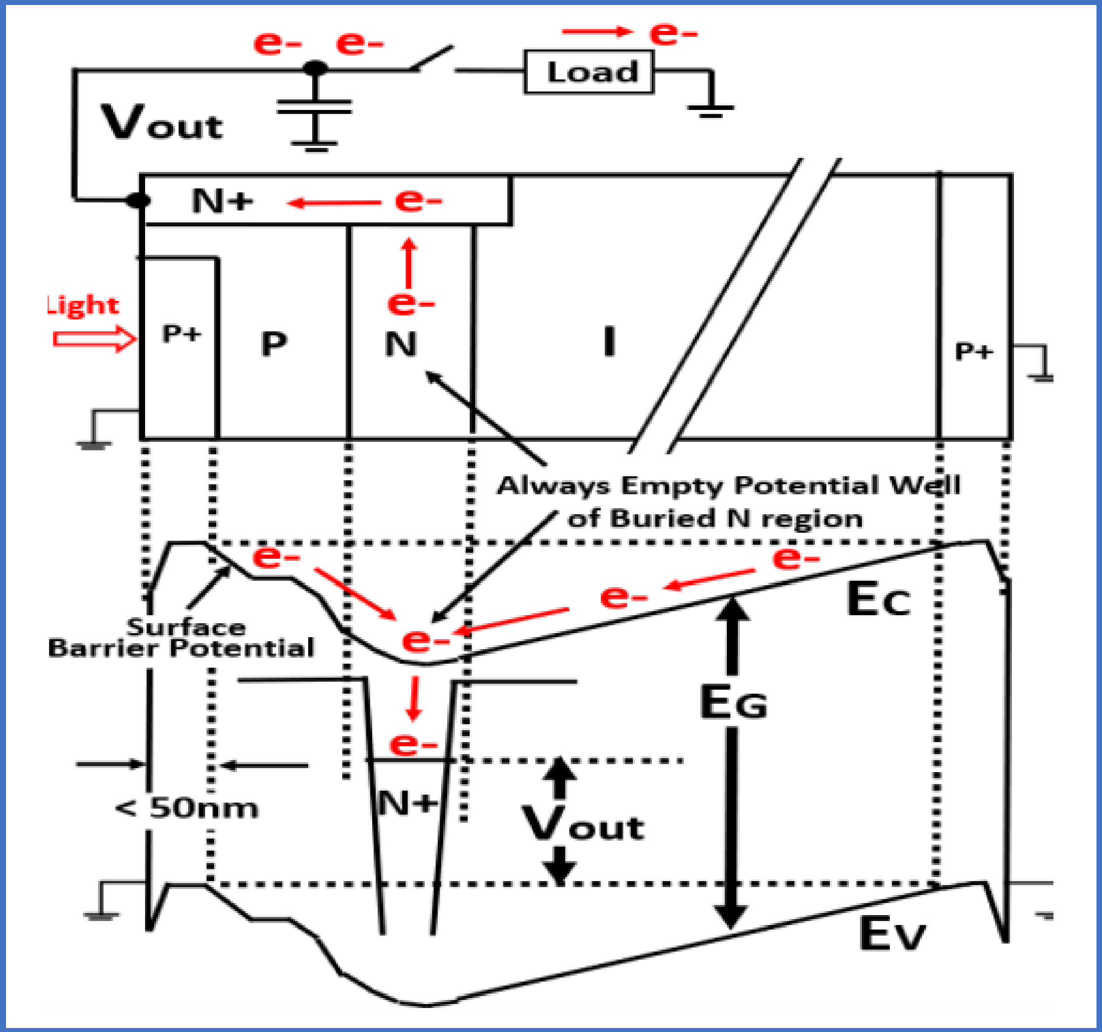


JPA2020-131313 by Hagiwara

(3) Pinned Buried PIN Photodiode



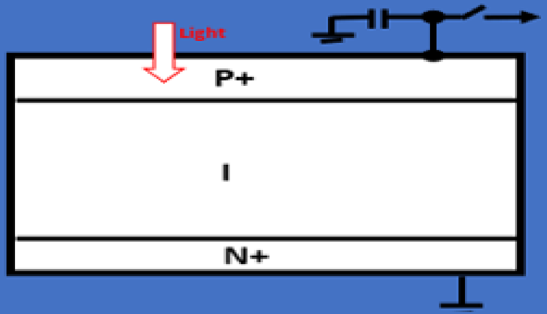
Yoshiaki Hagiwara, 2021



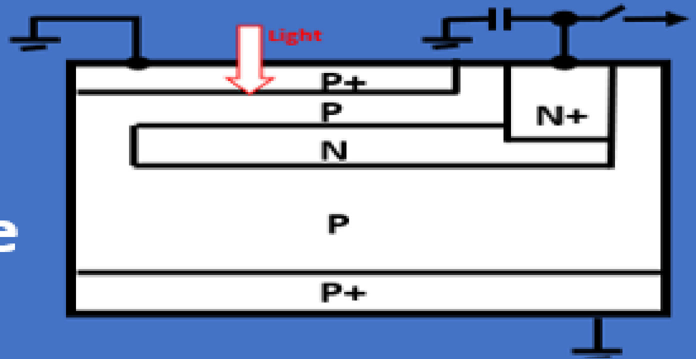
Pinned Buried P+PNIP+ Photodiode Structure type Solar Cell

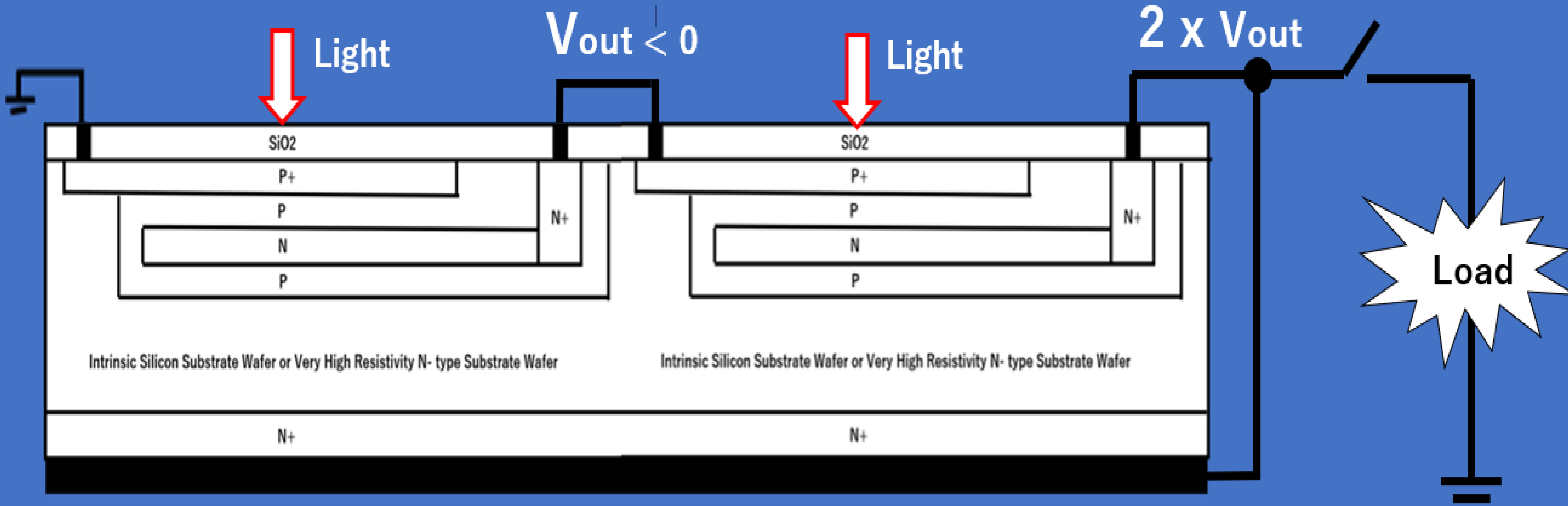
Jun-Ichi Nishizawa , 1950 JPA2020-131313 by Hagiwara

(1) PIN Diode



(2) Pinned Buried Photodiode



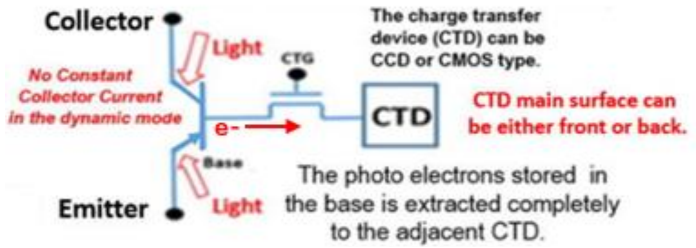


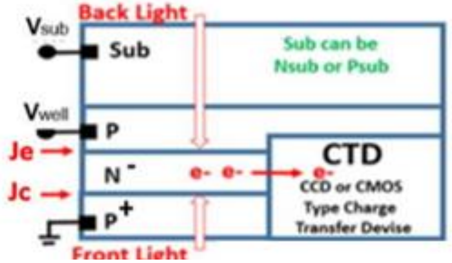
Two Units in Series Configuration of Pinned Buried PIN Photodiode type Solar Cell

Invention and Historical Development Efforts of Pinned Buried Photodiode.

JPA1975-134985

**P+NP Double Junction
Dynamic Photo Transistor type
Pinned Buried Photodiode**



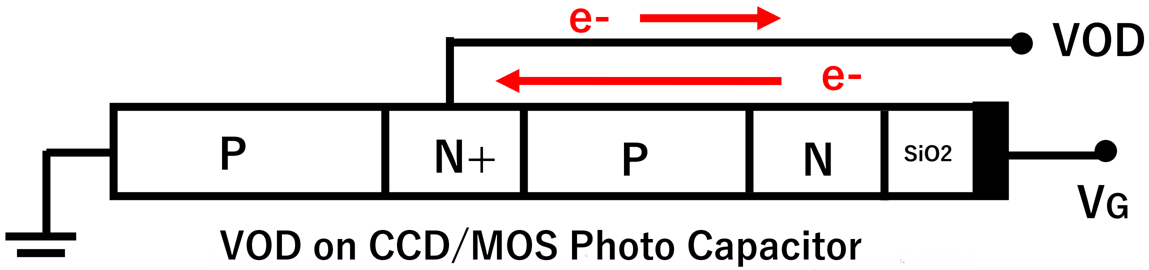


Electric Shutter Function Capability

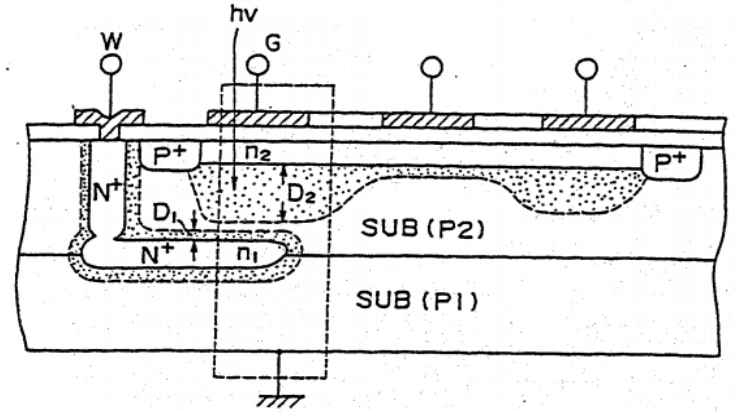
Complete Charge Extraction from the N base region for low image lag and high speed high quality action pictures

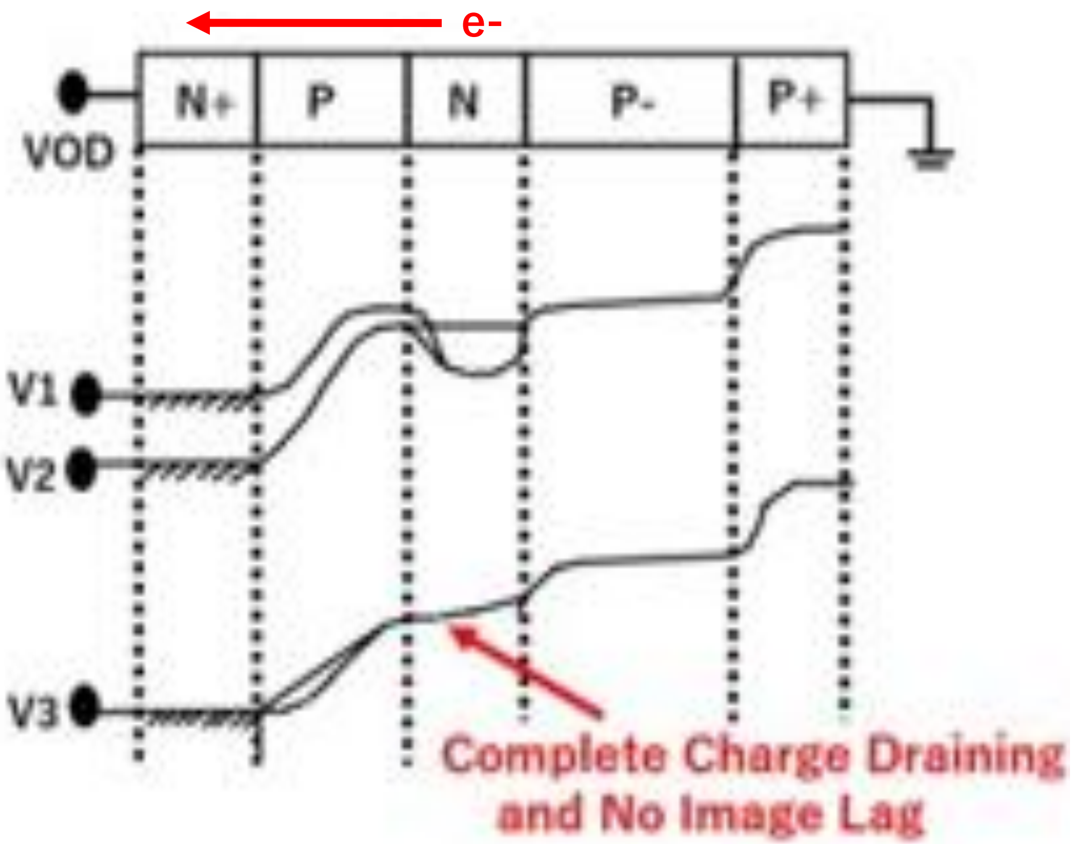
Two Early Works on VOD

- Sequin,"Blooming Suppression in CCDAIDs", Bell System Technical Journal, Oct.1972,
- James M. Early USP3896485 filed on Dec 3, 1973



VOD on CCD/MOS Photo Capacitor



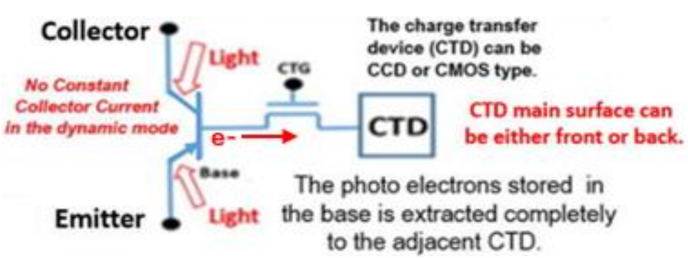


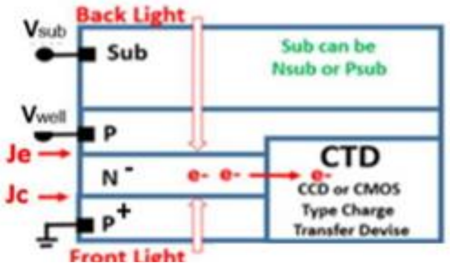
Yoshiaki Hagiwara JPA1975-134985 filed on Nov1975

Invention and Historical Development Efforts of Pinned Buried Photodiode.

JPA1975-134985

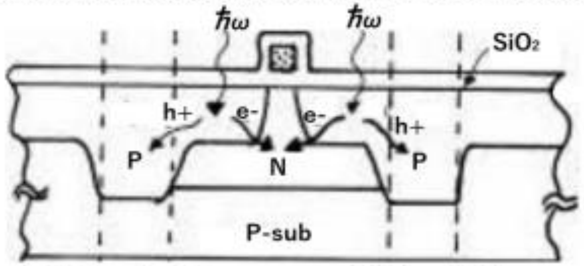
P+NP Double Junction
Dynamic Photo Transistor type
Pinned Buried Photodiode



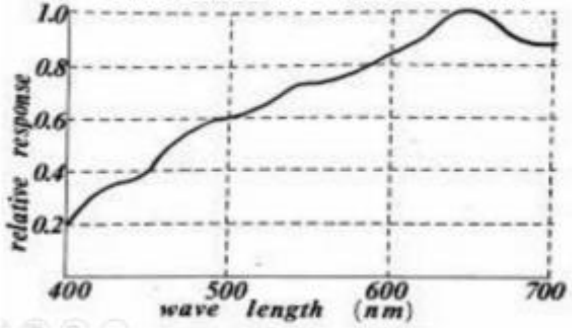


Electric Shutter
Function Capability
Complete Charge
Extraction from
the N base region
for low image lag
and high speed
high quality
action pictures

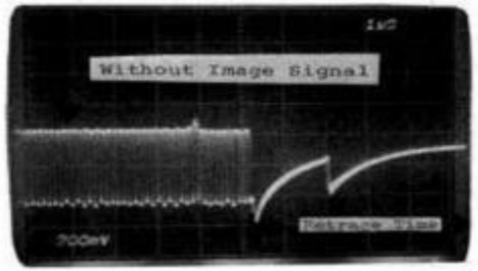
(A) Pinned-Surface and Buried-Storage
PNP Photodiode with Adjacent Channel Stops



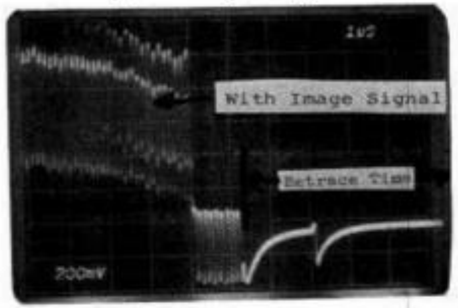
(B) Spectral Response with Very High
Short-Wave Blue Light Sensitivity



(C) Signal Output with No Light
showing Very Low Dark Current Feature



(D) Signal Output with Input Light
showing No Image Lag Feature

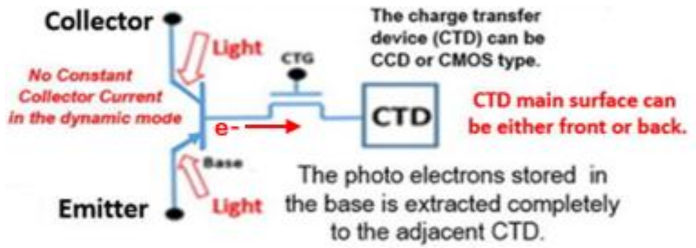


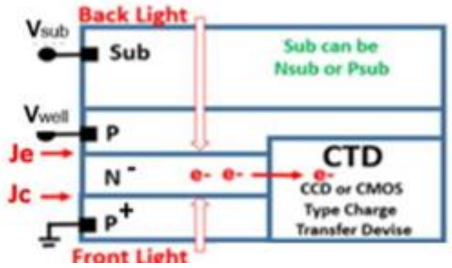
Yoshiaki Hagiwara, Motoaki Abe and Chikara Okada,
"A 380H X 488V CCD Imager with Narrow Channel Transfer Gates",
Proceeding of the 10th Conference on Solid State Devices, Tokyo 1978,
Japanese Journal of Applied Physics, Volume 18 Sup 18-1, pp. 335-340 November 1979.

Sony 1980 Video Movie has in one body
an 8 mm VTR and One Chip FT CCD Image Sensor
with the PNP Double Junction type Pinned Photodiode
developed by Hagiwara in 1978

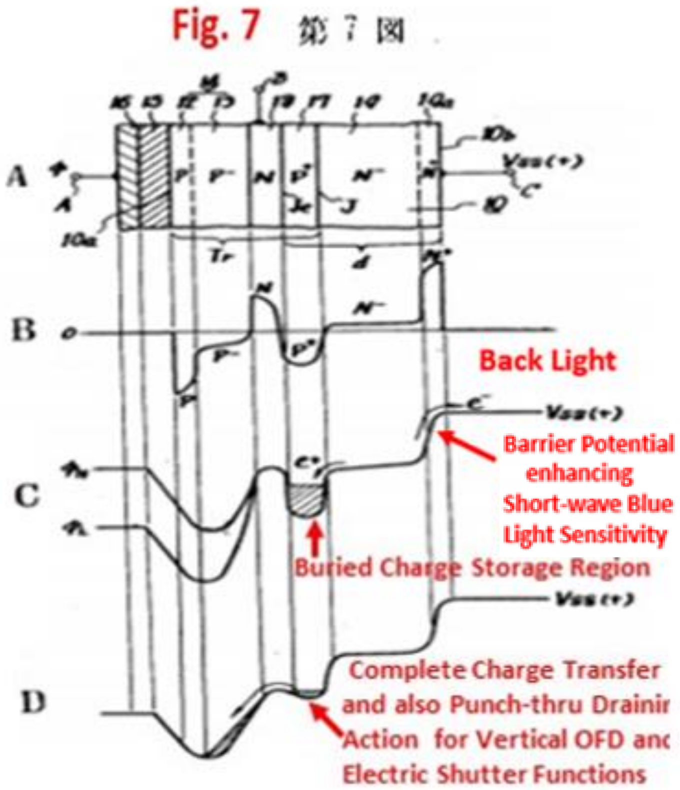
Invention and Historical Development Efforts of Pinned Buried Photodiode.

P+NP Double Junction
Dynamic Photo Transistor type
Pinned Buried Photodiode

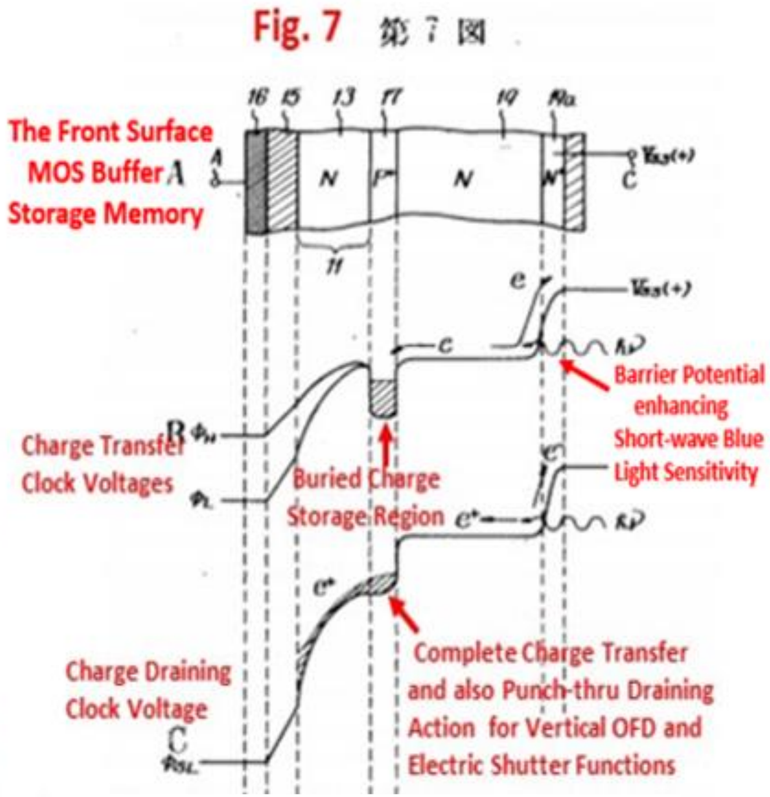




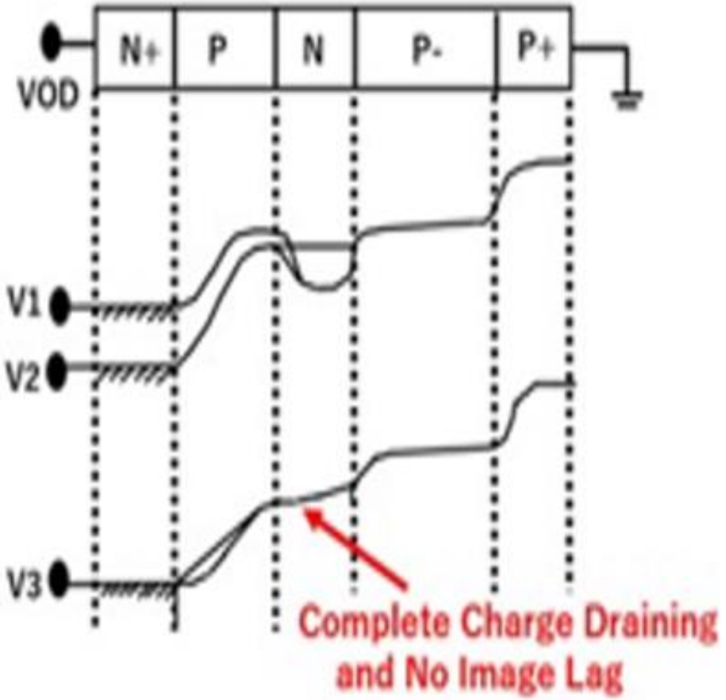
Electric Shutter Function Capability
Complete Charge Extraction from the N base region for low image lag and high speed high quality action pictures



JPA1975-127646 with
Global Shutter Function



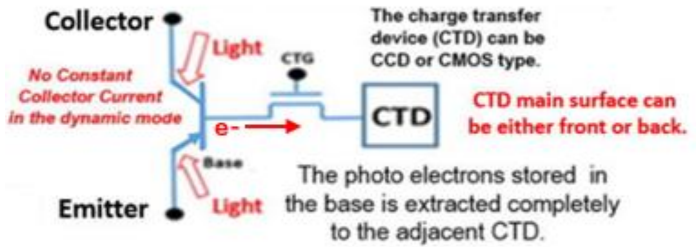
JPA1975-127647 with
Global Shutter Function

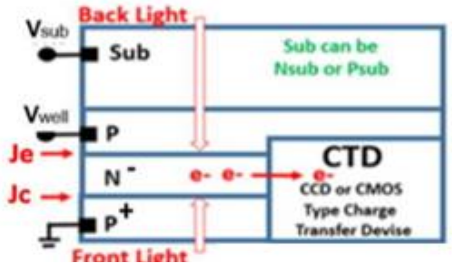


JPA1975-134985 with
Vertical Overflow Drain(VOD)

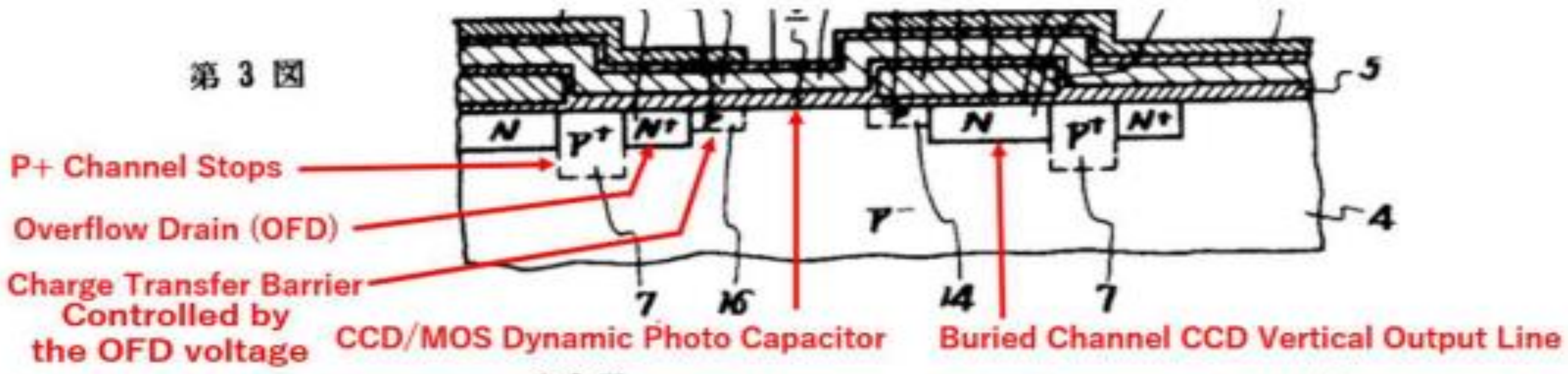
Invention and Historical Development Efforts of Pinned Buried Photodiode.

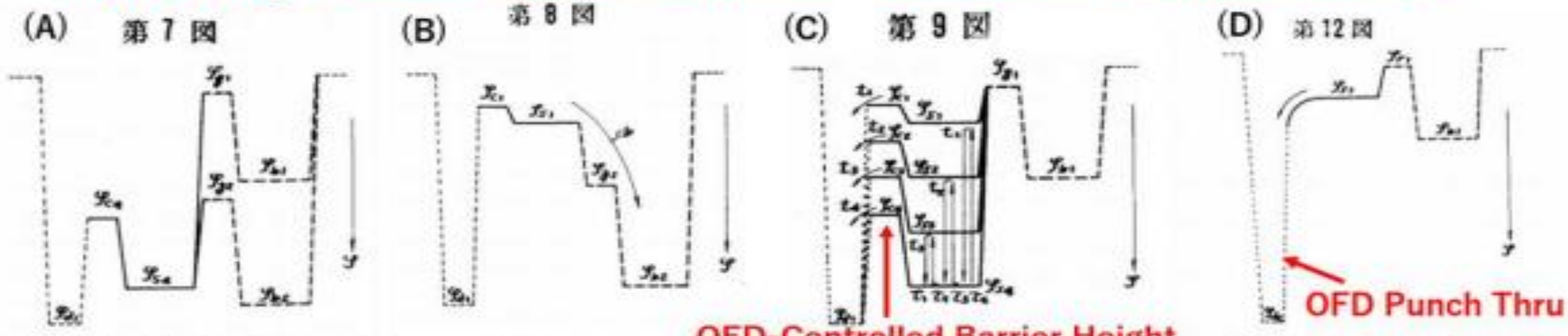
P+NP Double Junction
Dynamic Photo Transistor type
Pinned Buried Photodiode





Electric Shutter Function Capability
Complete Charge Extraction from the N base region for low image lag and high speed high quality action pictures



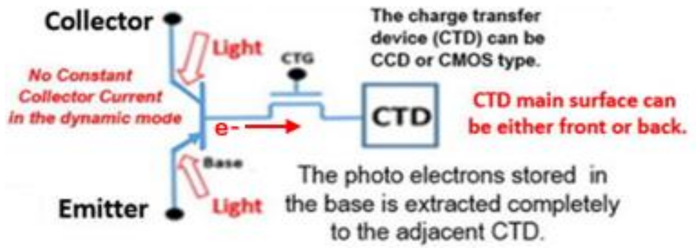


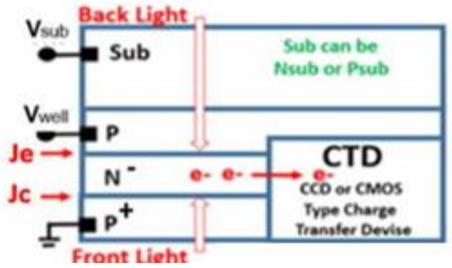
(A) Vertical CCD Charge Transfer (B) Reset Time (C) Gamma Control Mode (D) Electric Shutter Mode

Electric Shutter Function and Gamma Control defined in JPA1977-126885 patent proposed by Hagiwara in 1977.

Invention and Historical Development Efforts of Pinned Buried Photodiode.

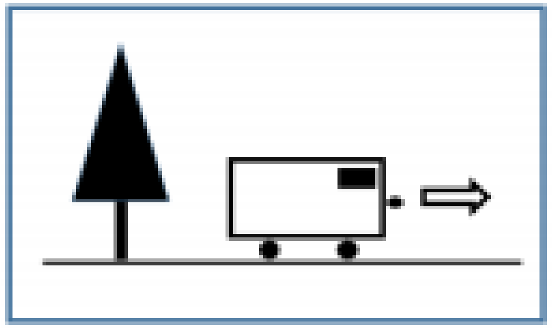
P+NP Double Junction Dynamic Photo Transistor type Pinned Buried Photodiode



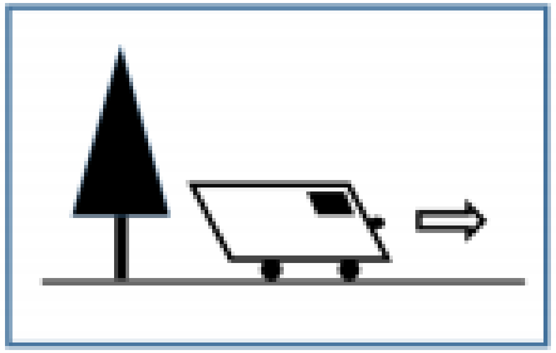


Electric Shutter Function Capability

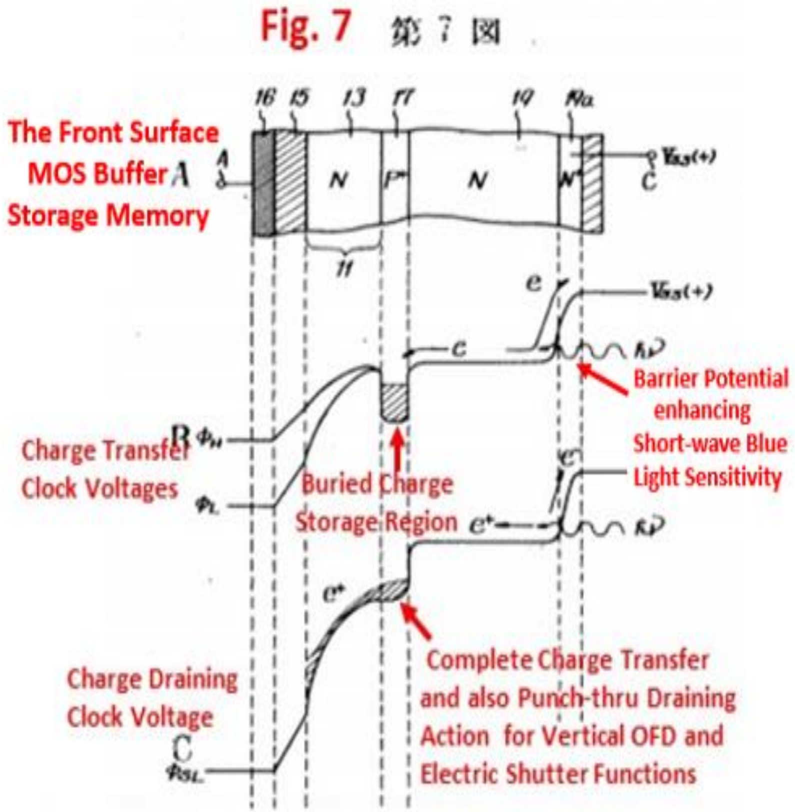
Complete Charge Extraction from the N base region for low image lag and high speed high quality action pictures



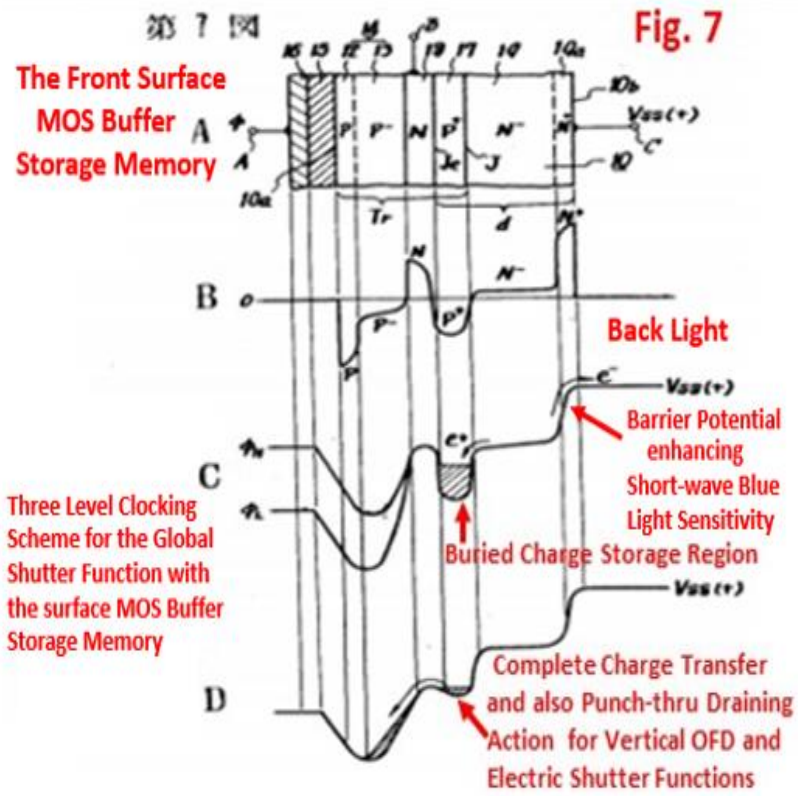
the CCD image sensors with the Built in Global Shutter Function



the classical CMOS image sensors with rotary shutter effect



JPA1975-127647 with Global Shutter Function



JPA1975-127646 with Global Shutter Function

Sweet Memory ♡

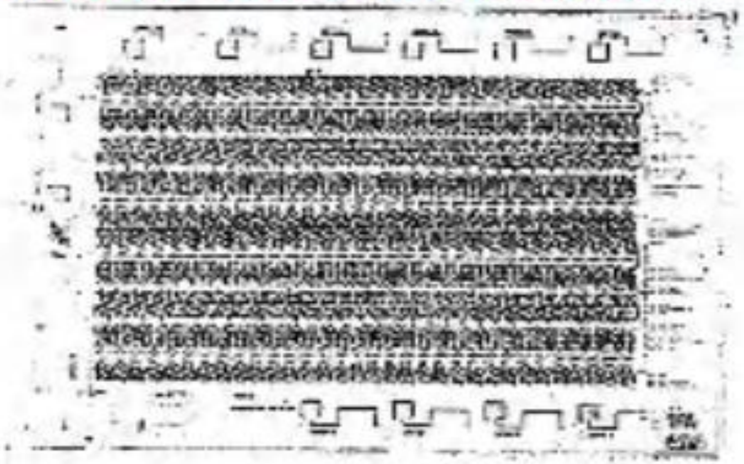
128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976


128-Bit Multicomparator

Prof. C. A. Mead and Yoshiaki Daimon Hagiwara working on the silicon chip design at Caltech in 1972

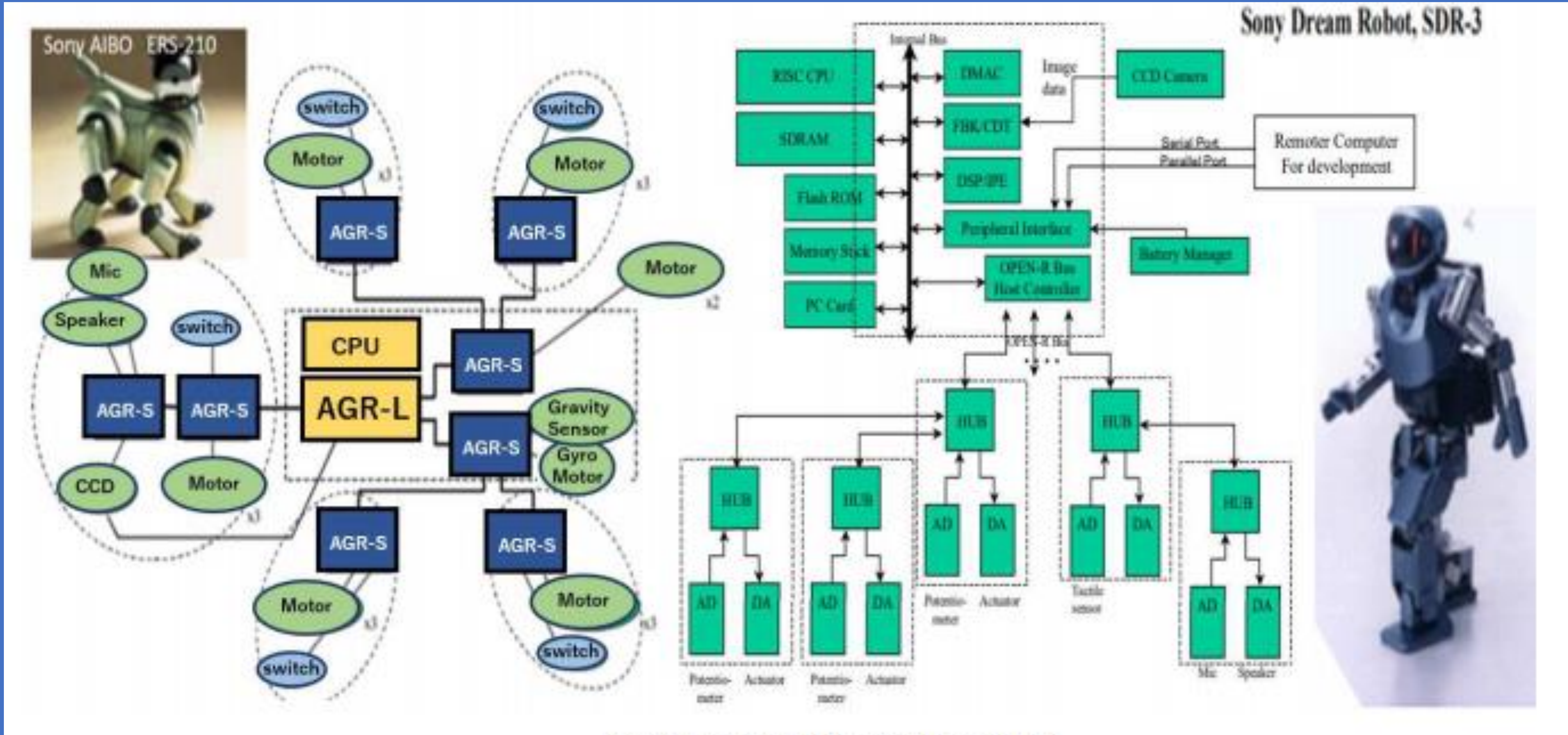
128-bit Multicomparator chip, designed by Hagiwara in 1972-1973 and fabricated by Intel PMOS process.



Sweet Memory ♡

Sweet Memory ♡

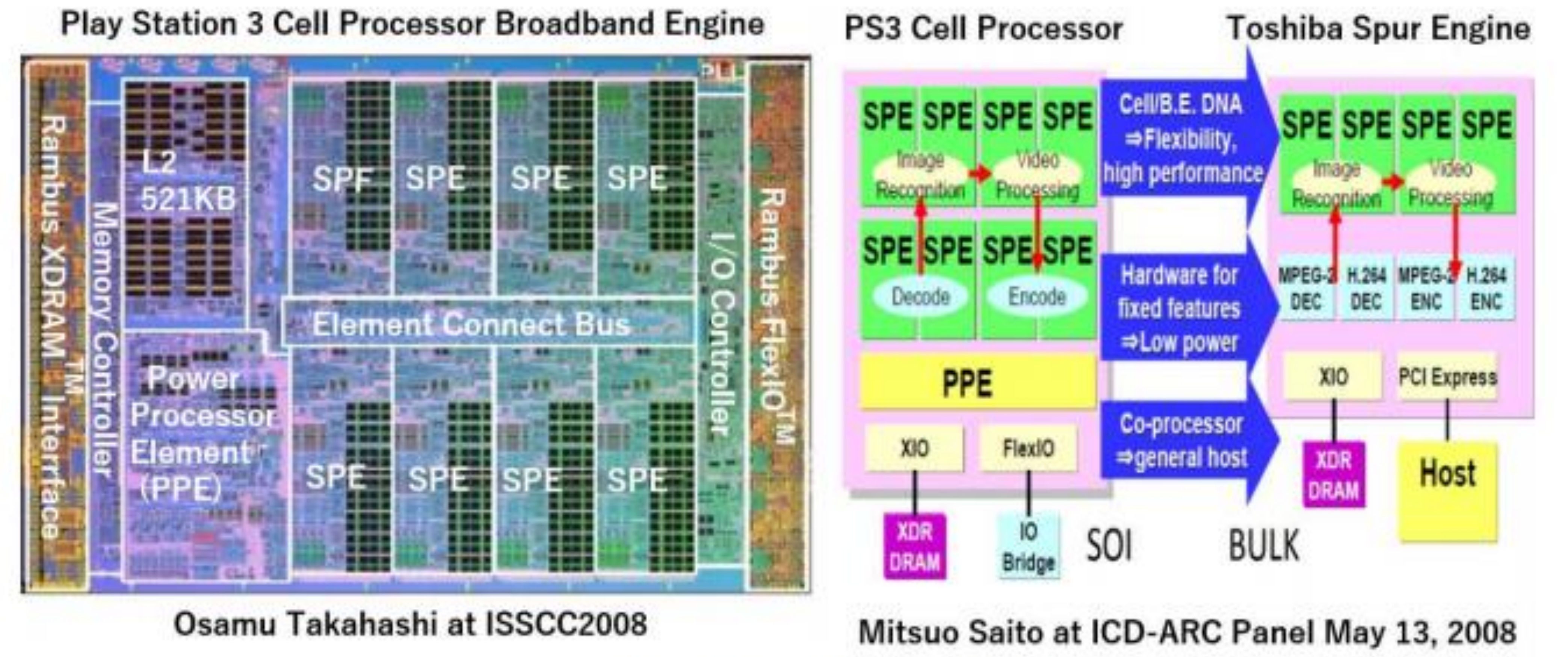
Yoshiaki Hagiwara, “Microelectronics for Home Entertainment”
ESSCIRC2001, Vilach , Austria, September 2001



Sony Dream Robot AIBO ERS-210 and SDR-3.

Sweet Memory ♡

Yoshiaki Hagiwara, “SOI Cell Processor and Beyond”
ESSCIRC2008, Edinburgh Scotland, U. K. September 2008



PS3 Cell / B. E. and Toshiba Spurs Engine.

ISSCC2013

Sweet Memory ♡

Antiques from
the Innovative Attic

Yoshiaki Hagiwara as a presenter at the ISSCC2013 Plenary Panel.

International Solid-State Circuits Conference

February 17–21, 2013 | San Francisco, CA

Welcome to the 2013 IEEE International Solid-State Circuits Conference (ISSCC). This year, we will celebrate the 60th anniversary of ISSCC. ISSCC is the flagship conference of the Solid-State Circuits Society, and is the premier forum for the presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity to network with leading experts in the field. For 2013, the Conference theme is "60 Years of (Em)Powering the Future". more

ISSCC2013 Sweet Memory ♡

Yoshiaki Hagiwara as a presenter at the ISSCC2013 Plenary Panel.

Yoshiaki Higihara: The p-n-p-n Diode in Future Linear Motor Cars and in Modern Imagers

John Louis Moll (1921–2011) was studying a p-n-p-n diode switch in his Ph.D. dissertation work when the first ISSCC was held in 1954. In a normal operation mode, this device works as a thyristor, which can drive a large current and is the key device structure of an IGBT applied for a linear motor car of the future (see Figure 9). In a dynamic operation mode, this device may work as a simple p-n-p-n dynamic capacitance that can detect and store one single electron, which is a key device structure of the modern image sensor (see Figure 10).

I recall, when I was taking his physics course at Caltech, that Feynman once said that an electron is always free, moving around rapidly in free space, even in solid, and it

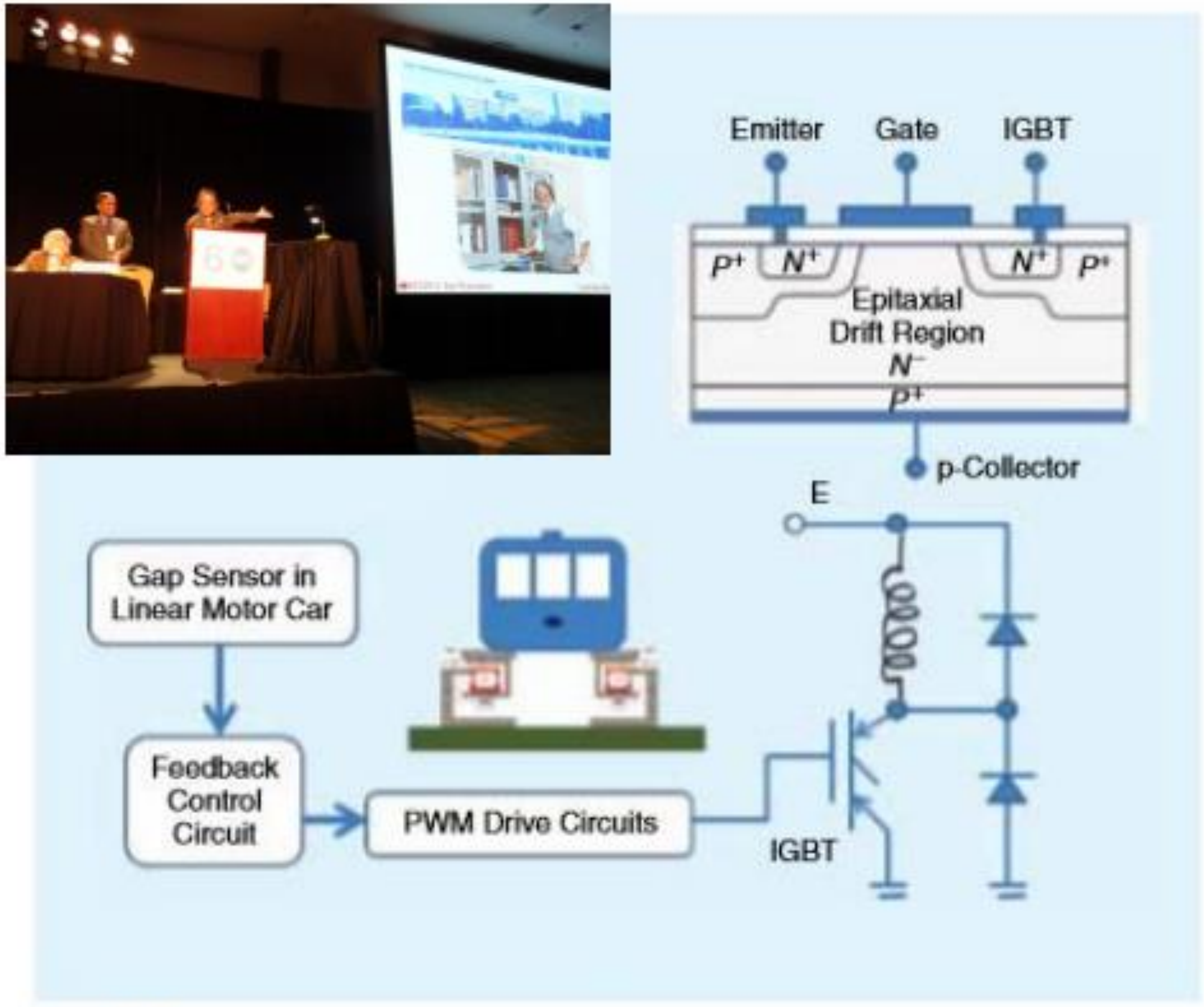


FIGURE 9: The p-n-p-n switch diode for a modern linear motor car.

ISSCC2013

Sweet Memory ♡

Antiques from the Innovative Attic

Yoshiaki Hagiwara as a presenter at the ISSCC2013 Plenary Panel.

Yoshi Hagihara, Eric Vittoz and Bob Brodersen.

Yoshiaki Hagihara shared his memories of Richard Feynman, his mentor and educator at Caltech, and how he learned from him that control of electrons is at the heart of all electronic devices. As an example from his attic, he pointed to the old p-n-p-n junctions that are now incorporated in modern-day image sensors.

never stops. It is very hard to catch an electron because we do not know exactly where it is. Our civilization today is based on a technology that controls electrons, down to a single one.

Imagine a photon incident to a bipolar transistor base region. The photon energy creates an electron-hole pair. And the photo-electron can be stored in the base region as one single majority carrier. That is, a bipolar transistor can also function as a photon detector and/or a storage container. I thought that a room in a hotel must be empty and clean before the first hotel guest arrives. So must be this transistor base region empty and clean with no guest electrons at the beginning. This transistor in a dynamic p-n-p capacitor mode is useful since it can capture, confine, and control one single electron. But as a

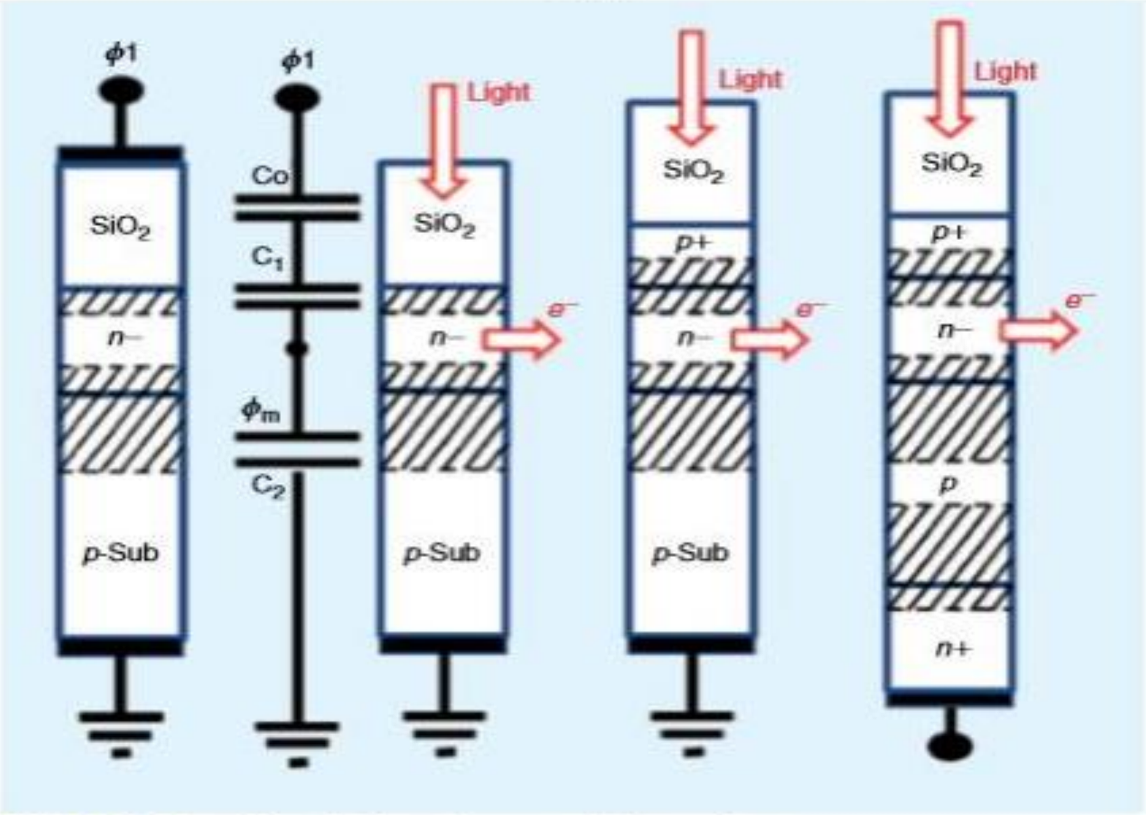


FIGURE 10: From CCD to the dynamic p-n-p-n diode capacitors.

ISSCC2013

Sweet Memory ♡

Antiques from the Innovative Attic

Yoshiaki Hagiwara as a presenter at the ISSCC2013 Plenary Panel.

student, I did not know yet how to move that single photoelectron sitting in the base region to the outside world so that we can make use of it as a signal. I had no way yet to know whether the hotel guest has arrived and is resting in the hotel room or not. We had no way yet to ask the hotel guest to come up to the hotel lobby to meet me. I had to wait a few more years (until 1970 in my senior year in college) to find the answer. We all know now it is the CCD structure that can store and transfer one single electron. With a precharge reset set gate and a source-follower circuit, a scheme invented by Walter Kosonocky. We could finally meet our hotel guest at the hotel lobby.

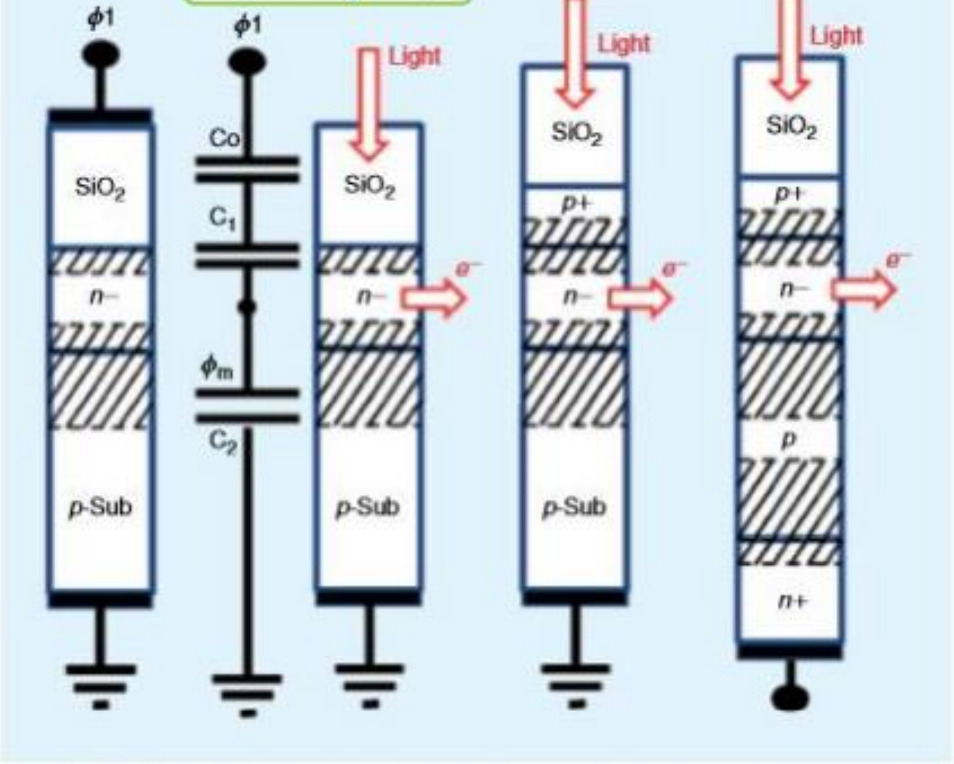
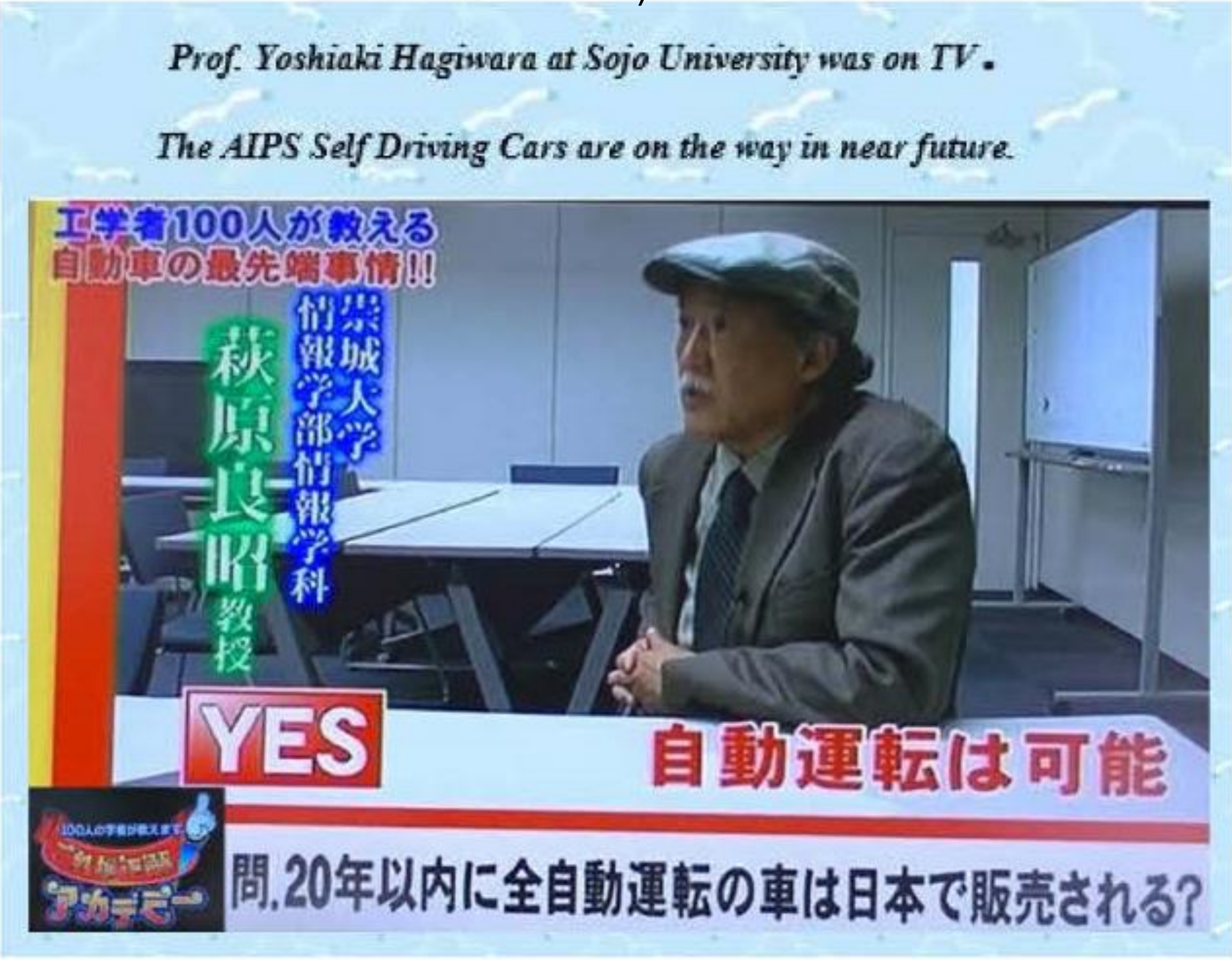


FIGURE 10: From CCD to the dynamic p-n-p-n diode capacitors.

Sweet Memory ♡

Yoshiaki Hagiwara was on TV once talking about the future of self-driving artificial intelligent cars.

March, 2013



Yoshiaki Hagiwara wrote a book in 2016 titled "World of intelligent Digital Circuits" explaining building blocks needed to produce Artificial Intelligent Partner System(AIPS).

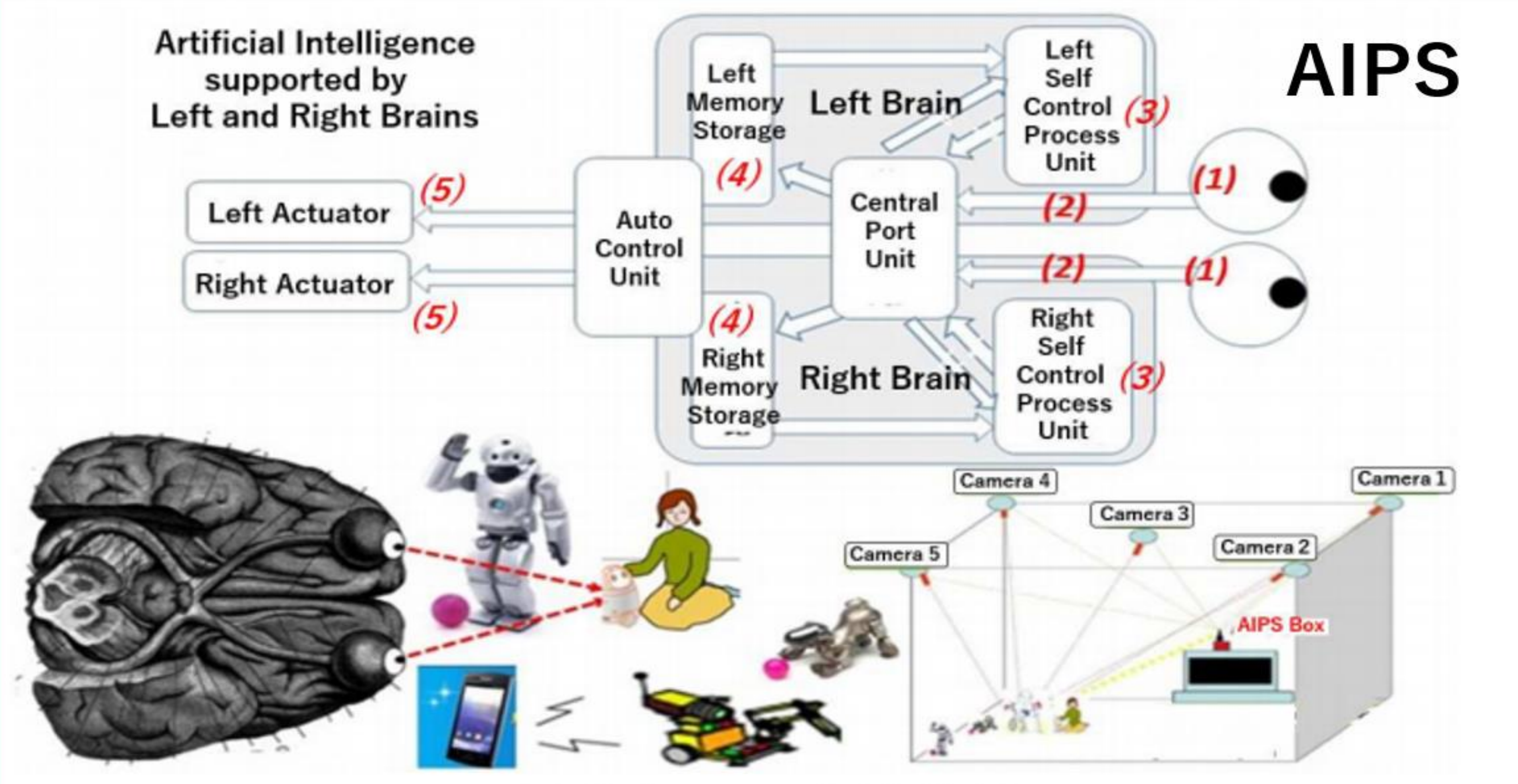
Sorry it is a 460 pages and hard cover book but written in Japanese.

ISBN978-4-88359-339-2

https://www.seizansha.co.jp/

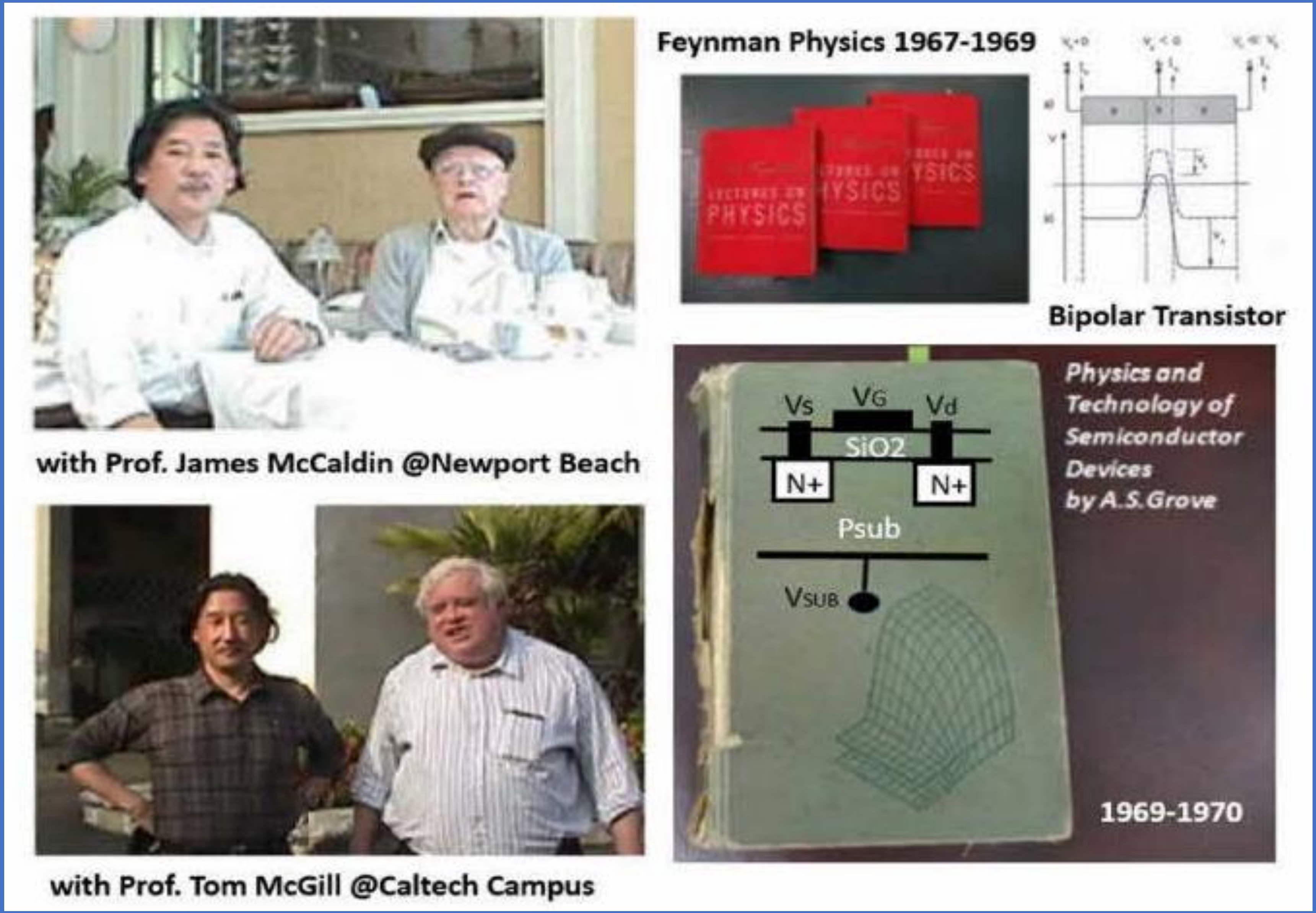
https://www.seizansha.co.jp/ISBN/ISBN978-4-88359-339-2.html

Sweet Dream ♡

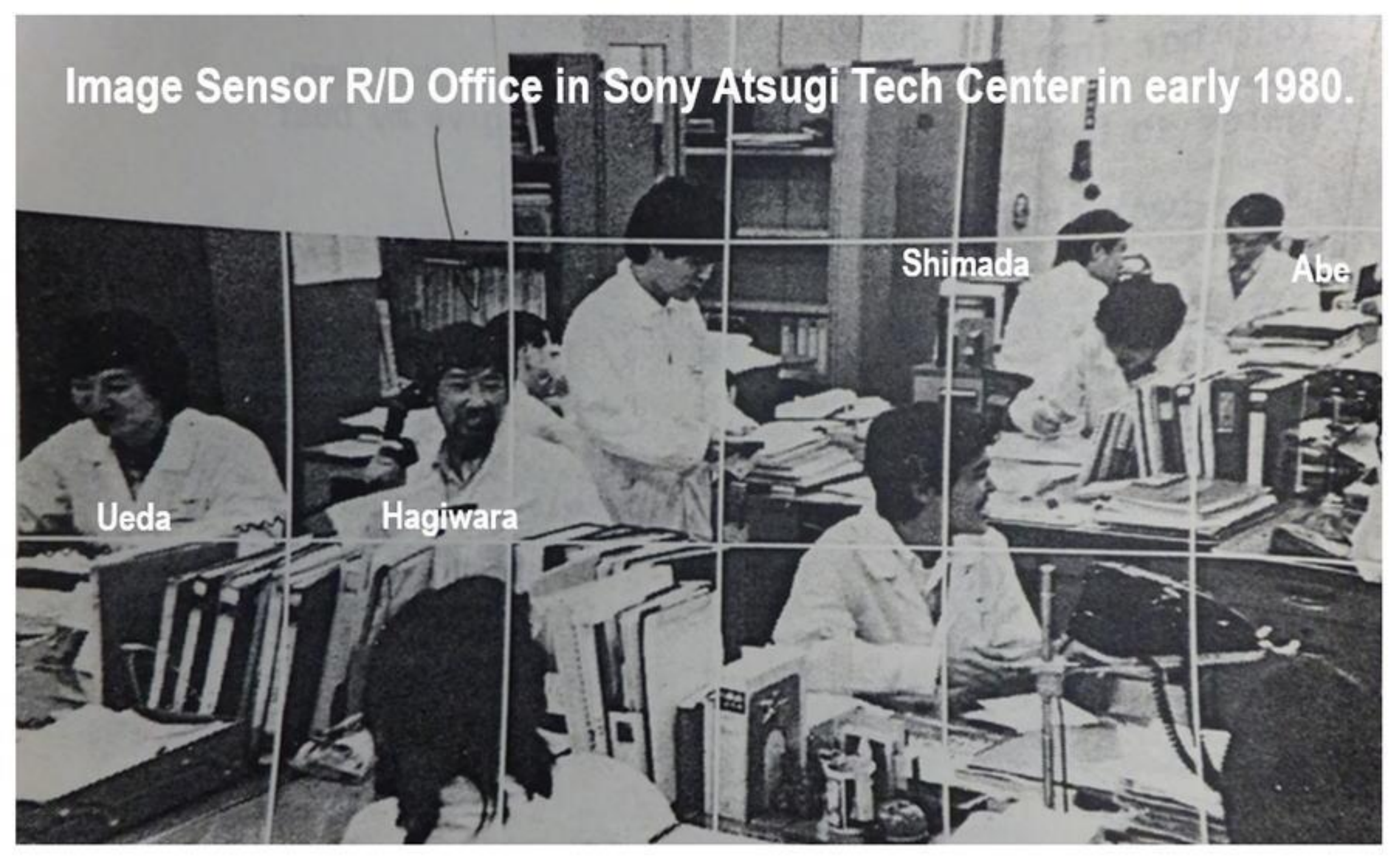


Artificial Intelligence supported by Left and Right Brains.

Acknowledgements



Acknowledgements



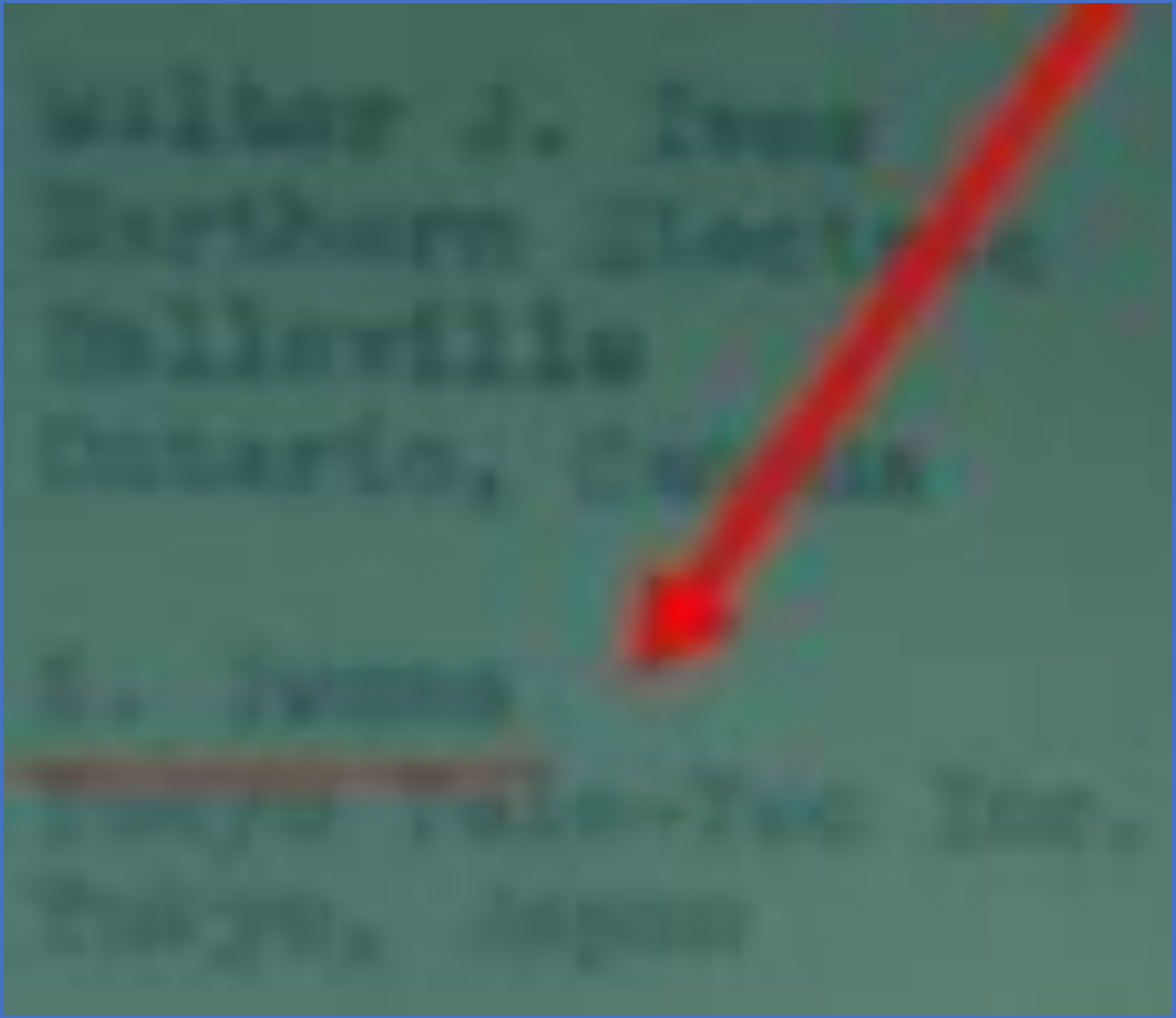
Acknowledgements

Acknowledgements

Sony Chairman Ohga and Hagiwara
at Chairman Office in Sony Tokyo Headquarter, 1996

Acknowledgements

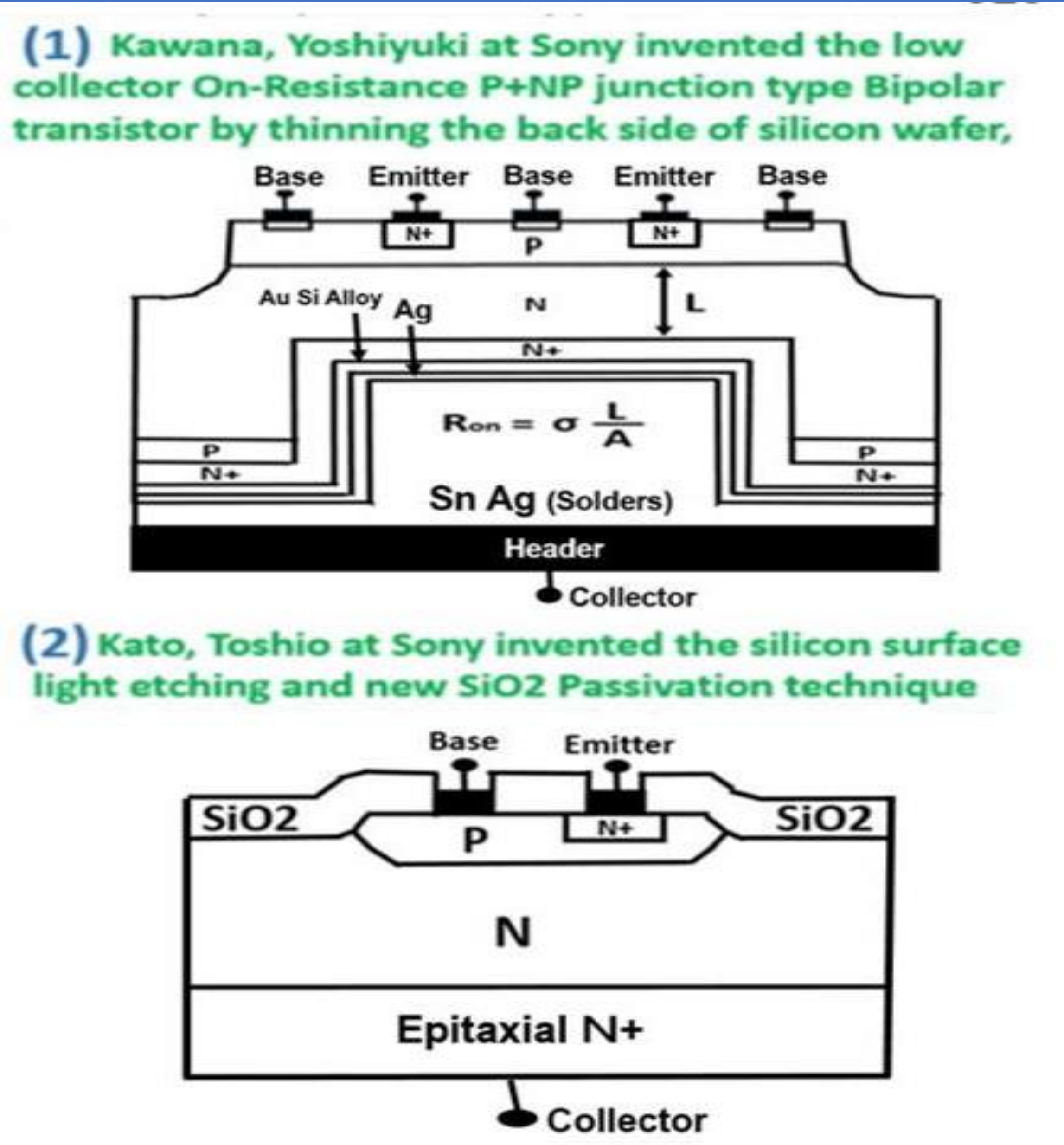
The ISSCC1954 attendee list shows **Iwama Kazuo in ISSCC1954.**



Iwama Kazuo working at Sony in 1954 attended the first ISSCC1954 conference held in Pennsylvania University. Iwama visited Bell Lab with Ibuka, the founder of Tokyo Tele-communication Laboratory, the origin of Sony Corporation , to purchase the Original Bipolar Transistor Patent from Bell Lab.

Iwama visited again in 1972 Bell Lab to discuss the future prospect of CCD image sensors in order to realize a completely mechanical-parts free consumer portable video camera with the electrical shutter function capability with no image lag feature.

Acknowledgements



Masaru Ibuka with Dr. Dr. John Bardeen visiting Sony in Tokyo , 1990

Yoshiyuki Kawan the inventor of Sony Power Bipolar Transistor.

Acknowledgements

Society of Semiconductor Industry Specialists(SSIS) founded in 1998

http://www.ssis.or.jp

Acknowledgements

Yoshiaki Hagiwara Family

Story of Pinned Buried Photodiode

Artificial Intelligent Partner System(AIPS)
hagiwara-yoshiaki@aiplab.com

by Yoshiaki (Daimon) Hagiwara
IEEE Life Fellow

AIPS

Thank You

Computer Image Recognition System