

Sweet Memory ♡

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

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Prof. C. A. Mead and Yoshiaki Daimon Hagiwara working on the silicon chip design at Caltech in 1972

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128-Bit Multicomparator

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Abstract—A 128-bit multicomparator was designed to perform the match-out function on arbitrary length data strings. Custom can be made for large data lengths or parallel for comparison, word-width applications. The device utilizes a 2-phase nonreturn-to-zero signal to encode data for data loading and a unique gate array structure to accomplish the match-out function. The output structure is prepared in parallel between a "data" register and a "key" register with a shift "mask" register controlling each. Careful bit-level design techniques. The multicomparator was fabricated using advanced silicon gate array technology (CMOS technology) on a 2.5 μm × 1.0 μm chip containing 2000 devices. MSB (most significant bit) input (TTL) level. Data rate is more than 100 Mbytes/sec. The average power dissipation was 228 mW at 100 MHz and 300 mW at 100 MHz.

INTRODUCTION

OVER the past several years, there have been significant amounts of energy devoted to the fabrication of large and faster semiconductor memories and conventional digital processing units (CPU) in chip form. In the process, many other applications of large-scale integration (LSI) to computer architecture have been neglected [1]. LSI has improved the technological distinction between logic and memory. It is now economically feasible to decentralize the CPU of a computer by replacing much of its combinatorial functions with functional hardware to improve system efficiency. Presently, an inefficient manner of processing data is spent on comparing and accessing data in peripheral. Peripherals are usually controlled directly by the CPU and have little or no associated logic of their own. A great improvement in this situation can be made by developing peripheral logic units. This article shows such a peripheral to accomplish data-to-data processing and data-to-CPU knowledge sharing. This paper describes a 128-bit multicomparator that is designed to perform the match-out function.

The block diagram of the multicomparator is shown in Fig. 1. The block consists of three independently clocked data registers with associated exclusive-or gates. In operation, the device indicates a match between the data word and the masked bits of the key word. The multicomparator is loaded with a key word by initially shifting the word into the key register and loading the register in static mode. While the key word is being loaded, the comparator is enabled by enabling word¹ in the appropriate locations of the

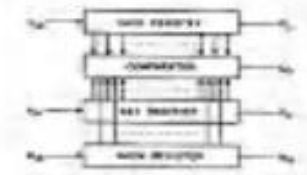


Fig. 1. Block diagram of multicomparator.

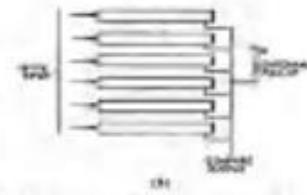
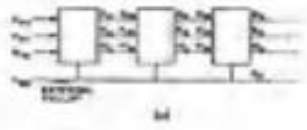
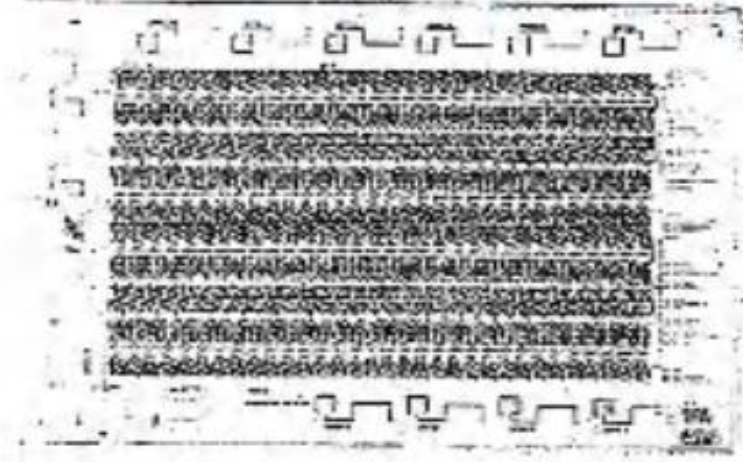


Fig. 2. Parallel structure of multicomparator. (a) Disabled. (b) Enabled, wordwise.

mask register. Masking allows the multicomparator to search for bit strings of varying length and composition. For example, assume it is necessary to search for all words containing a specific 113-bit code. By entering the 113-bit code in the key register and masking out the rest of the comparator, the multicomparator is configured to search for this code wherever it occurs in the data file. Once the multicomparator is loaded with "key" and "mask" words, the key being searched is usually shifted through the data register. The data words are compared in bit parallel with the masked bits of the key word as they pass through the data register. When a match is found, the compare output goes high. Large multicomparators can be constructed of the 128-bit device. Consider [Fig. 2(a)], the comparator can be used to search for words larger than 128 bits. By implementing multicomparators in parallel [Fig. 2(b)], a wordwise, bit-parallel



128-bit Multicomparator chip, designed by Hagiwara in 1972-1973 and fabricated by Intel PMOS process.



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