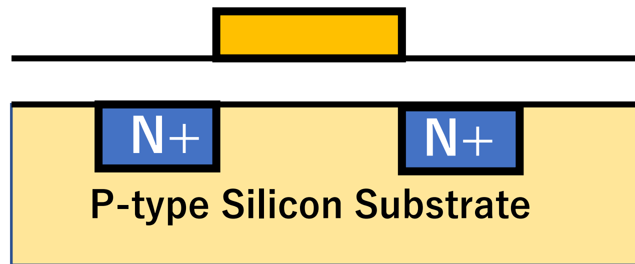
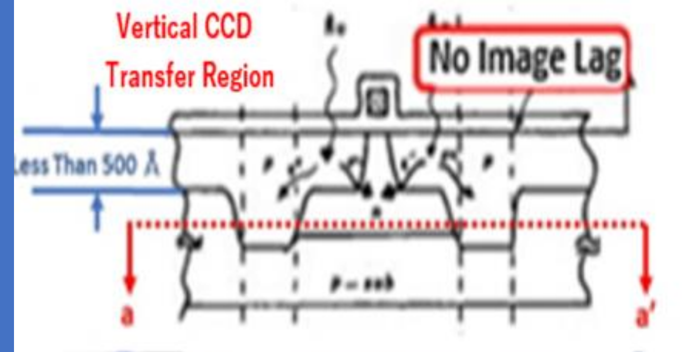
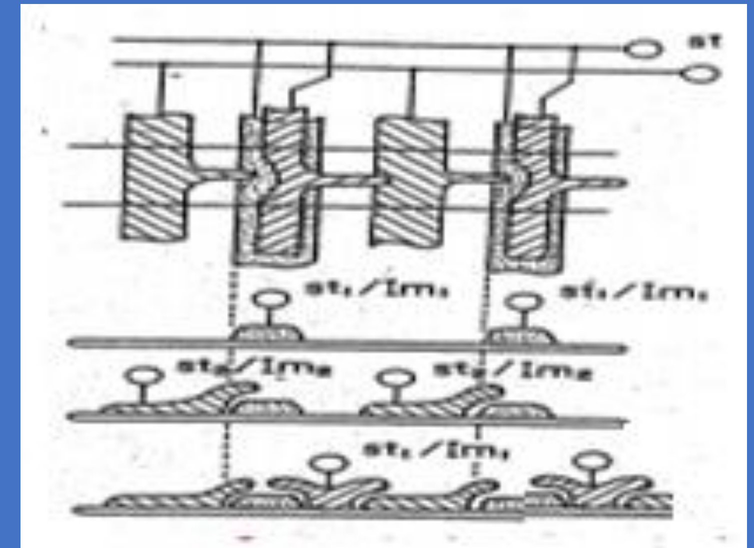
The self-aligned ion implantation technology using the Polysilicon Gate Patterns as Masking invented by Dr. Robert. W. Bower in 1966.

USP3472712, Oct 17, 1966 and USP3615934, Oct 30, 1967



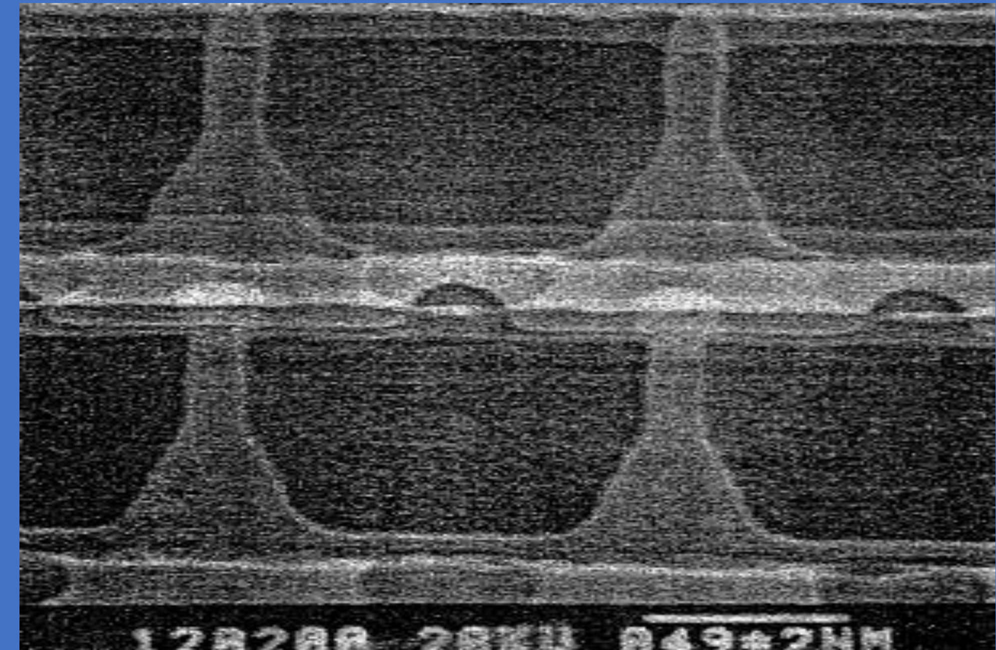




The cell size of the imaging area is 11 μm x 13 μm while the storage area has 11 μm x 13 μm cell size to keep the area occupation in the chip to the minimum.

The chip size of the device is 10.0 mm x 12.5 mm. The device is fabaricated in a buried-channel version of a-type (100) oriented 10-15Ω・cm silicon substrate with standard triple-layer overlapping-electrode-type polysilicon gate definition with the self-aligned boron atom ion implantation technology.

Using the polysiliocn patterning as an ion implantation mask, boron ions with a dose level of $7 \times 10^{12} cm^{-2}$ were implanted into the silicon substrate throughout the exposed portions of the thermall grown oxide The step provides self-aligned channel stops which surround the narrow-channel transfer part of each electrode.



(a) SEM picture of storage area.
Cell size is 11 μmH x 9 μmV