

1980年の特許にもIEDM1982の論文にもLocos Isolation の記載は皆無である。いつの間にかこの論文にはLocos Isolation が受光部に採用されている。

2014年12月1日(月)

映像情報メディア学会技術報告

ITE Technical Report Vol. 38, No. 47

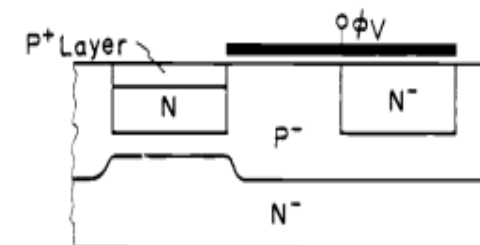
IST2014-52(Dec. 2014)

(Invited) Effect and Limitation of Pinned Photodiode

Nobukazu Teranishi^{1,2}

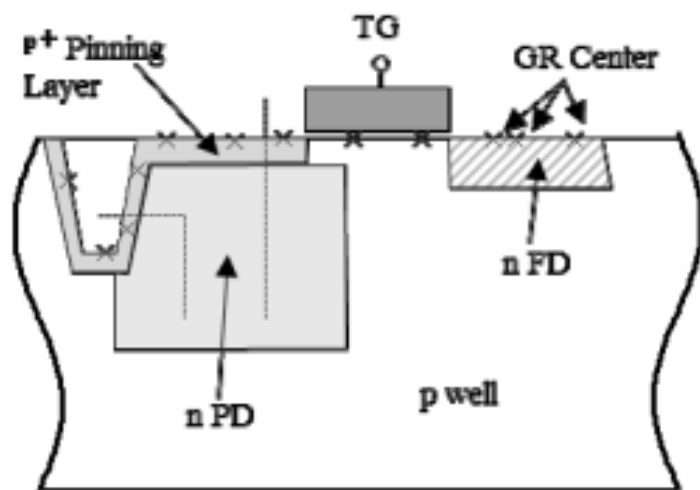
Abstract The pinned photodiode (PPD) is the primary technology for image sensors and used in almost all CCD image sensors and CMOS image sensors. This paper discusses effect and limitation of PPD, especially dark current and electronic shuttering. Even when PPD is used and silicon surface is neutralized, proposed model explains that GR centers at the silicon surface contribute the dark current. The temperature dependence is an activation type with activation energy, E_g , not $E_g/2$. It is important to reduce GR centers for dark current reduction at PPD also. It is also noted that the vertical overflow drain (VOD) shutter combined with PPD has potential of high speed shuttering with small skew.

(1) NEC (Teranishi) Buried Photodiode at IEDM1982

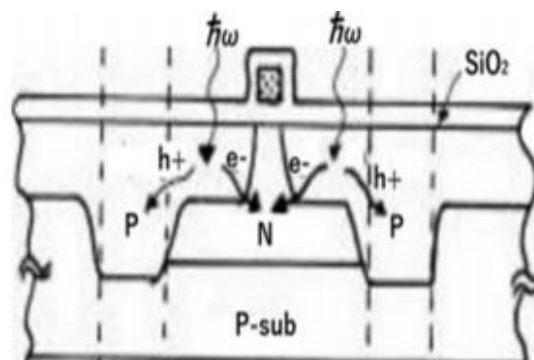


Practical and Actual Pinned Photodiode does not use LOCOS isolation, but with the adjacent P+ channel stops formed by Deep High Energy Implantation with Lamp Anneal technology developed by Kazuo Nishiyama at Sony in 1978

(2) Pinned Photodiode with LOCOS Isolation described by Teranishi in 2014



(3) Pinned Photodiode Sony(Hagiwara) 1978



(4) Pinned Photodiode explained by Semiconductor History Museum

