2026年秋季応用物理学会 paper 11p-N304-6 萩原良昭 AIPS

ダブルおよび多重接合型太陽電池のデバイス構造とプロセス製法の提案

Bipolar Transistor PP-NP-P+ Parallel Multi Junction Type Solar Cell

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P2026_09_11_応物_session_13.4_11p-N304-6_ダブルおよび多重接合型太陽電池のデバイス構造とプロセス製法の提案_Slides.pdf

P2026_09_11_応物_session_13.4_11p-N304-6_ダブルおよび多重接合型太陽電池のデバイス構造とプロセス製法の提案_Slides.mp4

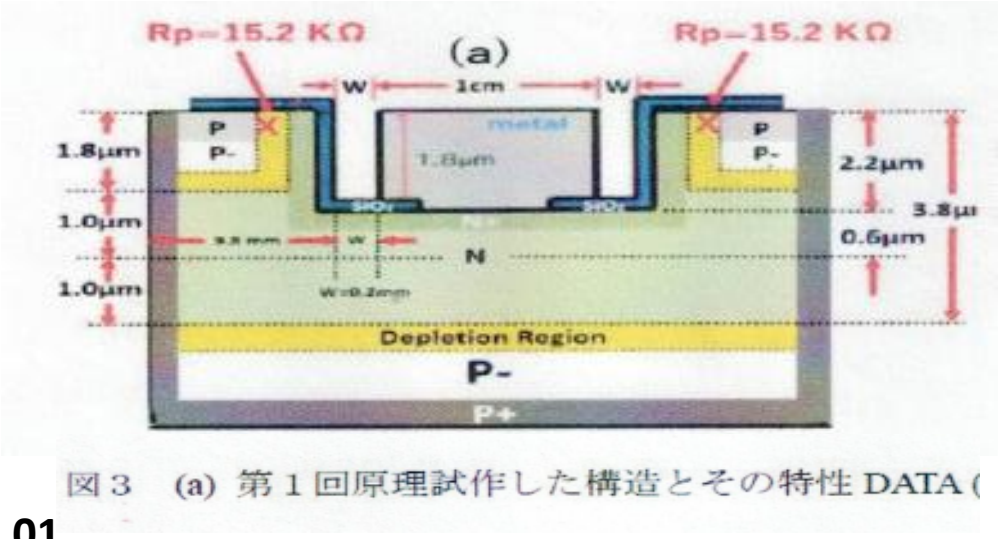


図３ (a) 第１回原理試作した構造とその特性 DATA (

Rpの値

Single	Double
14.4 MΩ	15.2 KΩ

Iscの値

Single	Double
8.4 mA	12.4 mA

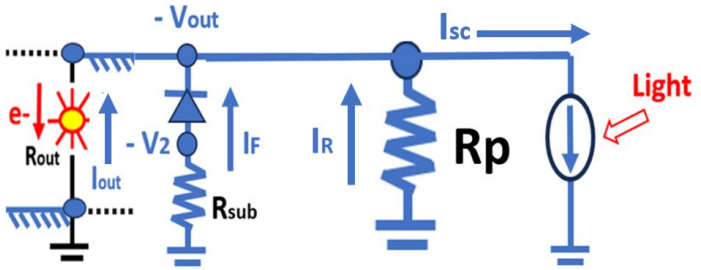
http://www.aiplab.com/

$$\text{Efficiency} \sim \frac{Isc - I_F - I_R}{Isc}$$

$Isc = I_F + I_R + I_{out}$

$I_R = V_{out}/Rp$

$I_F = Io\ (\exp(V_{out}/kT) - 1)$



ダブルおよび多重接合型太陽電池のデバイス構造とプロセス製法の提案

高エネルギーイオン打ち込み技術が必要

高価な描画装置不要

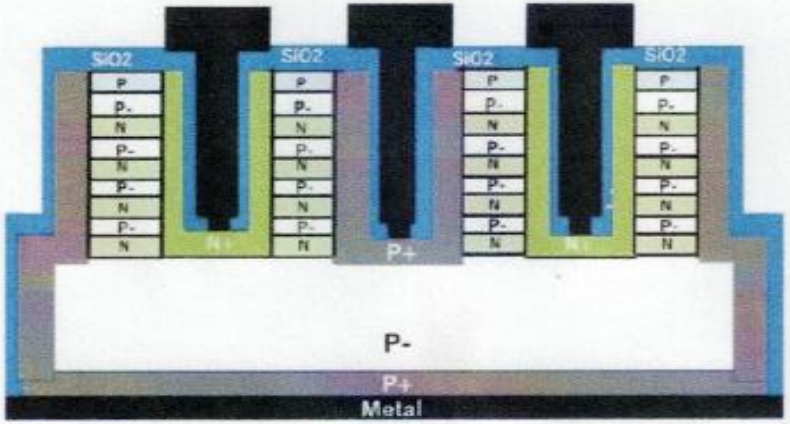


図１シリコン結晶型多重接合太陽電池の新構造

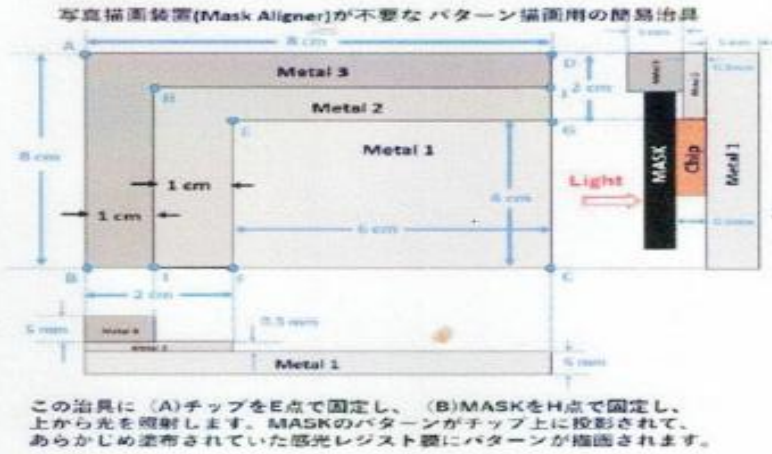
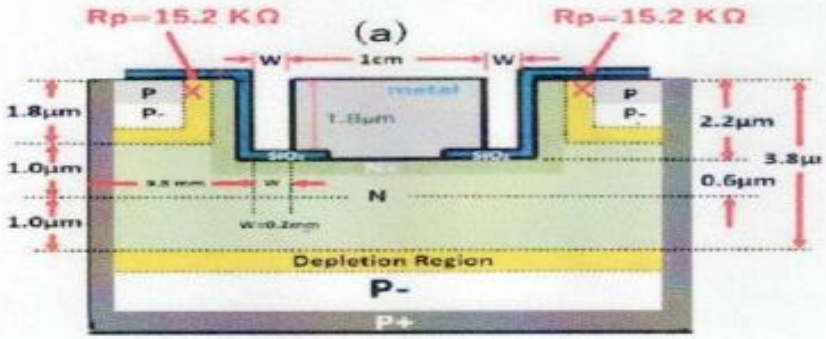
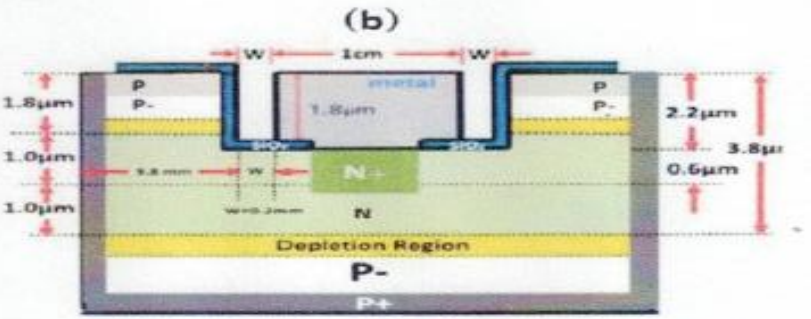


図２簡易生産用の治工具構造





	I_0 [A]	n	R_S [Ω]	R_P [Ω]	V_{oc} [V]	I_{sc} [mA]	η [%]	S [cm²]
(1) Single	2.4×10^{-10}	1.04	2.00	14.4M	0.46	8.4	0.29	9
(2) Double			2.37	15.2k	0.46	12.4	0.32	9

$I_{sc2}/I_{sc1} = 12.4/8.4 = 148\,\%$

図３ (a) 第１回原理試作した構造とその特性 DATA (b)Rp 値の低減を避けた改善構造案

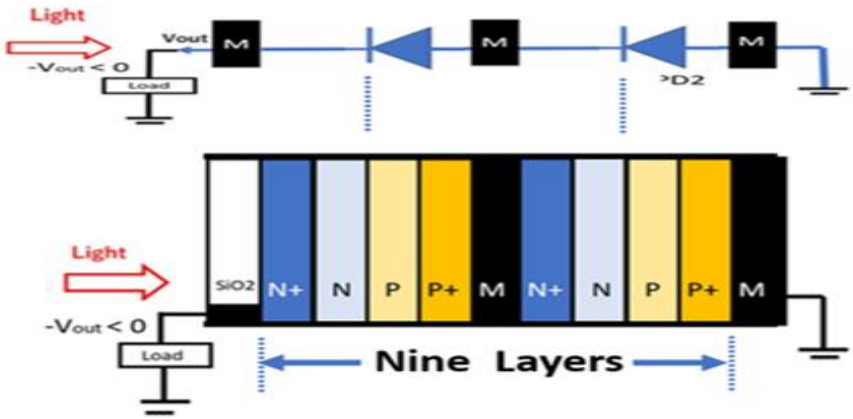
2026年秋季応用物理学会 paper 11p-N304-6 萩原良昭 AIPS

ダブルおよび多重接合型太陽電池のデバイス構造とプロセス製法の提案

光電変換効率の向上の為には、ダブルまたは多重 TANDEM 型接合構造を使い、光電変換に寄与する空乏層領域幅を増加させることが一般に知られている。しかし、TANDEM（直列）の直列構造ではホール吸収領域（P+)と光電子誘導領域（N+）の間に透明電極材料を使用としている。

ペロブスカイト等の有望な太陽電池の材料が実用化されている一方、まだまだ電気的安定性向上の為の努力が必要である。特にその透明電極の材質には信頼性と寿命の改善努力に課題が多い。

Tandem type Double Junction
Nine Layers Process Solar Cell



薄膜軽量で安価に生産できる
ペロブスカイト太陽電池では
ローラーに巻きつけて簡単に
破損ゴミ汚れや寿命による
特性劣化の場合は、簡単に
取り換える事が可能です。
大型太陽光発電でも将来
設備投資の節約につながると
期待します。透明電極の
寿命信頼性が課題に残ります。

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ダブルおよび多重接合型太陽電池のデバイス構造とプロセス製法の提案

一方シリコン材料には長年の生産実績があり、信頼性も寿命にも問題がない。大型設備投資を必要とする大型太陽光発電所の建設にはシリコン結晶シングル接合型太陽電池が広く採用されている。本研究は、タンデム（直列）型でなく、シリコン結晶を使い、BIPOLAR トランジスタ（並列）型の PNP 接合や PNPN 接合型の製法技術をヒントに、高エネルギーイオン打ち込み技術を駆使して新しいシリコン結晶型多重接合太陽電池の新構造と低コスト化に期待される製法を提案..

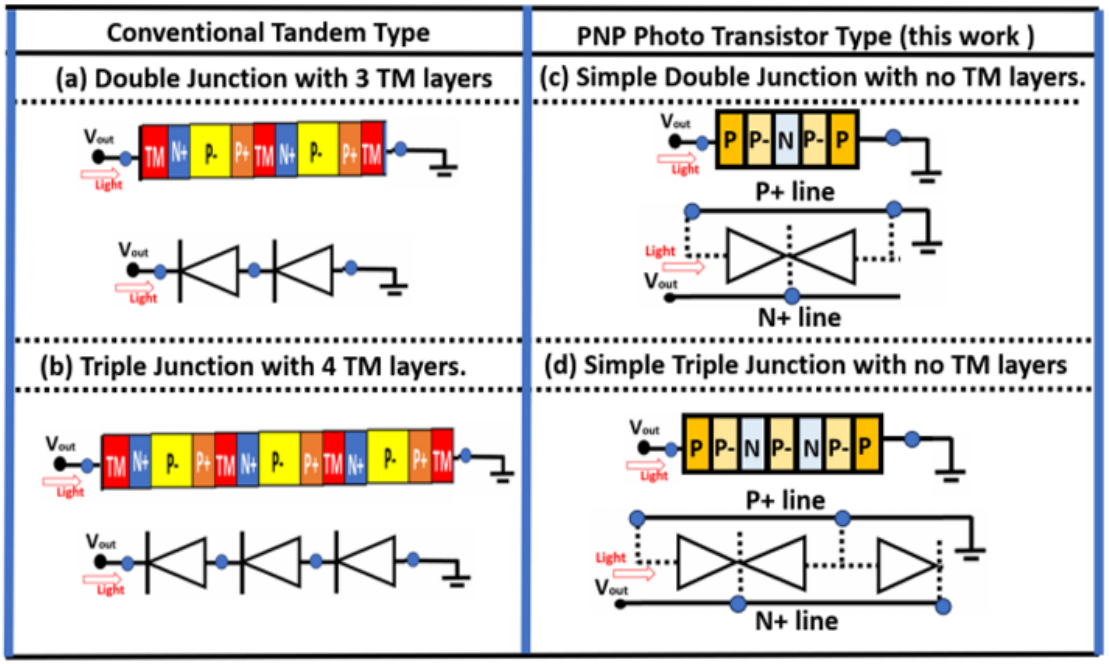

Fig.10 Difference of Tandem type and PNP&PNPN Photo Transsitor Type

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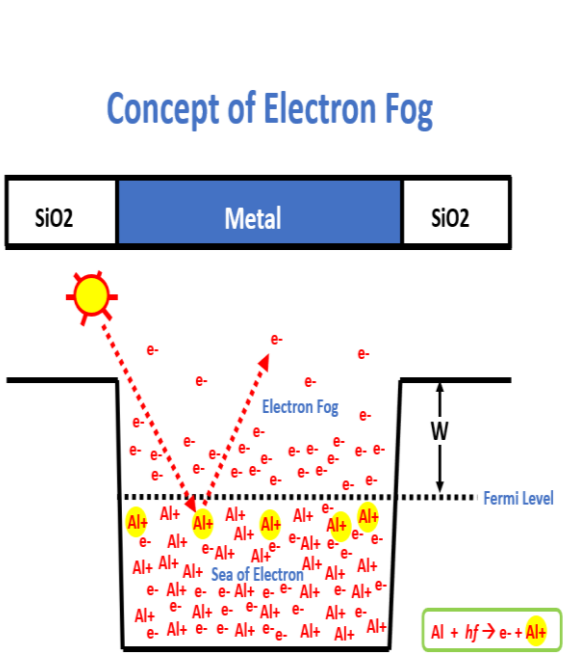
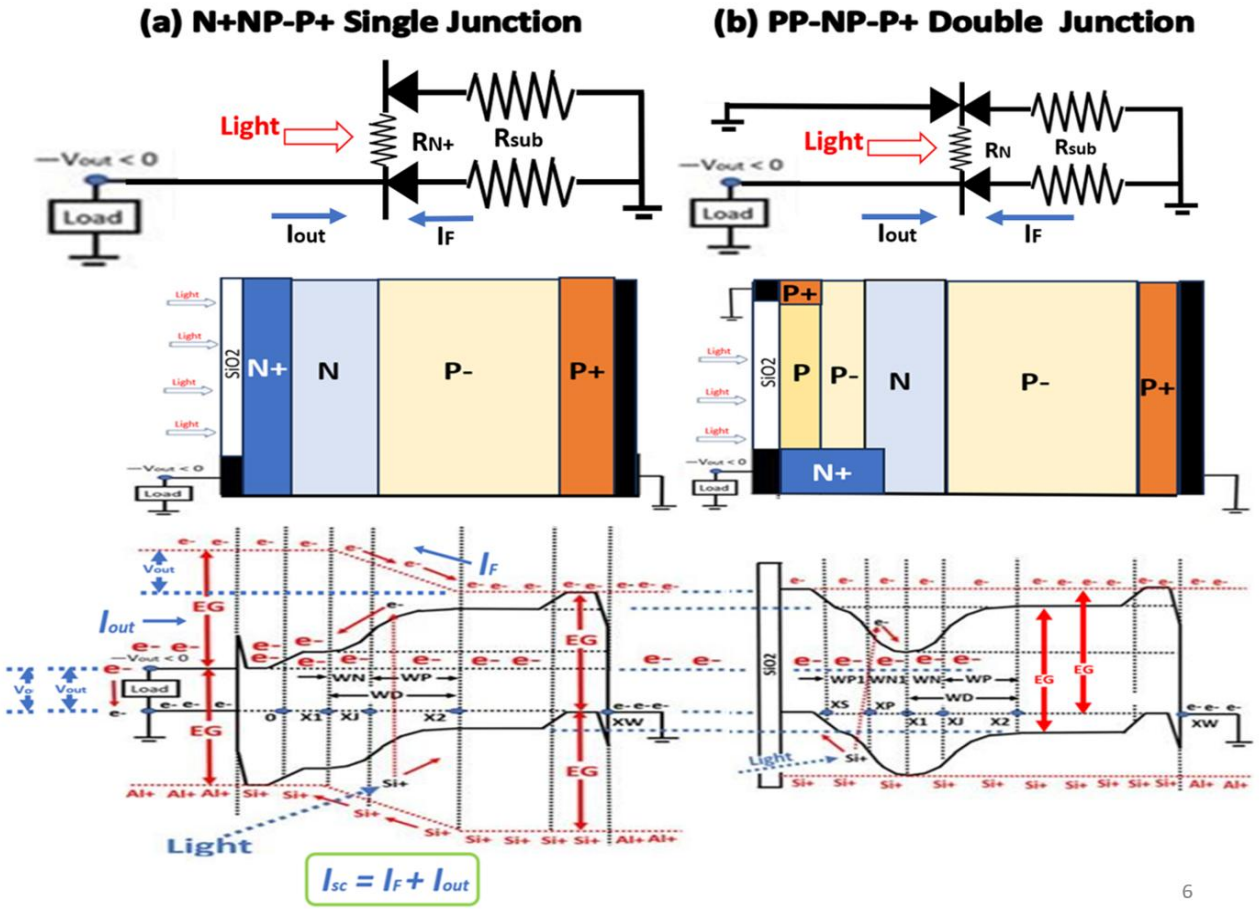
ダブルおよび多重接合型太陽電池のデバイス構造とプロセス製法の提案

電子の流れ（動き）を水の粒子だけでなく雲（水蒸気）の動きとして理解する必要がある。





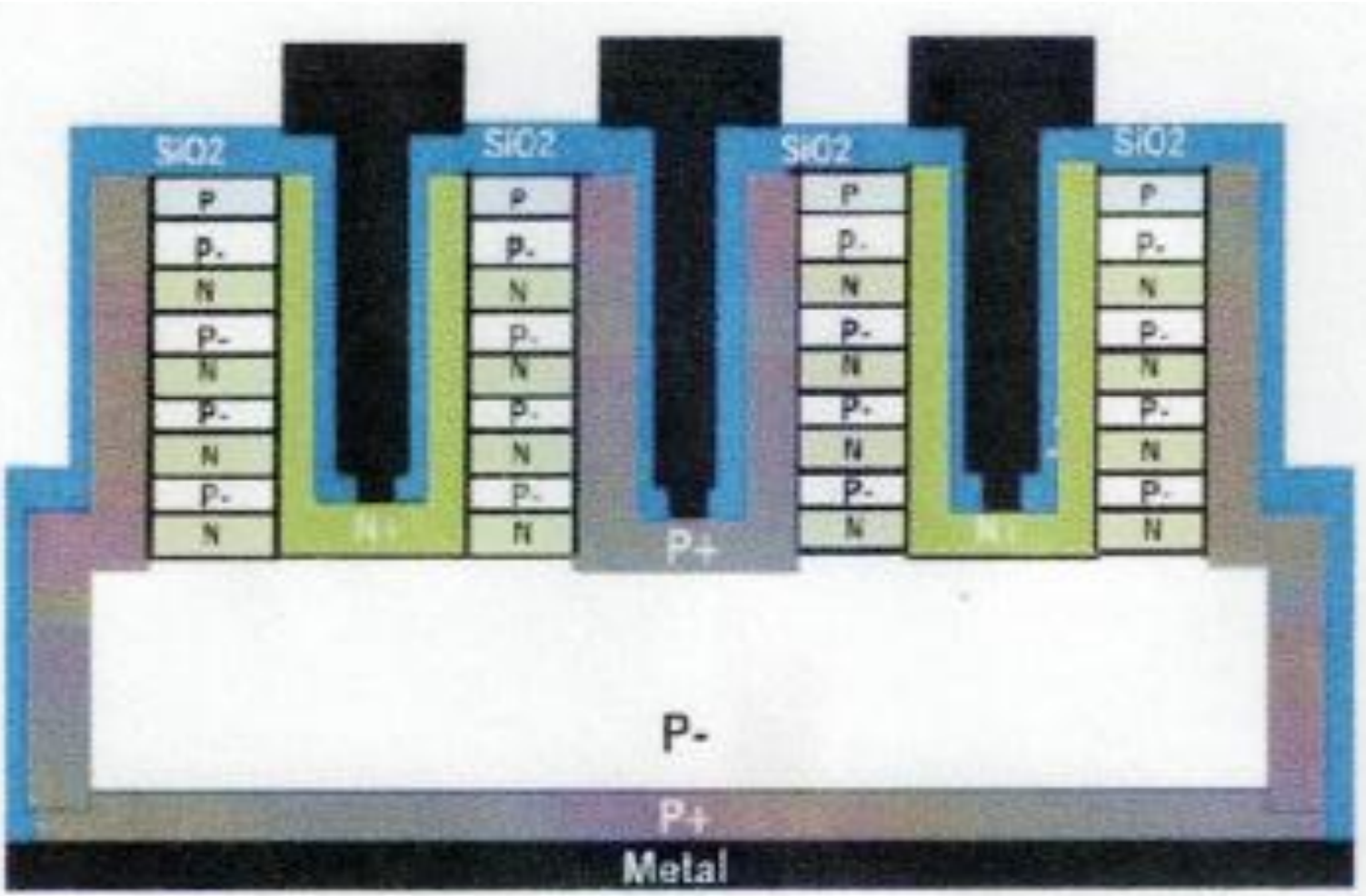


図１シリコン結晶型多重接合太陽電池の新構造

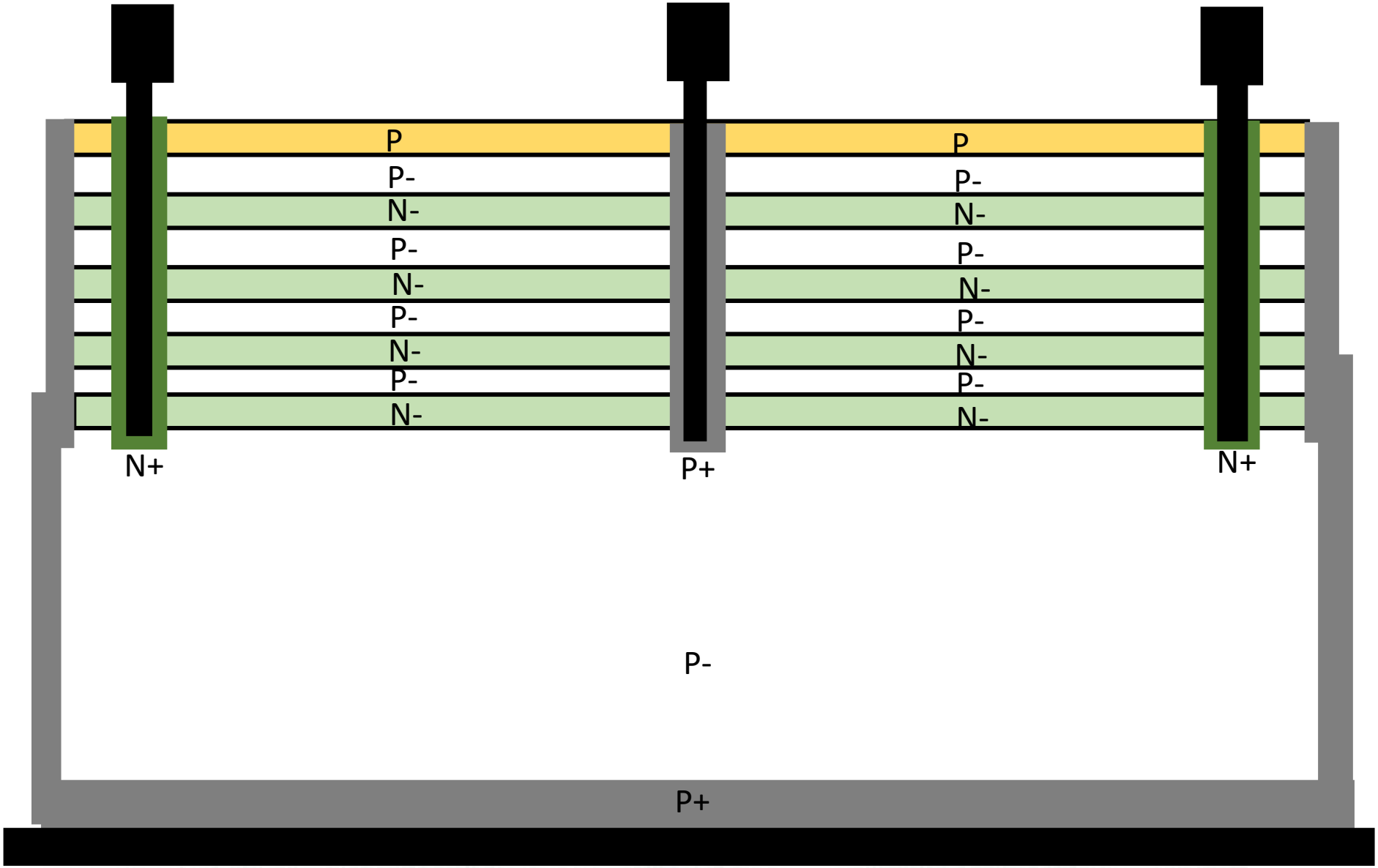


図１シリコン結晶型多重接合太陽電池の新構造

$DP= 10E14\ cm^{-3}$

P- (100Ωcm)

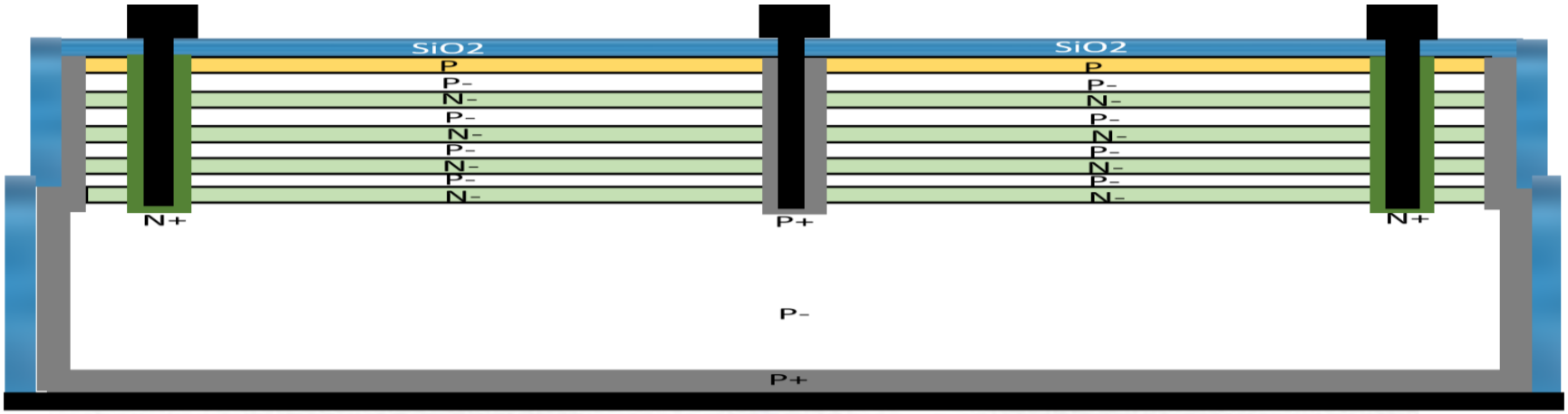
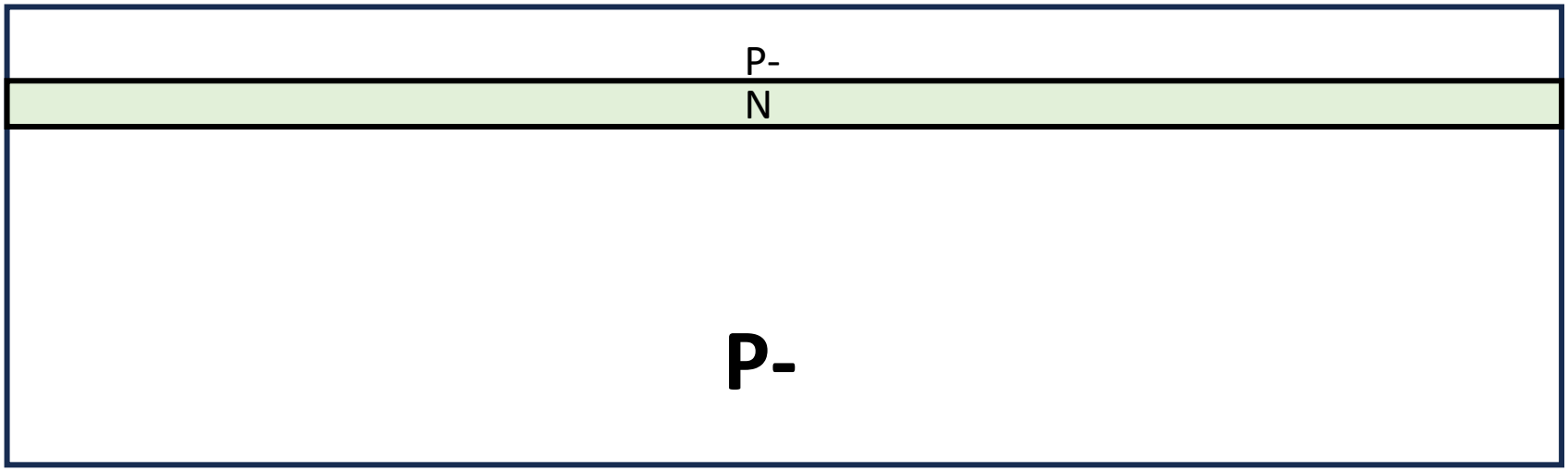


図１シリコン結晶型多重接合太陽電池の新構造



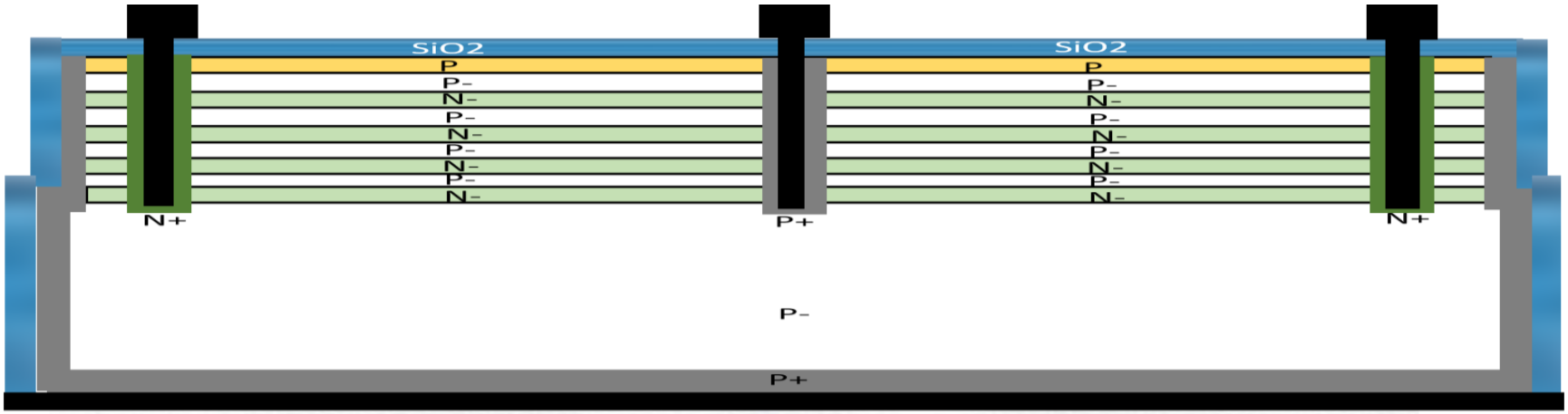


図１シリコン結晶型多重接合太陽電池の新構造

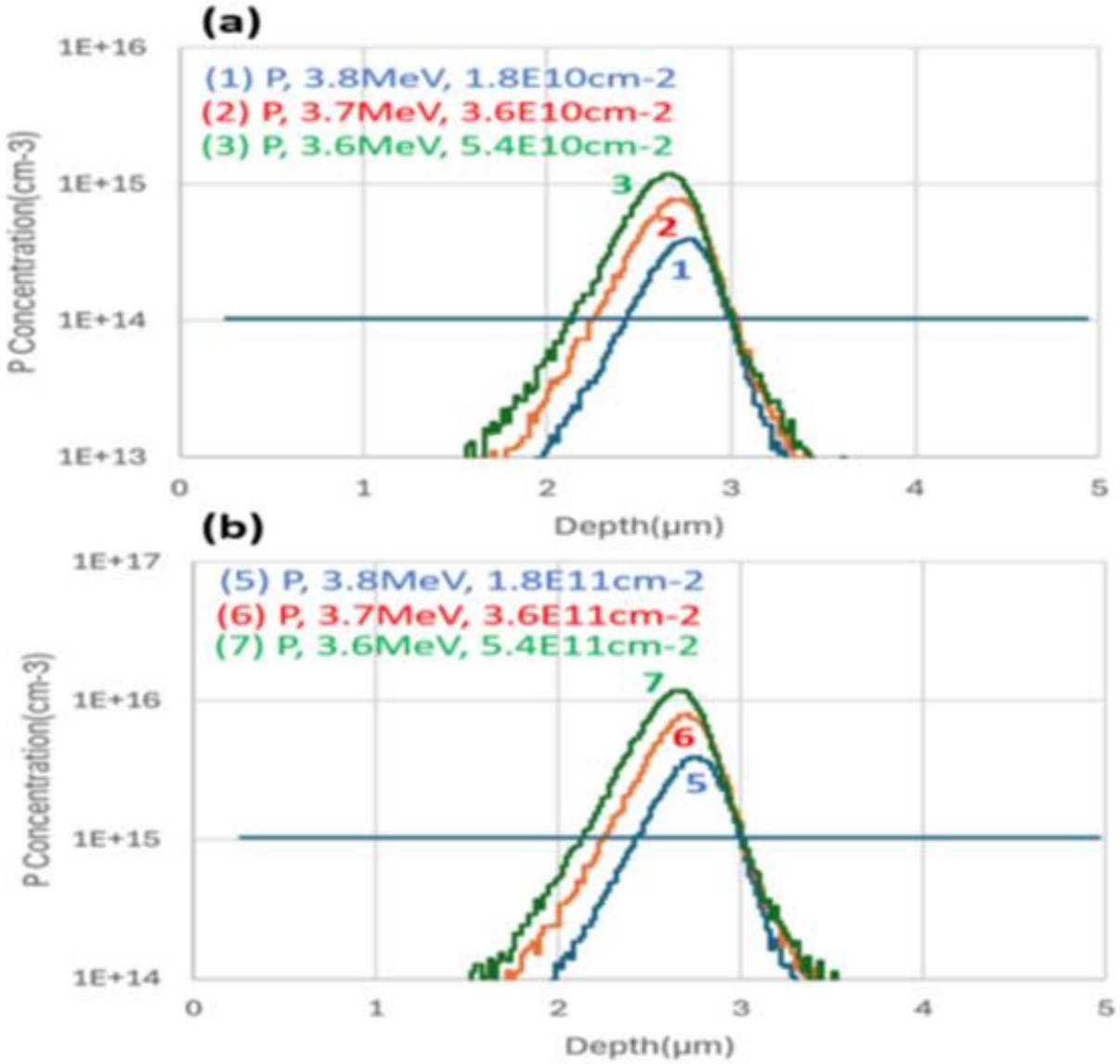
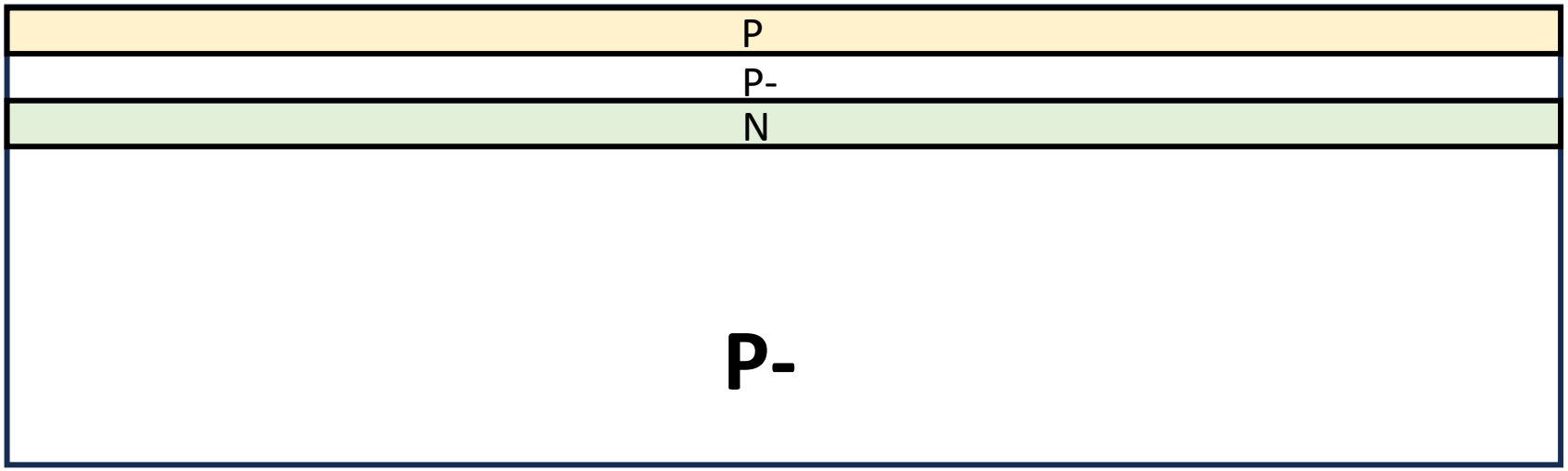


Fig.7 Impurity Doping Profile of Phosphoras Ion Implantaionl



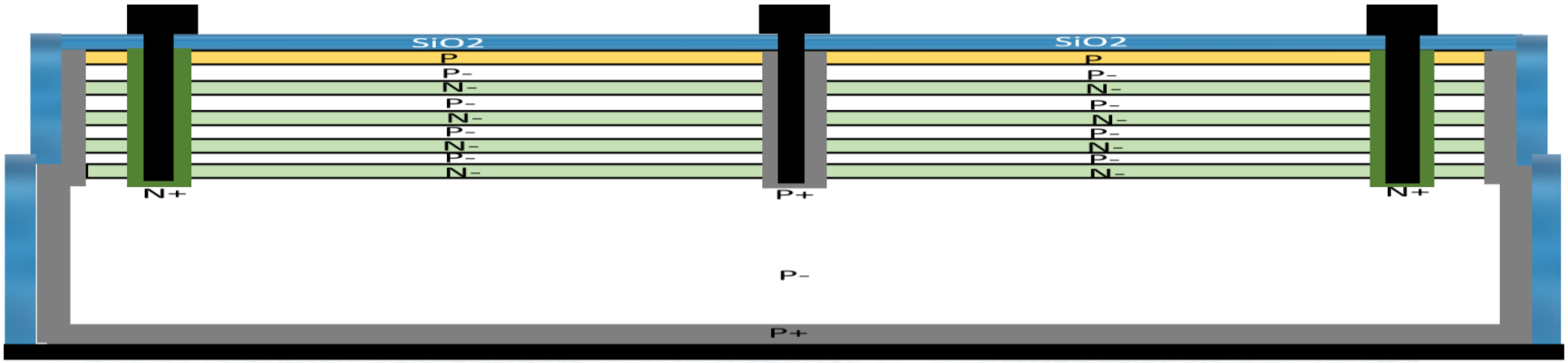


図１シリコン結晶型多重接合太陽電池の新構造

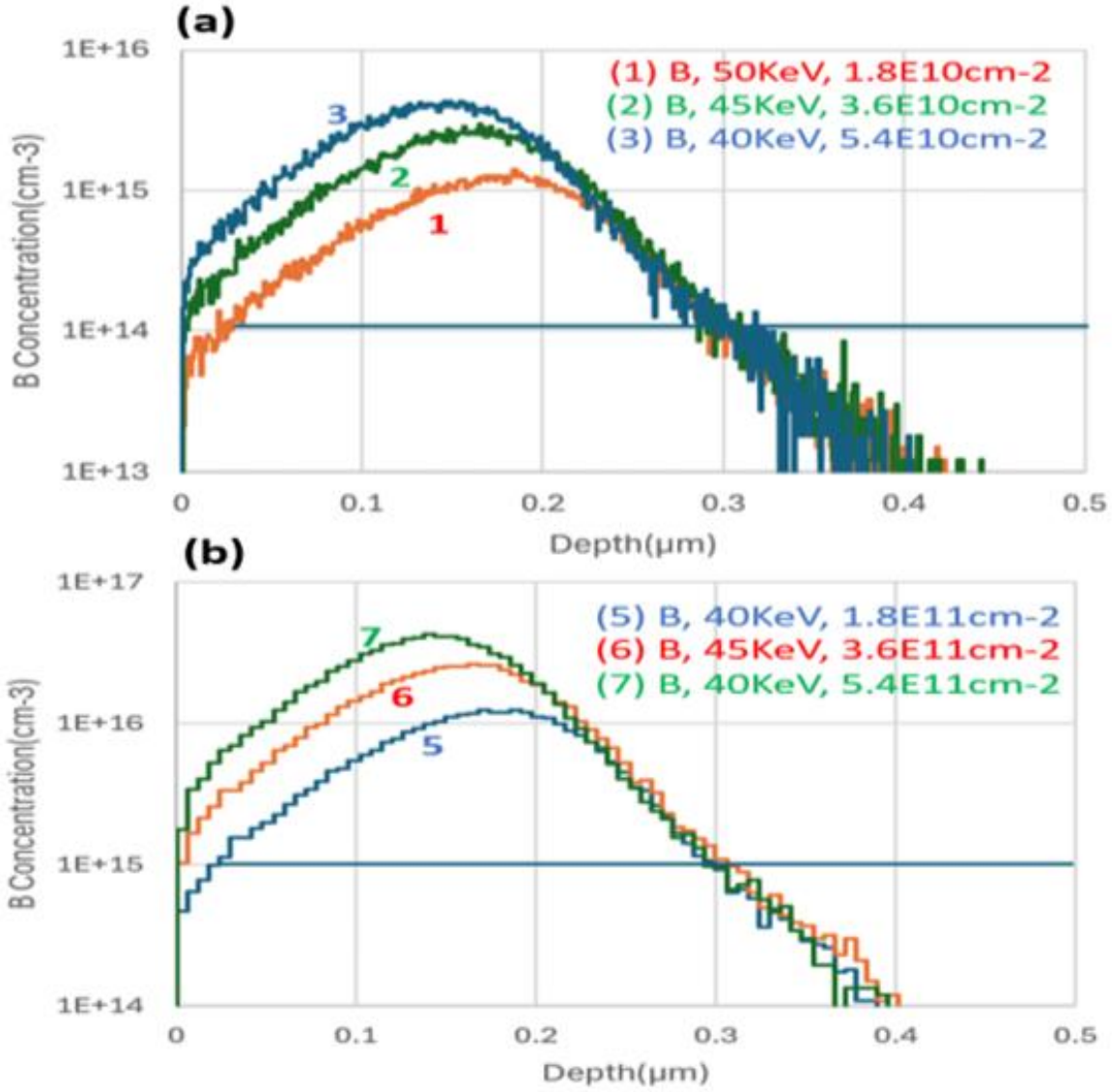


Fig.8 Impurity Doping Profile of Phosphoras Ion Implantaionl

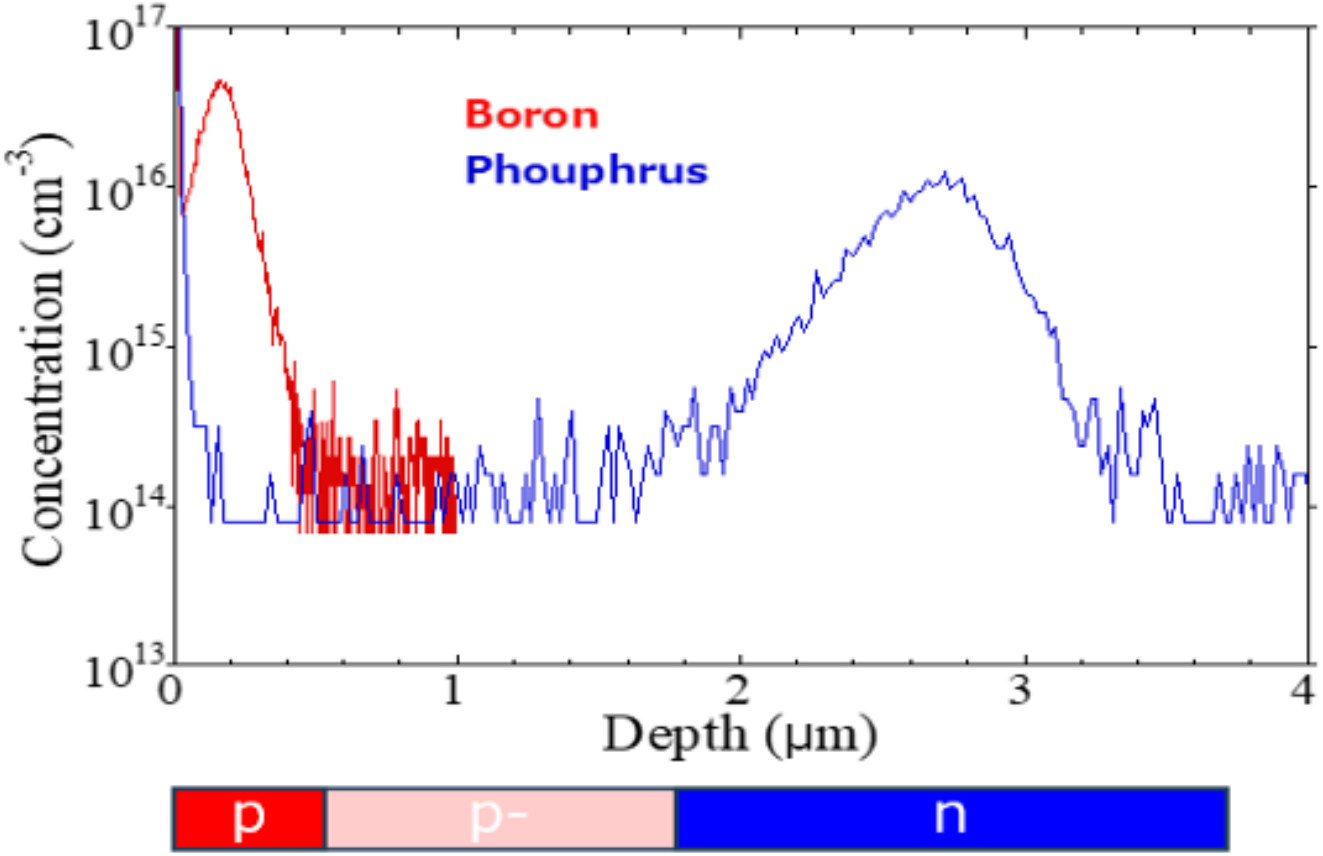
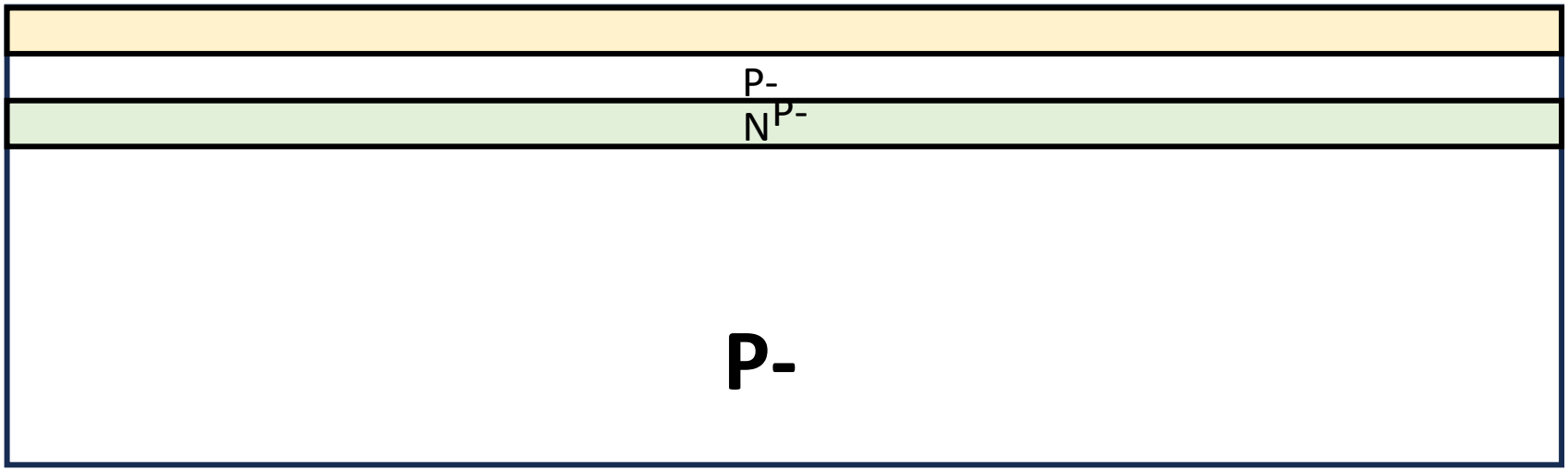
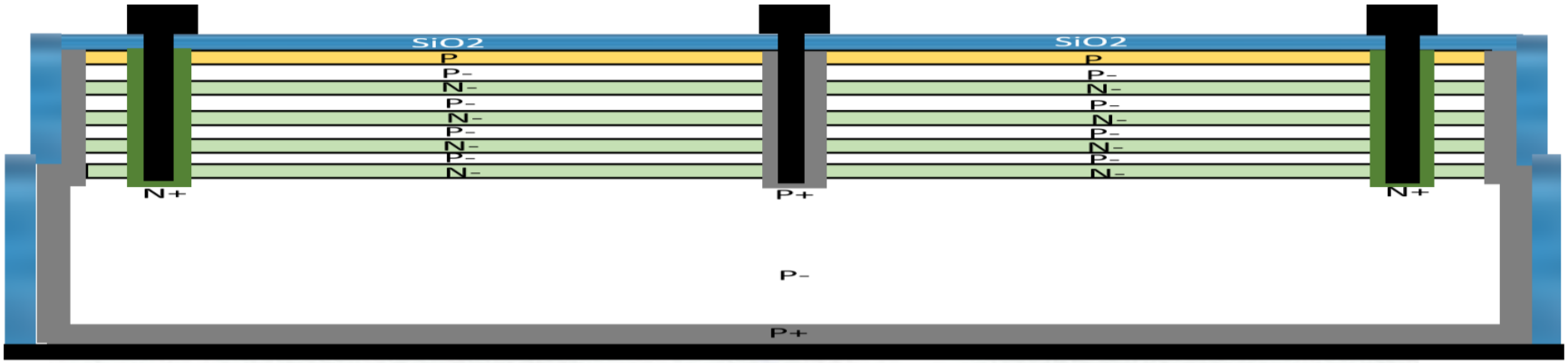


Fig.9 Impurity Doping Profile of Fabricated PP-NP- Junction Sample





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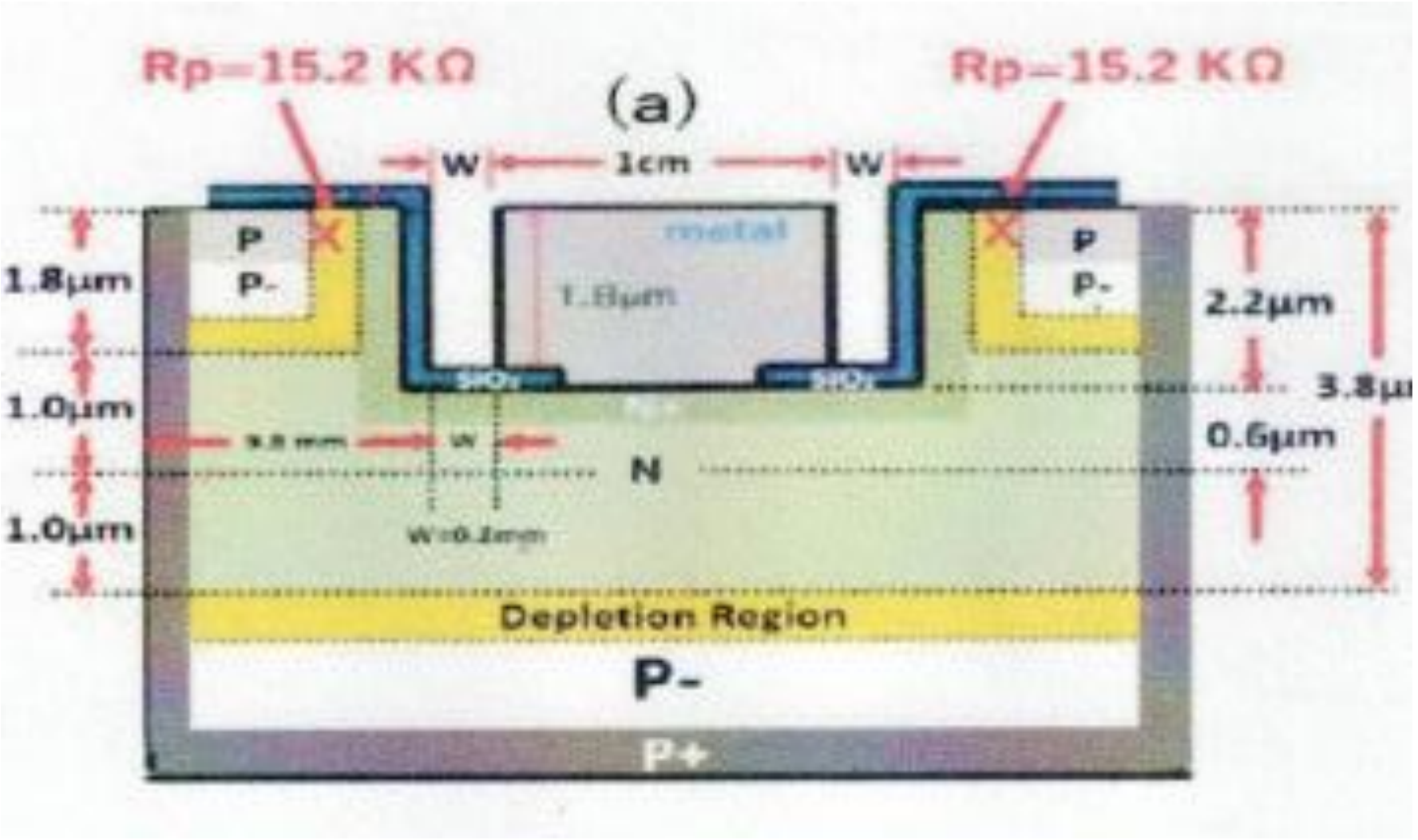
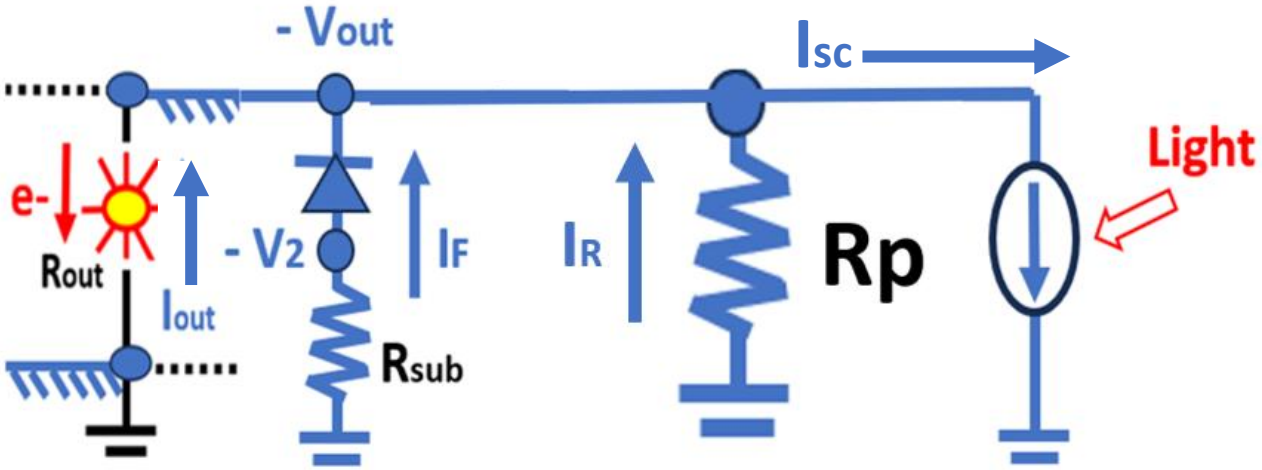


	I_0 [A]	n	Rs [Ω]	Rp [Ω]	V_{oc} [V]	I_{sc} [mA]	η [%]	S [cm²]
(1) Single	2.4×10^{-10}	1.04	2.00	14.4M	0.46	8.4	0.29	9
(2) Double			2.37	15.2k	0.46	12.4	0.32	9

図３　(a) 第１回原理試作した構造とその特性 DATA (b)Rp 値の低減を避けた改善構造案

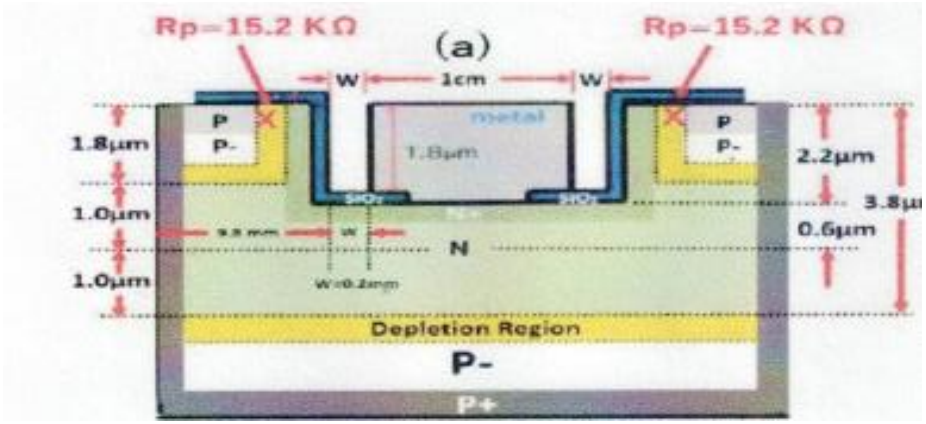


Rpの値

Single	Double
14.4 MΩ	15.2 KΩ

Iscの値

Single	Double
8.4 mA	12.4 mA



$$\text{Efficiency} \sim \frac{I_{sc} - I_F - I_R}{I_{sc}}$$

$I_{sc} = I_F + I_R + I_{out}$

$I_R = V_{out}/Rp$

$I_F = Io\ (\exp(V_{out}/kT) - 1)$

	I_0 [A]	n	Rs [Ω]	Rp [Ω]	V_{OC} [V]	I_{SC} [mA]	η [%]	S [cm²]
(1) Single	2.4×10^{-10}	1.04	2.00	14.4M	0.46	8.4	0.29	9
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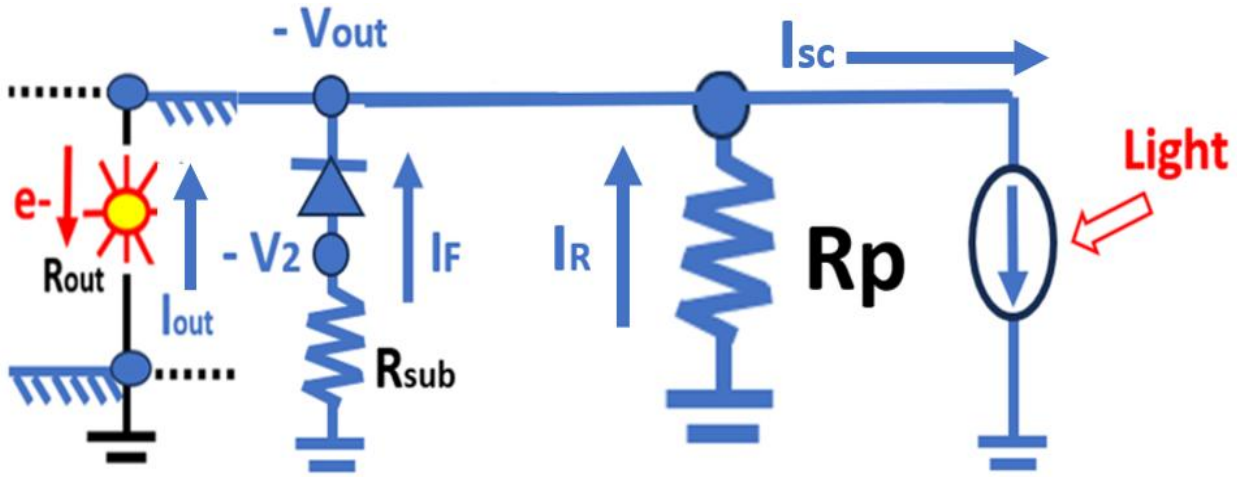
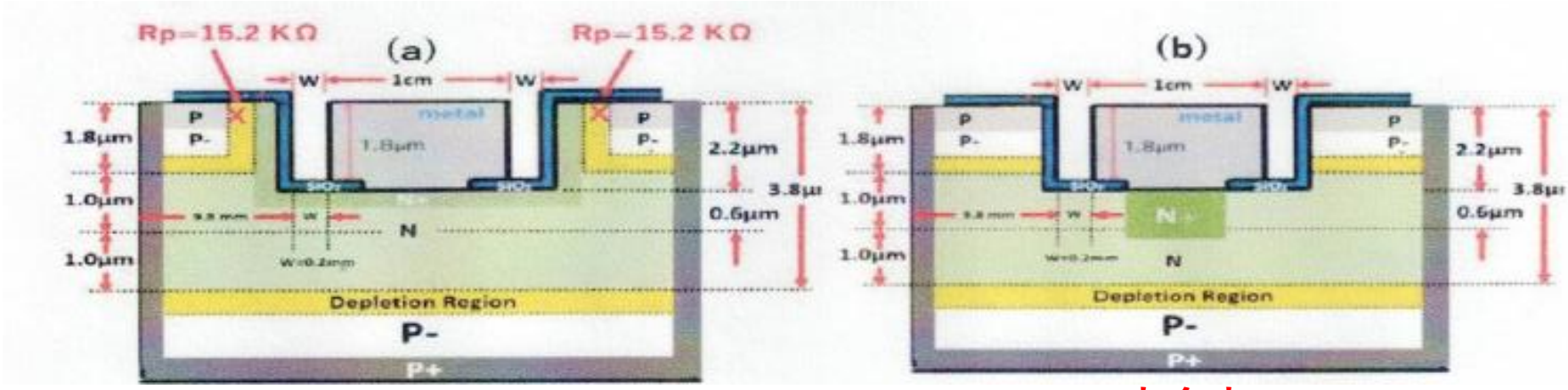


Rpの値

Single	Double
14.4 MΩ	15.2 KΩ

Iscの値

Single	Double
8.4 mA	12.4 mA



完全案

	I_0 [A]	n	Rs [Ω]	Rp [Ω]	V_{OC} [V]	I_{SC} [mA]	η [%]	S [cm²]
(1) Single	2.4×10^{-10}	1.04	2.00	14.4M	0.46	8.4	0.29	9
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図３　(a) 第１回原理試作した構造とその特性 DATA (b)Rp 値の低減を避けた改善構造案

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 43, NO. 12, DECEMBER 1996

https://ieeexplore.ieee.org/document/544383

Yoshiaki Hagiwara,

Affiliation: SC Logic MCU Business Department, Sony Corporation, Atsugi, Japan

"High-density and high-quality frame transfer CCD imager with very low smear, low dark current, and very high blue sensitivity"

Published in: IEEE Transactions on Electron Devices,

Volume: 43, Issue: 12, December 1996, pp. 2122-2130.

ABSTRACT:

When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of the threshold voltage is observed. This narrow channel effect has been applied successfully in creating an asymmetric potential well under an electrode for two-phase CCD operation. The feasibility of this structure has been confirmed in a 242-element analog delay line. The application is now extended to a 800 H/spl times/492 V frame transfer-type buried channel CCD imager with 14.31818 MHz frame shift, which results in a very low smear level of 0.01%, which is good enough for low-cost multimedia video camera applications.

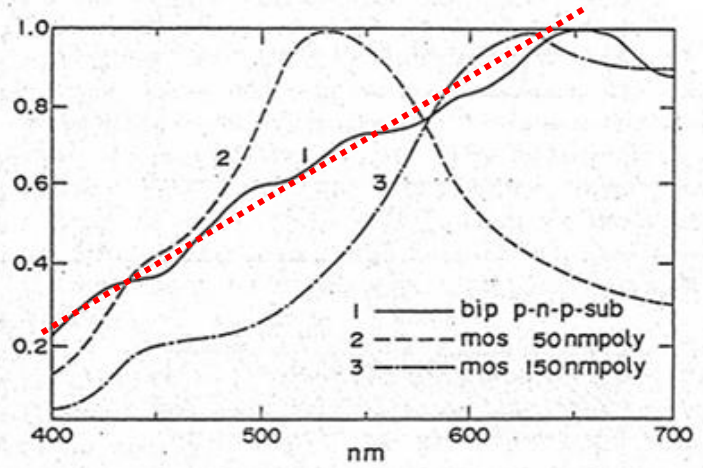
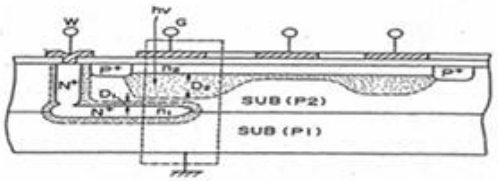


Fig. 7. Relative spectrum response. The relative response of the bipolar-type SiO_2–P2–N1–P1–SUB structure is compared with poly–SiO_2–N2–P(SUB) structures of the polysilicon thickness of 50 and 150 nm.

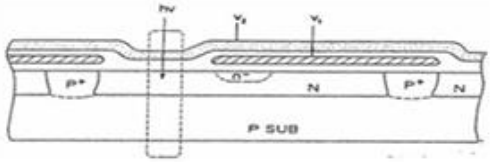
Early 1973

(3) mos 150nmpoly



Sony 1974

(2) mos 50nmpoly



Philips 1975

(1) bip p-n-p-sub

June 9,1975

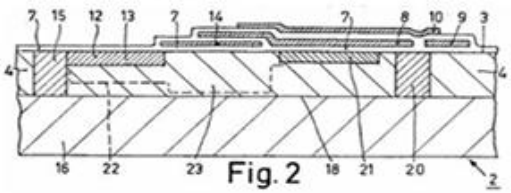
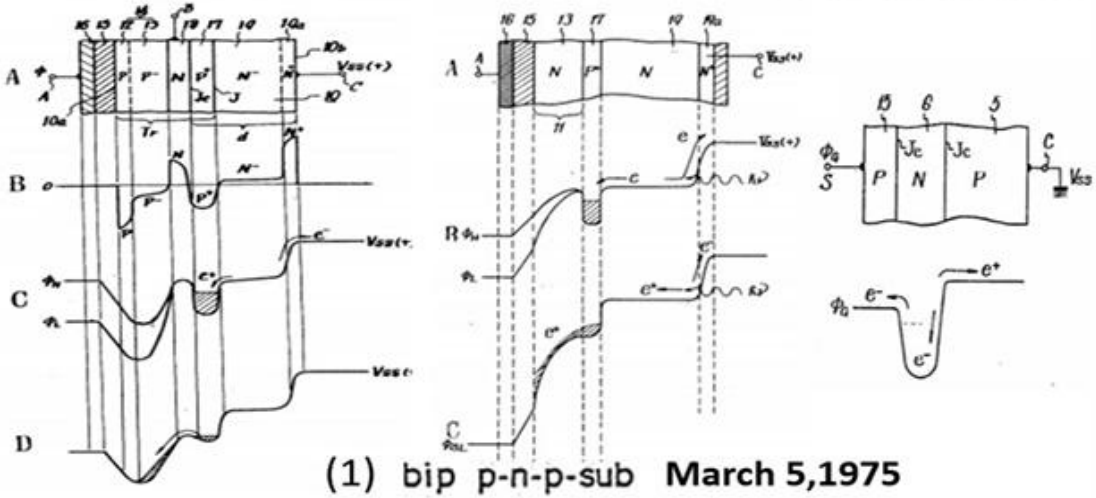


Fig. 2

世界最初のPNPダブル接合Photodiodeの発明

Sony (Hagiwara) March 5,1975

JPA1975-127646 JPA1975-127647 JPA1975-134985



(1) bip p-n-p-sub **March 5,1975**

受光面も裏面も金属端子で電圧固定された構造

世界最初のNPNP トリプル接合Photodiodeの発明(Sony萩原）

18

トランジスター生誕７５周年記念に際し、IEEE EDS学会からイメージセンサーの開発歴史について特別論文寄稿する機会をいただきました。

P2023_IEEE_EDS_Newsletter_Jan_2023_on_Chronology_of_Silicon_based_Image_Sensor_Development.pdf　*pp.18-21 参照*

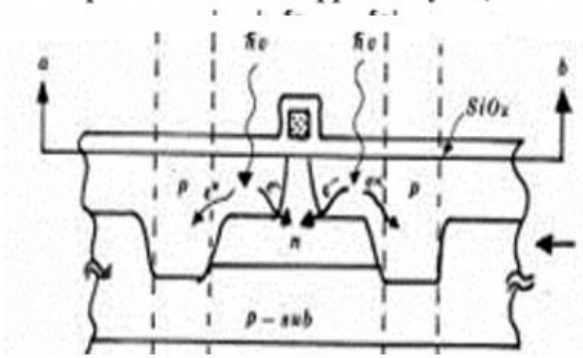
Image Sensorへの応用ではすでに1978年に日本応用物理学会主催の国際会議SSDM1978にて、SONY(萩原)が、あまり詳細な説明はしいませんが、図13で量子変換効率８０％を、ほぼ直線の傾きで、実している事を明示しています。

Image Sensorへの応用ではすでに1984年にKODAKも、IEEEの国際会議 IEDM1984 で詳細に図４で量子変換効率８０％実現している事を明示しています。

Image Sensorへの応用ではPNP接合の完全空乏化された埋め込みN層のConduction Band の谷底の電位 Minimum Potential (Vm)は深く逆バイアスされプラスの値になります。Vm＞０　になります。

太陽電池ではＮ層が順方向バイアスとなり、Vm＜０ になります。しかし多重接合にして、空乏層の幅を広げることが可能であり、変換効率も限りなく理論限界の８０％まで実現可能です。

Proceeding of the 10th Conference on Solid State Devices, Tokyo, 1978;
Japanese Journal of Applied Physics, Volume 18 (1979) Supplement 18-1, pp.335-340



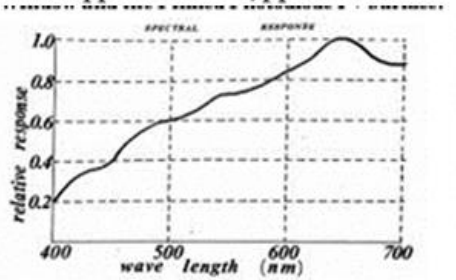


Fig.13 Spectral Response of the Pinned Photodiode with Pinned SiO2 Window and Pinned Surface.

Hagiwara_SSDM1978_Paper_on_Pinned_Buried_Photodiode.pdf

THE PINNED PHOTODIODE FOR AN INTERLINE-TRANSFER CCD IMAGE SENSOR

B. C. Burkey, W. C. Chang, J. Littlehale, T. H. Lee,
T. J. Tredwell, J. P. Lavine, E. A. Trabka

Research Laboratories, Eastman Kodak Company
Rochester, New York 14650

28 — IEDM 84

KODAK used LOCOS isolation which induced serious dark current and crystal defects degrading chip yield.

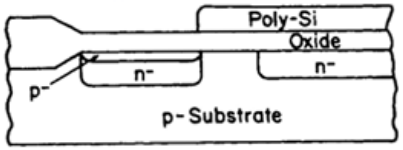


Fig. 1. Image cell schematic.

In this KODAK Pinned Photodiode IEDM1984 Paper, the Quantum Efficiency of 80% has been already achieved !

ABSTRACT

A pinned photodiode has been developed for use in an interline-transfer CCD. This photoelement has excellent blue response and high charge capacity. Both modeling and experimental results will be presented, including process considerations necessary to avoid unwanted barriers at the diode/transfer-gate edge.

CONCLUSION

Both the excellent blue response and high charge capacity of the pinned diode have been demonstrated. The processing of this device requires some care, however, to avoid the formation of potential barriers at the pinned diode/transfer-gate edge. This photoelement is ideal for applications requiring good blue response, large dynamic range, and no image lag. The processing considerations should also apply to the virtual-phase CCD.

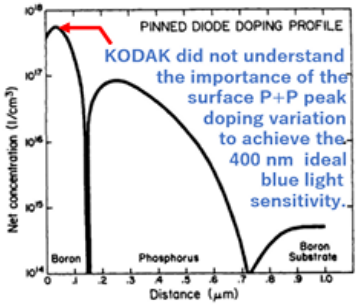


Fig. 2. Pinned diode doping profile.

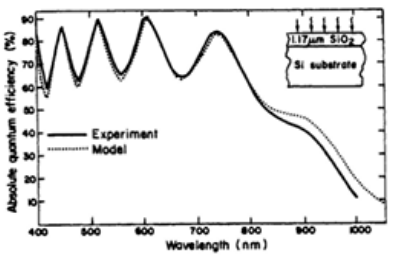
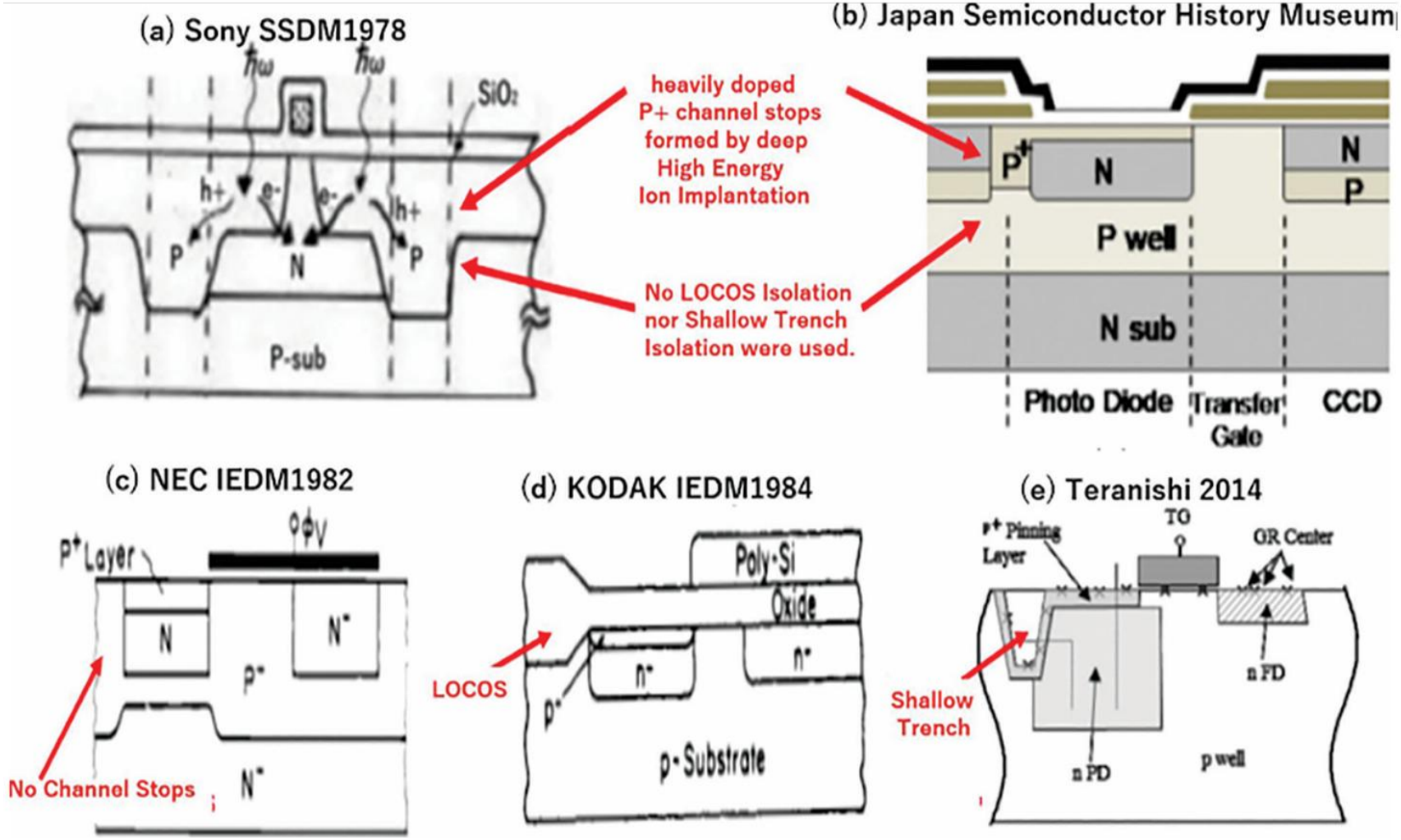


Fig. 4. Pinned diode spectral quantum efficiency. Solid and dotted curves are the experimental and theoretical curves, respectively.

The pinned photodiode for an interline-transfer CCD image sensor | IEEE Conference Publication | IEEE Xplore

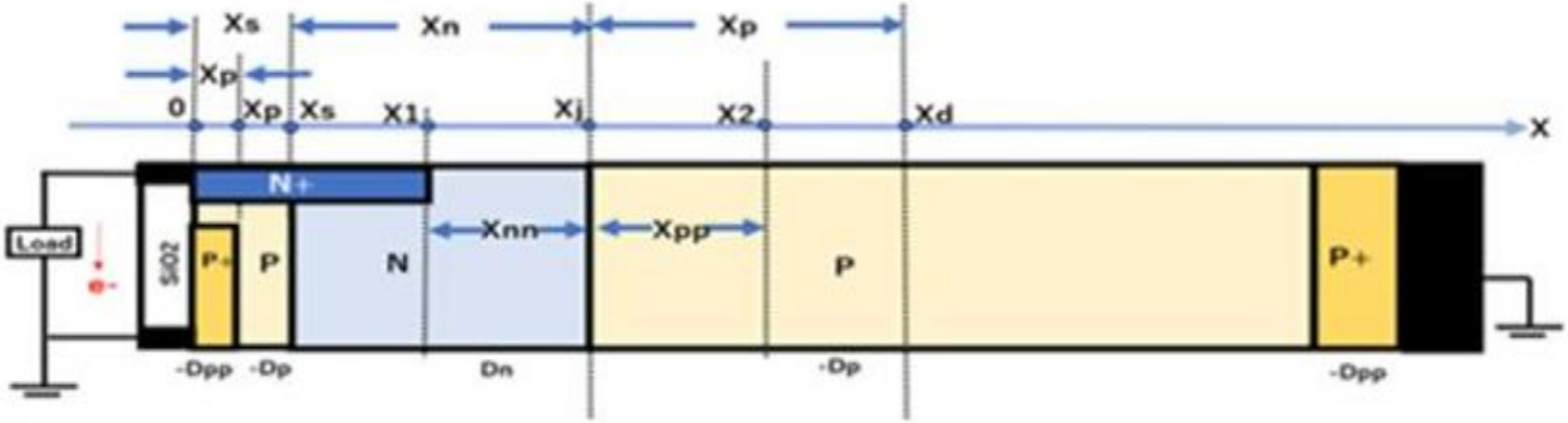
"ADVANCES in CCD IMAGERS" by Yoshiaki Daimon-Hagiwara,Sony

at CCD79 Conference, Edingburgh Scotland UK, Sept 1979

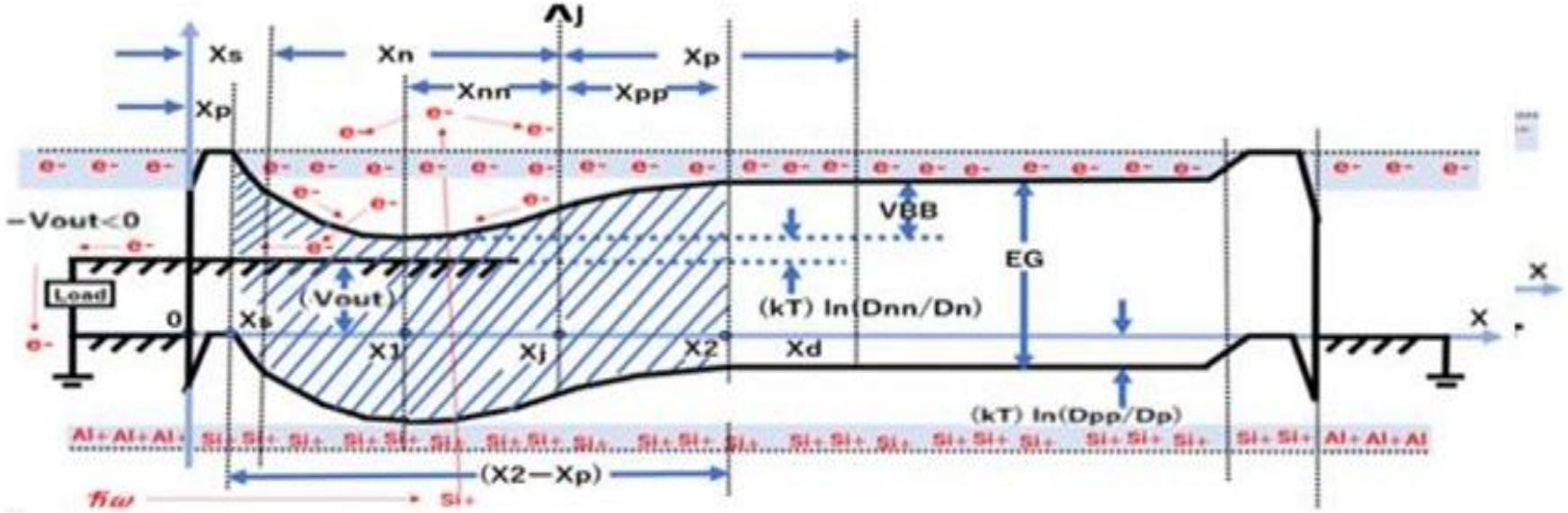


20

Cross Sectional View of P+PNPP+ Double junction Solar Cell

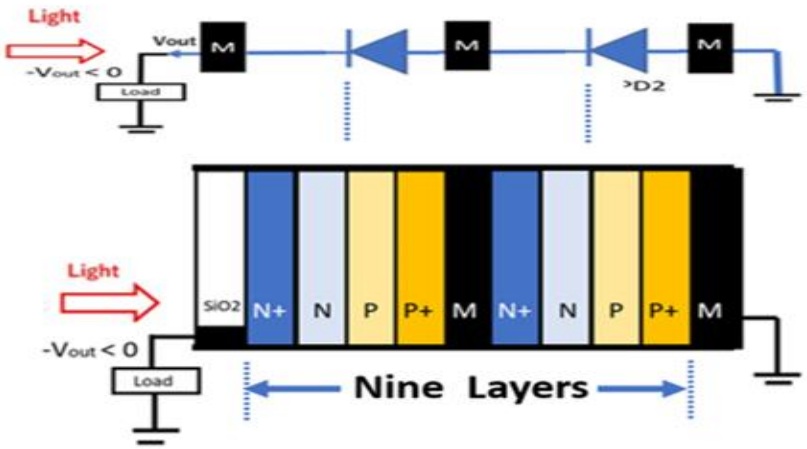


Band Diagram of P+PNPP+ Double junction Solar Cell

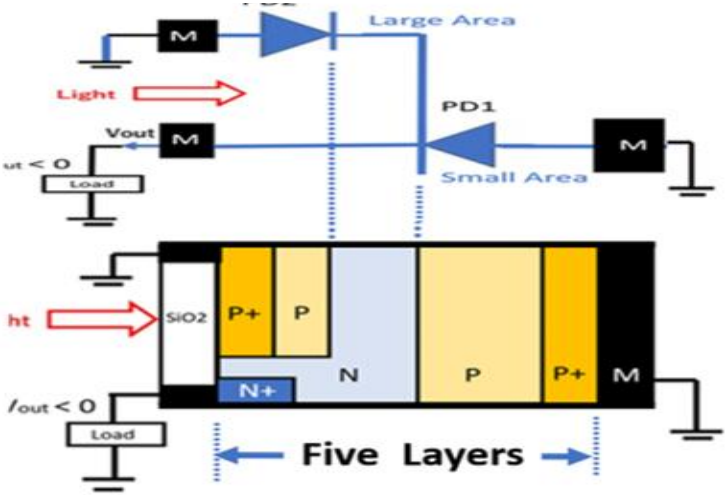


21 電子の流れ（動き）を水の粒子だけでなく雲（水蒸気）の動きとして理解する必要がある。

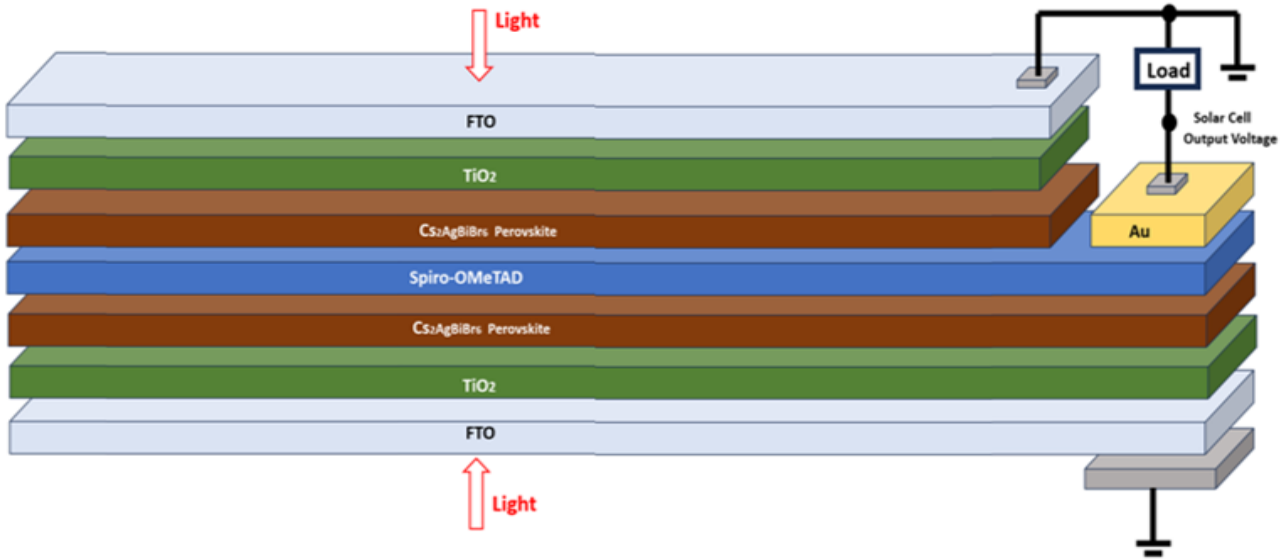
Tandem type Double Junction Nine Layers Process Solar Cell



Face-to-Face type Double Junction Five Layers Process Solar Cell



Double Junction type Perovskite Solar Cell



22

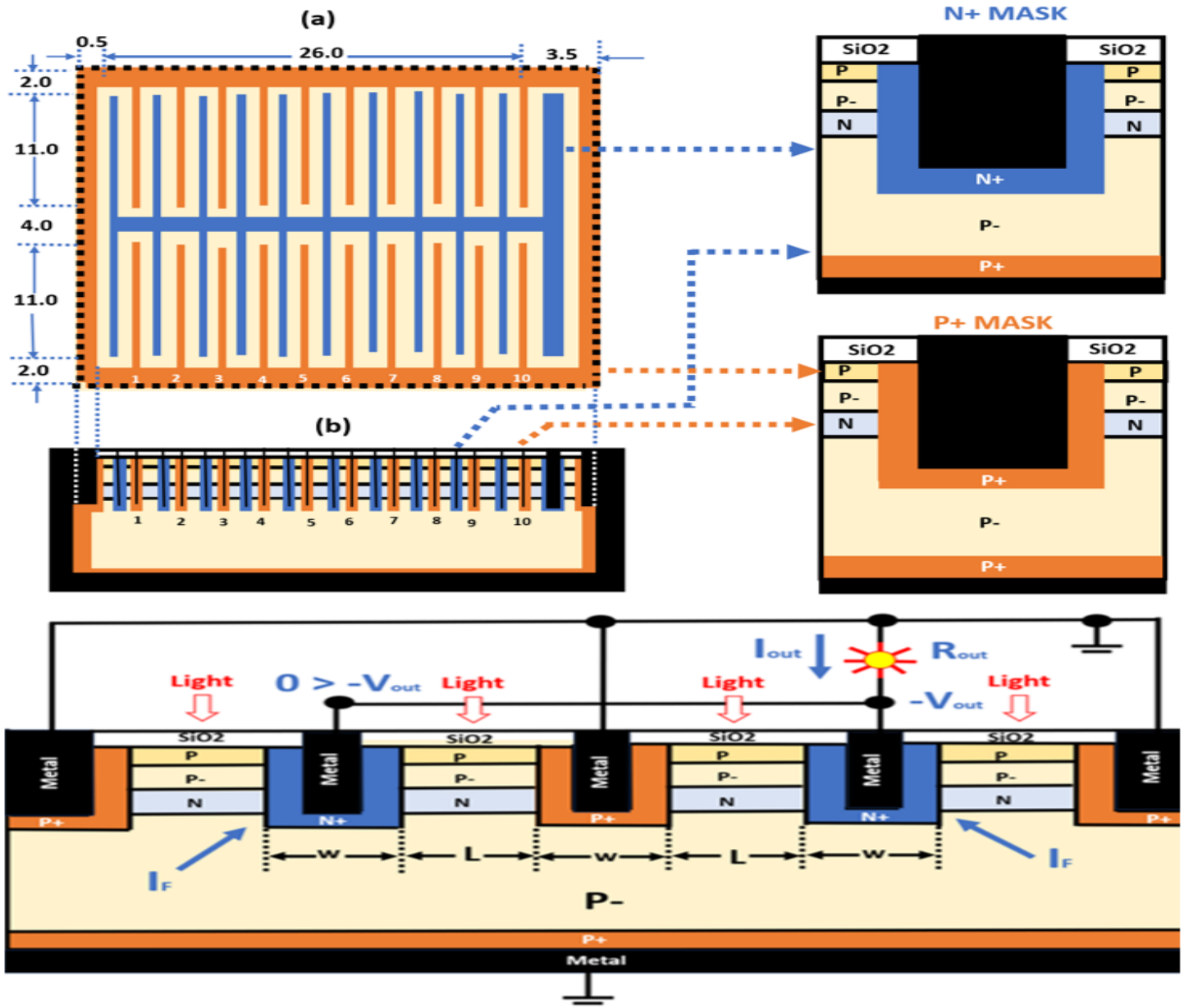


Fig. 1. Cross-sectional and top views of P+PNPP+ junction Solar Cell

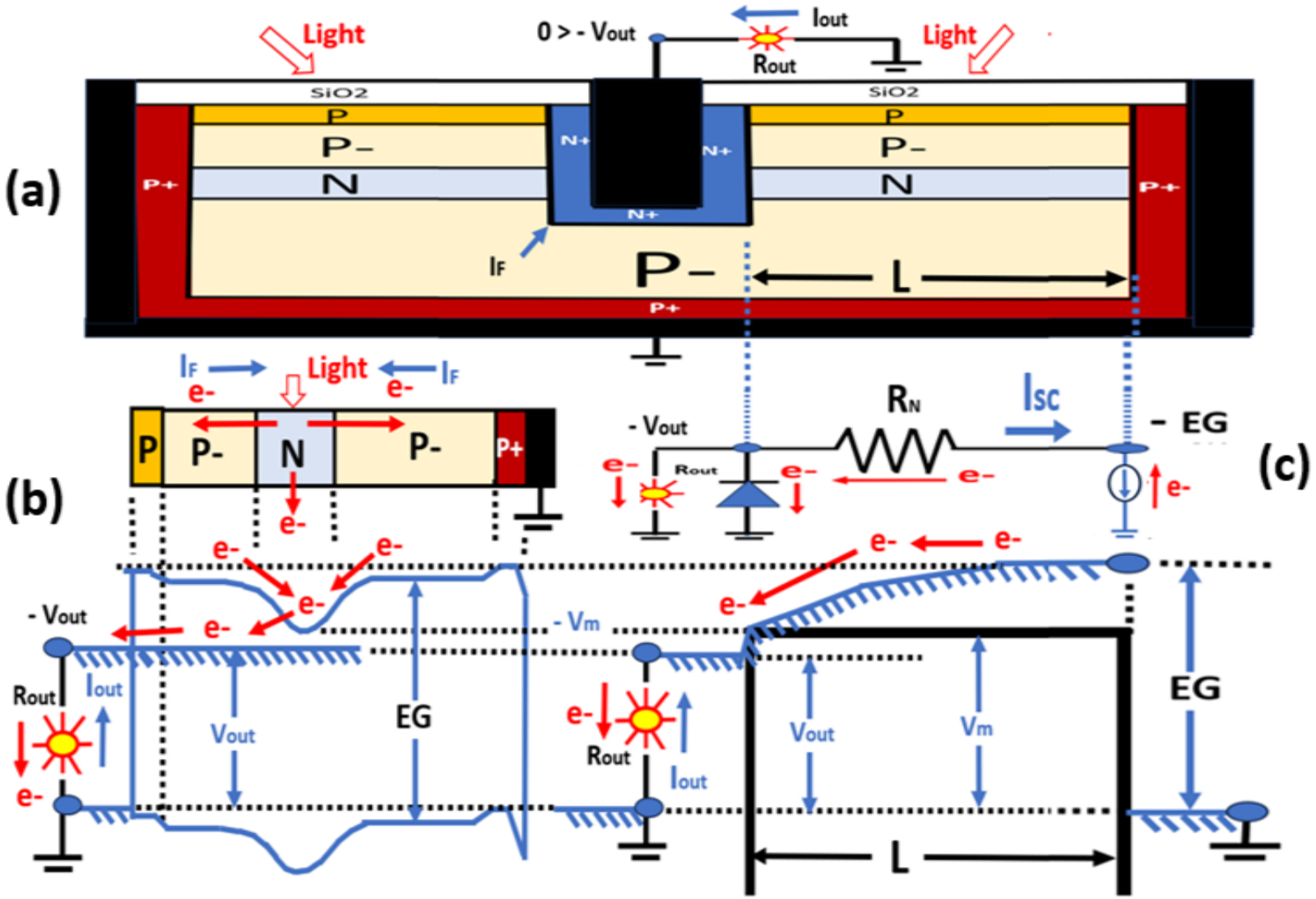


Fig. 2. A cross sectional view and a band diagram of PP-NP-P+ double-junction solar cell. Generated Photo electrons are directed to the N+ diffusion outlet drain thru the buried deep N-channel passage of the length L.↵

電子の流れ（動き）を水の粒子だけでなく雲（水蒸気）の動きとして理解する必要がある。

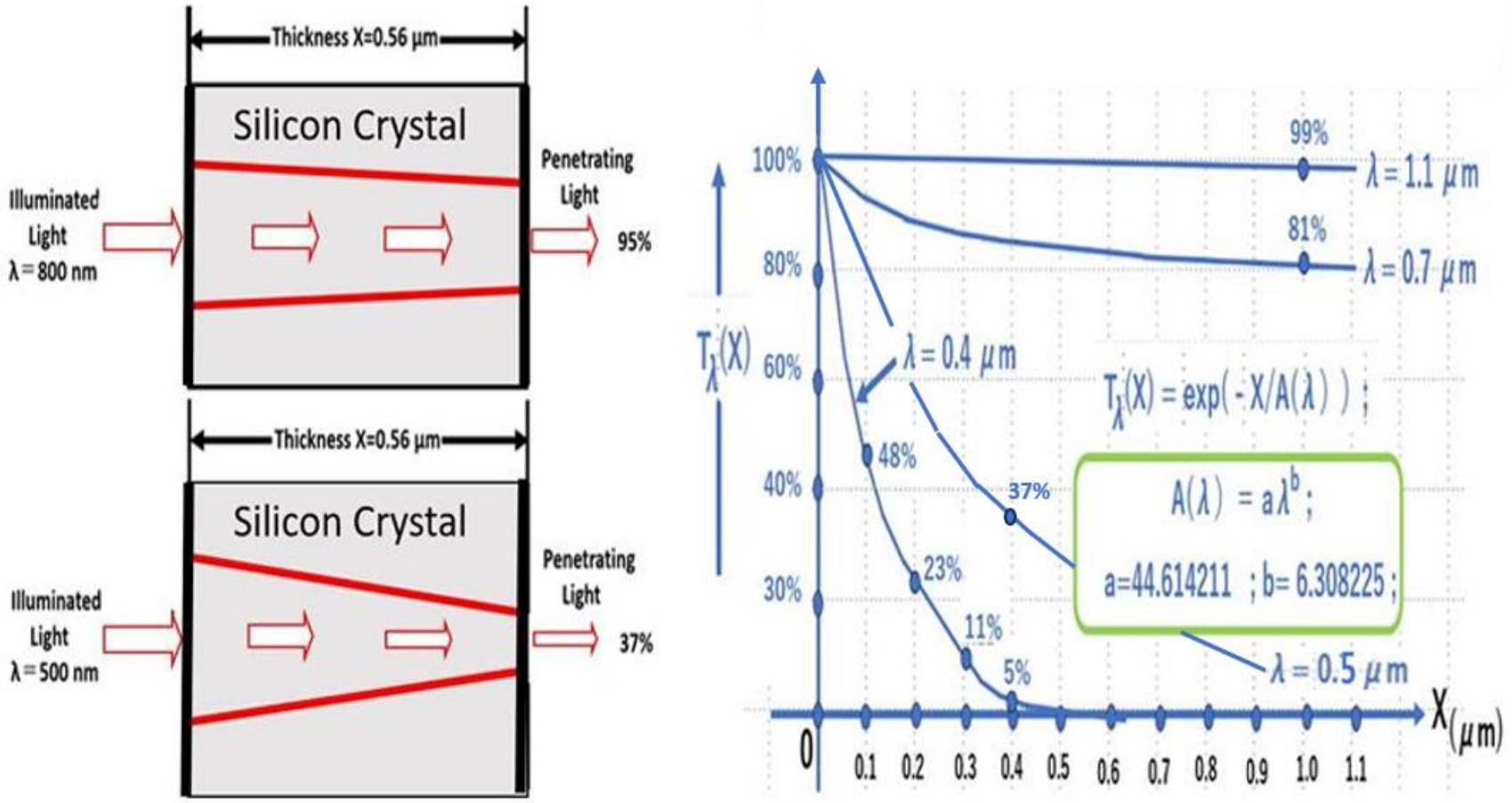


Fig. 3.Percentage (%) of the number of photons $T_\lambda(X) = \exp(-X/A(\lambda))$ penetrating into silicon crystal at the depth X (μ m). The short-wave high-energy blue light is completely absorbed within the 0.3 μ m in depth.↵

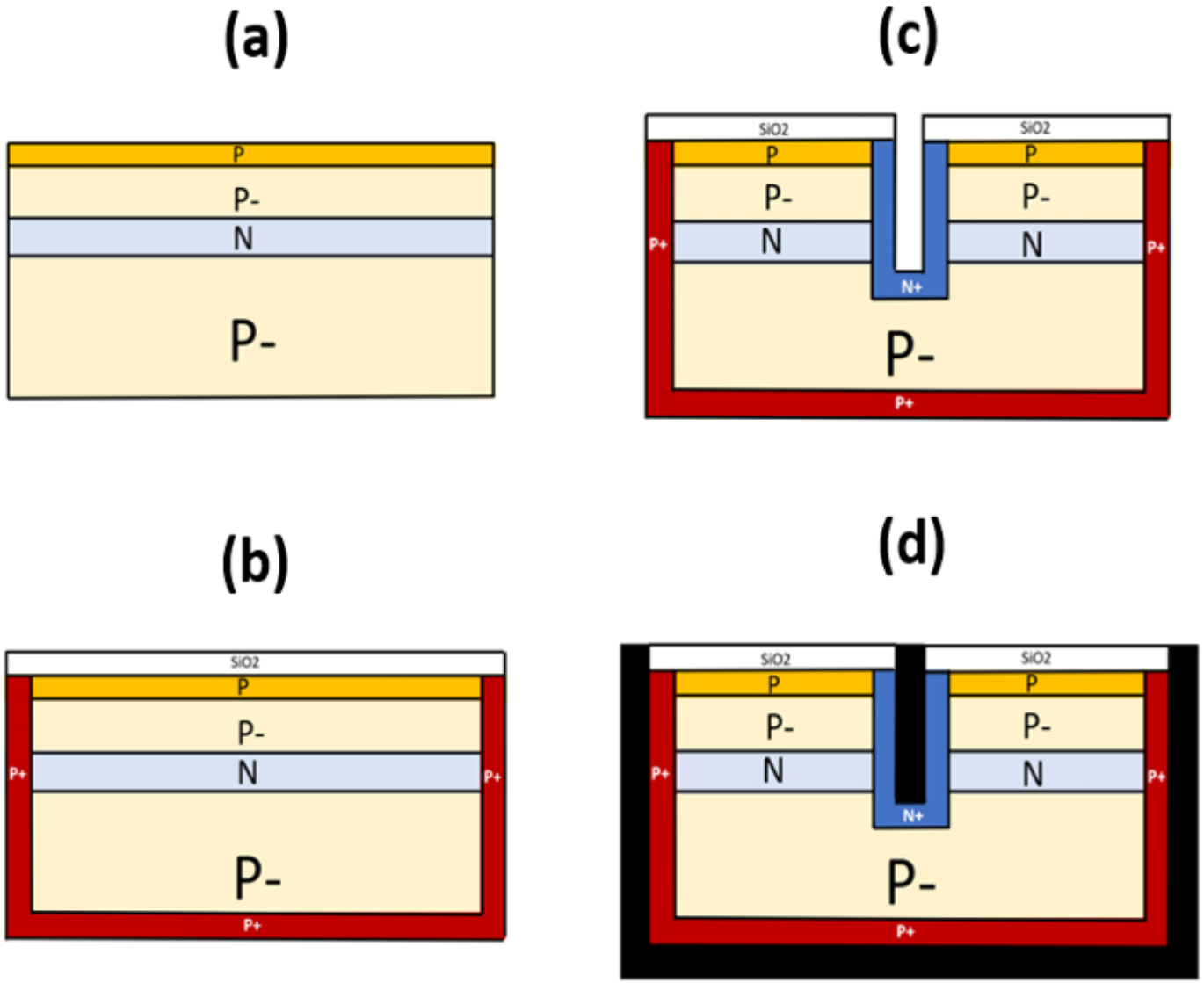
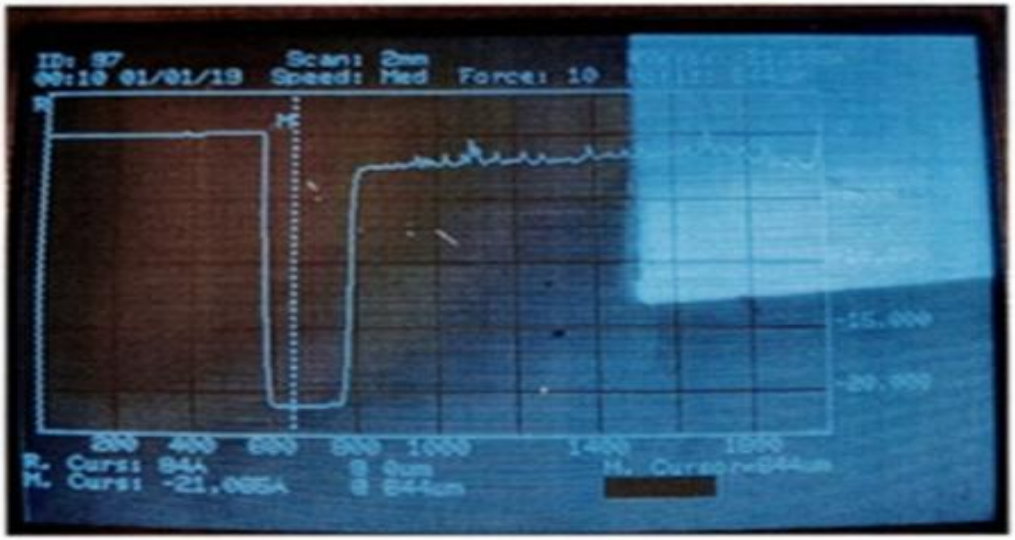
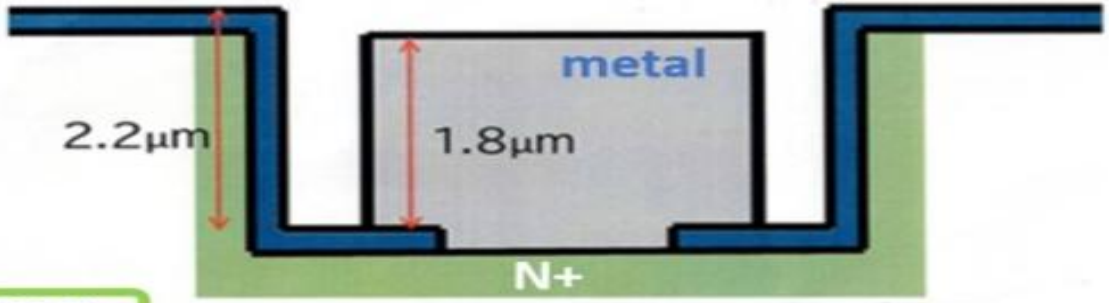


Fig.6 One-Mask Process Flow of PP-NP-P+ Double Junction Solar Cell

(1) Single Junction
Sample Photo



(2) Double Junction
Sample Photo



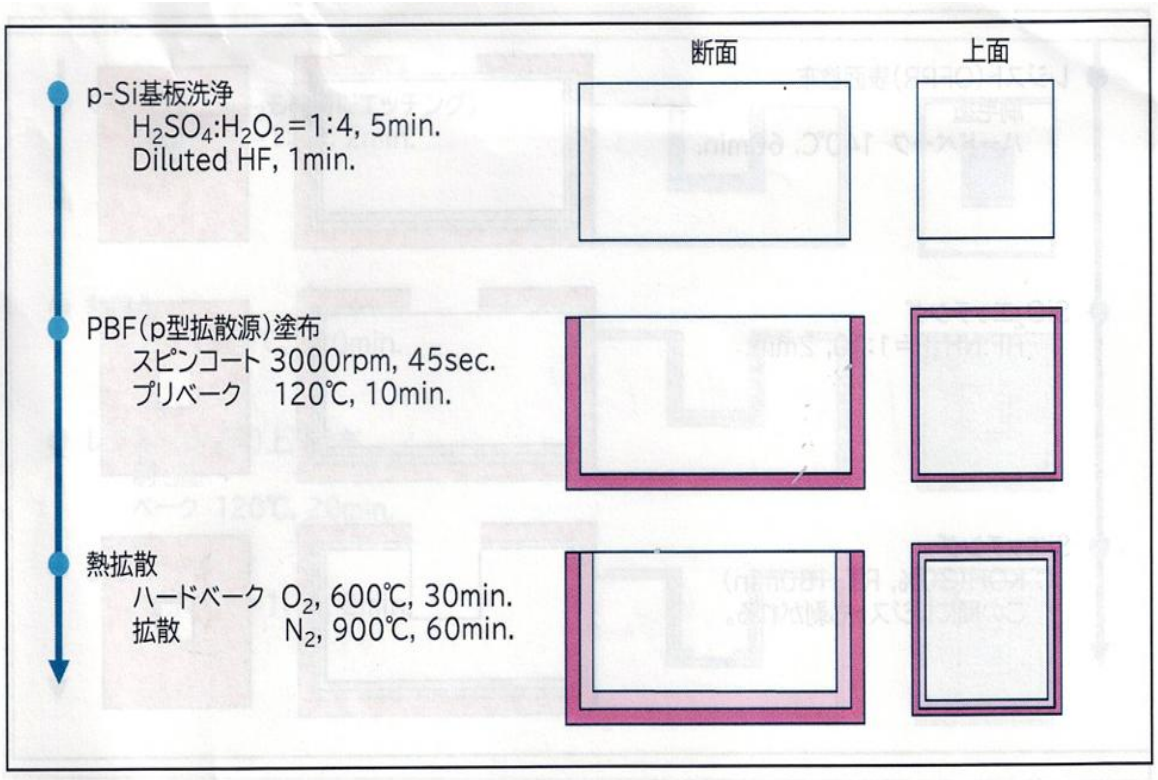
I_{SC2} / I_{SC1} = 12.4 / 8.4 = 148 %

	I_0 [A]	n	Rs [Ω]	Rp [Ω]	V_{OC} [V]	Photo Current I_{SC} [mA]	η [%]	Chip Size S=3 cm x 3 cm S [cm^2]
(1) Single	2.4×10^{-10}	1.04	2.00	14.4M	0.46	8.4	0.29	9
(2) Double			2.37	15.2k	0.46	12.4	0.32	9

Fig.11 Measurement data of the first silicon chip of the PP-NP-P+ double junction photodiode type solar cell

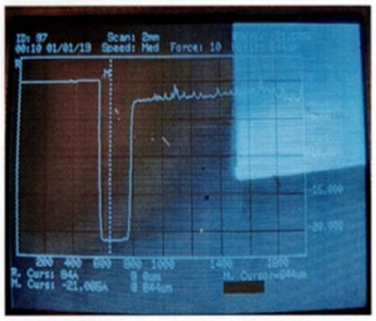
高価な描画装置不要

手書きでレジストを塗る！

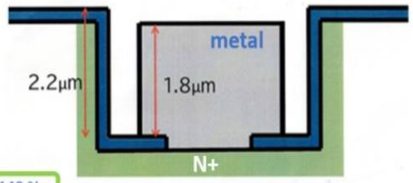


A1

(1) Single Junction Sample Photo



(2) Double Junction Sample Photo



I_{SC2} / I_{SC1} = 12.4 / 8.4 = 148 %

	I_0 [A]	n	Rs [Ω]	Rp [Ω]	V_{OC} [V]	Photo Current I_{SC} [mA]	η [%]	Chip Size S=3 cm x 3 cm S [cm^2]
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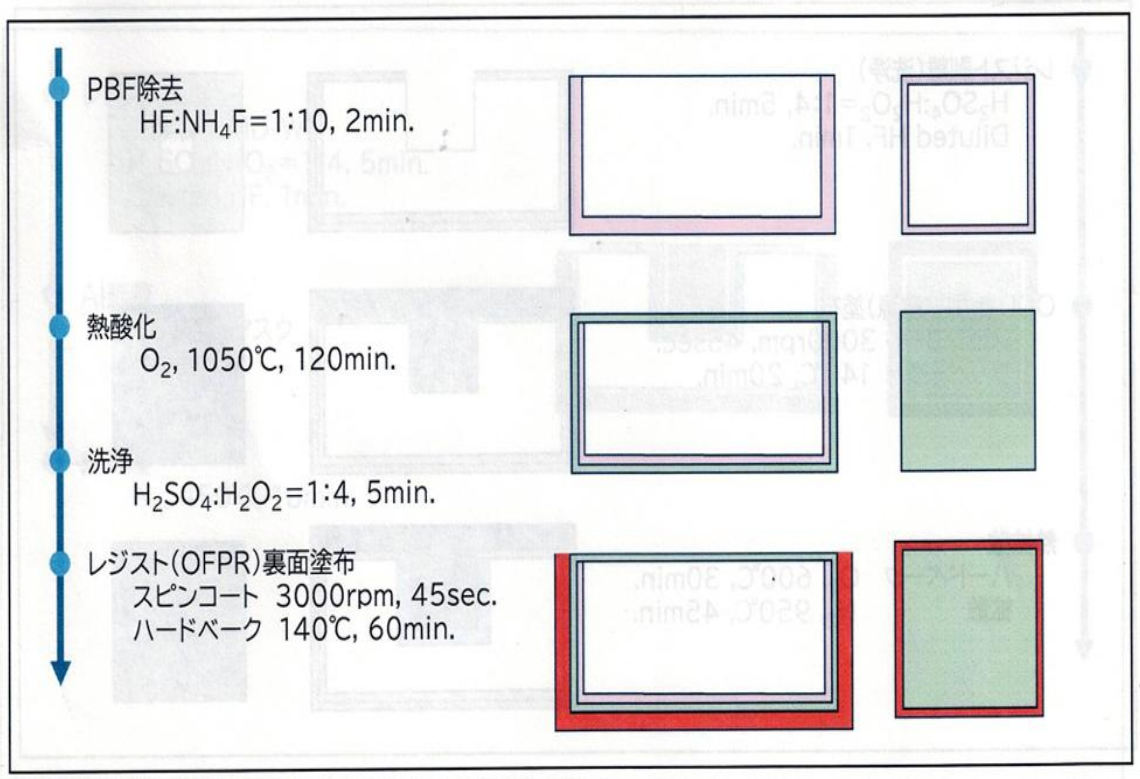
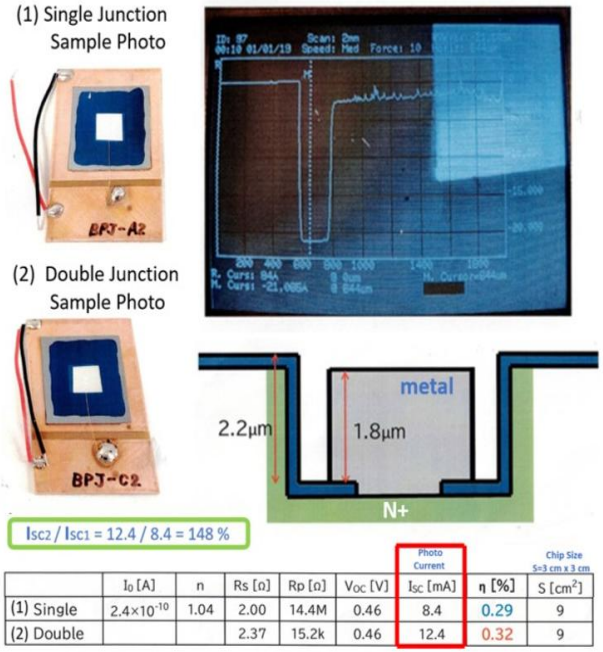
Fig.11 Measurement data of the first silicon chip of the PP-NP-P+ double junction photodiode type solar cell

高価な描画装置不要

手書きでレジストを塗る！



A2

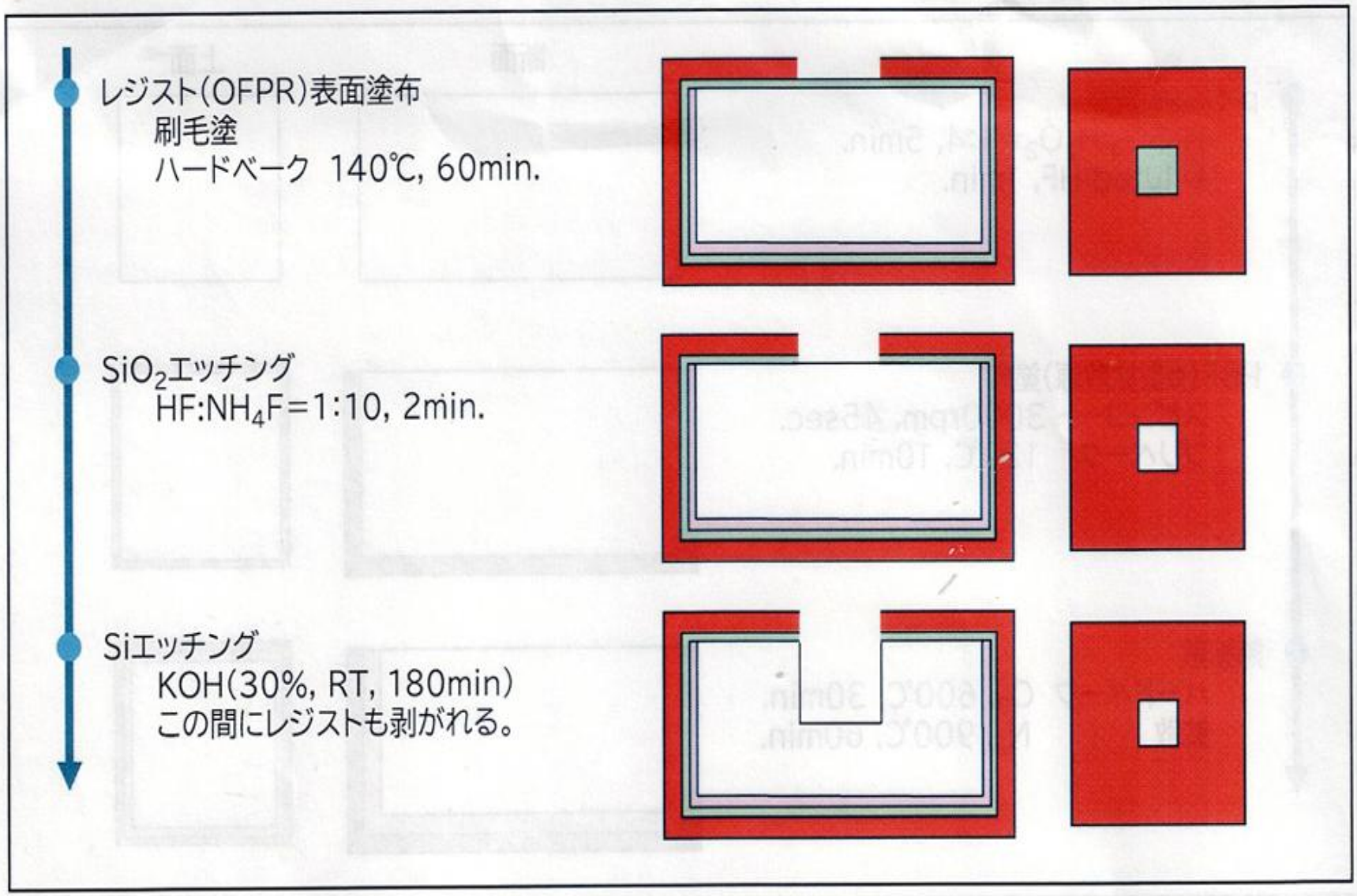


	I_0 [A]	n	Rs [Ω]	Rp [Ω]	V_{OC} [V]	I_{SC} [mA]	η [%]	S [cm^2]
						Photo Current		Chip Size 5=3 cm x 3 cm
(1) Single	2.4×10^{-10}	1.04	2.00	14.4M	0.46	8.4	0.29	9
(2) Double			2.37	15.2k	0.46	12.4	0.32	9

Fig.11 Measurement data of the first silicon chip of the PP-NP-P+ double junction photodiode type solar cell

高価な描画装置不要

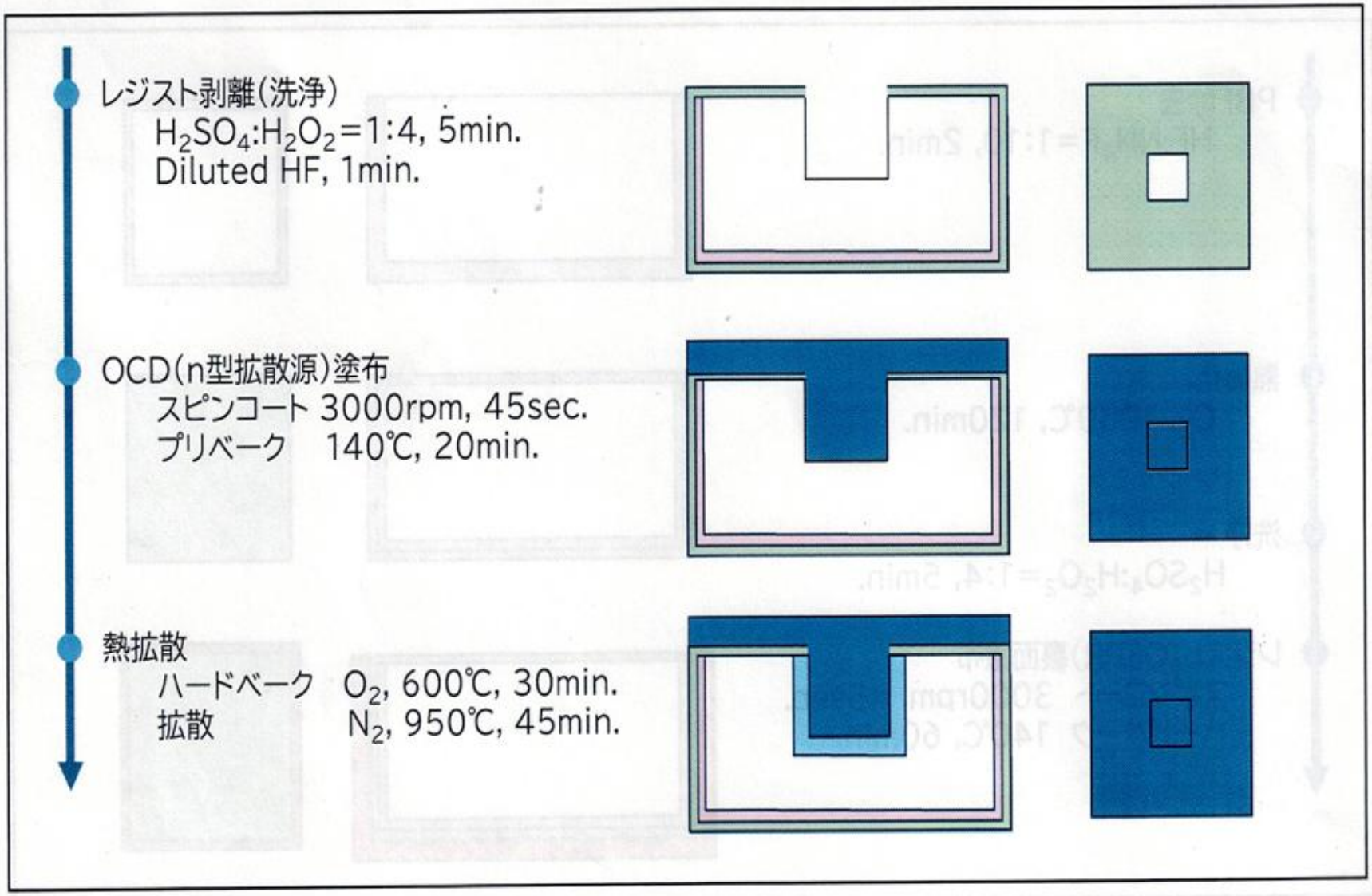
手書きでレジストを塗る！



A3

高価な描画装置不要

手書きでレジストを塗る！



A4

高価な描画装置不要

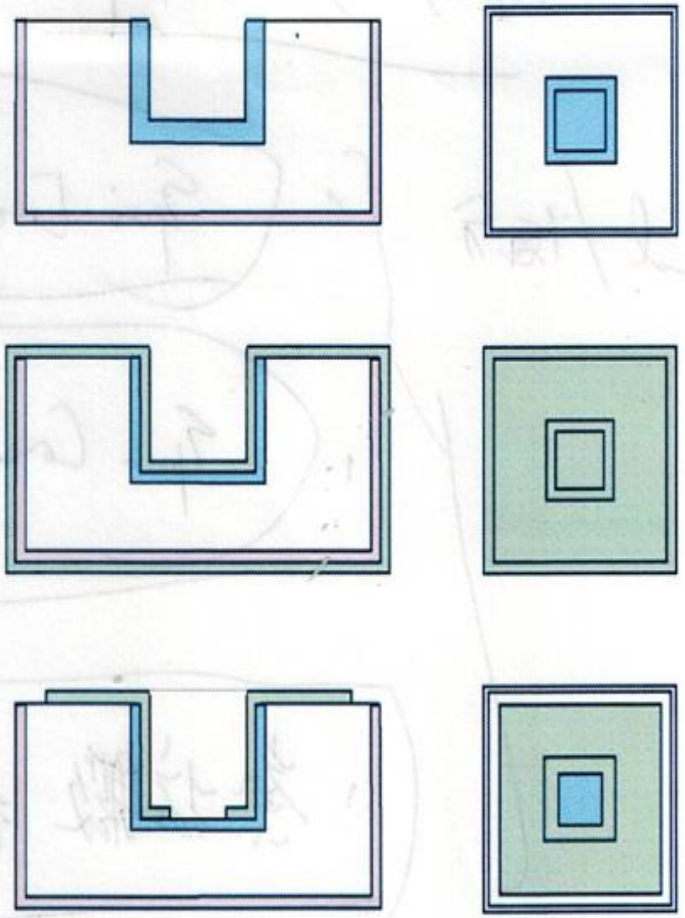
手書きでレジストを塗る！

OCD除去(SiO_2も同時にエッチング)
$HF:NH_4F=1:10$, 2min.

熱酸化
O_2, 1050℃, 120min.

レジスト(OFPR)上面塗布
刷毛塗
ベーク 120℃, 20min.

SiO2エッチング
$HF:NH_4F=1:10$, 2min.



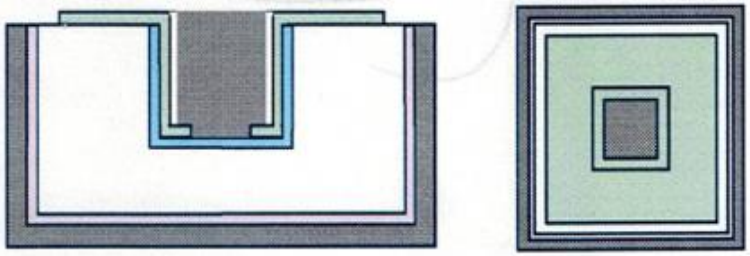
高価な描画装置不要

手書きでレジストを塗る！

レジスト剥離
現像液(NMD-W)
H_2SO_4:H_2O_2=1:4, 5min.
Diluted HF, 1min.

Al蒸着
表 ガラスマスク
裏 全面

熱処理
N_2, 450℃, 10min.



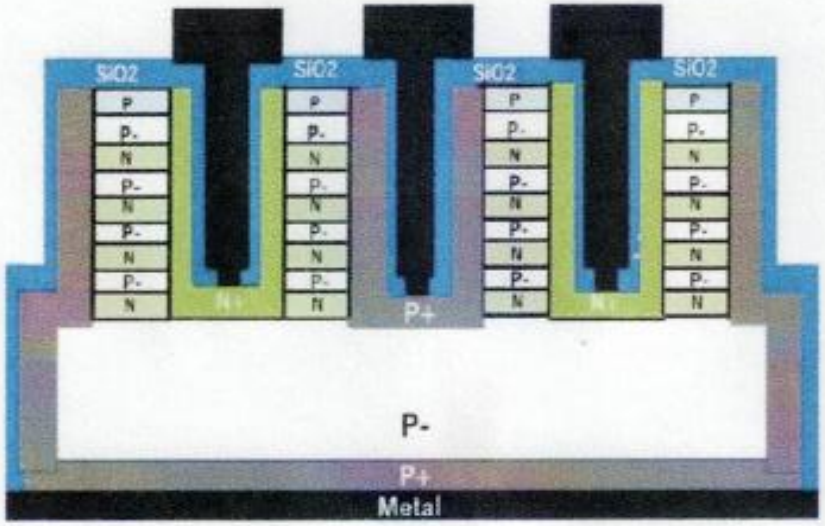


図１シリコン結晶型多重接合太陽電池の新構造

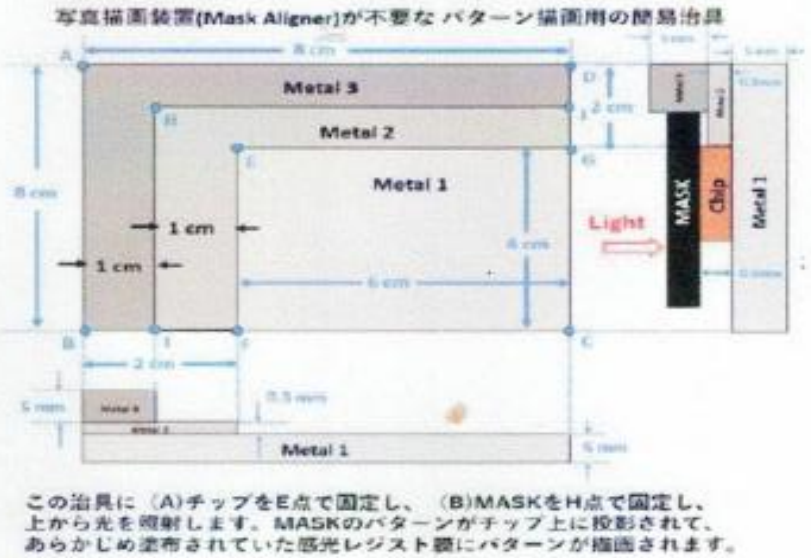
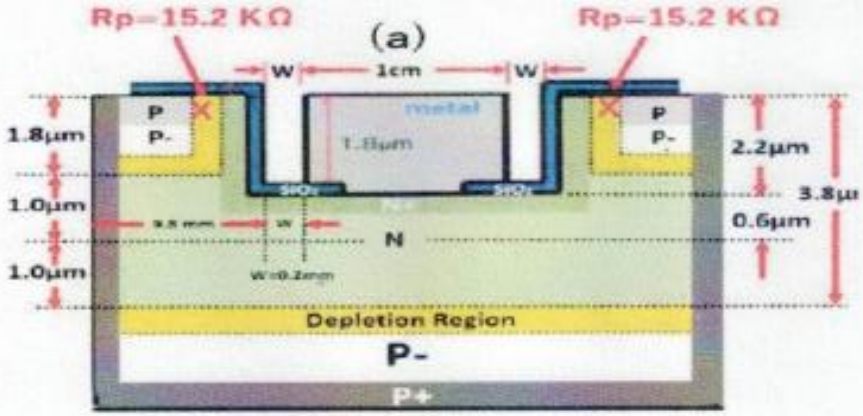
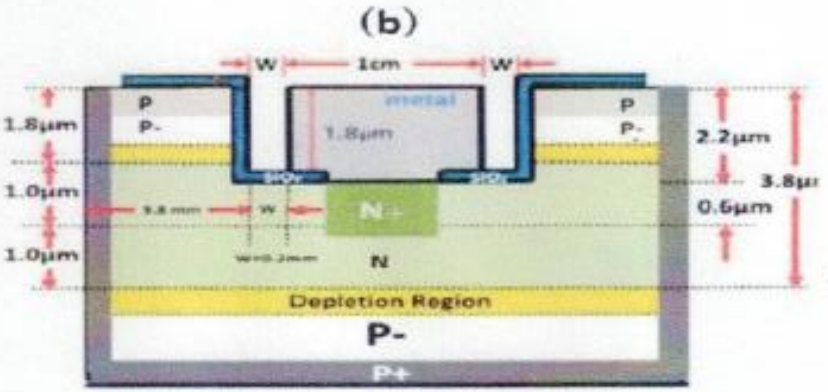


図２簡易生産用の治工具構造





	I_0 [A]	n	Rs [Ω]	Rp [Ω]	V_{oc} [V]	I_{sc} [mA]	η [%]	S [cm²]
(1) Single	2.4×10^{-10}	1.04	2.00	14.4M	0.46	8.4	0.29	9
(2) Double			2.37	15.2k	0.46	12.4	0.32	9

$I_{sc2}/I_{sc1} = 12.4/8.4 = 148\,\%$

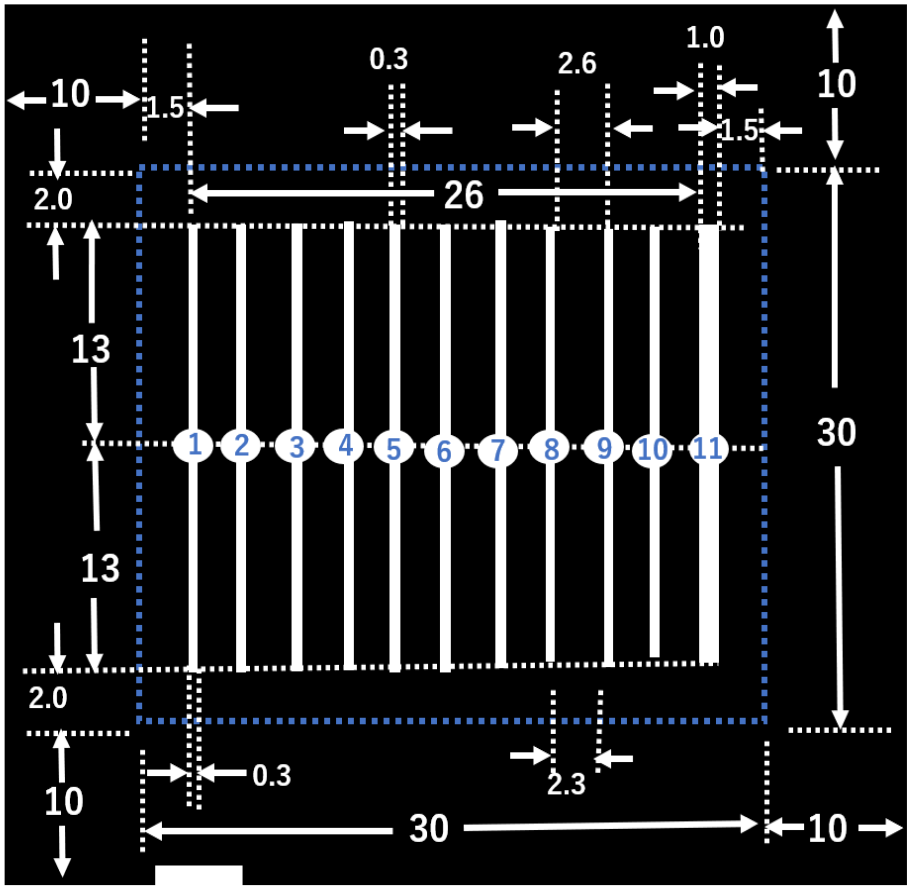
図３　(a) 第１回原理試作した構造とその特性 DATA (b)Rp 値の低減を避けた改善構造案

高価な描画装置不要

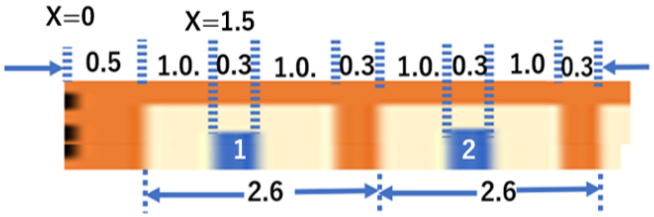
MASK１A　長さ 26mm 幅 0.3mm の10本の線と、さらに
右の端に長さ 26mm 幅 1.0mm の線をもう１本形成します。

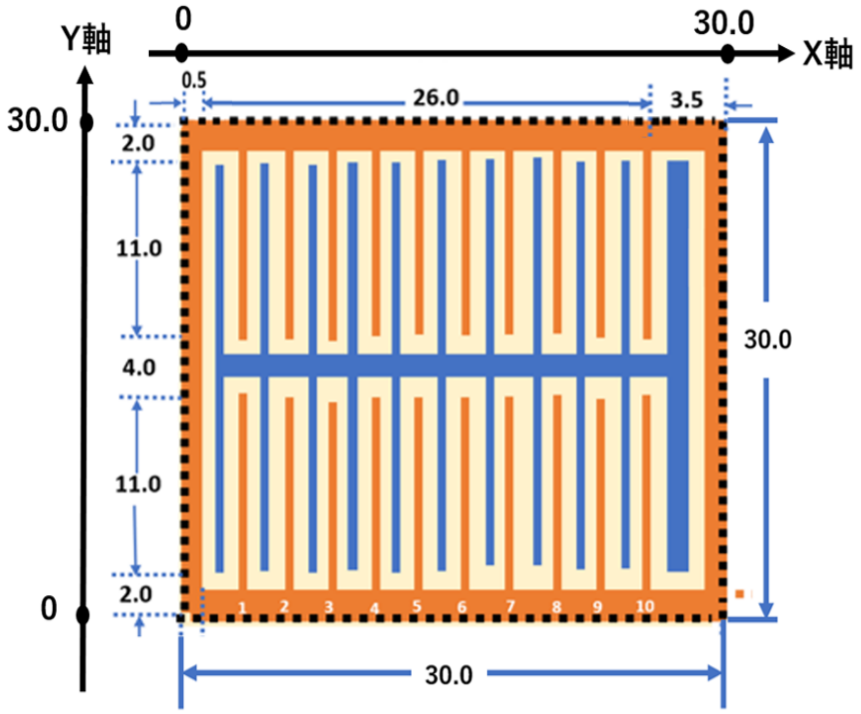
MASK Size 50 mm x 50 mm

Mask1A for N+ Line



●N+線 （青色の細い線）の幅は 0.3 mmです。
左端（X＝０）から、１本目は X=1.5 に位置します。
2.3 mm 間隔で合計１０本のN+線があります。
１１本目の幅は　1.0 mm です。





A-3

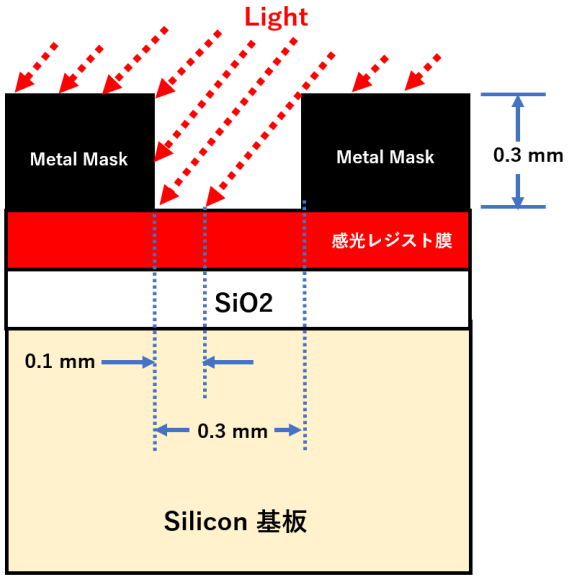
高価な描画装置不要

P+PNPP+ Double Junction Photodiode
for AIPS Robot Vision and Solar Cell Applications

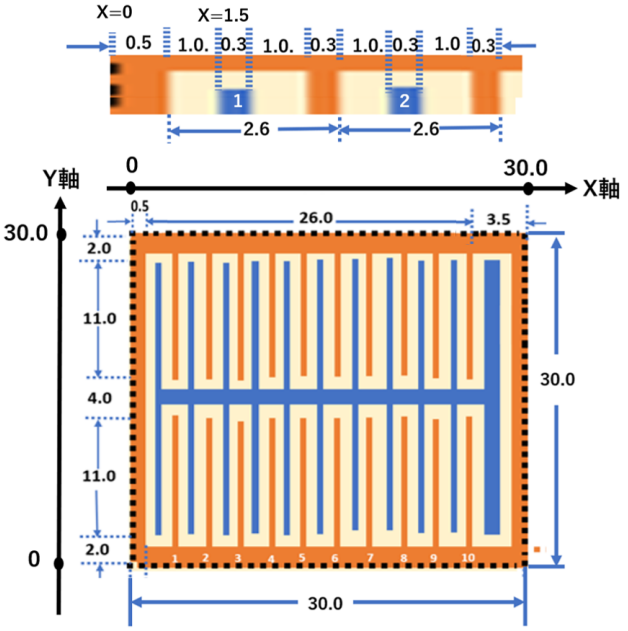
Yoshiaki Daimon Hagiwara (FIEEE)

Appendix : Simple Mask Aligner Tool and Preparation of Photo Masks

今回の試作MASKの最小線幅は　0.3 mm ですが、
感光レジストの光源の照射角度を調整する事により、
より細い、0.1 mm の線幅も加工が可能となります。

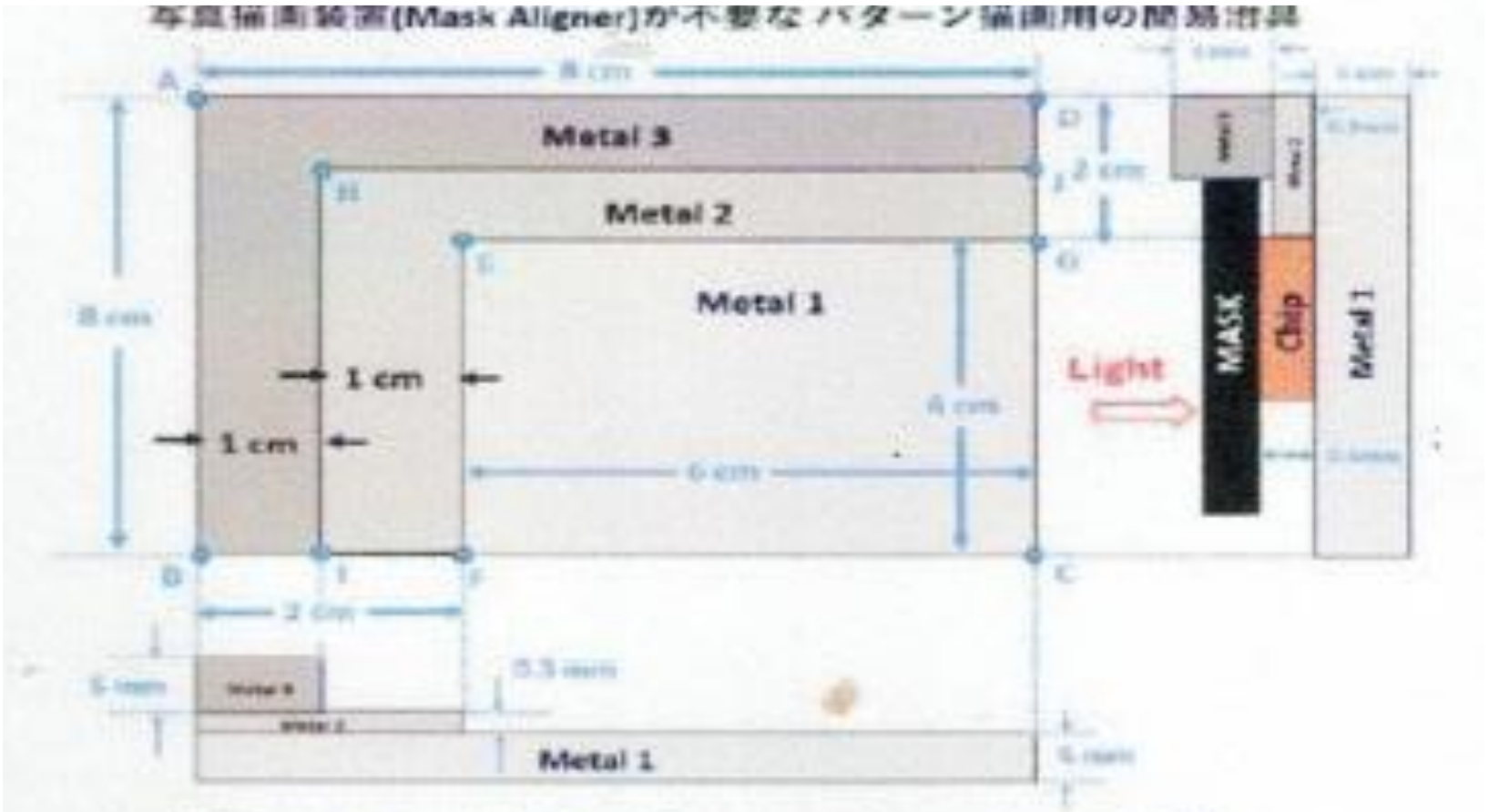


●P+線 （茶色の細い線）の幅は 0.3 mmです。
左端（X=０）から、１本目は X=3.5 に位置します。
2.6 mm 間隔で合計１０本のN+線があります。
１１本目の幅は　1.0 mm です。



高価な描画装置不要

パターン描画を目的とする、簡単なコンタクト型の CHIP と MASK 合わせ用の治工具構造を提案する。

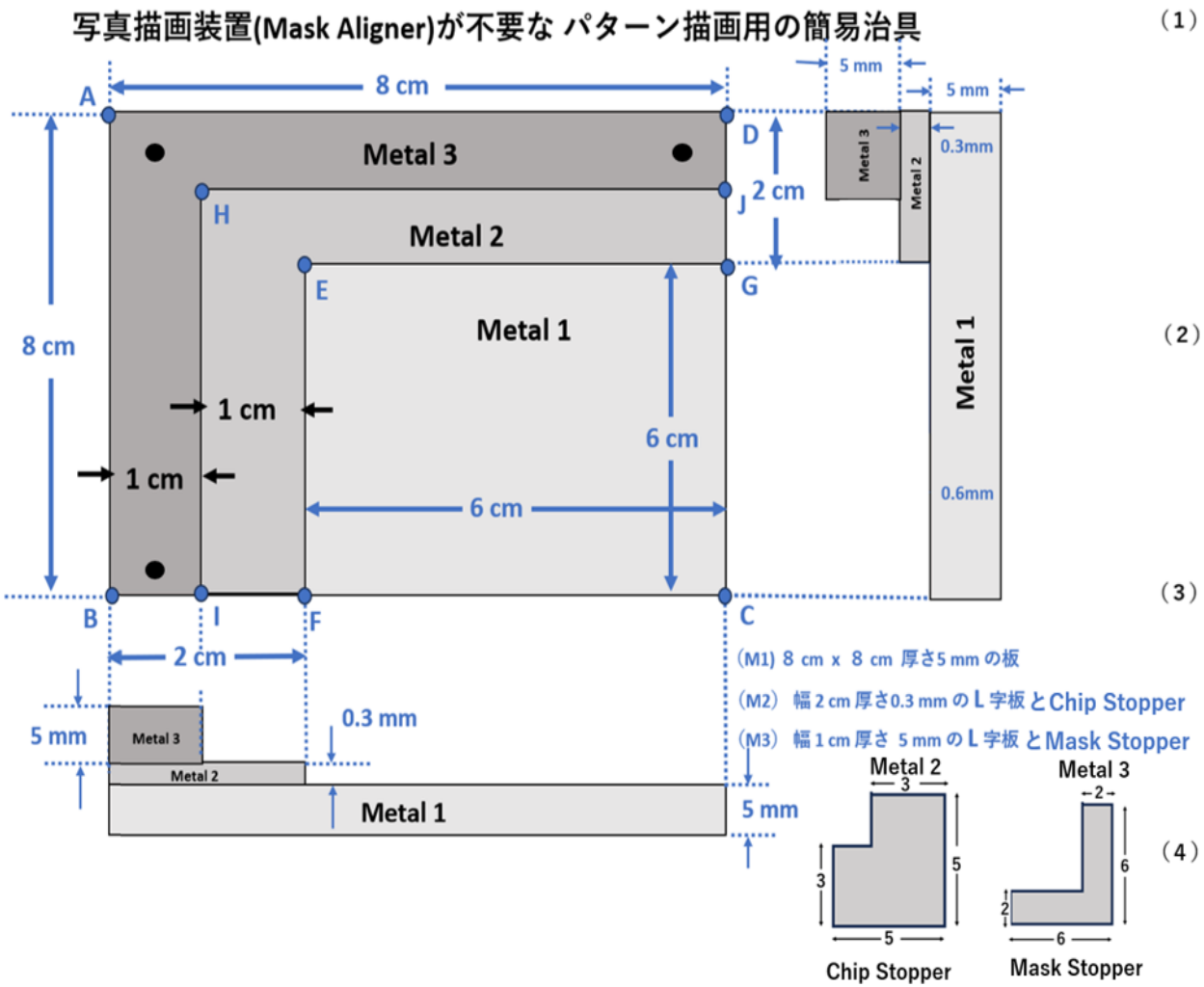


この治具に（A)チップをE点で固定し、（B)MASKをH点で固定し、
上から光を照射します。MASKのパターンがチップ上に投影されて、
あらかじめ塗布されていた感光レジスト膜にパターンが描画されます。

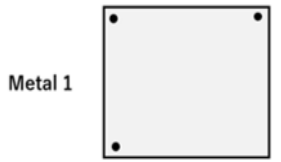
図２簡易生産用の治工具構造

高価な描画装置不要

Simple Mask Aligner Tool and Preparation of Photo Masks

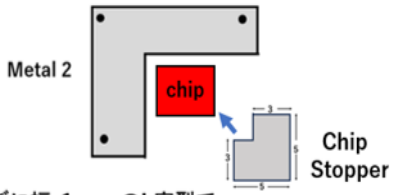


（1）まず 8 cm x 8 cmの大きさで
厚さ 5 mm の金属板を用意します。

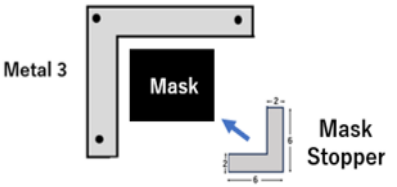


ボルトで固定する穴（•）を開けます。

（2）つぎに幅 2 cm のL字型で
厚さ 0.3 mm の金属板を用意します。



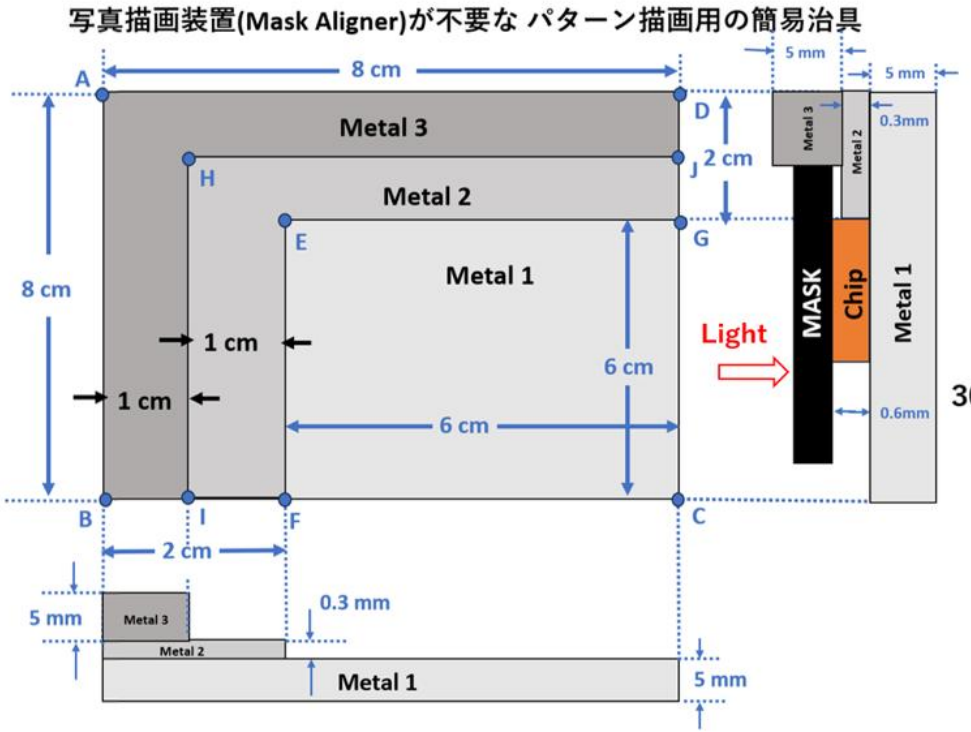
（3）つぎに幅 1 cm のL字型で
厚さ 5 mm の金属板を用意します。



（4）最後にこの 3 枚の金属板を
重ねてボルトで密着固定します。

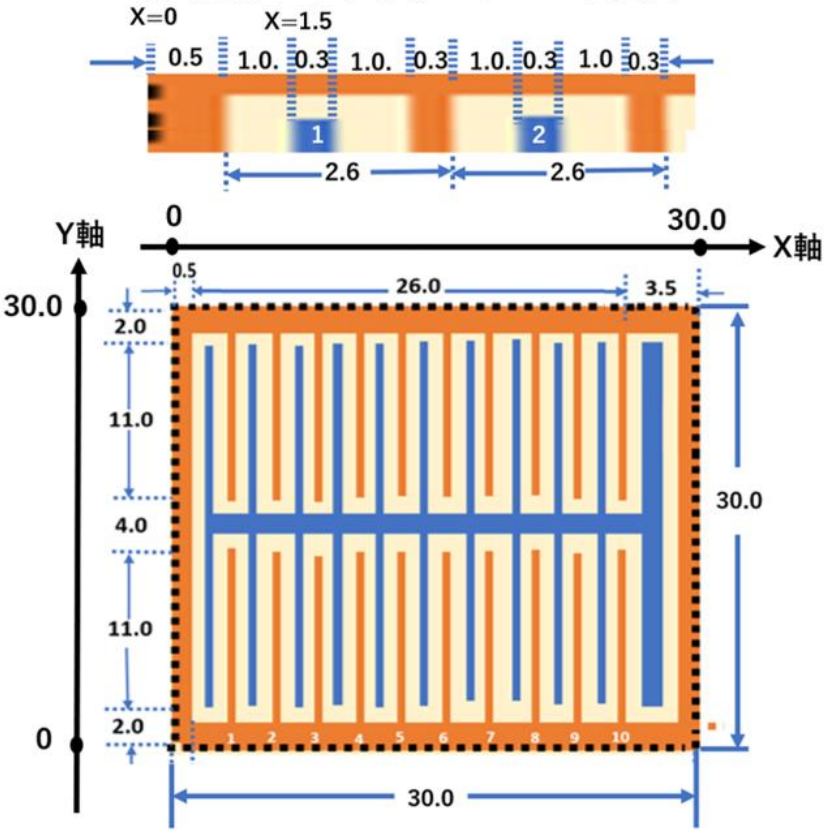
高価な描画装置不要

Simple Mask Aligner Tool and Preparation of Photo Masks



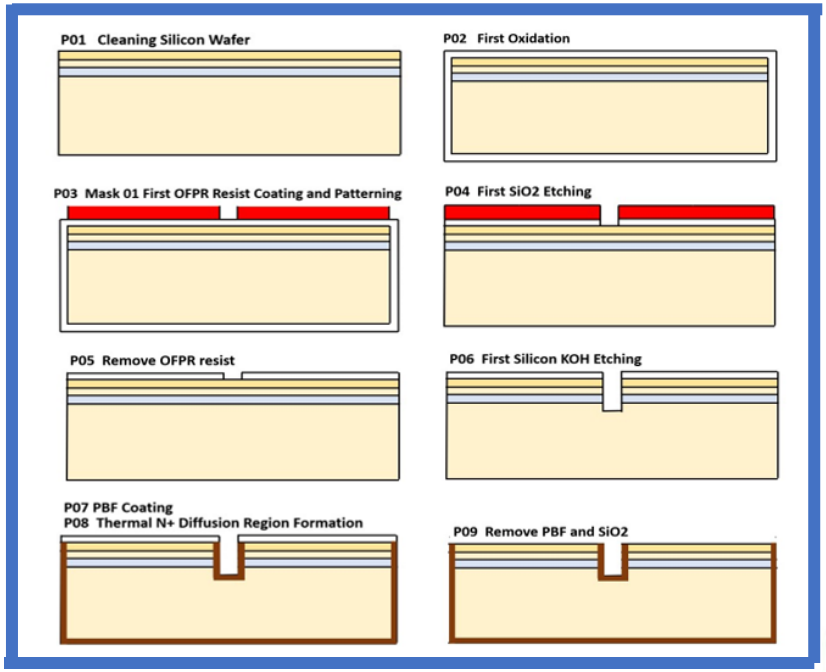
この治具に（A)チップをE点で固定し、（B)MASKをH点で固定し、
上から光を照射します。MASKのパターンがチップ上に投影されて、
あらかじめ塗布されていた感光レジスト膜にパターンが描画されます。

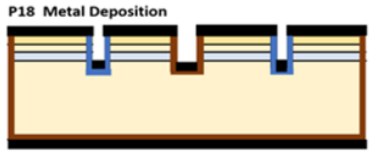
今回試作する半導体チップは厚さは 0.7 mm
3 cm x 3 cm の大きさです。

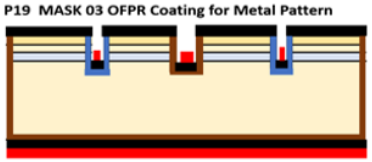


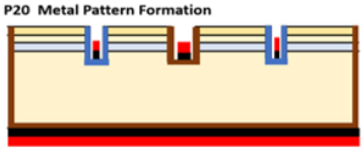
(1) MASK01 Process to form P+ Region

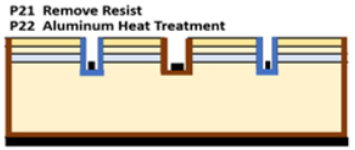
KOH Silicon Etching and P+/N+ Channel Stops are used instead of LOCOS Isolation

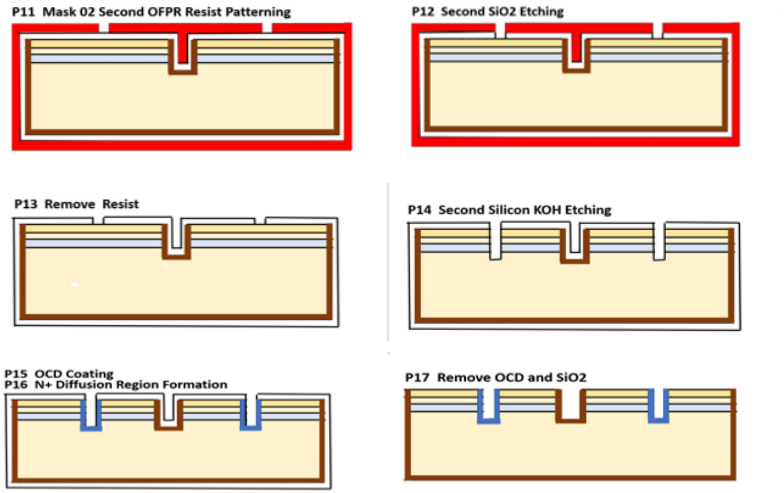


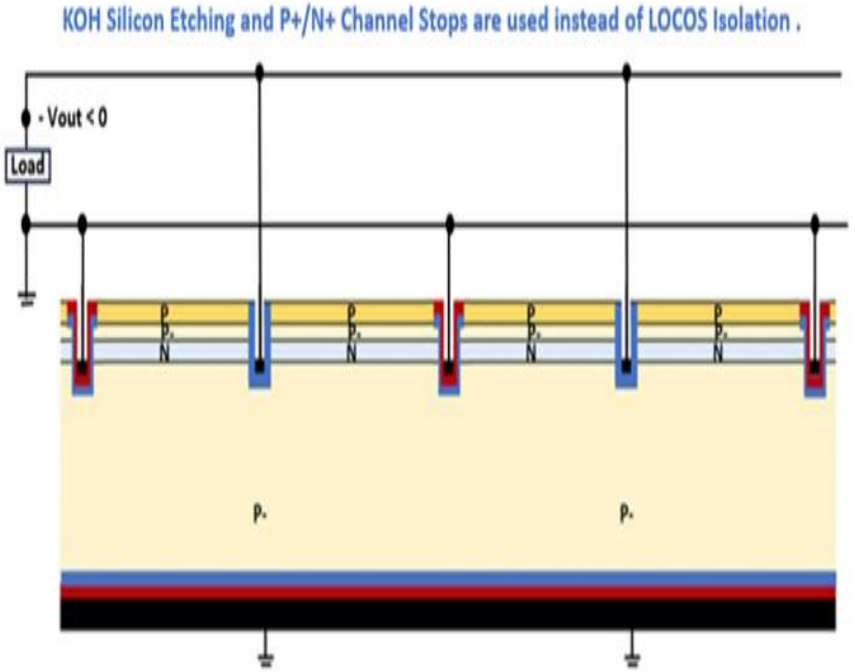










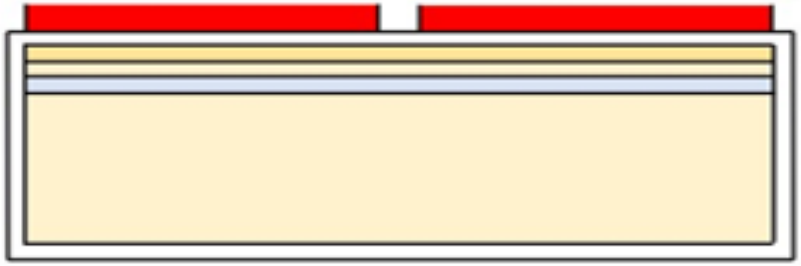


(1) MASK01 Process to form P+ Region

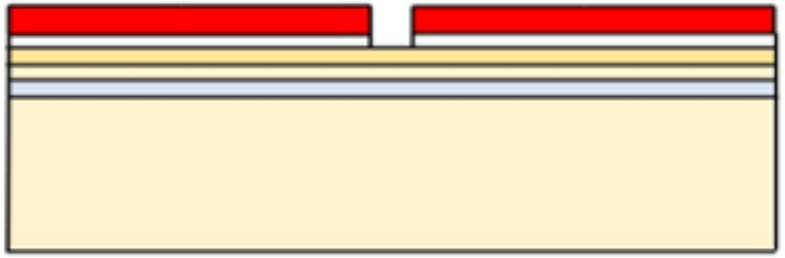
P01 Cleaning Silicon Wafer

P02 First Oxidation

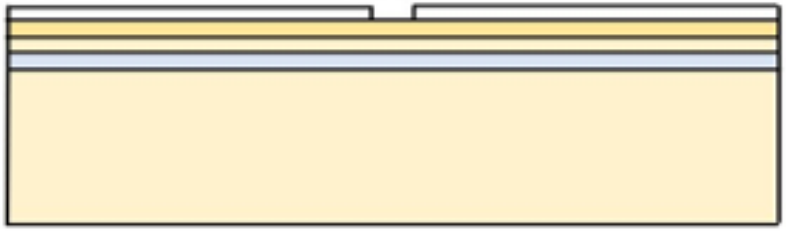
P03 Mask 01 First OFPR Resist Coating and Patterning



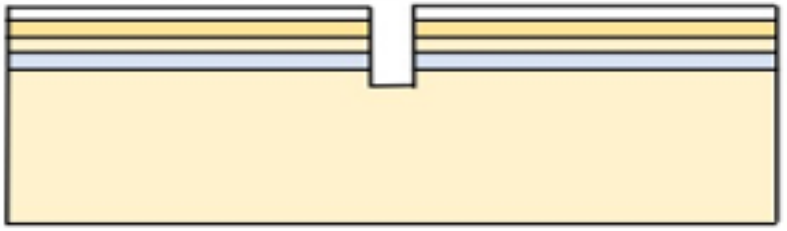
P04 First SiO2 Etching



P05 Remove OFPR resist

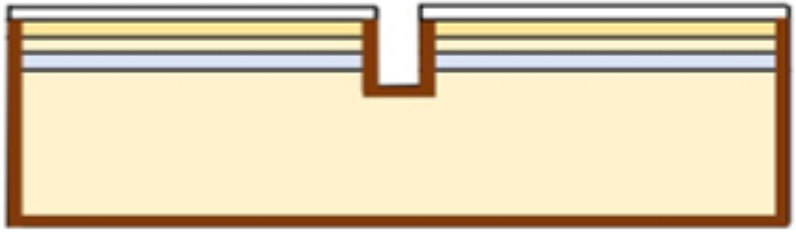


P06 First Silicon KOH Etching

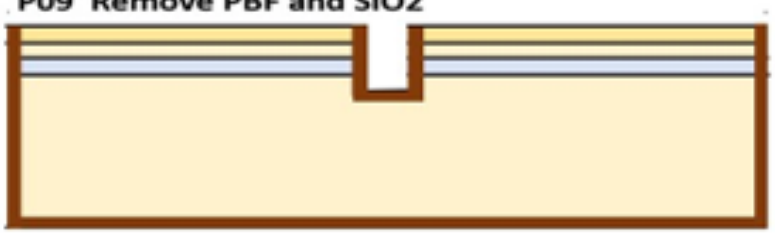


P07 PBF Coating

P08 Thermal N+ Diffusion Region Formation

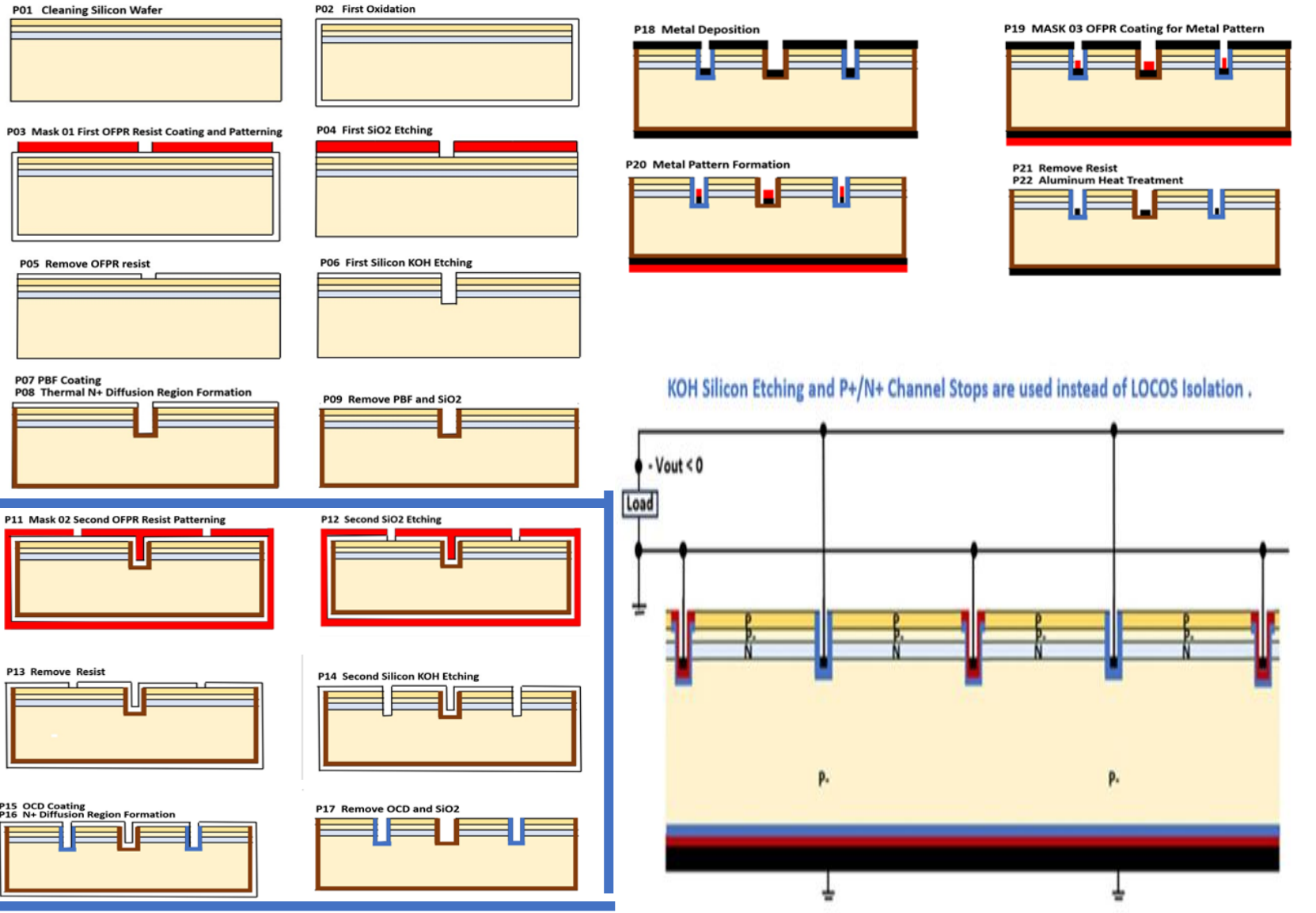


P09 Remove PBF and SiO2



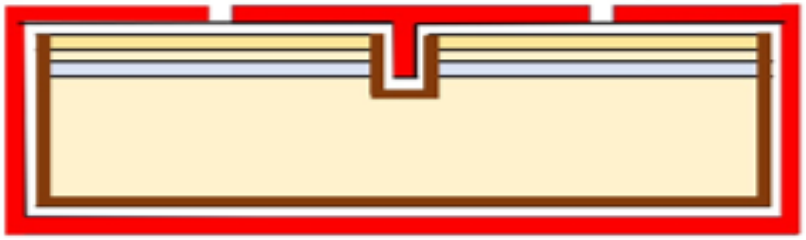
(2) Process to form N+ Region

KOH Silicon Etching and P+/N+ Channel Stops are used instead of LOCOS Isolation

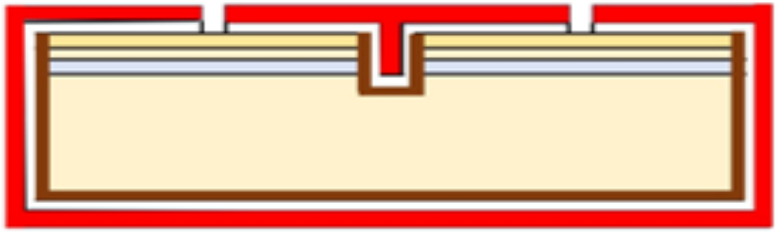


(2) Process to form N+ Region

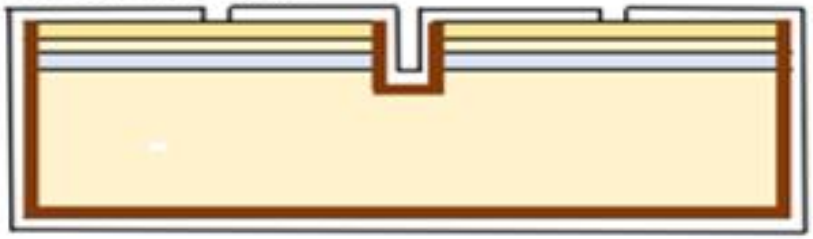
P11 Mask 02 Second OFPR Resist Patterning



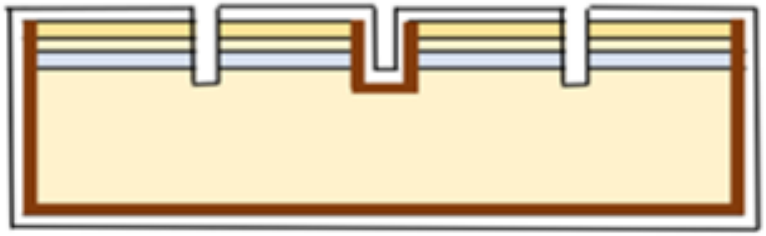
P12 Second SiO2 Etching



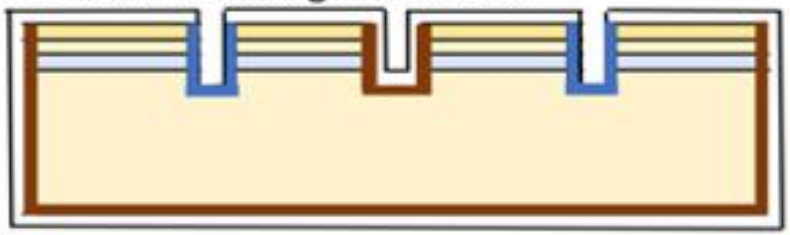
P13 Remove Resist



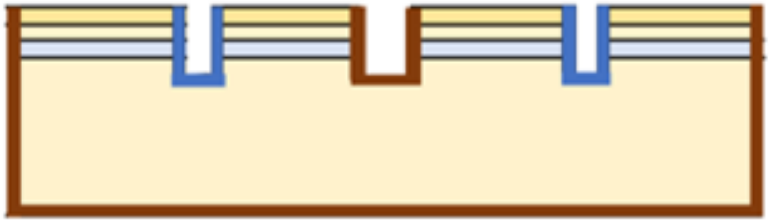
P14 Second Silicon KOH Etching



P15 OCD Coating
P16 N+ Diffusion Region Formation

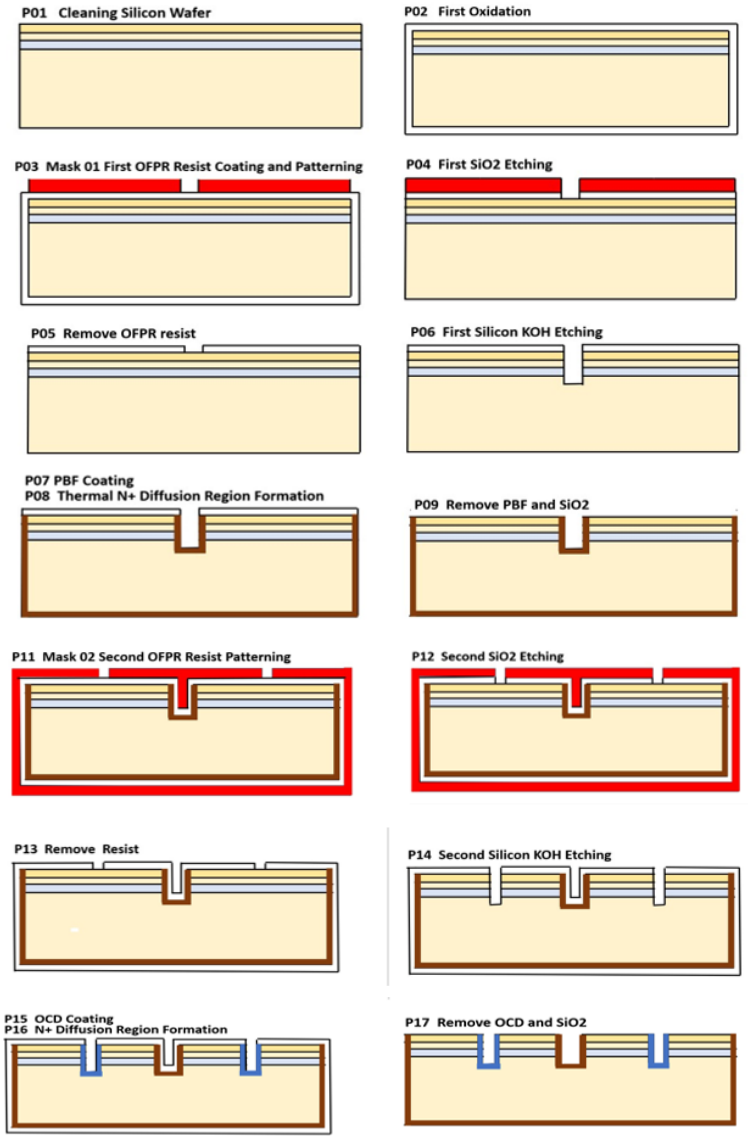


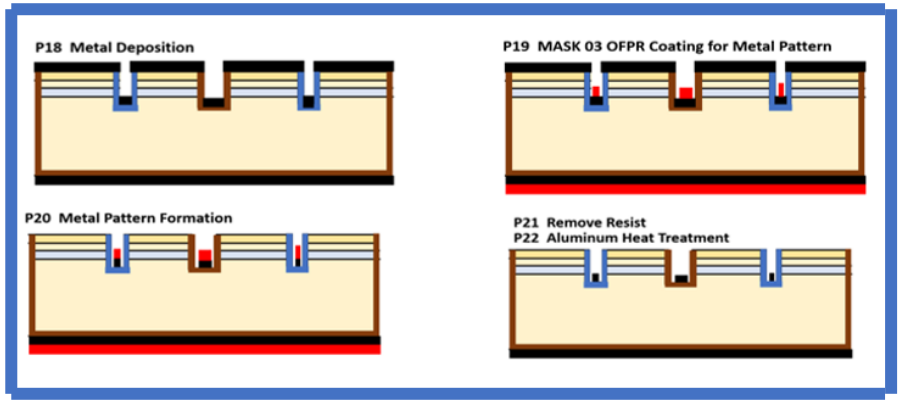
P17 Remove OCD and SiO2

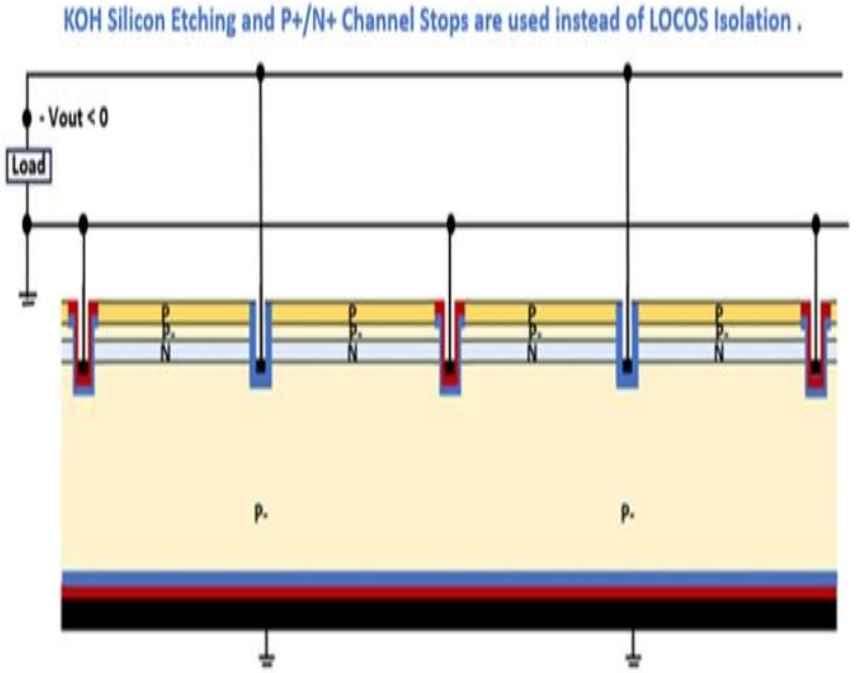


(3) Process to form Contact and Metal Wire Patterns with 3 masks

KOH Silicon Etching and P+/N+ Channel Stops are used instead of LOCOS Isolation

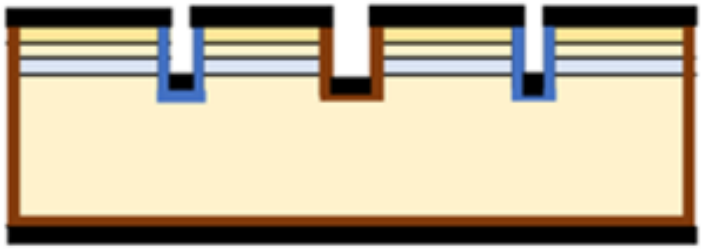




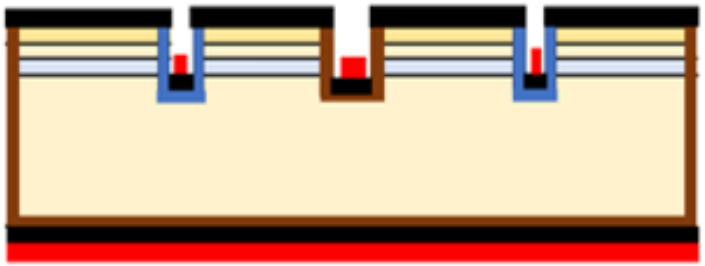


(3) Process to form Contact and Metal Wire Patterns

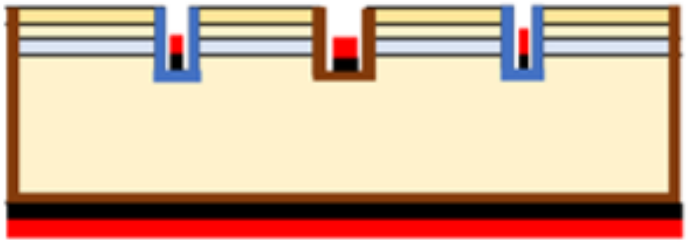
P18 Metal Deposition



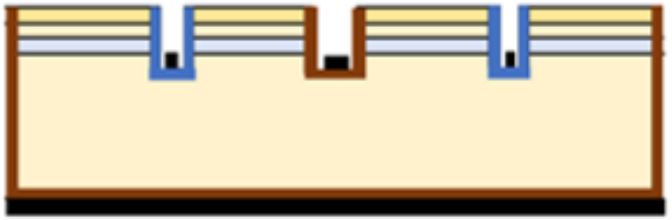
P19 MASK 03 OFPR Coating for Metal Pattern



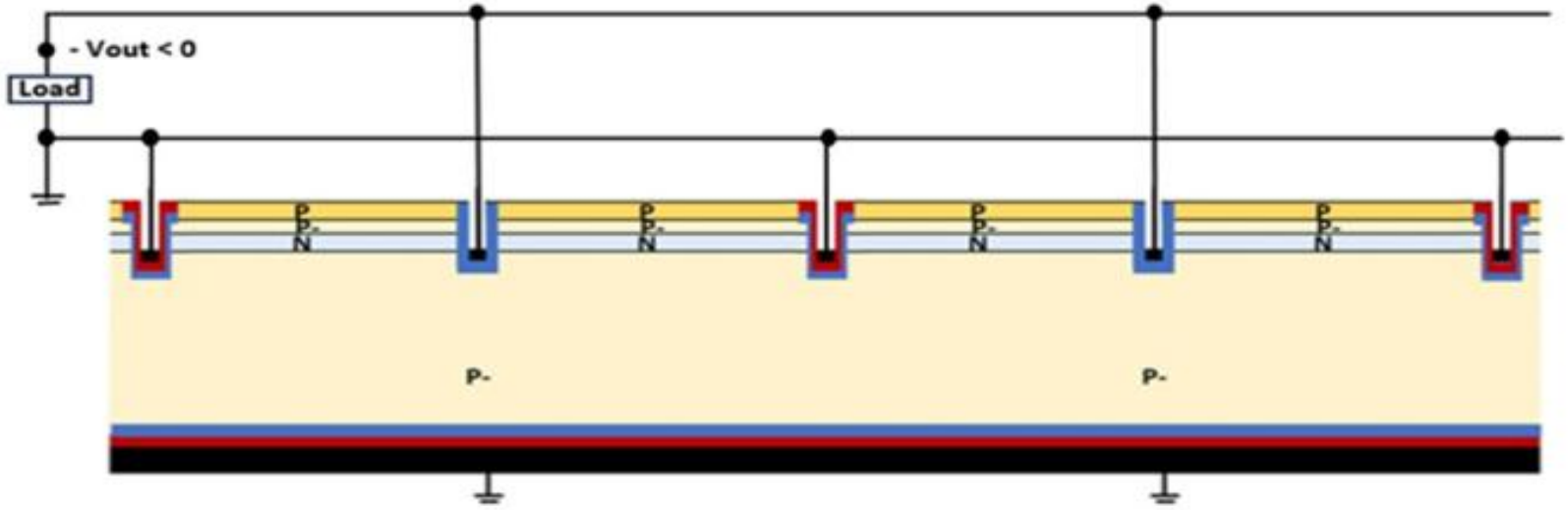
P20 Metal Pattern Formation



P21 Remove Resist
P22 Aluminum Heat Treatment

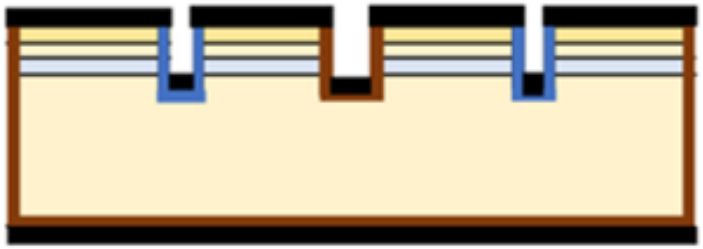


KOH Silicon Etching and P+/N+ Channel Stops are used instead of LOCOS Isolation .

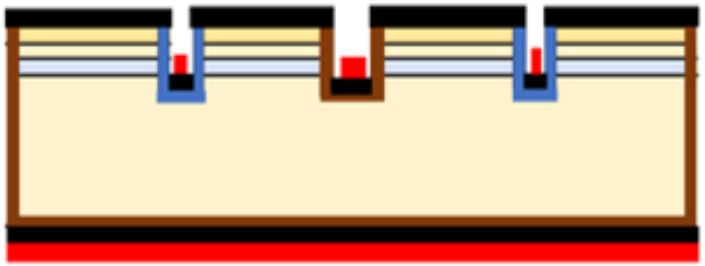


(3) Process to form Contact and Metal Wire Patterns with 3 masks

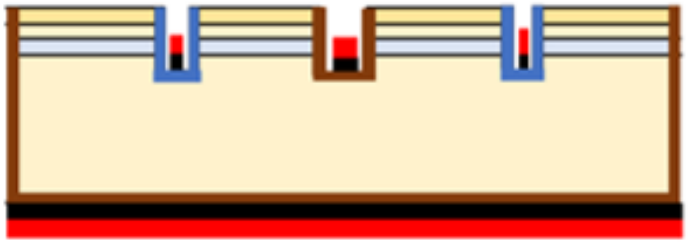
P18 Metal Deposition



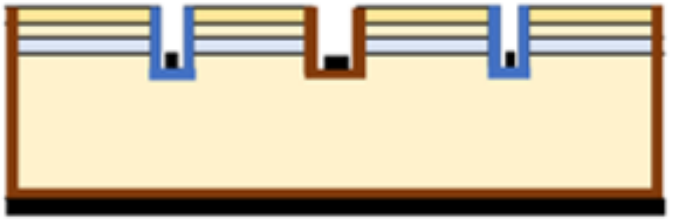
P19 MASK 03 OFPR Coating for Metal Pattern



P20 Metal Pattern Formation

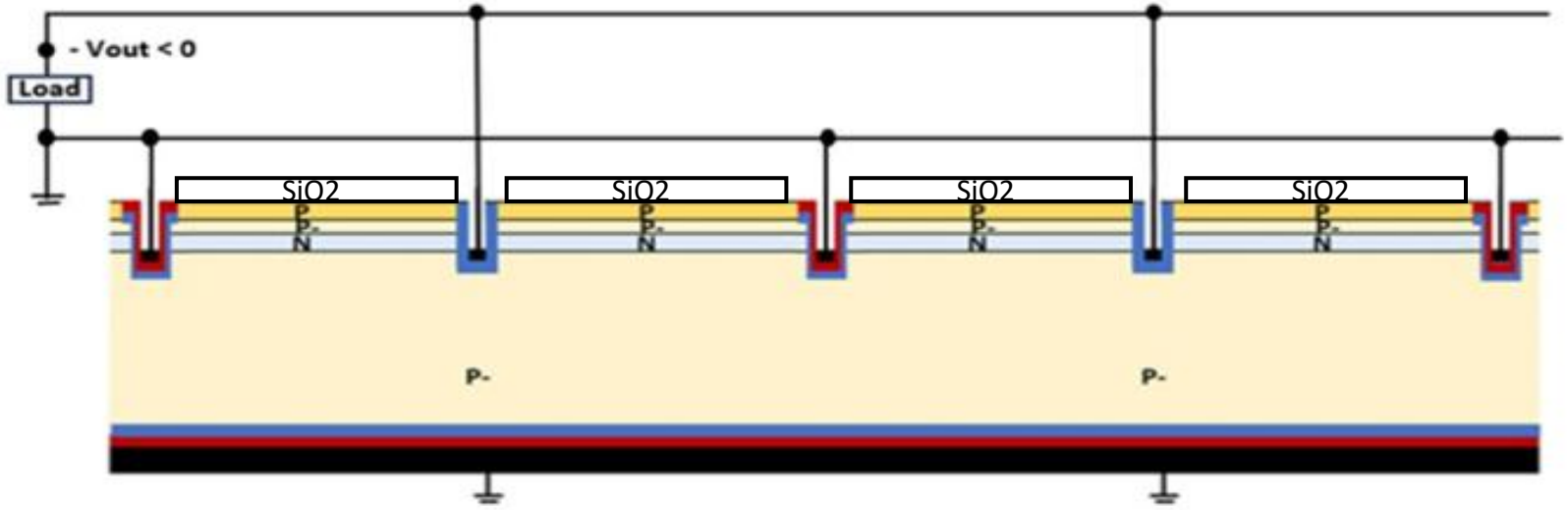


P21 Remove Resist
P22 Aluminum Heat Treatment



(4) Process to form Contact and Metal Wire Patterns with 4 masks.

KOH Silicon Etching and P+/N+ Channel Stops are used instead of LOCOS Isolation .



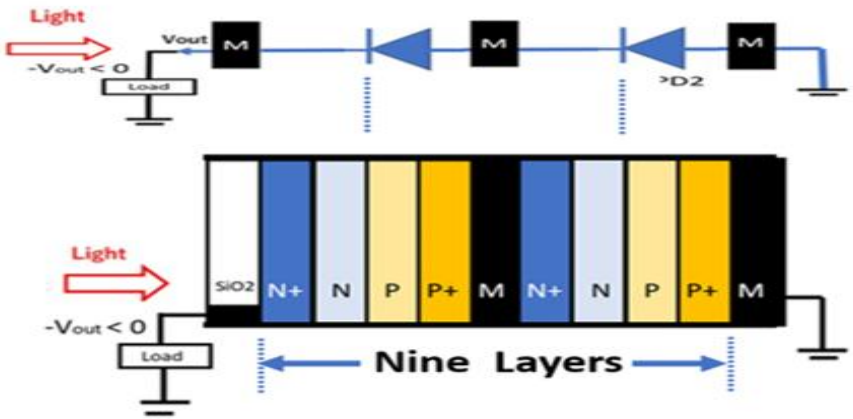
本研究は、タンデム（直列）型でなく、シリコン結晶を使い、BIPOLAR トランジスタ（並列）型の PNP 接合や PNPN 接合型の製法技術をヒントに、高エネルギーイオン打ち込み技術を駆使して新しいシリコン結晶型多重接合太陽電池の新構造と低コスト化に期待される製法を提案..

SONYの1950年代のBipolar Transistor 技術をヒントにした、
HADセンサー型の太陽電池の第1回目の原理試作が実現しました。
IEEEの国際会議（ICCCAS2026）でKey Note Speech　基調講演の
機会をいただき、2026年7月7日に報告しました。
また、詳細をIEEEのジャーナル EXPLORE に掲載されまました。

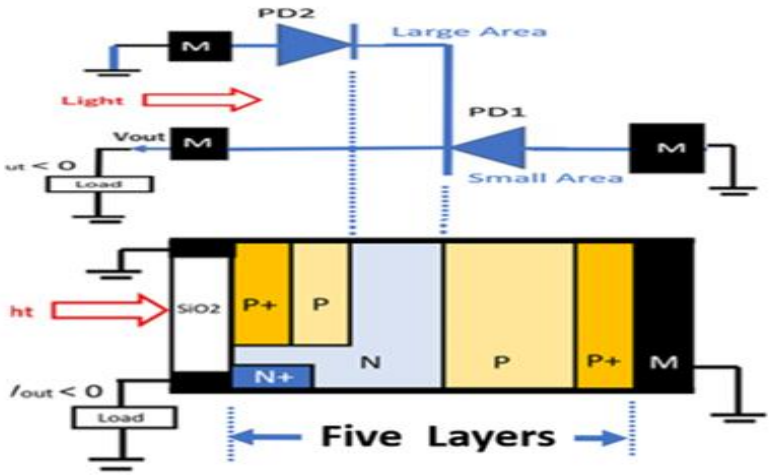
https://ieeexplore.ieee.org/document/11672441

Sony Bipolar Transistor (HAD Sensor型 ）

Tandem type Double Junction
Nine Layers Process Solar Cell



Face-to-Face type Double Junction
Five Layers Process Solar Cell



本研究は、タンデム（直列）型でなく、シリコン結晶を使い、BIPOLAR トランジスタ（並列）型の PNP 接合や PNPN 接合型の製法技術をヒントに、高エネルギーイオン打ち込み技術を駆使して新しいシリコン結晶型多重接合太陽電池の新構造と低コスト化に期待される製法を提案..

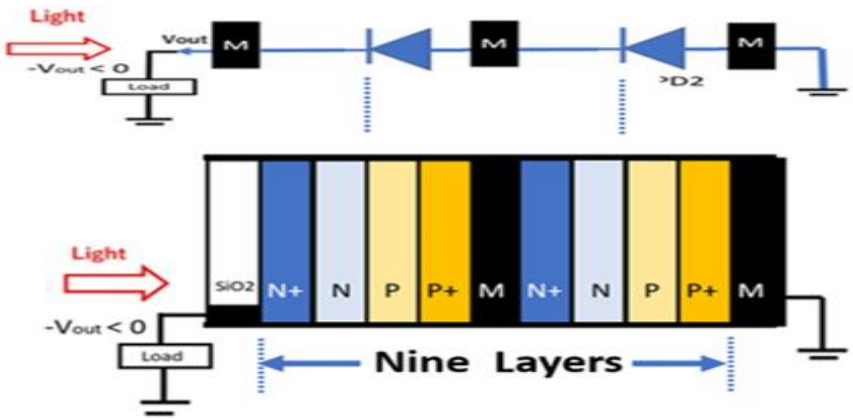
シングル接合では光電変換電流が20%台がシングル接合の限界ですがダブル接合太陽電池でも30%を簡単に実現する事を実験証明しました。今回の挑戦は格安のシリコン結晶でも実現、シリコン材料だけで30%の光電変換出力電流を実現しました。

透明電極材料が不要です。シリコン結晶材料だけで造れます。低コストで寿命が長く信頼性にも実績があると期待されます。このダブル接合構造をさらにペロブスカイト等の現在注目される新材料に適応する事により、薄膜太陽電池でも寿命と信頼性のさらなる改善向上が期待されます。

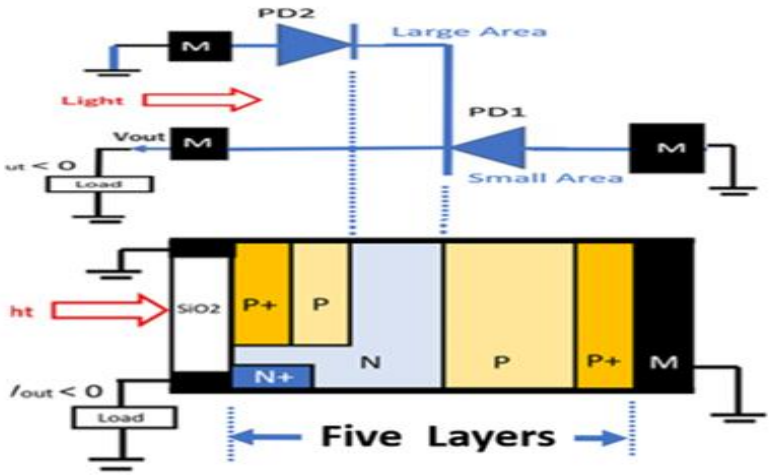
https://ieeexplore.ieee.org/document/11672441

Sony Bipolar Transistor (HAD Sensor型)

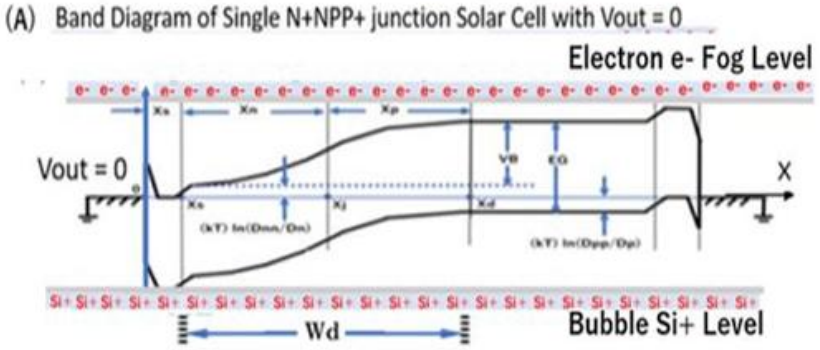
Tandem type Double Junction
Nine Layers Process Solar Cell

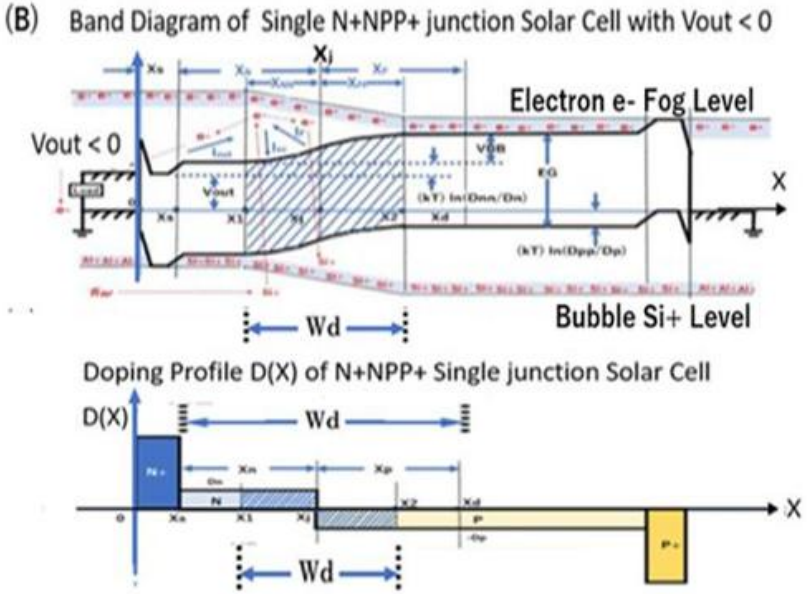


Face-to-Face type Double Junction
Five Layers Process Solar Cell



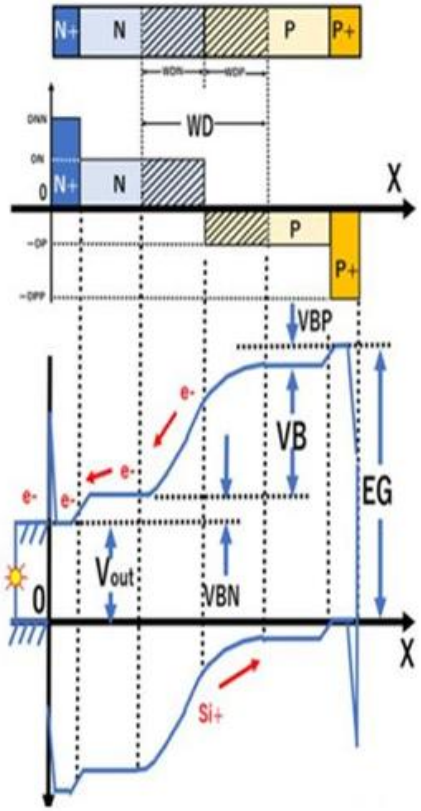
The depletion width (WD) of N+NPP+ Single Junction Solar Cell is limited about 2 µm.



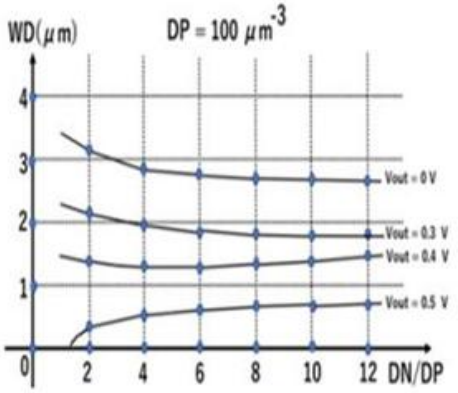


In forward-biased condition, the depletion width WD gets smaller.

$$WD = \mathrm{sqrt}(2*Esi*VB*DP*DN/(DP+DN)) < \sim 2\,\mu m;$$



	Vout= 0.0	Vout= 0.1	Vout= 0.2	Vout= 0.3	Vout= 0.4	Vout= 0.5
DN= 100	WD=3.549056	WD=3.162872	WD=2.722455	WD=2.195395	WD=1.492568	—
DN= 200	WD=3.129827	WD=2.802109	WD=2.430600	WD=1.999034	WD=1.421202	WD=0.275348
DN= 300	WD=2.981419	WD=2.675978	WD=2.330845	WD=1.924801	WD=1.406008	WD=0.498858
DN= 400	WD=2.907578	WD=2.614194	WD=2.283421	WD=1.895788	WD=1.404995	WD=0.594988
DN= 500	WD=2.864565	WD=2.578863	WD=2.257284	WD=1.881534	WD=1.408876	WD=0.655539
DN= 600	WD=2.837110	WD=2.556794	WD=2.241694	WD=1.874352	WD=1.414635	WD=0.699424
DN= 700	WD=2.818521	WD=2.542227	WD=2.231989	WD=1.870997	WD=1.421087	WD=0.733720
DN= 800	WD=2.805416	WD=2.532263	WD=2.225639	WD=1.869855	WD=1.427711	WD=0.761812
DN= 900	WD=2.795911	WD=2.525296	WD=2.221963	WD=1.870059	WD=1.434267	WD=0.785570
DN= 1000	WD=2.788888	WD=2.520367	WD=2.219606	WD=1.871110	WD=1.440642	WD=0.806134
DN= 1100	WD=2.783688	WD=2.516874	WD=2.218296	WD=1.872703	WD=1.446790	WD=0.824246
DN= 1200	WD=2.779823	WD=2.514419	WD=2.217725	WD=1.874643	WD=1.452688	WD=0.840419



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電子の流れ（動き）を水の粒子だけでなく雲（水蒸気）の動きとして理解する必要がある。

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ダブルおよび多重接合型太陽電池のデバイス構造とプロセス製法の提案

Bipolar Transistor PP-NP-P+ Parallel Multi Junction Type Solar Cell

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Thank You !