Chronology of Silicon-based Image Sensor Development

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Introduction

The article presents key steps of development of silicon-based image sensors. The author's intention has been to present them chronologically. However, since different aspects of the sensor design are discussed, some contents have been duplicated. Hopefully, they do not obscure the overall picture of the image sensor development.

The P+P doping variation in the base region of a bipolar transistor was first proposed by Herbert Kroemer in 1953 to realize the drift-field transistor for high frequency operations as shown in Fig. 1. The forward biased emitter-base junction injects electrons from the electron fog in the emitter into the base. There, the minority carriers swiftly migrate towards the collector thanks to the electric field induced by the P+P doping variation in the base region. Properly shaped doping profiles became later an indispensable building block of silicon image sensors.

In 1970, the CCD image sensor was invented that provided a complete charge transfer capability without image lag. The CCD image sensors were next intensively studied and refined [1-5]. However, the MOS photo capacitor used in the CCD image sensor employed metallic electrodes that impeded transmission of the short-wave blue light.

In 1975, three double and triple junction pinned photodiodes (PPDs) were invented and patented [7-9]. Reproductions of figures in the Japanese Patent Applications of (a) the N+N-P+NP-P triple junction PPD (JPA1975-127646), (b) the N+N-P+N double junction PPD (JPA1975-127647) and (c) the PNP double junction PPD (JPA1975-134985) are shown in Fig. 2. All of them behave as photo junction-capacitors and have the CCD-like complete charge transfer capability, no image lag feature with in-pixel vertical overflow drain (VOD) structure for the anti-blooming function, and the electronically adjustable exposure time for fast moving action pictures. Potential distributions shown in Fig. 2 clearly illustrate the mentioned above importance of doping profiles in those devices. Devices (a) and (b) both have in-pixel MOS capacitor buffer

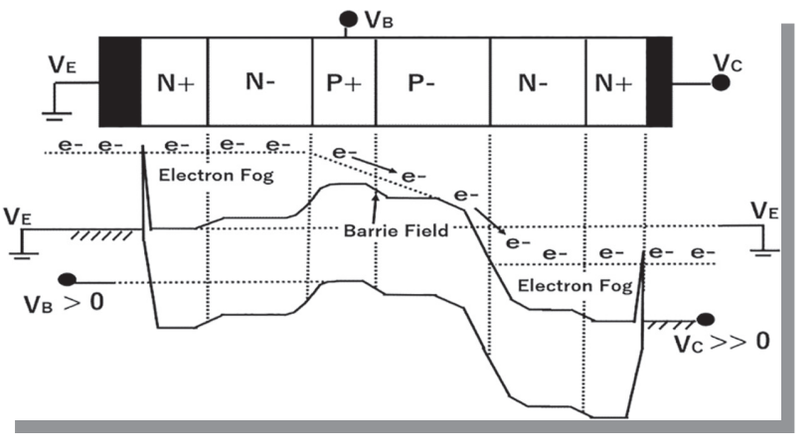

Figure 1: The drift-field transistor for high frequency operations, invented by Herbert Kroemer in 1953.

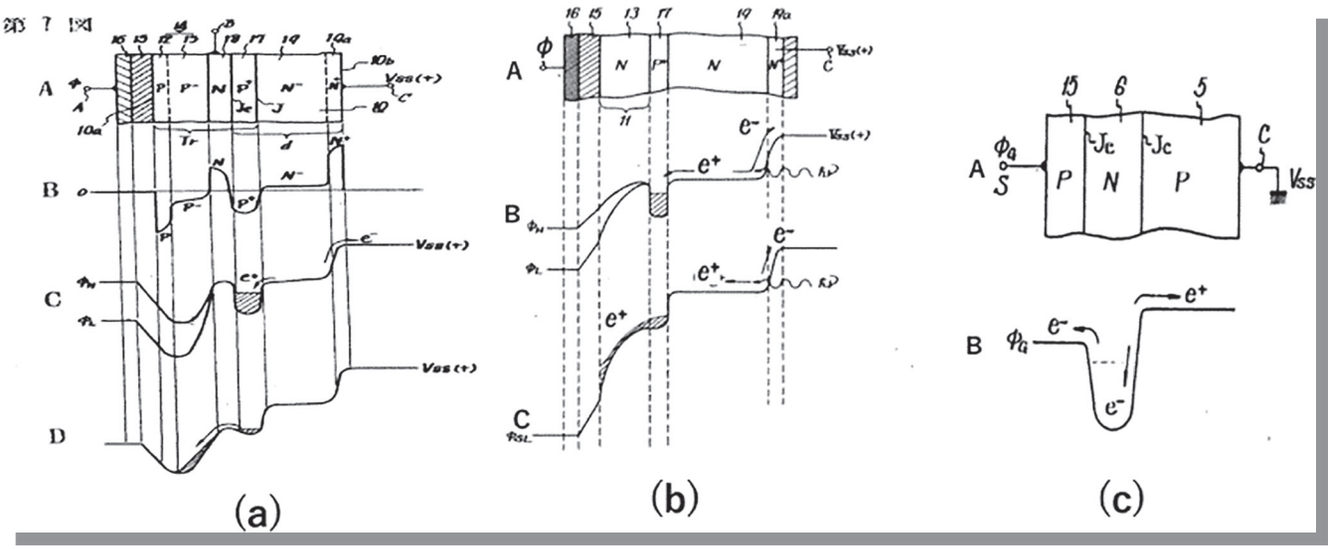

Figure 2: Reproductions from the Japanese Patent Applications of (a) the N+N-P+NP-P triple junction PPD, (b) the N+N-P+N double junction PPD, and (c) the PNP double junction PPD.

memory for realization of the global shutter function in the CMOS imagers.

Short-wave blue light with the photon energy higher than 1.1 eV is absorbed in the vicinity of the silicon surface and cannot penetrate deep into the silicon crystal. Therefore, in order to guide the short wave blue light into the deep bulk semiconductor region, wide bandgap semiconductors are generally used, instead of silicon, for high-performance solar cells. However, the problem is that the PN junction barrier potential in the PN junction depletion region cannot be formed at the semiconductor surface because the strong barrier electric field in the depletion region invites the undesired surface dark current. This problem was solved in 1975 for image sensor applications by using the pinned surface P+P doping variation to enhance the short wave blue light sensitivity in the P+PNPN triple junction type pinned photodiode [7-9] which preserves the CCD-like complete charge transfer capability without image lag in the blue light transmission. The pinned surface P+P doping variation effect was used in this device, creating the surface band bending of kT ln(P+/P) to separate the photo electron and hole pairs generated by short wave blue light effectively at the silicon surface.

A 128-bit analog CCD delay line [12] was developed and reported at the SSDM 1977 conference in Tokyo. It used the PNP junction PPDs with the complete charge transfer capability and the unique directionality resulting from the narrow-channel transfer gates for the virtual charge transfer operation (Fig. 3).

In 1978, a frame transfer (FT) CCD area image sensor was reported at the SSDM 1978 conference [13]. That image sensor used the same PPDs with a very low dark current, the complete charge transfer capability and the no image lag feature, as proved by a spectral response and signal output waveforms (Fig. 4). Fig. 4a shows a pinned-surface and buried-storage PNP junction type photodiode. Fig. 4b shows the spectral response of the imager with short-wave blue light sensitivity. Fig. 4c shows the output signal at no illumination showing very low surface dark current level. Fig. 4d shows the output signal waveform with input light, showing the no image lag feature. The hole accumulation region providing the surface pinning is formed by the adjacent heavily doped channel stops obtained using the high energy ion implantation followed by the lamp anneal step, invented and developed by Kazuo Nishiyama at Sony. Many other companies, including Kodak and NEC apparently used either the LOCOS isolation technology or the shallow trench isolation (STI) technology since they are standardized processes widely used for the digital CMOS LSI chips. However, the LOCOS and STI processes induce the extra thermal stress and the undesired crystal damage, degrading the chip yield and reliability. Therefore, since 1978 Sony has used neither LOCOS nor STI in the image sensor productions. The image sensor reported at the SSDM 1978 conference [13] was the world's first PNP double junction PPD.

Fig. 5 shows different variants of photodiodes. Fig. 5a shows again the PNP double junction PPD developed by Sony in 1978. Fig. 5b shows the PPD defined and presented by the Semiconductor History Museum of Japan. Both photodiodes have the adjacent heavily doped P+ channel stop regions formed by the deep high energy ion implantation and without the use of LOCOS or STI isolation. For a comparison, Fig. 5c shows the buried photodiode developed by NEC [17], Fig. 5d shows the PPD developed

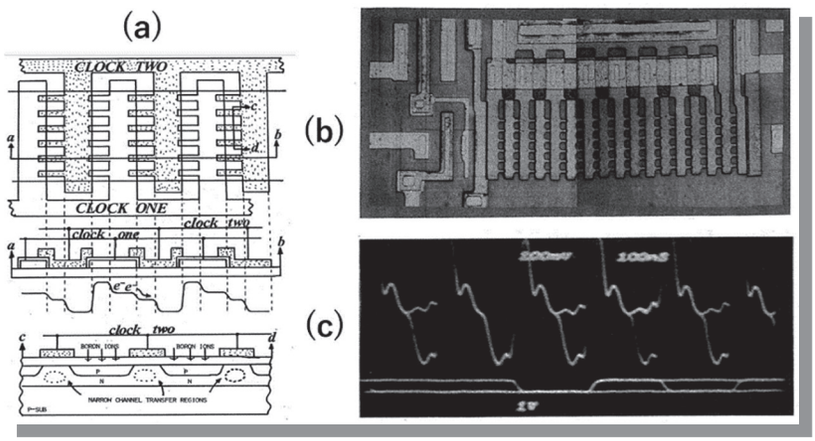

Figure 3: (a) Top and cross-sectional views with the PPD type SiO_2-exposed light-receiving windows; (b) the chip photograph at both ends of the two-phase narrow-channel CCD analog delay line; (c) the output waveform showing the complete charge transfer capability without image lag.

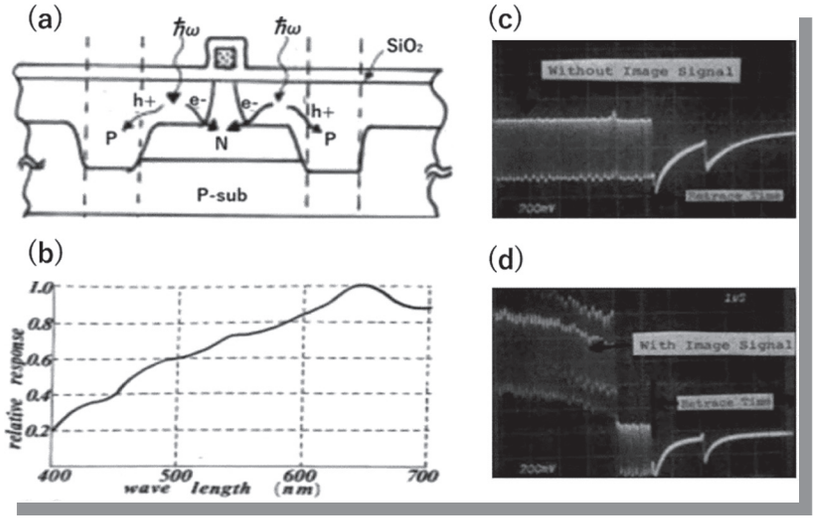

Figure 4 (a) Pinned-surface and buried-storage PNP photodiode; (b) spectral response of the blue-light sensitive imager; output signal (c) without (d) with illumination.

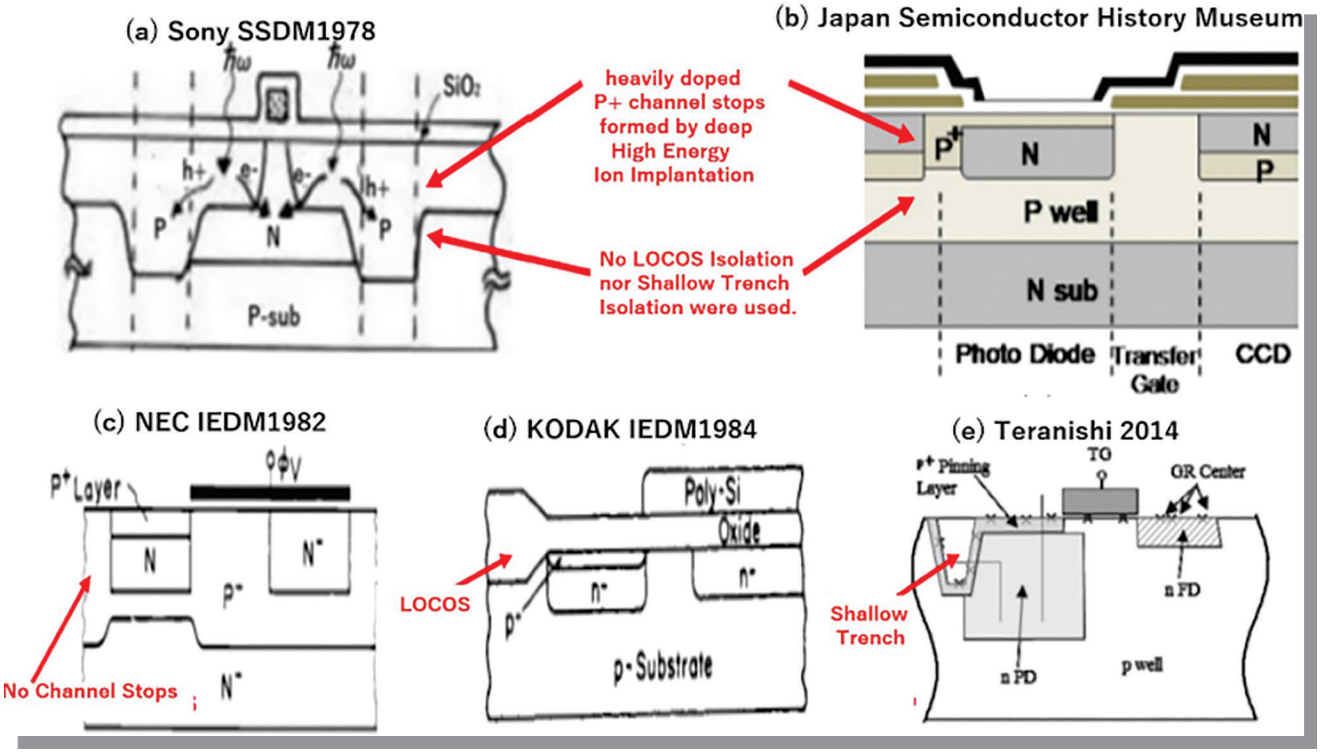

Figure 5: (a) PNP double junction PPD developed by Hagiwara team at Sony in 1978; (b) PPD defined and shown by Semiconductor History Museum of Japan, (c) NEC buried photodiode [17], (d) Kodak PPD [18], (e) PPD reported by Teranishi [25,26].

by Kodak [18] and Fig. 5e shows another conventional pinned photodiode reported by Teranishi [25-26].

A subsequent review paper [21] in 1996 revisited the 1975 invention [9] and the SSDM 1978 paper [13], and explained that it was essentially the invention of both the virtual-phase CCD with the built-in narrow-channel type directionality and the no-image-lag feature, which became the basis of Sony's so-called "Hole Accumulation Diode," (HAD) with the anti-blooming function capability and with the low thermal and crystal stress.

The image sensors include not only detection diodes but also control circuitries. Bipolar transistor and thyristor are switching devices using the base region as a gating-switch while the double and triple pinned photodiodes use the in-pixel clocked overflow-drain (OFD) to realize the anti-blooming, the global shutter function and the electronic shutter function, by controlling the light exposure time with a complicated external clocking sequence according to the TV scanning system.

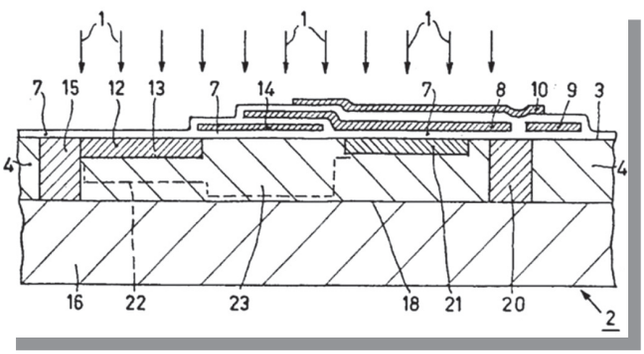

Figure 6: The double junction type buried photodiode image sensor reproduced from Netherland Patent Application NPA [6].

The world's first Double Junction-type Buried Photodiode

As it has been mentioned above, the MOS photo capacitor used in a CCD image sensor employs metallic electrodes which impede the short-wave blue light transmission. Philips solved this problem in 1975 using the first double junction type buried photodiode [6]. In Fig. 6 from the NPA7506795 patent, a dashed potential profile (12) is drawn to show an empty potential well of a complete charge transfer. No image lag feature was expected in this design. However, in reality the surface P region is connected to the high resistivity substrate (16) by a resistive region (15). Evidently, the surface region (13) may have a large RC delay time constant, introducing a serious image lag problem. Thus, the surface region (13) potential is not completely pinned and is floating with a RC delay-time, inviting time-lag and image-lag problems. Therefore, by definition such a structure cannot be considered to be a pinned photodiode.

The world's first Triple Junction-type Pinned Buried Photodiode

The double junction buried photodiode without the metallic electrode has a fair light-sensitivity. More detailed surface doping engineering is required to enhance the short-wave

blue-light sensitivity of such a device. This problem was solved by using the pinned surface P+P doping profile in the PNPN triple junction type PPD [7], which preserves the CCD-like complete charge transfer capability without image lag in the blue-light transmission. By analogy with a rubber belt that must be fixed at one end in order to be stretched by strong pulling down, also the surface potential of the photodiode must be pinned in order to create the potential profile enabling a punch-through mode to realize the complete transfer of charge without the image lag.

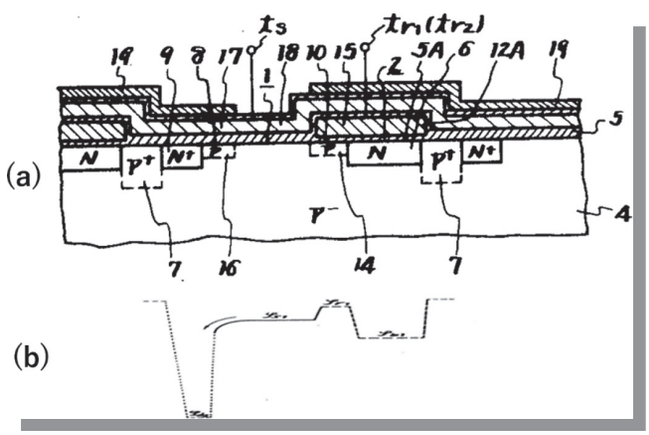

Figure 7: Figures reproduced from Japanese Patent Application JPA1977-126885 [10]: (a) sensor, (b) potential profile for the OFD punch-through action.

The world's first Pinned Photodiode with the Global Shutter and the Electronic Shutter functions

The JPA1975-127646 patent application [7] defined the world's first PNPN triple junction type PPD, also equipped with an in-pixel MOS capacitor type buffer memory. This device together with two other ones, also invented by Sony [8, 9], enabled realization of the global shutter clocking scheme needed for modern CMOS image sensors. The electronic shutter clocking scheme was invented in 1977 by Sony and used in the MOS/CCD dynamic photo capacitor [10] (Fig. 7a) with the in-pixel lateral anti-blooming overflow-drain (OFD). The potential profile at the OFD punch-through action with the complete photo signal-charge transfer-and-draining action into the in-pixel lateral OFD is presented in Fig. 7b. Both pictures are reproductions of drawings in [10]. This punch-through action-mode clocking-scheme can also be applied in the PNPN-triple-junction pinned photodiode. Such a punch-through action corresponds to a triple-junction photo-thyristor switching-on action as originally invented in 1975 [7] (see Fig. 2a).

The two mentioned above types of global shutter clocking schemes in CMOS image sensors are illustrated in Fig. 8a, 8b. Fig. 8a shows the normal global shutter mode, where the light integration time is the same as the unit scanning period (1/60 sec) of the television scanning system, which

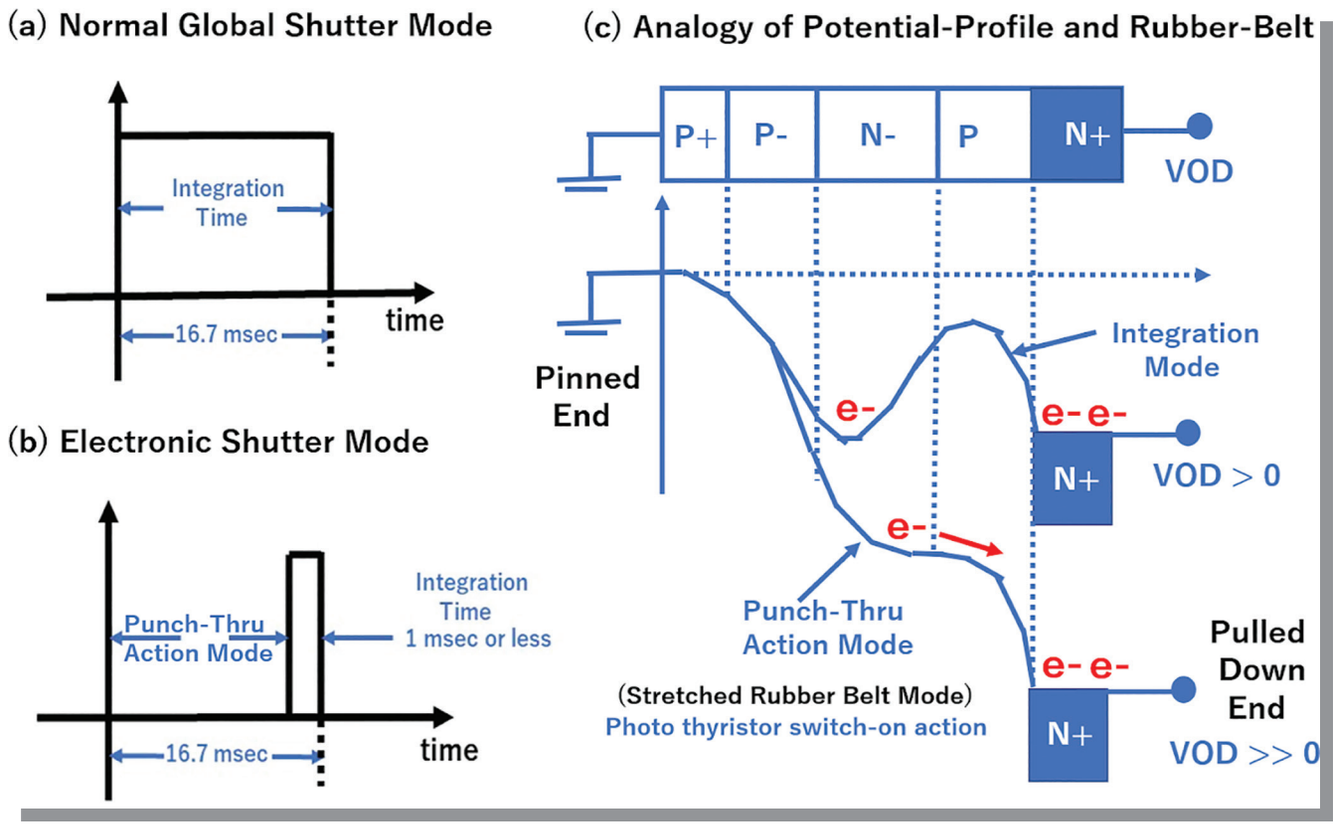

Figure 8: (a), (b) Global shutter clocking schemes for CMOS image sensors: normal global shutter mode, electronic shutter mode; (c) the electrical potential profile of the P+PN-PN+ triple junction type PPD in the photo thyristor switch-on mode and in the integration mode.

is too long to obtain a clear still picture of a fast-moving action-object. Fig. 8b shows a special case of the global shutter with a shorter exposure time, namely the electronic shutter which is controlled by adjusting the clocking pulse width of the in-pixel clocked overflow drain (OFD). Invention of the electronic shutter revolutionized the completely mechanical parts-free solid-state image sensor world [10].

In 1987, Kikuyo Ishikawa and her team at Sony used the electronic shutter clocking scheme and applied successfully for the first time in the world in a complete and finalized form for production of the P+PN-PN+ triple junction type PPD [19, 20] with the anti-blooming vertical-overflow-drain (VOD). Fig. 8c illustrates in a simplistic way a principle of operation of such a device in the integration mode and in the punch-through mode. In both modes the potential is pinned at the P+ area and the analogy to the rubber belt stretching model is visible.

The world's first Interline Transfer-type CCD Image Sensor

When the first interline transfer (ILT)-type CCD image sensor was proposed, the widely used floating surface N+P single junction type photodiode suffered from the serious image lag problem. Philips 1975 patent application on the buried photodiode [6] and Sony 1975 patent applications on the pinned photodiode [7-9] both were originally intended to apply for the ILT type CCD image sensors. Teranishi at NEC also filed in 1980 a patent [15] on the buried photodiode structure, very similar to the one proposed in 1975 by Philips, and reported at IEDM 1984 [17]. These photodiodes also apply in modern CMOS image sensors. However, it has to be mentioned that in the scope of the patent [15] the floating surface with surface electric field exists in the device. Consequently, both the surface and the buried charge storage region become floating. Due to this, the buried photodiode defined in the patent [15] may have a serious image lag. Therefore it cannot be deemed a PPD.

Sony developed in 1980 and reported in [14] the ILT-type CCD image sensor, using a thin polysilicon (SIPOS) gate type MOS photo-capacitive type sensor structure with the in-pixel lateral OFD for the anti-blooming and electronic shutter function capabilities. The photo sensor structure was of a MOS/CCD photo capacitor-type which had the complete charge transfer capability and the no image lag feature as shown in Fig. 7 reproduced from Japanese Patent Application JPA1977-126885 [10].

At IEDM 1982, Teranishi's team presented a NEC-developed ILT-type CCD image sensor, using the PNP double junction type Buried Photodiode [17]. The details of the image lag data were reported. Neither LOCOS nor STI were used in the manufacturing process. The schematic view of the device is shown in Fig. 5c.

KODAK developed and reported at IEDM 1984 the ILT-type CCD image sensor using the PNP double junction type pinned photodiode [18]. KODAK emphasized there the importance of the pinned surface in order to achieve the complete charge transfer capability and the no image lag feature. The LOCOS step was used in manufacturing of the device that is shown in Fig. 5d.

Sony reported in a Japanese domestic journal [19] and also at SPIE 1989 conference [20] the ILT-type CCD image sensor, using the PPD of the PNPN triple junction-type with the anti-blooming and the electronic shutter function capabilities. Also in this work, it was emphasized that the pinned surface is a prerequisite for the complete charge transfer capability, the no image lag feature and also the high frequency electric shutter function, in order to achieve the completely mechanical-part-free solid-state image sensors.

The lost invention of the Pinned Photodiode

The Pinned Photodiode technology greatly contributed to design, development, and improving the performance of back-illuminated CMOS image sensors. Sony applied for three basic patents JPA 1975-127646 [6], JPA 1975-127647 [7] and JPA 1975-134985 [8] on pinned photodiodes in the Japanese Patent Office. However, Sony did not apply to any US Patent Office and other overseas patent offices. The invention was completely forgotten by the rest of the world until June 26, 2020 when Sony finally disclosed officially the 1975 patent applications and quoted the Sony efforts in 1978 of developing the first PNP junction type PPD [33]. Subsequently, Semiconductor-History Museum of Japan also published a supporting article [34].

Pinned Photodiode adopted for Back-Illuminated CMOS Image Sensors

The Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development is as below.

After the invention of the back-illuminated N+NP+N double junction-type PPDs, the N+NP+NP triple junction-type PPDs, and the PNP double junction-type PPDs, Sony succeeded in making for the first time in the world a principle-prototype of a frame transfer (FT) CCD image sensor that adopted the PNP junction-type PPD technology, having the P+ channel stop region formed by ion implantation near the light receiving section. The related technical paper was presented at the academic conference SSDM 1978 [13]. This achievement was commercialized soon. In 1980, Sony succeeded in making a camera integrated VTR which incorporated the new one-chip FT CCD image sensor. This development was announced during the press conferences held on the same day in Tokyo and New York by the President of Sony, Kazuo Iwama and the Chairperson of Sony, Akio Morita respectively. This announcement surprised the world.

In 1987, Sony succeeded in developing an 8 mm video camcorder that adopted, for the first time in the world, the ILT CCD image sensor with VOD function, which incorporated PPDs with the P+ channel stop region formed

by ion implantation near the light receiving section. This camcorder became the pioneer of the video camera market [23-32]. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors [33-34].

Sony's announcement on the invention of Hole Accumulation Diode (HAD)

In 1987, Sony developed a 2/3-inch, 380,000-pixel CCD image sensor using a Hole Accumulation Diode (HAD) [19-20]. It was a new type of the PPD. Its construction enabled efficient reduction of the dark current noise. This image sensor was next installed in the 8mm VTR integrated video camera "CCD-V90". In the 1990s, the era of passport size video cameras demanded compact CCD image sensors with large numbers of pixels (1/2 inch or smaller with 400,000 pixels or more). As a result, Pinned Photodiodes came to be widely used by manufacturers of the CCD/CMOS image sensors [21]. In 1995, Kodak adopted them for their CMOS imagers.

The future application of Pinned Photodiode for High Quantum Efficiency Solar Cells

Japanese Patent Applications (JPA) [7-9] by Sony in 1975 explained in details and defined the first triple junction type Pinned Buried Photodiode with the in-pixel vertical overflow drain (VOD) function with the electronic shutter capability of the electrically-adjustable exposure time control, realizing the completely film-free and mechanical-parts-free all-digital solid-state image sensors. Sony showed in 1975 in the patent applications that the conventional PN junction depletion region is not the only place to have a barrier potential needed for photo electron hole pair separation. A clever doping-engineering of the pinned surface P+P hole accumulation region can also create the surface barrier electric field to enhance drastically the photoelectron and hole pair separations to increase the short-wave blue light sensitivity. This surface P+P doping-engineering with the completely-depleted buried N- region, together with the metallic-trench formation, by eliminating the substrate-resistance of the cause of Joule-heat, may realize a high quantum efficiency (QE) pinned-buried double-junction pinned-photodiode type solar cell. Thus, the double and multi-junction pinned photodiodes with the excellent QE for the short-wave blue-light spectrum widely used now in image sensors may have a possible application for future high QE solar cells by using the low-cost high-resistivity silicon crystals.

Image sensors and solar cells both convert the photon energy into the electron energy. Fig. 9 shows a possible

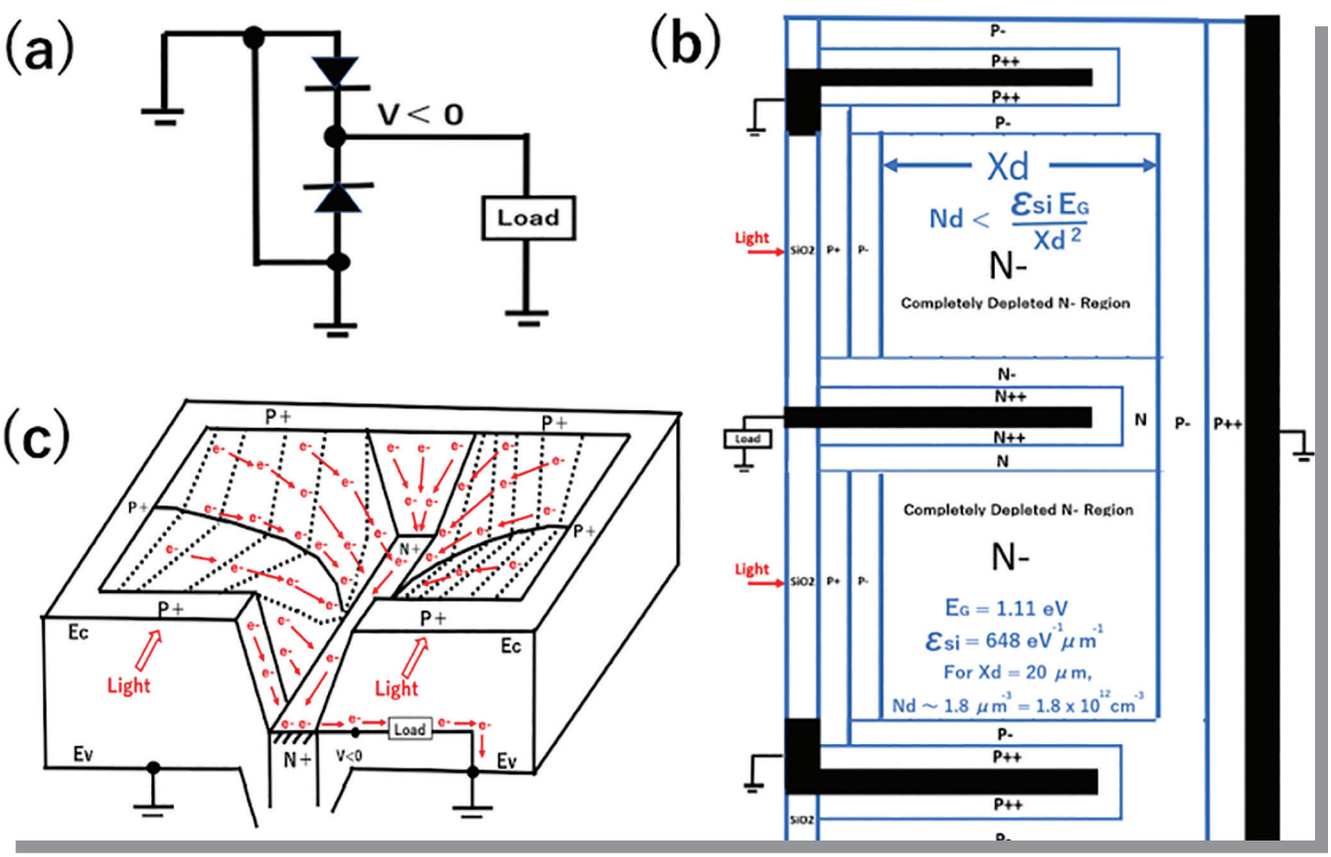

Figure 9 (a) The equivalent circuit of double junction pinned photodiode type solar cell, (b) the cross-sectional view and (c) the two-dimensional potential profile with a completely-depleted buried N- region of strong electric field, guiding photo electrons swiftly into the heavily doped metallic N+ chare collecting region.

future solar cell application of the double junction-type PPD. The lightly doped buried N- region is completely depleted. Thus a strong electric field exists for the photo-electron and hole pair separations. Fig. 10 shows another possible future solar cell application of a multi-junction type pinned buried photodiode with the P+P surface doping variation and the fully depleted multiple buried N and P regions. Fig. 11 explains the advantage of the P+PNPP+ double junction-type solar cell over the conventional N+P single junction-type solar cell. The P+P surface doping profile creates the surface conduction-band bending that enhances photo-electron and hole pair separation at the semiconductor surface resulting in a high quantum efficiency for the short-wave blue light. Contrary to the multi-junction solar cell, the floating-surface N+P single-junction type photodiode has no surface electric field that could support separation of the photo electrons and holes generated in the vicinity of the N+ flat surface, The photogenerated carriers do not move and eventually they recombine with each other, resulting in a poor QE for the short-wave blue-light.

Fig. 11 The PNP double-junction PPD with the completely depleted N region and the floating N+ storage region has an excellent quantum efficiency (QE) for the bluelight. The floating-surface N+P single-junction-type photodiode has no surface electric field, where the photogenerated electron and hole pairs do not move and eventually they recombine with each other, resulting in a poor QE for the short-wave blue-light.

Summary

The article reviews the chronology of development of different types of the pinned photodiodes. Steps towards achieving the excellent short-wave blue-light sensitivity are emphasized. These steps were followed in the past by many successful realizations of the pinned photodiodes and their applications in different image sensors and equipment.

The article is focused on works done by teams from Sony, including double junction-, triple junction-type PPDs, ILT PPDs, HADs, to name a few. Obviously, only a part of the achievements in this area are presented in this

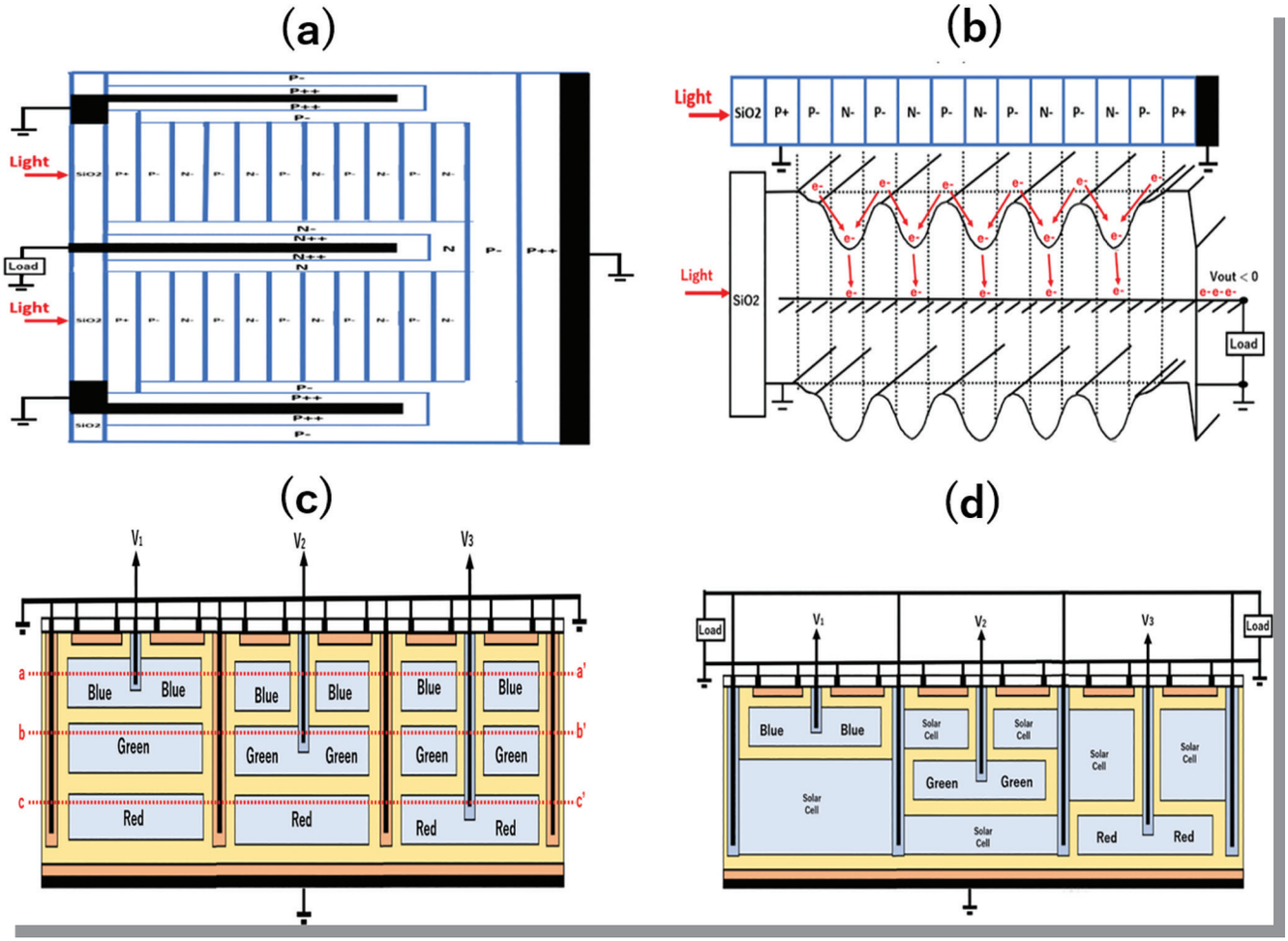

Fig. 10 (a) The cross-sectional view and (b) the potential profile of a multi-junction pinned photodiode type solar cell; (c) a color-filter-less color image sensor; (d) a combination of a color-filter-less color image sensor and a solar cell.

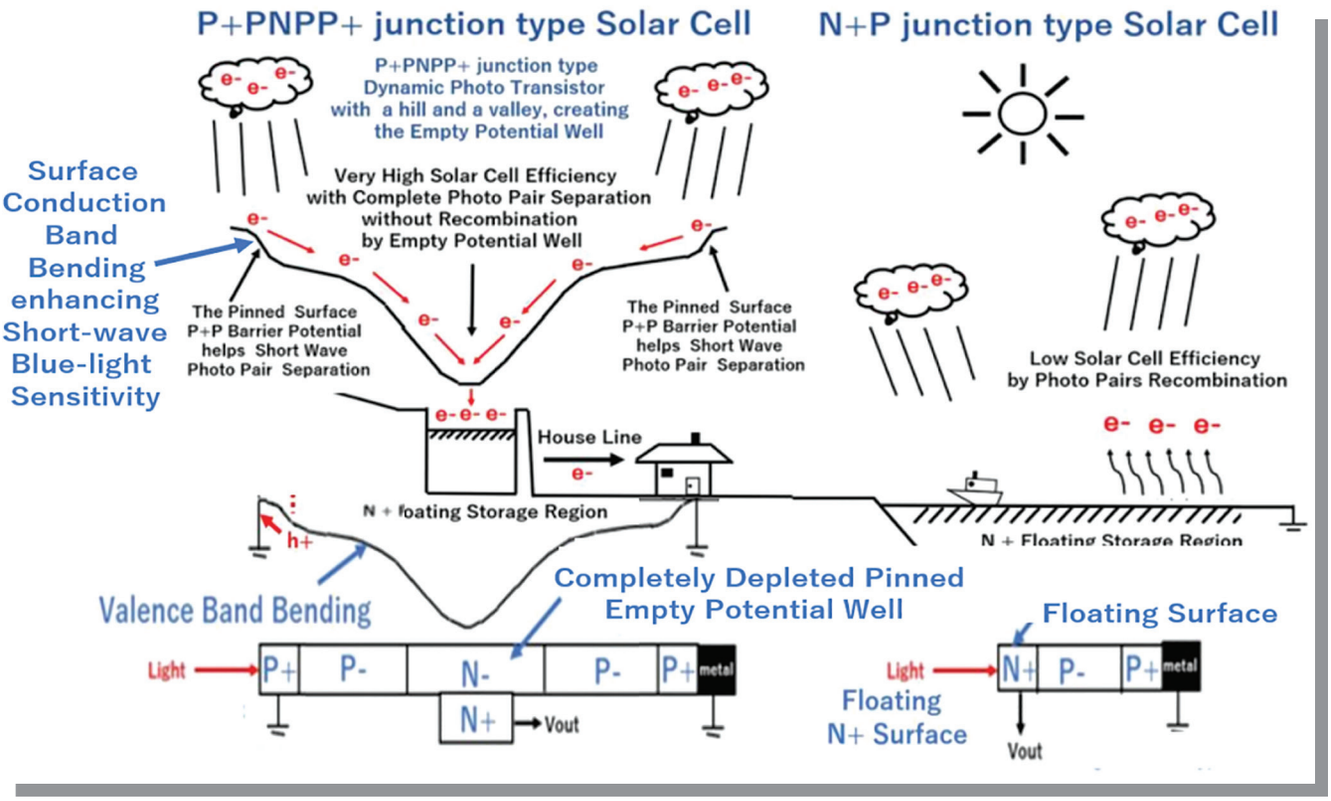

Fig. 11 The PNP double-junction PPD with the completely depleted N region and the floating N+ storage region has an excellent quantum efficiency (QE) for the bluelight. The floating-surface N+P single-junction-type photodiode has no surface electric field, where the photogenerated electron and hole pairs do not move and eventually they recombine with each other, resulting in a poor QE for the short-wave blue-light.

paper. The inventions made by teams from the companies like Kodak or Hitachi are reported elsewhere.

The main author's message in this article is that (i) the short-wave blue light sensitivity is the most important advantage of the double- and multi-junction pinned buried photodiodes, (ii) the pinned buried photodiodes enabled implementation of the electronic shutter in the image sensors. These are two factors that revolutionized the completely mechanical parts-free solid-state image sensor world.

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Prof. C. A. Mead and Prof. T. C. McGill at Caltech advised my original 1971 undergraduate work on the Ga2O3-Au Schottky Barrier interface study and characterization, and for guiding my 1974 PhD thesis work on Charge Transfer Analysis of Buried Channel CCD Image sensors.

Sony Image Sensor R/D efforts started in 1969 with the strong initiative of the ex-president of Sony Corporation, Kazuo Iwama, who emphasized the market need of the portable small video camera with no image lag feature for the fast-action and snap-shot pictures. Kazuo Iwama gave Hagiwara a chance to work at Sony in 1975 to build an artificial intelligent image sensor system with the real time robot vision and the powerful digital circuit engines for real time operations.

Under the guidance of Dr. Sei-ichi Watanabe, Sony team of Miyaji, Nakagawara, and other young engineers helped me to develop in 1989 for the first time in the world the 25-nano sec access-time 4 Megabit fast-cache SRAM chip, needed to realize a fast- snapshot full-size image-capturing system for digital solid-state cameras.

SONY bipolar process and device technology gave many hints and guided me to the original 1975 invention and the 1978 successful development for the P+PNP double junction type Pinned Photodiode.

Yoshiyuki Kawana at Sony in 1950s invented the low-collector on-resistance P+P-N+N-P-P+ junction type bipolar transistor for high frequency operation by thinning the back side of the silicon wafer, a technique now widely used for the modern backside illumination CMOS image sensors to improve sensitivity.

Toshio Kato at Sony in early 1960 invented the silicon surface light etching technique and new SiO2 passivation technique for the P+NP junction type bipolar transistor with the MESA like isolation, which is now known as the shallow trench isolation with the excellent side wall SiO2 to reduce the device leakage current. Both ideas of Yoshiyuki Kawana and Toshio Kato hinted to form in 1975 the concept of the Pinned PNPN triple junction type dynamic photothyristor with the electronic shutter switch-on action.

Sony young-generation engineers, including Hamazaki and Ishikawa chip-design team and Kambe CCD-process team, used in 1987 the triple junction type pinned buried photodiode invented in 1975, which has the built-in VOD structure capable of the electronic shutter and snapshot picture functions, and produced for the first time in the world the all-solid-state snapshot fast-action video cameras, completely free from mechanical parts. The feature of the global shutter function using an in-pixel MOS-capacitor-type global buffer memory became a reality in modern backlit CMOS image sensors by the young generation of Sony engineers after the 45 years since the invention in 1975.

Special thanks go to Prof. Hiroshi Iwai, Dr. Tsugio Makimoto, Ki-ichiro Mukai, Terushi Shimizu, Yasuhiro Ueda, and Dr. Tadakuni Narabu for their encouragement and kind advice. Lastly but not the least, Dr. Sei-ichi Watanabe, Yoshiyuki Kawana and Toshio Kato guided and helped me whenever I was in need. They are all dear friends and mentors in private and public.

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A Review of the 2022 ESSDERC-ESSCIRC Conference: the Annual European Forum on Recent Advances in Solid-State Devices and Circuits

The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on-chip design is rapidly increasing. This is made possible by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers, and system designers is necessary. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both device and circuit communities. ESSDERC and ESSCIRC have evolved over the last years to follow recent fast-growing R&D device, circuit, and system topics. Besides the traditional ESSDERC and ESSCIRC tracks, a number of joint tracks have been introduced, to encourage and facilitate interactions between circuit, system, and device researchers. Along this line, this year for the first time the governance structure of the Technical Program Committees was revised to have a single Technical Program Chair who coordinated the actions of three different Technical Program Co-Chairs, one for the ESSDERC tracks, one for the ESSCIRC tracks, and one for the joint tracks. Attendees registered for either conference had the chance to attend any of the scheduled parallel sessions, regardless to which conference they registered to.

University of Milan-Bicocca was very proud to organize the 52nd European Semiconductor Device Research Conference (ESSDERC) and the 48th European Semiconductor Circuits Conference (ESSCIRC). The event was held in presence, in Milan, Italy, September 19-22 2022. Notwithstanding the echoes of the global pandemic, which forced the last two editions of the conference to offer virtual attendance, the participation to the event exceeded the expectations, with over 870 registered participants from all over the world (including a significant share from the US and the Far East), i.e., the highest attendance in the last ten years, confirming the event as the flagship European meeting in the field of semiconductor devices and circuits. We would like to thank the organizing team who coordinated the event as well as the administrative team set up around the company Sistema Congressi. The ESSDERC conference was financially sponsored by the IEEE Electron Devices Society and ESSCIRC by the IEEE Solid-State Circuits Society. Many world-class as well as local companies in the field of micro- and nano-electronics present in the northern Italy area co-sponsored the conference:

- *Diamond*: Bosch, Huawei, Infineon, STMicroelectronics
- *Gold*: Sony, Synposys
- *Silver*: ams OSRAM, Analog Devices, INVENTVM, Kioxia, Knowles, Melexis, RedCat Devices, Samsung, SERMA, TDK