

Invention and Historical Development Efforts of Pinned Buried Photodiode

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Abstract— This paper reviews the invention of Pinned Buried Photodiode in 1975 by Yoshiaki Hagiwara at Sony which is also called as Hole Accumulation Device (HAD) which was originally defined in the form of the P+NPNsub triple junction type dynamic photo thyristor structure with the in-pixel vertical overflow drain (VOD) function to realize the electric shutter function capability. The evidence of the invention is explained with the three Japanese Patent Applications applied by Hagiwara at Sony in 1975. The first double junction type Pinned Photodiode was also developed by Hagiwara Team at Sony in 1978 and reported in the Japanese domestic SSDM1978 conference in Tokyo. The three original Japanese Patent Applications, filed by Hagiwara in 1975, were the evidence of the invention, however, being written only in Japanese and unfortunately never having been applied in USP and other overseas patents. The details are now reviewed and disclosed here with the English translation of the original Japanese Patent Applications for the first time in the IEEE English speaking community. The triple junction type Pinned Buried Photodiode has inherently the image-lag-free feature, the in-pixel VOD function and the electric shutter function capability, that have completely replaced film media and mechanical parts from the modern high-definition solid-state digital cameras.

Keywords—PIN Diode, Buried Photodiode, Pinned Photodiode, Drift Field Bipolar Transistor, Dynamic Photo Transistor, In-pixel Vertical Overflow Drain, Electrical Shutter Function, Global Shutter Function, Pinned Surface Gaussian Doping Profile, Barrie Potential, Solar Cell, Quantum Efficiency,

I. INTRODUCTION

Fig. 1 explains a conventional MOS image sensor in the ITIC read-out circuit configuration. A very small N+P single junction photodiode area capacitance with a floating surface N+ diffusion photo-charge storage region and a large output-data-line capacitance are the cause of the serious clock interference noise and the CKT thermal noise. The clock reset time is very short while the channel resistance R gets very large, causing a very large RC delay time and the serious image lag problem.

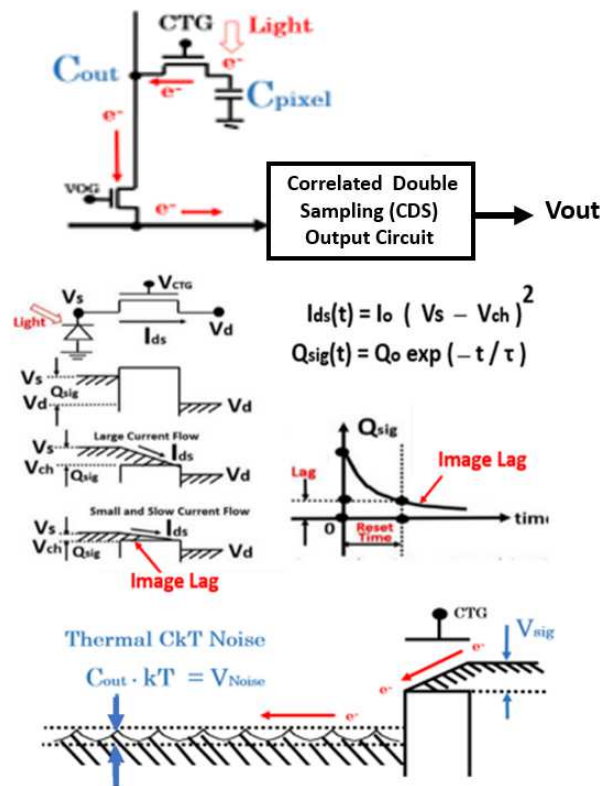


Fig. 1 Classical N+ Floating Surface Single Junction N+P Type Photodiode

The CCD dynamic photo capacitor type solid state image sensor was invented in 1970 by Boyle and Smith in Bell Lab. The image sensors using the CCD type CTD were prevailing in 1980s and 1990s. Specially Buried Channel CCD type image sensors have an excellent charge transfer efficiency of about 99.999%, which was good enough in the analog TV era. The CCD image sensors have no image lag problem and very suited for the snapshot and fast action pictures in the analog TV era.

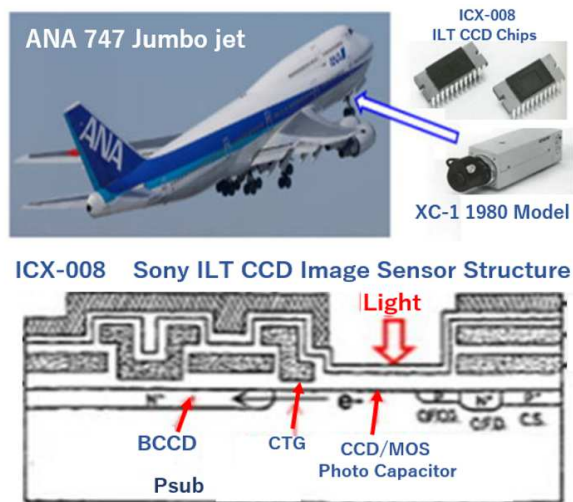


Fig. 2 SONY Two-chip CCD Color Camera XC-1 used in 747 Jumbo, with fast-action movie-pictures of landing and lifting-off with no image lag problem.

However, presently the high definition digital CMOS image sensors have replaced the CCD image sensors completely. The reason was very clear. The CCD/MOS type dynamic photo capacitors are formed with the metal-like polysilicon electrodes which do not let the short-wave blue light pass thru. Historically, Sony once used in early 1980s the thin polysilicon electrode for the CCD/MOS dynamic photo capacitors with the CCD type charge transfer device (CTD) [1]. See Fig. 2. Sony in 1980 commercialized the all-CCD type video cameras with the completely free-image-lag feature for fast-action and snapshot digital still pictures. However, the surface electric field under the CCD/MOS electrode induced the serious surface dark current and generated many white defects, causing serious chip-yield problems. Hagiwara proposed in 1975 a triple junction type Photodiode with the vertical overflow drain (VOD). See Fig. 3.

For the high-definition (HD) picture size of 8000H x 6000H pixels and more in our digital TV era, we would need to have at least $8000+6000=24000$ charge transfers if the CCD type charge transfer device (CTD) was used. Since 0.001% times 24000 gives 24%, the significant percentage of the signal charge would be lost, and pictures would be buried in the noise. Therefore now, the CCD type charge transfer device (CTD) was replaced completely by the low-power digital-CMOS type CTD for modern digital high definition cameras in our digital HD TV era.

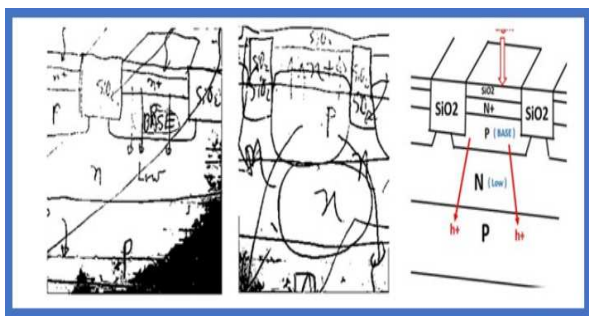


Fig. 3 Hagiwara March 1975 Lab Note, sketching N+PNP triple junction type Dynamic Photo Thyristor type Pinned Buried Photodiode with the vertical overflow drain (VOD) function with the electrical Shutter function capability.

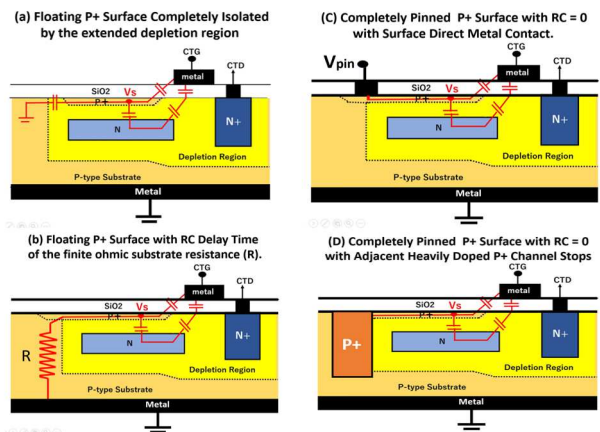


Fig.4 Difference of Buried Photodiode and Pinned Photodiode

The non-zero RC time delay was always a serious problem in 1950s for high frequency device operations, especially for the collector and the emitter non-zero on-resistance problems for high performance power bipolar transistors. The collector and the emitter terminal of a PNP power bipolar transistor had to be pinned to the external voltage with the zero on-resistance to achieve the zero RC time delay for high frequency operations. The concept of Pinned Surface Device was already well understood in early 1950s. When Hagiwara at Sony invented Pinned Buried Photodiode in 1975, the concept of the buried base storage region was also well understood. See Fig.4. There are two types of Buried Photodiode. NEC type [2] is shown in Fig. 4a while Philips type [3] is shown in Fig. 4b. They are Buried Photodiodes with a floating surface and a floating empty potential well with the serious image lag. The other two are Buried Photodiodes with a pinned surface and a pinned empty potential well. Hinted by Pinned Surface Devices produced by Sony bipolar IC technology, Hagiwara invented Pinned Buried Photodiode [4] as shown in Fig. 4c. Hagiwara Team developed in 1978 Pinned Buried Photodiode [5] as shown in Fig. 4d.

II. DIFFERENCE BETWEEN FLOATING SURFACE AND PINNED SURFACE BURIED PHOTODIODES

On a public electrical and electronics engineering Q/A internet WEB site by the electronics-stack exchange.com the difference between Buried Photodiode and Pinned photodiode is explained in details [6]. The question was given as below. "What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?" The answer said, "This is a commonly misunderstood misused set of terminologies. First off these are not PIN Photodiodes - which stands for P - Intrinsic - N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though. Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space. You can get surface state pinning from the dangling Si/SiO₂ bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps."

“The Si/SiO₂ surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface. A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. “

“The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today. A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise as sqrt(KTC) also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from. I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly [7] attributed to Teranishi and to Fossum in CMOS image sensors.”

III. TRIPLE JUNCTION PINNED BURIED PHOTODIODE

Yoshiaki Hagiwara at Sony in 1975 applied Japanese patent on a triple junction type Pinned Buried Photodiode with the back light illumination scheme. Fig. 5 shows the N+N-P+NP-N triple junction Pinned Photodiode which is a reproduction of a figure drawn in Japanese patent application JPA1975-127646. The English translation is also given blow [8].

“An array of charge transfer gates is formed on the oxide layer of a semiconductor substrate (Nsub). The first charge transfer region (P1) is formed under the oxide layer. There is a base gating region (N) between the first region (P1) and the second photo charge collecting region (P2) which is formed in the substrate (Nsub). By proper gating clocks (1), the photo charge is drained to the surface region (P1) from the second region (P2) and subsequently transferred along the semiconductor surface by another proper clocks (2).”

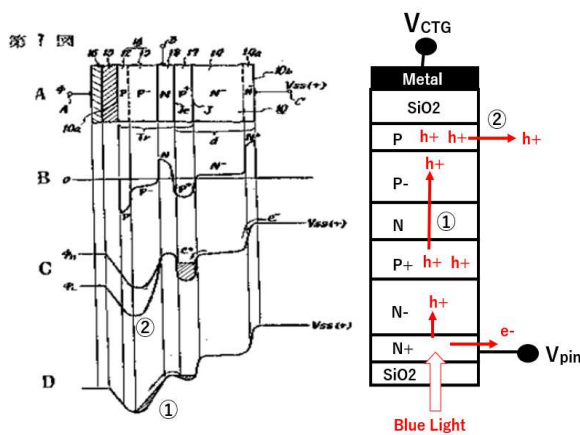


Fig. 5 The N+N-P+NP-N triple junction Pinned Photodiode which is a reproduction of a figure drawn in Japanese patent application JPA1975-127646.

During the photo signal integration time, the output read-out vertical data lines becomes idle. And the excess photo signal charge (holes) is drained out to the output idle read-out data line from the P+ buried charge storage region thru the N base gating region by a strongly attractive voltage on the surface MOS gate, which is also serving as the temporary MOS type dynamic capacitor buffer storage memory. Inherently this triple junction type photo sensor can also be used to drain out the excess photo signal charge by a proper surface MOS gate voltage clocking.

Fig.6 shows another Pinned Buried Photodiode defined in the Japanese patent claim of JPA1975-127647, this time on an N+N-P+N double junction type dynamic photo transistor structure type with Global Shutter Function capability and the electrical shutter capability using the same MOS/CCD type dynamic capacitor buffer storage memory. The English translation is given blow [9].

“ Along the main surface (S) of the semiconductor substrate (Nsub), the charge transfer gate (CTG) is formed on the oxide layer where the charge transfer region (N) of the first conductivity is formed. Along the opposite side of the said semiconductor main surface (S), another region (P) of another conductivity type is formed. With the said first conductivity region (N) a photo sensing structure (NPNsub) is formed. By applying a proper voltage (1) on the said charge transfer gate (CTG) the charge (h+) in the structure (NPNsub) is transferred to the said surface charge transfer region (N). Applying a different voltage (2) on the said charge transfer gate (CTG), the charge (h+) is transferred along the said main surface (S).”

Inherently this double junction type photo sensor can also be used to drain out the excess photo signal charge by a proper surface MOS gate voltage clocking any time by external controls. Only Pinned Buried Photodiode with the in-pixel punch-thru mode VOD function capability can have the electrical shutter function [10] and the no-image-lag feature at the same time to realize fast action video cameras completely free of mechanical parts. This type of back-light CMOS image sensors are now being produced and used in smart phones and many other applications widely after 45 years since the invention in 1975.

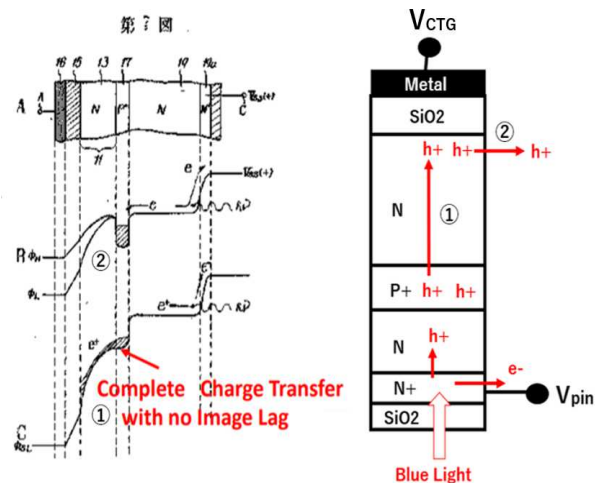


Fig. 6 The N+N-P+N double junction Pinned Photodiode which is a reproduction of a figure drawn in Japanese patent application JPA1975-127647.

As explained in the patent claims of these three Japanese Patent Applications, the proposed double and triple junction type Pinned Buried Photodiodes can be used both in two kinds of Charge Transfer Device (CTD), the analog CCD type CTD and also the modern digital CMOS type CTD image sensors.

Fig.7 shows a reproduction of a PNP double junction type photodiode with an empty potential well of the buried N type storage region which is the result of complete charge transfer and draining action by the adjacent charge transfer device (CTD). Japanese Patent Application JPA1975-134985 defines a PNP double junction dynamic photo transistor structure type Pinned Photodiode in a substrate wafer, consequently forming a P+NPNsub triple junction dynamic photo thyristor type Pinned Buried Photodiode with the VOD function and the electrical function capability. English translation is given below [4].

“In the semiconductor substrate (Nsub), the first region (P1) of the first impurity type is formed, on which the second region (N) of the second impurity type is formed. The photo charge is stored in the second region (N) and is transferred to the adjacent charge transfer device (CTD). Both are placed along the main surface of the semiconductor substrate. A rectifying (P2/N) emitter junction (Je) is formed on the second region (N) while the (N/P1) collector junction (Jc) is formed by the first region (P1) and the second region (N), forming a (P2/N/P1) photo transistor structure in the substrate (Nsub)..”

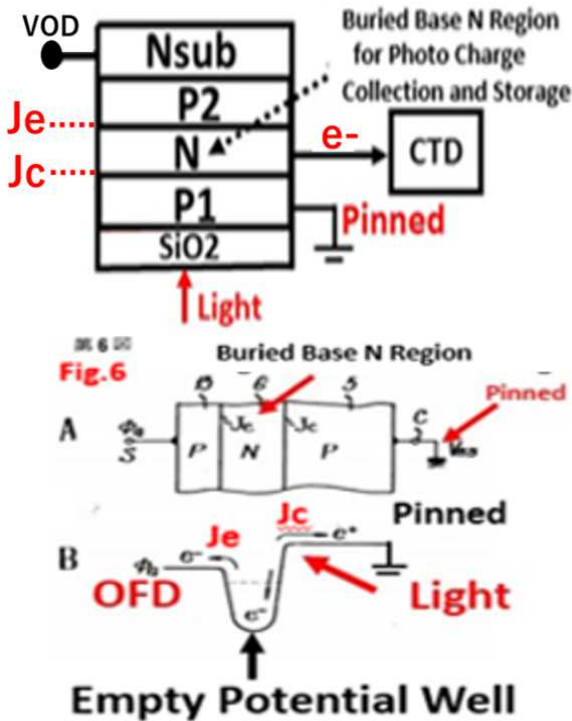


Fig 7 The patent claims in Japanese and an English translation with a reproduction of a figure drawn in Japanese patent application JPA1975-134985 which defined an PNP double junction dynamic photo transistor type Pinned Buried Photodiode with in-pixel overflow draining (VOD) capability.

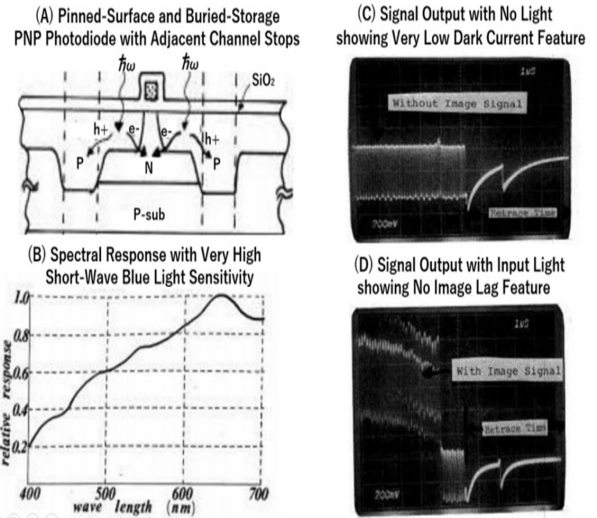


Fig 8 The PNP double junction dynamic photo transistor type Pinned Buried Photodiode reported at SSDM1978 in Tokyo. Sony was working secretly on the critical image-lag problem since 1975 and had no image lag problem completely by 1980 while other companies were suffering image lag problems with the N+P floating-surface single-junction type photo sensor with poor blue light sensitivity.

IV. COOMON MISUNDERSTANDING ON BUIRED PHOTODIODES

In the SSDM1978 paper [5] reported by Hagiwara team at Sony the pinned surface P+P hole accumulation is directly connected with the adjacent heavily doped P+ channel stops which was formed by high energy ion implantation technology rather than by the commonly used LOCOS technology. Thermal oxidation stress was minimized and the image sensor chip-yield was drastically improved by the IR lamp anneal method developed by Kazuo Nishiyama at Sony by suppressing white spot defects and local high surface dark current [11]. This is Pinned Buried Photodiode defined in Fig. 4(d). The P+ Surface is pinned effectively with zero RC delay time. See Fig. 8.

In the IEDM1982 conference, NEC reported the P+NPN-Triple Junction Buried Photodiode without the adjacent P+ channel stops [12] which is the case defined by Fig 4(a). As expected, NEC reported in IEDM1982 the serious image lag. Note the NEC ILT CCD image sensor has the lightly doped P-region with the depletion region isolating the P+ surface region from the substrate with a very high bulk silicon resistivity. The RC delay time cannot be ignored in this case. See Fig. 9.and 10.

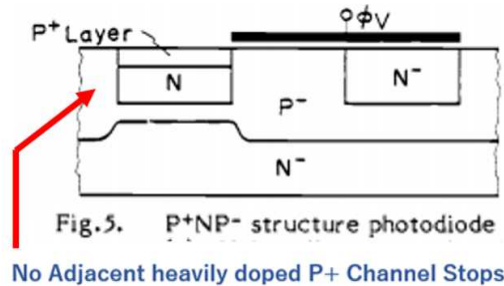


Fig. 9 NEC P+NP- Buried Photodiode reported in IEDM1982

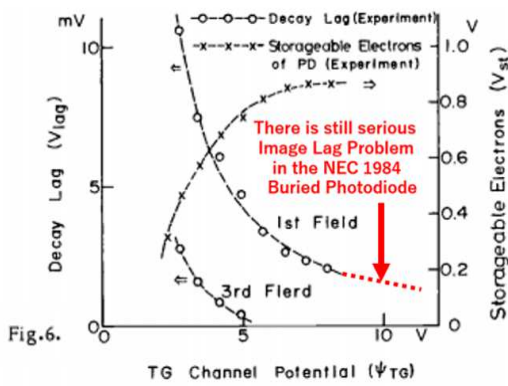


Fig. 10 NEC Buried P+NP-N- Photodiode reported in IEDM1982

NEC explained in details that the buried photodiode can be completely depleted of the photo signal charge resulting the empty potential well and the no-image-lag feature. NEC IEDM1982 paper looked very fresh to these people who were still using the floating surface N+P single junction photodiode for their image sensors. The problem is that NEC IEDM1982 paper neglected the important necessary condition of Pinning the P+ Surface Hole Accumulation region. No matter how heavily the surface P+ region is doped, it becomes floating with the finite RC delay time constant unless the P+ Surface Hole Accumulation region is electrically pinned by a direct metal contact or by an adjacent deep and heavily doped P+ channel stops region. The NEC IEDM1982 paper reported the serious image lag problems. The reason was very clear.

The NEC IEDM1982 paper is based on the NEC Japanese Patent Application JPA1980-138026 [2] filed in 1980 which shows a floating surface potential profiles of the double junction type Buried Photodiode. Since the surface is not pinned, the empty potential becomes floating and the complete charge transfer is not possible with the image lag problem. See Fig. 11. This is the evidence NEC photodiode was NOT Pinned Photodiode. NEC IEDM1982 reports the serious image lag problem as shown in Fig. 9 while the no-image-lag problem was already solved by 1975 in Sony, but Sony kept silent and focused for mass- production and yield-enhancement efforts. In 1984 two years later KODAK reported in IEDM1984 the pinned surface P+ photodiode and named it Pinned Photodiode [13]. See Fig.12. KODAK became the second company who recognized the importance of the pinned surface device.

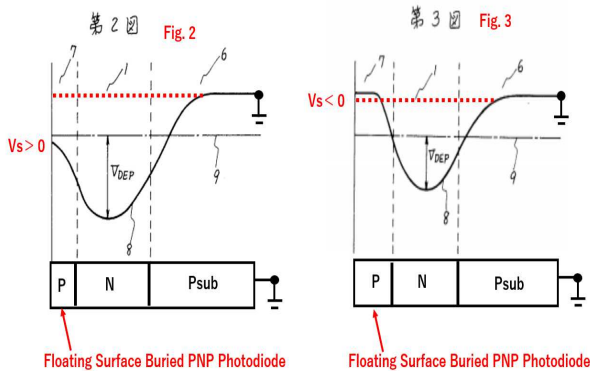


Fig. 11 NEC Patent (JPA1980-138026) on Floating Surface Photodiode

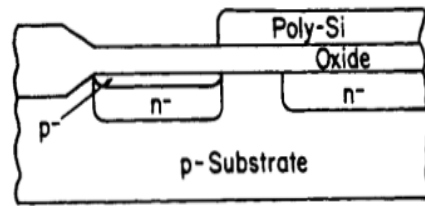


Fig.12 Pinned Surface Photodiode reported in IEDM1984 by KODAK

KODAK named it as Pinned Photodiode and used it in an Interline Transfer CCD type Charge Transfer Device (CTD) for the first time in the world. The importance of the adjacent heavily doped P+ channel stops was recognized which keeps the P+ surface region and the buried N storage region always pinned and kept from being floating. KODAK paper concluded that this photo element is ideal for applications requiring good blue response, large dynamic range, and no image lag. However, NEC IEDM1982 and KODAK IEDM1984 papers did not quote Sony SSDM1978 paper while Theuwissen in his IEDM2005 paper [14] quoted Hagiwara SSDM1978 paper on the PNP double junction type Pinned Buried Photodiode, for the first time in IEEE English speaking community. "This photodiode (Hagiwara developed in 1978) may be considered as the mother of NEC Buried Photodiode, KODAK Pinned Photodiode and Sony Hole Accumulation Diode (HAD)". Mother is a word commonly used for the inventor while Father is a word used for the leader of development efforts.

V. SONY DISCLOSED THE INVENTOR OF SONY HAD SENOSR

In 2020, Sony developed a multi-chip back-light CMOS image sensor based on Hagiwara's original 1975 ideas. Sony then for the first time in the public explained the facts on the original 1975 inventions by Hagiwara in details and the development efforts by Hagiwara Team in 1978 details. Sony official public WEB site [15] said, "In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 JPA1975-134985 applied by Yoshiaki Hagiwara on November 23, 1975)." See Fig. 13.

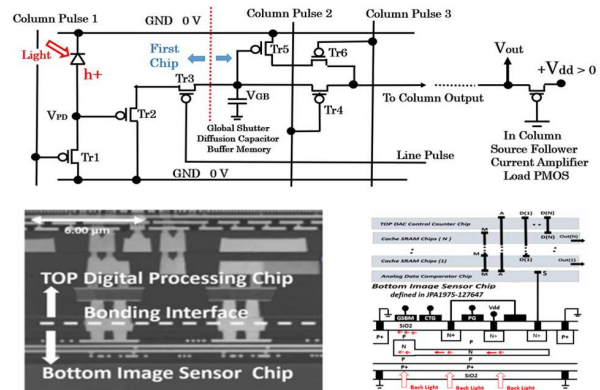


Fig. 13 Active In-Pixel Current AMP 1C6T Circuit (Hagiwara 2020) and Two-chip Stacked Back-Light CMOS Imager (Courtesy of Sony Corporation)

“After that, Sony succeeded in making a principle-prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors [16]." See Fig. 13.

Semiconductor History Museum of Japan [17] quoted, as shown below, the 1975 inventions by Hagiwara and his development efforts reported at the SSDM1978 conference. It said, “In 1975, Sony proposed using a PNP transistor as the photodetector. By providing a P+ layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated to improve the light sensitivity greatly. It was a basic proposal for a pinned photodiode with a P+ layer on the surface of the light receiving part. “. And it said also “In 1978, Sony announced an FT (Frame Transfer) -CCD image sensor, using the photodiode with the same structure. Sony succeeded for the first time in the world in prototyping a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor [18] that developed this technology, in 1981.”.

VI. CONCLUSION

Secret patent disputes and attacks by KODAK, NEC and Fairchild against Sony, on the issues of Hagiwara 1975 invention of Pinned Buried Photodiode with the VOD function capability, lasted for more than 20 years since 1990. But SONY successfully protected Hagiwara 1975 patents. The US supreme court made a final decision favoring Sony over Fairchild [19]. And on June 26, 2020, Sony proudly disclosed that Hagiwara is the true inventor of Pinned Buried Photodiode with the VOD function [15]. Sony and KODAK chose to enjoy a friendly technical collaboration while NEC stopped the imager business.

Besides, this P+PNPP+ double junction type Pinned Buried Photodiode can also be used for a possible future solar cell application for a better quantum efficiency [20]. With the image-lag-free feature and the built-in Electric Shutter and Global Shutter function capabilities [21], the Pinned Buried Photodiode with the in-pixel VOD function and Electric Shutter capability [22] have now replaced film media and mechanical parts, realizing modern solid-state cameras with instant-snapshots and fast-action pictures in our HD digital TV era [23].

ACKNOWLEDGMENT

The author expresses sincere gratitude to Dr. Vojin Vgoklobdzija, Dr. Sei-Ichi Watanabe, Yoshiyuki Kawana, Toshio Kato, Dr. Tsugio Makimoto, Ki-ichiro Mukai, Terushi Shimizu, Yasuhiro Ueda, Dr. Naohisa Ohta, Dr. Tadakuni Narabu and many fellow engineers in Sony who helped me to prepare this paper thru many fruitful discussions. They are my dear friends and mentors in private and public life.

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