III. TRIPLE JUNCTION PINNED BURIED PHOTODIODE

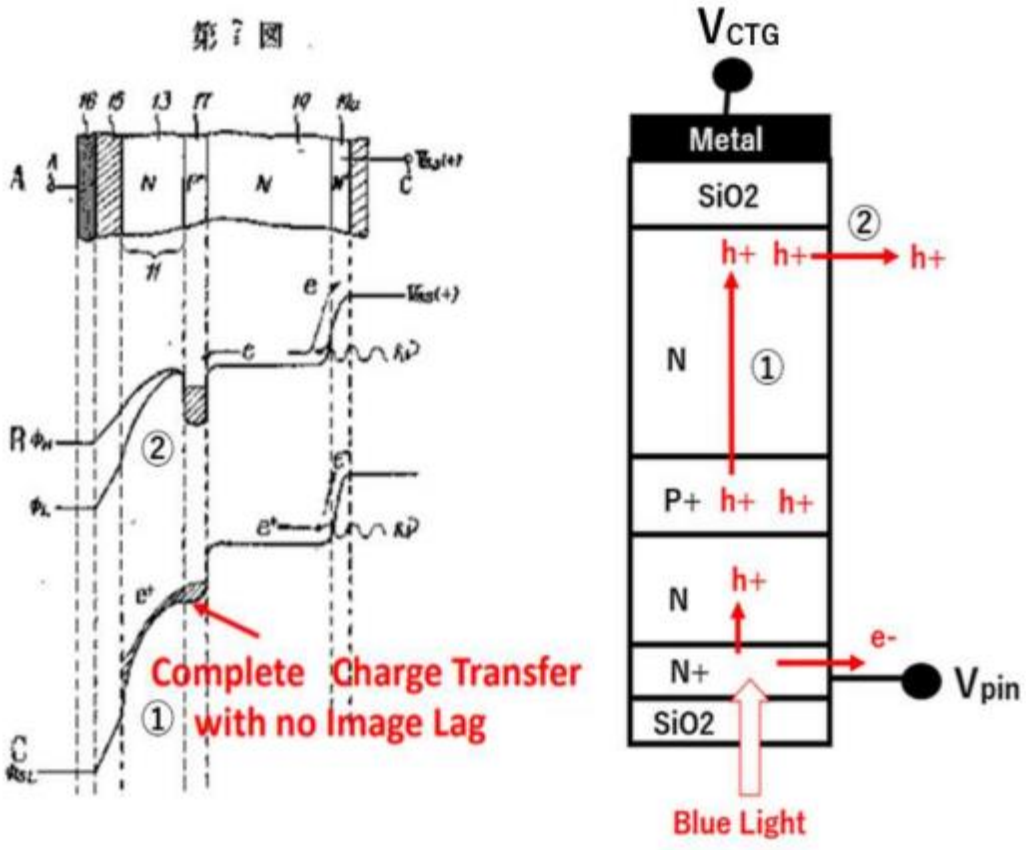

Fig. 6 The N+N-P+N double junction Pinned Photodiode which is a reproduction of a figure drawn in Japanese patent application JPA1975-127647.

During the photo signal integration time, the output read-out vertical data lines becomes idle. And the excess photo signal charge (holes) is drained out to the output idle read-out data line from the P+ buried charge storage region thru the N base gating region by a strongly attractive voltage on the surface MOS gate, which is also serving as the temporary MOS type dynamic capacitor buffer storage memory. Inherently this triple junction type photo sensor can also be used to drain out the excess photo signal charge by a proper surface MOS gate voltage clocking.

Fig.6 shows another Pinned Buried Photodiode defined in the Japanese patent claim of JPA1975-127647, this time on an N+N-P+N double junction type dynamic photo transistor structure type with Global Shutter Function capability and the electrical shutter capability using the same MOS/CCD type dynamic capacitor buffer storage memory. The English translation is given blow [9].

[9] http://www.aiplab.com/JPA_1975_127647_on_NPN_type_PPD.html