III. Triple Junction Pinned Buried Photodiode

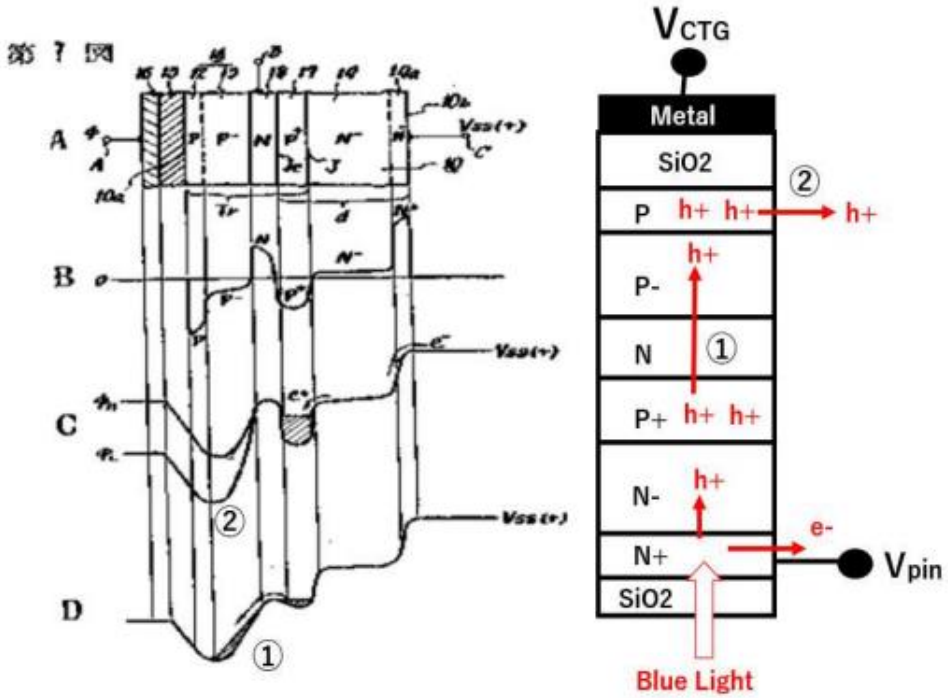

Fig. 5 The N+N-P+NP-N triple junction Pinned Photodiode which is a reproduction of a figure drawn in Japanese patent application JPA1975-127646.

Yoshiaki Hagiwara at Sony in 1975 applied Japanese patent on a triple junction type Pinned Buried Photodiode with the back light illumination scheme. Fig. 5 shows the N+N-P+NP-N triple junction Pinned Photodiode which is a reproduction of a figure drawn in Japanese patent application JPA1975-127646. The English translation is also given blow [8].

"An array of charge transfer gates is formed on the oxide layer of a semiconductor substrate (Nsub). The first charge transfer region (P1) is formed under the oxide layer. There is a base gating region (N) between the first region (P1) and the second photo charge collecting region (P2) which is formed in the substrate (Nsub). By proper gating clocks (1), the photo charge is drained to the surface region (P1) from the second region (P2) and subsequently transferred along the semiconductor surface by another proper clocks (2)."

[8] http://www.aiplab.com/JPA_1975_127646_on_NPNP_type_PPD.html