Proc. of the International Conference on Electrical, Computer and Energy Technologies (ICECET)
9-10 December 2021, Cape Town-South Africa

Pinned Buried PIN Photodiode Type Solar Cell

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***Abstract*— This paper reviews the origin of Pinned Buried Photodiode and its historical development efforts. Three original Japanese Patent Applications filed by Hagiwara at Sony in 1975 are explained in details which defined the first triple junction type Pinned Buried Photodiode with the in-pixel vertical overflow drain (VOD) function with the electrical shutter capability, realizing the completely film-free and mechanical-parts-free all-digital solid-state image sensors. It is shown that the conventional PN junction depletion region is not the only place to have a barrier potential needed for photo electron hole pair separation. A clever doping-engineering of the pinned surface P+P hole accumulation region can also create the surface barrier electric field to enhance drastically the photo electron and hole pair separations to increase the short-wave blue light sensitivity. It is concluded that this surface P+P doping-engineering possibly creates Pinned Buried PIN Photodiode Type Solar Cell with a better quantum efficiency.**

Keywords—Pinned Buried PIN Photodiode, Drift Field Bipolar Transistor, In-pixel Vertical Overflow Drain, Electrical Shutter, Pinned Surface Barrie Potential, Double Junction Solar Cell

I. INTRODUCTION

In this paper three types of photo sensor structures are explained in details. Fig.1 shows the single junction type PIN Photodiode type Solar Cell invented by Jun-Ichi Nishizawa [1]. Fig.2 shows the double junction type Pinned Buried Photodiode type Solar Cell [2] proposed by Yoshiaki Hagiwara in 2020.

Then a new double junction type Pinned Buried P+PNIP+ photodiode Solar Cell is explained in details which is a combination of the PIN Photodiode by Nishizawa and the Pinned Buried Photodiode structure by Hagiwara. It is concluded that this newly proposed double junction type Solar Cell structure is expected to have a higher quantum efficiency.

The classical PIN diode shown in Fig. 1 is a single junction type diode with the undoped intrinsic I-type semiconductor region between the P-type and the N-type semiconductor regions. The P-type and the N-type regions are typically heavily doped to form ohmic contacts. The presence of the wide intrinsic I-type region is in contrast to an ordinary PN diode.

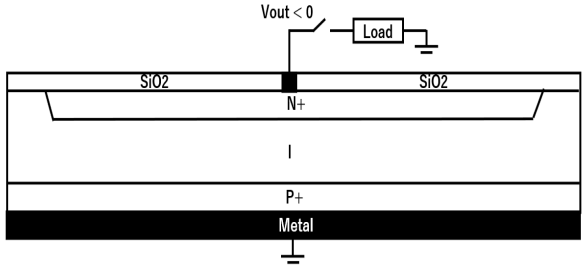

Fig. 1 Single junction PIN photodiode type Solar Cell (Nishizawa 1950)

The typical function of a diode is the rectifying function but the wide intrinsic region makes the PIN diode an inferior rectifier. However, the wide intrinsic I-type region makes it suitable for high-voltage power electronics, attenuators, fast switches, and specially photodetectors applications. See Fig. 1.

Pinned Buried Photodiode now widely used in image sensors is a double or triple junction type photodiode with the buried charge collecting and storage region and with the pinned-surface hole-accumulation region with no surface electric field and with no surface dark current noise [3]. The photo signal charge is transferred and drained from the buried charge storage region with the no-image-lag feature and with the complete charge transfer capability, realizing a digital imaging snapshot camera and a fast action video camera with the electrical shutter function capability [4], free from any film and mechanical parts. Fig. 2 shows the double junction Pinned Buried Photodiode proposed by Yoshiaki Hagiwara in 2020 for a possible future Solar Cell application for a higher quantum efficiency [2].

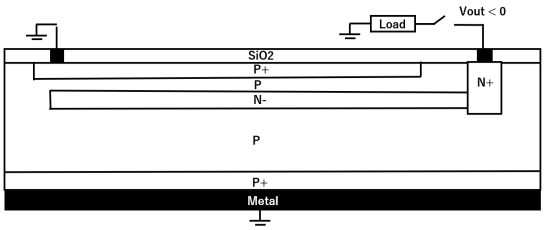

Fig. 2 Double Junction Pinned Photodiode type Solar Cell (Hagiwara.2020)

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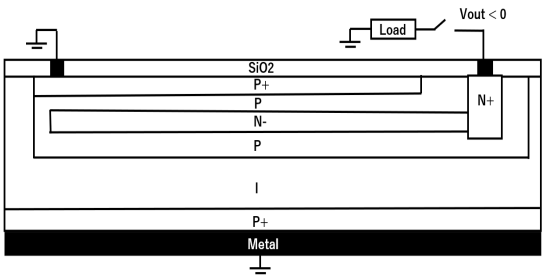

Fig. 3 Pinned PIN Photodiode type Solar Cell (Hagiwara.2021)

Fig. 3 shows the new double junction type Pinned Buried PIN Photodiode used for a possible future Solar Cell application for a higher quantum efficiency. The N- type photo charge collecting buried region is designed to be always completely depleted with an empty potential well. The photo electrons are all directed swiftly to the receiving N+ diffusion storage region connected to the metal output terminal leading to the output load.

II. SINGLE JUNTTION SOLAR CELL

Fig.4 shows a single junction N+NPP+ type photodiode for low cost Solar Cell applications. Both P+ and N+ regions have Ohmic contacts to the connecting metal terminals in both sides. Positive hole charge carriers in the P+ region can exchange the charge by recombination with the negatively charged electrons in the metal by tunneling at the metal/P+ ohmic interface while negatively charged electrons in the N+ region can exchange the charge by moving freely by tunneling at the metal/N+ ohmic interface. There is a PN junction potential barrier in the central PN junction depletion region that can effectively separate the hole and electron pairs generated by the light illumination. The P+P and N+N doping level variations also create the potential barriers for hole and electron pair separations. However, the N+ surface floating potential region is flat with no electric field where the generated hole and electrons pairs in the vicinity of the semiconductor surface stay where they are and eventually they all recombine with each other. So we expect very poor short-wave blue light sensitivity in this N+NPP+ single junction type Solar Cell which is widely used in low cost Solar Cells.

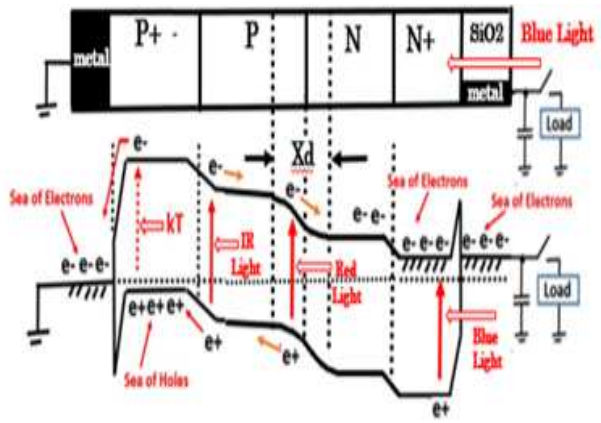

Fig. 4 Single Junction N+NPP+ Photodiode type Solar Cell

III. ORIGIN OF PINNED BURIED PHOTODIODE

Yoshiaki Hagiwara at Sony in 1975 applied three Japanese patents on Pinned Buried Photodiodes [3,5,6]. However, USP and other oversea patents were never applied and the details of his 1975 inventions were never disclosed in the IEEE English speaking community. The original patent claims and the original figures drawn in these three 1975 Japanese patent applications are now reproduced here for the first time in the IEEE English speaking community.

Fig.5 shows the Japanese patent claim of JPA1975-127646 [5], which defined the first Pinned Buried Photodiode patent on an N+N-P+NP-P triple junction dynamic photo thyristor structure type Pinned Buried Photodiode with a Global Shutter function capability using an MOS/CCD type dynamic capacitor buffer photo charge storage memory. During the photo signal integration time, the output read-out vertical data lines becomes idle. And the excess photo signal charge (holes) is drained out to the output idle read-out data line from the P+ buried charge storage region thru the N base gating region by a strongly attractive voltage on the surface MOS gate, which is also serving as the temporary MOS type dynamic capacitor buffer storage memory. Inherently this triple junction type photo sensor can also be used to drain out the excess photo signal charge by a proper surface MOS gate voltage clocking.

Pinned Buried Photodiode invented by Yoshiaki Hagiwara as defined in Japanese Patent Claim of JPA1975-127646 filed on October 23, 1975

特許請求の範囲

半導体基体の一方の主面側に、絶縁膜を介して電荷転送用電極が被着配列される1の導電型の転送領域が形成され、之に対向し且つ之より上記半導体基体の他方の主面側に上記転送領域との間に他の導電型のベース領域を介して受光領域が形成され、上記ベース領域に所定電圧を印加することにより上記受光領域に蓄積した電荷を上記転送領域に転送し、上記電荷転送用電極に所定のクロック電圧を印加して電荷の転送を行うようにしたことを特徴とする固体撮像装置。

Pinned Buried Photodiode shown in Figure 7 in JPA1975-127646 filed on October 23, 1975

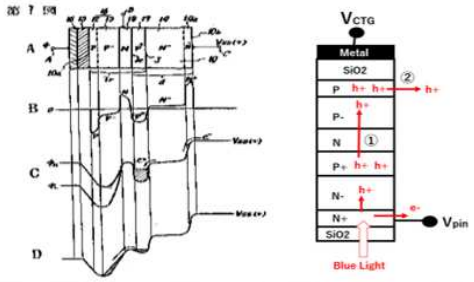

Fig 5 A reproduction of Patent Claim and a figure in JPA1975-127646

This N+N-P+NP-P triple junction type Pinned Buried Photodiode invented by Hagiwara in 1975 has inherently the most important features of the in-pixel vertical overflow drain (VOD) function and the electrical shutter capability needed to realize the completely film-free and mechanical-parts-free modern solid-state digital cameras.

Fig.6 shows the Japanese patent claim of JPA1975-127647 [6], which is also a Pinned Buried Photodiode patent on an N+N-P+N double junction type dynamic photo transistor structure type with the Global Shutter Function capability and the electrical shutter capability using the same MOS/CCD type dynamic capacitor buffer storage memory.

During the photo signal integration time, the output read-out vertical data lines becomes idle. And the excess photo signal charge (holes) can be drained out to the output idle read-out data line from the P+ buried charge storage region thru the base N region with a strongly attractive voltage on the surface MOS gate. Inherently this double junction type photo sensor can also be used to drain out the excess photo signal charge by a proper surface MOS gate voltage clocking any time by external controls.

Only Pinned Buried Photodiode with the in-pixel punch-thru mode VOD function capability can have the electrical shutter function and the no-image-lag feature at the same time to realize fast action video cameras completely free of mechanical parts.

Pinned Buried Photodiode invented by Yoshiaki Hagiwara as defined in Japanese Patent Claim of JPA1975-127647 filed on October 23, 1975

特許請求の範囲

半導体基体の一方の主面側に、絶縁膜を介して電荷転送用電極が被着配列される1の導電型の転送領域が形成され、之より上記半導体基体の他方の主面側に上記転送領域に接する他の導電型の領域と該領域に接する1の導電型の領域とより成る受光領域が形成され、上記転送用電極に所要の電圧を印加することにより、上記受光領域に蓄積した電荷を上記転送領域に転送し、上記電荷転送用電極に上記所要の電圧とは異るクロック電圧を印加して上記基体の上記一方の主面に沿つて電荷の転送を行うようにしたことを特徴とする固体撮像装置。

Pinned Buried Photodiode shown in Figure 7 in JPA1975-127647 filed on October 23, 1975

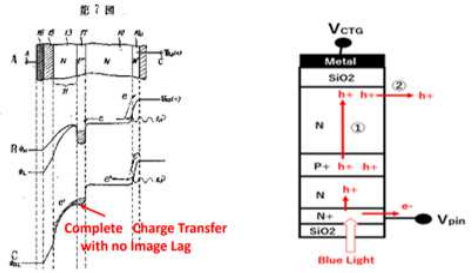

Fig 6 A reproduction of Patent Claim and a figure in JPA1975-127647

As explained in the patent claims of these three Japanese Patent Applications, the proposed double and triple junction type Pinned Buried Photodiodes can be used both in two kinds of Charge Transfer Device (CTD), the analog CCD type CTD and also the modern digital CMOS type CTD image sensors.

.Fig.7 shows the patent claims of Japanese patent application JPA1975-134985 [3], with a reproduction of a PNP double junction type photodiode with an empty potential well of the buried N type storage region which is the result of complete charge transfer and draining action by the adjacent charge transfer device (CTD).As explained in the Japanese patent claims, Japanese Patent Application JPA1975-134985 defines a PNP double junction dynamic photo transistor structure type Pinned Photodiode in a substrate wafer, effectively forming the triple junction dynamic photo thyristor structure type Pinned Photodiode with a VOD function.

The three important features of Pinned Buried Photodiode are (1) the excellent short-wave blue light sensitivity achieved by the very efficient photo electron-hole-pair separation in the presence of the strong surface barrier electric field created by the surface Gaussian P+P hole accumulation doping profile, (2) the very low surface dark current achieved by the pinned and flat surface potential of no surface electric field and (3) the no-image-lag feature achieved as a result of the complete charge transfer capability of Pinned Buried Photodiode as shown by the empty potential well of the pinned and buried charge storage base N region where the photo signal charge are completely drained out to the adjacent charge transfer device (CTD) during the short signal read-out reset period.

Pinned Buried Photodiode invented by Yoshiaki Hagiwara as defined in Japanese Patent Claim of JPA1975-134985 filed on November 10, 1975

特許請求の範囲

半導体基体に、第1導電型の第1半導体領域と、之の上に形成された第2導電型の第2半導体領域とが形成されて光感知部と之よりの電荷を転送する電荷転送部とが上記半導体基体の主面に沿う如く配置されて成る固体撮像装置に於いて、上記光感知部の上記第2半導体領域に整流性接合が形成され、該接合をエミッタ接合とし、上記第1及び第2半導体領域間の接合をコレクタ接合とするトランジスタを形成し、該トランジスタのベースとなる上記第2半導体領域に光学像に応じた電荷を蓄積し、ここに蓄積された電荷を上記転送部に移行させて、その転送を行うようにしたことを特徴とする固体撮像装置。

Pinned Buried Photodiode shown in Figure 6 in JPA1975-134985 filed on November 10, 1975

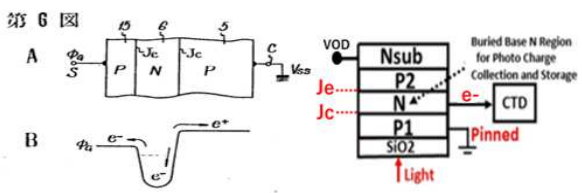

Fig 7 A reproduction of Patent Claim and a figure in JPA1975-134985

Among the three features of Pinned Buried Photodiode, the feature of the excellent short-wave blue light sensitivity is the most important and unique feature of Pinned Buried Photodiode. The excellent short-wave blue light sensitivity is achieved by the very efficient photo electron-hole-pair separation in the presence of the strong surface barrier electric field created by the doping-engineering of the surface Gaussian P+P hole accumulation region within the 50 nm in depth of the surface vicinity in the silicon crystal. This is due to the fact that the short-wave blue light cannot penetrate the silicon crystal surface more than 50 nm in depth. The other two features, the no-image-lag feature and the low surface dark current noise feature, are NOT the unique features of Pinned Buried Photodiode.

CCD has the no-image -lag feature while the single junction N+P floating surface photodiode has the low surface dark current noise feature. However, only Pinned Buried Photodiode has all of the three important features. The charge coupled device (CCD) invented in 1970 already had the no-image-lag feature, which was achieved as a result of the complete charge transfer capability of about 99.999 % charge transfer efficiency in the case of the buried channel CCD type charge transfer device (CTD). The concept of the buried charge storage is also nothing new. We already had the Pinned and Buried MOS dynamic Photo capacitor type CCD image sensors. However the CCD/MOS photo capacitor has a strong surface electric field and inducing the serious surface dark current noise.

On the other hand, the conventional N+P single junction type photodiode with the heavily doped N+ floating surface has a floating but a flat surface potential with no surface electric field and suffers no serious surface dark current noise. However, the N+ floating surface causes the incomplete charge transfer RC delay time of the charge transfer gate and the serious image lag.

The single junction N+P photodiode does not have the metal electrode on the top and it seems that it may have a very good light sensitivity. But the truth is not the case. See Fig. 4 again. The surface heavily doped N+ region has a floating and flat surface potential with no surface electric filed to separate the hole electron pairs generated at the silicon surface vicinity within 50 nm in the silicon crystal in depth. Hence most of the electron and hole pairs generated by the short-wave blue light cannot be separated and eventually recombined again to become heat. None of the pairs can contribute to the photon energy to the electron energy conversion, resulting a very poor quantum efficiency. Table I summarizes these discussions.

TABLE I. HISTORICAL PHOTOSENSOR DEVELOPMENT EFFORTS

Three important Features \ Three types of Photo Sensing Devices	1 N+P Single Junction Photodiode with Floating N+ Surface	2 Charge Couple Device CCD/MOS Dynamic Photo Capacitor	3 P+NP Double Junction Dynamic Photo Transistor Pinned Buried Photodiode
1 Image Lag Problem	Serious Image Lag Problem	No Image Lag Problem	No Image Lag Problem
2 Surface Dark Current Noise	No Surface Dark Current Noise	Serious Surface Dark Current Noise	No Surface Dark Current Noise
3 Short-Wave Light Sensitivity	Poor Short-Wave Light Sensitivity	Very Poor Short-Wave Light Sensitivity	Excellent Short-Wave Light Sensitivity

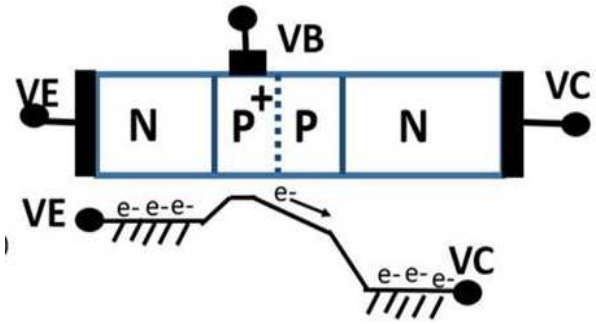

Fig. 8 Drift Field Transistor with the base barrier electric field formed by the P+P base doping-engineering for high frequency operations.

IV. SURFACE BARRIER FIELD FOR BLUE-LIGHT SENSITIVITY

The drift-field transistor, invented by Herbert Kroemer in 1953 [7], has a graded base. See Fig. 8. The graded base. was formed by diffusing the base dopant in a clever way. Having a doping-engineered electric field in the graded base, a higher doping concentration is formed near the emitter reducing towards the collector, resulting in a high-speed bipolar junction transistor with the reduced charge carrier base transit time. Hagiwara in 1975 used P+P doping engineering to enhance the short-wave blue light sensitivity in Pinned Buried Photodiodes.

Fig.9 is a reproduction of figures reported in the SSDM1978 paper [8]. A very high quantum efficiency with an excellent short-wave blue light sensitivity was achieved in the PNP double junction Pinned Buried Photodiode developed in 1978 by Hagiwara team at Sony. The pinned buried region is always completely depleted of photo electrons. Photo electrons are directed and removed very swiftly to the adjacent charge storage region acting as the receiving storage bucket for electrons.

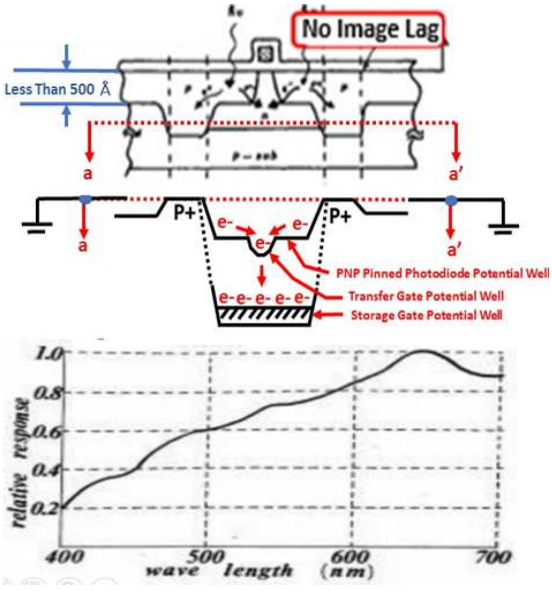

Fig. 9 Spectral Response of Pinned Buried Photodiode, reported at SSDM1978 in Tokyo. Sony had no image lag problem by 1980 using first all-CCD process and then this PNP Double junction Photo Transistor Process while all other companies suffered image lag problem with the N+P floating-surface single-junction type photo sensor with poor blue light sensitivity.

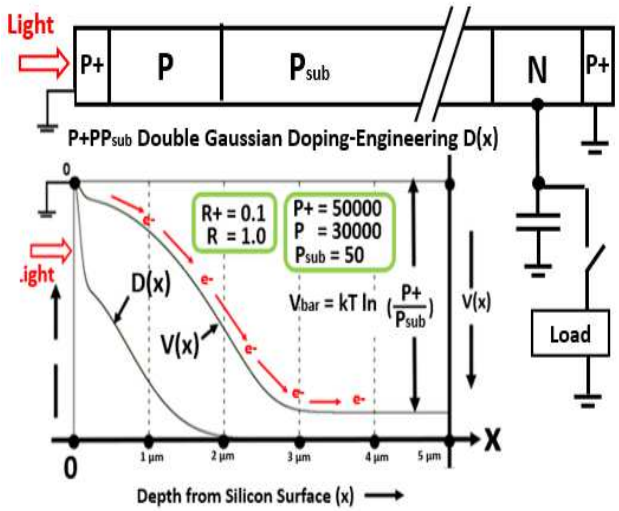

Fig. 10 Exact Numerical Computation of P+P Surface Barrier Potential V(x)

The P+ surface hole accumulation region must be directly connected with an adjacent external direct metal contact as an option as originally defined by Hagiwara in 1975 Japanese patents or with an adjacent heavily doped P+ channel stops which is formed by high energy ion implantation technology rather than by LOCOS technology. Thermal oxidation stress was minimized in order to suppress generation of white spot defects and local high surface dark current for better wafer yield.

Fig. 10 shows an exact numerical computation of the P+P surface barrier potential V(x) for a two-step double doping-engineering of the double Gaussian doping D(x) with the spread parameters R+ = 0.1µm and R = 1µm. The substrate doping level is taken as Psub = 50 μm^{-3} while the two-step double Gaussian peak surface doping levels are taken as P=3000μm^{-3} and P+=5000μm^{-3} . The surface barrier electric field was found to be extending up to 3µm in depth into the silicon crystal. Thus by a proper surface double doping-engineering D(x) with the high energy ion implantation technology an ideal surface barrier electric field can be achieved to separate efficiently the electron and hole pairs generated by the short-wave blue light, which cannot penetrate more than 50 nm in depth in the silicon crystal. In this way, the ideal spectral response was achieved for the PNP double junction type Pinned Buried Photodiode. See the spectral response of the PNP double junction type Pinned Photodiode shown in Fig. 9 which is a reproduction of a figure reported in Hagiwara SSDM1978 paper [8] .

V. Pinned Buried PNIP Photodidoe Type Solar Cell

Image sensors and solar cells both operate by the same physical principle of converting the photon energy to the electron energy. Pinned Buried Photodiode has an excellent quantum efficiency and is also expected to improve the quantum efficiency of Pinned Buried Photodiode type solar cells. PIN diode invented by Jun-Ichi Nishizawa is also a simple photodiode with the wide intrinsic I-type middle region. PIN diode is suitable for high-voltage power electronics, fast switches and photodetectors applications. The floating surface N+P single junction-type photodiode is now used widely in solar cells because of its simple structure and the cost performance consideration, but with a poor low quantum efficiency problem.

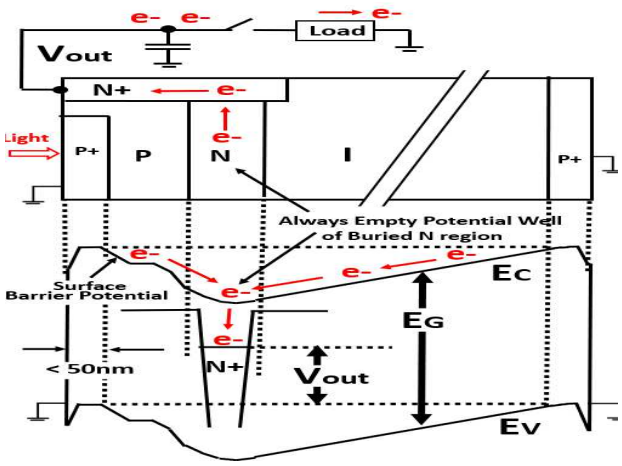

Fig. 11 Pinned Buried P+PNIP+ Photodiode Structure type Solar Cell

The Pinned Buried PNIP Photodiode type Solar Cell shown in Fig.11 has a receiving charge storage bucket of a heavily-doped N+ region for the ohmic contact connecting the output power line which is connected via the output switch to the solar cell load. The output voltage of a single solar cell unit is less than the silicon energy gap E_G of 1.1 eV but the total output voltage can be boosted by connecting many of the solar cell units in series.

Note that there is a constant electric field and no bending in the electron potential Ec in the intrinsic region. The right edge P+ region has a very small depletion region to absorb the constant electric field in the intrinsic region.

If Pinned Buried Photodiode and PIN diode are combined, we may have a solar cell with a better performance but still keeping the structure relatively simple. Fig. 12 shows two units of Pinned Buried PIN photodiode structure in serios to boost the output voltage. This triple junction Solar Cell can be integrated and connected in series on one single chip. The conventional N+P floating surface single junction type low-cost Solar Cells require a very complex and advanced packaging technology.

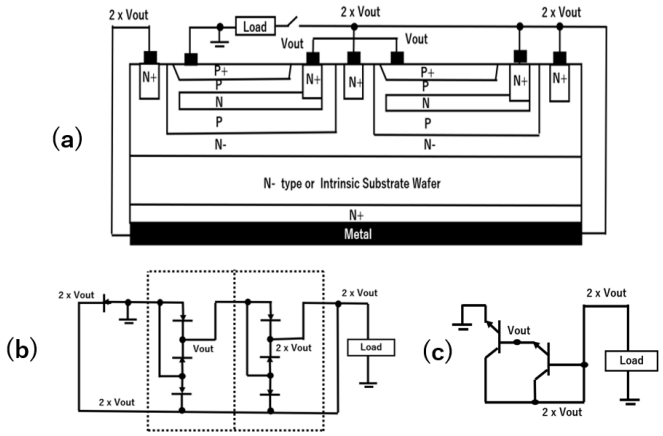

Fig. 12 (a)Two Units of Triple Junction Pinned Buried P+PNPIP+ Photodiode type Solar Cells in series with (b) a diode circuit formation and (c) a two- photo-transistor formation which can be fabricated by Bipolar Tr Process.

VI. Future of Pinned Photodidoe and Solar Cell

Fig. 13 shows a cross sectional view of a back-illuminated CMOS Image Sensor and a new 3D multichip CMOS image sensor configuration for flash image acquisition [12,13,14] used in a 3D multichip CMOS image sensor, utilizing a newly developed Cu-to-Cu direct contact technology by Sony [15].

In summary, the most important feature of Pinned Buried Photodiode is the short-wave blue light sensitivity. Sun light has a great amount of short-wave blue light energy. Pinned Buried Photodiode type solar cell is similar to a very efficient rain-drops collecting system of a mountain hill and a valley with a storage dam while the simple N+P single junction type conventional solar cell is like collecting rain-drops at the open sea where most of rain drops are wasted. See Fig.14.

VII. Conclusion

The origin of Pinned Buried Photodiode was reviewed and its historical development efforts were discussed. As has been proposed in Hagiwara 1975 patent applications, a clever doping-engineering of the surface P+P hole accumulation region can also create the surface barrier electric field to enhance drastically the short-wave blue light sensitivity. It is concluded that this surface P+P doping-engineering is a key to create Pinned Buried PIN Photodiode Solar Cell with a better quantum efficiency.

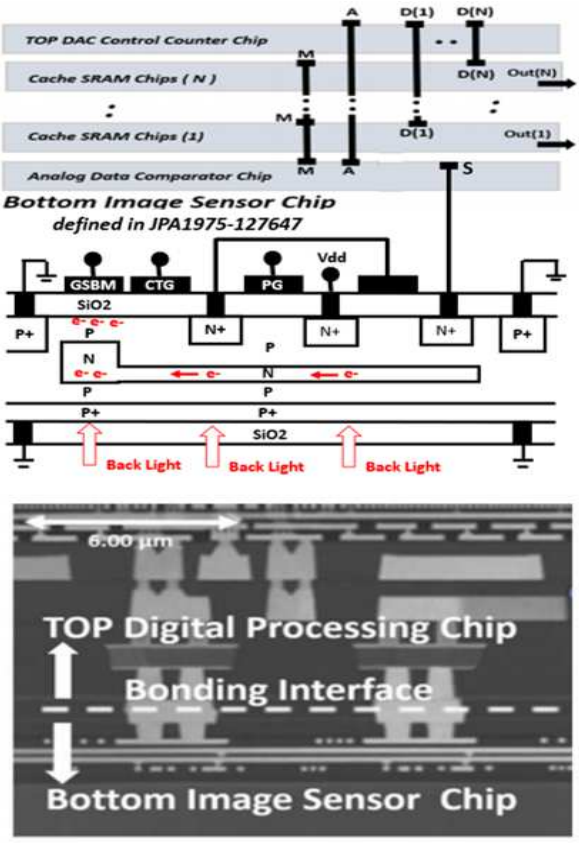

Fig. 13 Cross Sectional View of two-chip stacked back-illuminated CMOS Image Sensor (Curtesy of Sony Corporation) and the future 3D Multichip CMOS Image Sensor Structure using P+PNP junction Pinned Buried Photodiode.

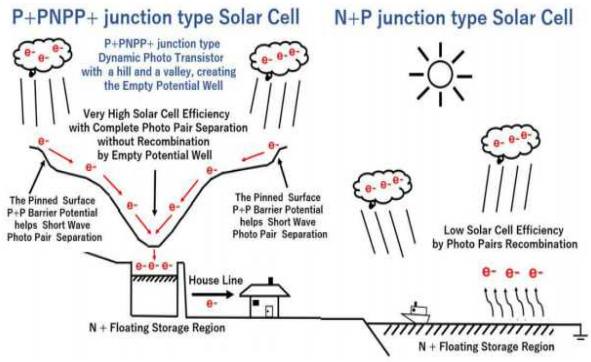

Fig. 14 Analogy of rain drops and photo electrons under the sunshine.

Acknowledgment

The author expresses sincere gratitude to Dr. Vojin Vgoklobdzija, Dr. Sei-Ichi Watanabe, Yoshiyuki Kawana, Toshio Kato, Dr. Tsugio Makimoto, Ki-ichiro Mukai, Terushi Shimizu, Yasuhiro Ueda, Dr. Naohisa Ohta, Dr. Tadakuni Narabu and many fellow engineers in Sony who helped me to prepare this paper thru many fruitful discussions. They are my dear friends and mentors in private and public life.

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