V. PINNED BURIED PNIP PHOTODIDOE TYPE SOLAR CELL

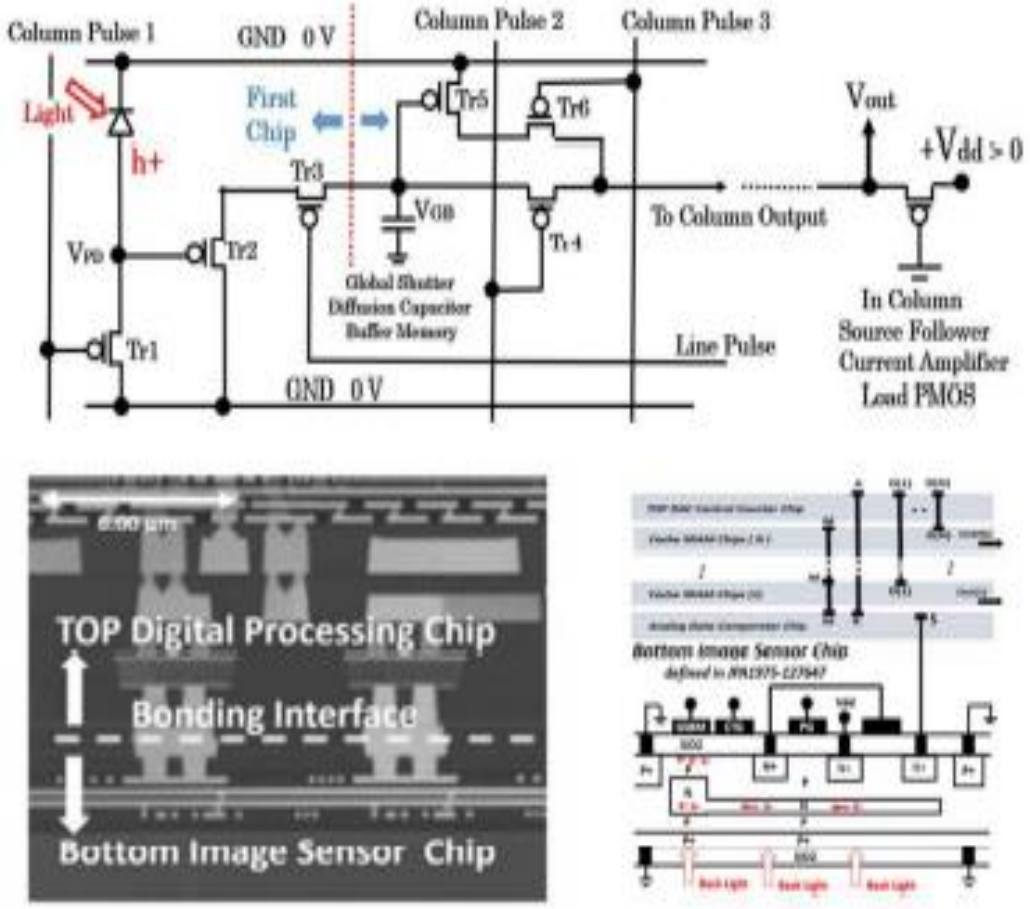

Fig. 13 Active In-Pixel Current AMP 1C6T Circuit (Hagiwara 2020) and Two-chip Stacked Back-Light CMOS Imager (Curtesy of Sony Corporation)

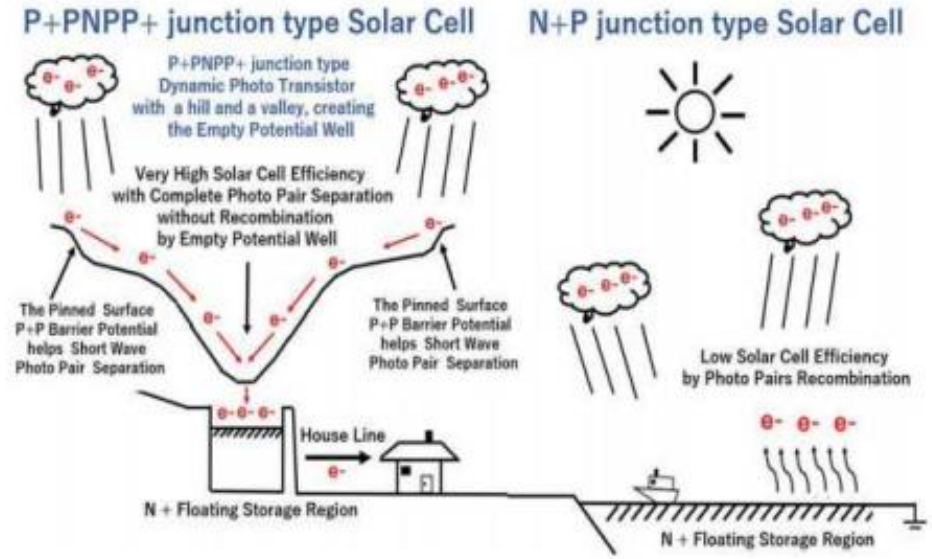

Fig. 14 Analogy of rain drops and photo electrons under the sunshine.

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[14] Y. Hagiwara,"Electrostatic and Dynamic Analysis of P+PNP Double Junction and P+PNPN Triple Junction Pinned Photodiodes",Inter. Jour.of Sys. Sci. and Appl. Math. Vol. 6,Issue 2,June 2021,PP.55-76.

[15] Taku Umebayashi, Hiroshi Takahashi, Reijiro Soji, Japanese Patent No. 5773379 (JPA2014-260268), on the Cu-to-Cu direct contact technique to achieve the 3D stacked multi-chip LSI system (2014).