http://www.koueki.jiii.or.jp/innovation100/

http://www.koueki.jiii.or.jp/innovation_detail.php?eid=00059&test=open&age=stable-growth

戦後日本のイノベーション100選

公益社団法人 発明協会 Japan Institute of Invention and Innovation

本事業について　イノベーション100選　関係者インタビュー　お問合せ・その他

HOME > イノベーション100選 > 安定成長期 > イメージセンサー（CCD・CMOS）

イノベーション100選　トップ10　戦後復興期　高度経済成長期　安定成長期　現代まで　印刷

安定成長期

イメージセンサー（CCD・CMOS）

概要　イノベーションに至る経緯　発明技術開発の概要　主な受賞歴　参考文献等

概要

撮像デバイスの研究開発は、19世紀後期のテレビジョン研究がスタートである。機械式、撮像管、固体撮像素子（以下「イメージセンサー」と呼ぶ）と発展し、社会に大きなインパクトを与えつつ、大きく発展してきた。

真空管の一種である撮像管は、サイズが大きい、割れ物である、消費電力が大きい、画像にゆがみがある、高価である、などの欠点があり、固体化が望まれていた。1960年代半ばにイメージセンサーの開発がスタートした。そのときは、ＭＯＳ（Metal Oxide Semiconductor）型が中心であった。

1970年にBoyleとSmith（当時Bell研究所）がＣＣＤ（Charge-Coupled Device、電荷結合素子）を発表した[1]。構造が単純であり、イメージセンサーのような大規模なアレイ構造を製造するのに適していること、矢継ぎ早にＣＣＤに改善が加えられたことから、イメージセンサー開発の中心はＣＣＤになった。1970年後半からは開発の中心は日本に移った。1978年、山田哲生（当時 東芝）は、強い光が入射したときに縦線の偽信号を発生させるブルーミングを抑制する縦型オーバーフロードレイン構造を発明した[2]。1979年には寺西信一（当時 ＮＥＣ）が、白傷や暗電流を大幅に低減し、残像や転送ノイズを解消する埋込フォトダイオード（Pinned Photodiode）を発明した[3]。これらの結果、ＣＣＤはまずムービーを、引き続きコンパクトデジタルスチルカメラを主な市場として量産されていった。

1990年代になると、CMOSの微細化が進み、4個ほどのトランジスターを画素内に配置することが可能になり、さらに

1990年代になると、CMOSの微細化が進み、4個ほどのトランジスターを画素内に配置することが可能になり、さらには、埋込フォトダイオードをCMOSイメージセンサーに適用することでＣＣＤと同等以上の低ノイズが達成でき、世界の多くの機関で熱心に開発が進められた。2000年に米田智也ら（当時 キヤノン）が、強い光が入射したときに発生するシェーディングを抑制する構造を発明した[4]。2001年に鈴木亮司ら（当時 ソニー）が、裏面照射型に関する発明をした[5]。これらの技術開発によりCMOSイメージセンサーが主役になり、低消費電力という特性のお陰もあり、携帯電話に搭載され、生産量を爆発的に増加させていった。2010年に梅林拓ら（当時 ソニー）が、イメージセンサーに画像処理回路を積層する構造を発明し[6]、高速化と多機能化を飛躍的に推し進めた。

2014年には携帯電話用を中心に約38億個もの生産が行われた。パソコンカメラ、デジタルスチルカメラ、ゲームなどのコンシューマー用途、監視用、車載用、放送用カメラなどの社会インフラとして、さらには医療、科学用などあらゆる

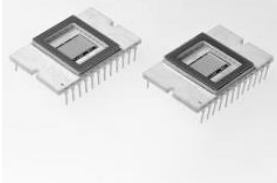
参考文献等

1. W. S. Boyle and G. E. Smith 「Charge Coupled Semiconductor Devices」, The Bell System Technical Journal, vol.49 (1970) pp.587-593
2. 山田哲生「固体撮像装置」特開昭54-95116、1978年1月13日出願
3. 寺西信一　外「固体撮像装置」特開57-62557、1980年10月2日出願
4. 米田智也　外「固体撮像装置」特開2001-230400、2000年11月30日出願
5. 鈴木亮司　外「X-Yアドレス型固体撮像素子およびその製造方法」特開2003-31785、2001年7月11日出願
6. 梅林拓　外「半導体装置とその製造方法、及び電子機器」特開2015-65479、2010年1月22日原出願

イノベーション100選

トップ10（年代順）
- 内視鏡
- インスタントラーメン
- マンガ・アニメ
- 新幹線
- トヨタ生産方式
- ウォークマン®
- ウォシュレット®
- 家庭用ゲーム機・同ソフト
- 発光ダイオード
- ハイブリッド車

戦後復興期（年代順）
高度経済成長期（年代順）
安定成長期
現代まで
一覧を見る



（画像提供：ソニー

萩原良昭の特許出願と関連学会発表資料

1）萩原良昭　特許出願　JPA 1975-127646 裏面照射型N+NPNP接合型　Pinned Photodiode
2）萩原良昭　特許出願　JPA 1975-127647 裏面照射型N+NPN接合型　Pinned Photodiode
3）萩原良昭　特許出願　JPA 1975-134985 OFD機能付きPNP接合型　Pinned Photodiode
4）萩原、阿部、岡田、日本応用物理学会主催個体素子国際学会SSDM1978 Paper@Tokyo, 1978

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

1975-85

Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

~ Discrete Semiconductor/Others ~

In 1975, Sony proposed using a PNP transistor as the photodetector [3]. By providing a P+ layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated to improve the light sensitivity greatly. It was a basic proposal for a pinned photodiode with a P+ layer on the surface of the light receiving part.

Next, proposals were made separately by Hitachi and Sony to use the P+ layer as the substrate potential. In 1977, Hitachi presented a structure in which the high-concentration surface P+ layer is connected to a P-type substrate (well) and pinned it to the same potential as the substrate to increase the charge storage capacity and widen the dynamic range of the photodiode [4]. In 1978, Sony announced an FT (Frame Transfer) -CCD image sensor, using the photodiode with the same structure [5]. Sony succeeded for the first time in the world in prototyping a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor that developed this technology, in 1981 [6].

Photodiodes are used for photodetectors of image sensors. In 1987, Sony developed a 2 / 3-inch, 380,000-pixel CCD image sensor using a new type of photodetector, now called a Pinned Photodiode (Sony named it HAD: Hole Accumulation Diode) [1], and installed it in the 8mm VTR integrated video camera "CCD-V90". In the 1990s, the era of passport size video cameras demands compact CCD image sensors with large numbers of pixels (1/2 inch or smaller with 400,000 pixels or more).

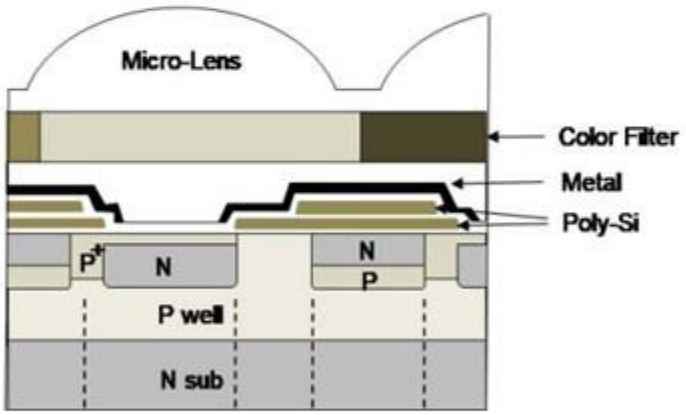


Fig-1 Cross-sectional structure of the IT-CCD image sensor (surface irradiation type)

References:

【1】M. Hamasaki, T. Suzuki, Y. Kagawa, K. Ishikawa, K. Miyata and H. Kambe, "An IT-CCD imager with electronically variable shutter speed" , Technical Report of The Institute of Image Information and Television Engineers. vol. 12, no. 12, pp. 31-36, (1988)

【3】Y. Hagiwara, Japanese Patent JP1975—134985

【4】N. Koike, I. Takemoto. Japanese Patent JP1977—837

【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

【6】I. Kajino, M. Shimada, Y. Nakada, Y. Hirata and Y. Hagiwara, "Single Chip Color Camera Using Narrow channel CCD Imager with Over Flow Drain"、Technical Report of The Institute of Image Information and Television Engineers、vol. 5, no. 29, pp. 32-3S, (1981)

The Photodiode of JP1977-837 is Not Pinned Photodiode !

https://www.sony.com/en/SonyInfo/News/notice/20200626/

Sony's Representative Inventions Supporting Stacked Multi-Functional CMOS Image Sensors

Sony Corporation
Sony Semiconductor Solutions Corporation

Taku Umebayashi, an employee of Sony, was awarded the Purple Ribbon Medal in the 2020 Spring Conferment of Medals of Honor. The Purple Ribbon Medals honor influential characters with their outstanding achievement in inventions and discoveries in the field of science and technology, and in the academic, sports, and arts and cultural fields. The medal was awarded to Mr. Umebayashi in appreciation to his achievement in the development of stacked multi-functional CMOS image sensors. His achievement in research and development had already received the Prime Minister Award of the National Commendation for Invention in 2016, and also with recommendation from the Japan Institute of Invention and Innovation ("JIII"), he received the Awards for Science and Technology (Development Category) of the Commendation for Science and Technology by the Minister of Education, Culture, Sports, Science and Technology in 2018. JIII had also recommended Mr. Umebayashi for the Purple Ribbon Medals.

Provided below are explanations of stacked multi-functional CMOS image sensors and Sony's notable inventions which support them.

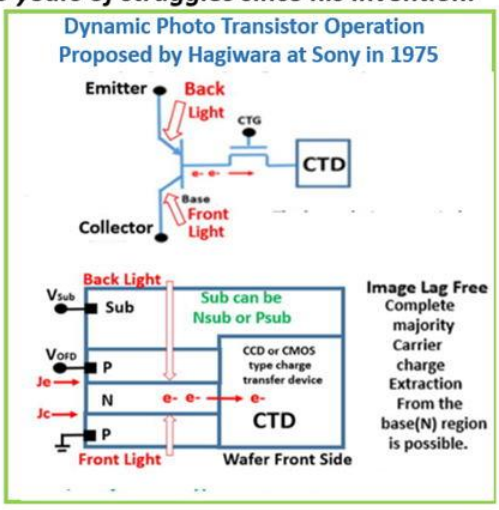
Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

Finally the Sony-Fairchild Patent Wat(1991-2000) ended over the Sony HAD Sensor which is identical to the P+NPNsub junction type Pinned Photodiode with Vertical Overflow Drain, originally invented by Hagiwara at Sony in 1975.

And finally Hagiwara received for his 1975-134985 Japanese Patent officially , the First Patent Award from Mr. Ando, Sony president in April, 2001 after more 26 years of struggles since his invention.



●Prof. Albert Theuwissen は　IEDM2005 の招待論文 “ The Hole Role” で、萩原の SSDM1978 の論文を初めて引用した。萩原が 1975 年に発明し、萩原自身が開発し、SSDM1978 の学会で論文発表した　P+NPNsub 接合型受光素子が NEC の埋込み Photodiode と KODAK の Pinned Photodiode と SONY の Hole Accumulation Device の生みの親(Mother)ではないかと賞賛した。Mother とは「生みの親」を意味し、発明者に対する最高の賞賛の言葉である。開発者を賞賛する「育ての親」を意味する父(Father) に対応する言葉が母(Mother)である。

Albert J.P. Theuwissen, Jan T.J. Bosiers, Edwin Roks, “ The Hole Role “,
an invited paper at IEDM2005, Washington DC, Techn. Dig. , 2005.

But in the case that parts of the depleted n-type CCD channels are not covered by gate material, their surface potential is undefined ! Such a structure will suffer from charge transport issues during operation, because charge can be trapped in local potential pockets. The effect can be solved by defining the potential in the open areas through an extension of the p^+ channel stopper. A simple self-aligned implant of $2x10^{13}$ /cm^2 boron ions is sufficient to extend the channel stop areas to the gate edge and consequently fix the potential in the open areas [2]. The result after this self-aligned implant is shown in Figure 3. The presence of enough holes plays a crucial role in fixing the potential for the regions “beyond control” of the gates. (Is this structure the mother of the pinned-photodiode or buried diode or hole-accumulation device ?)

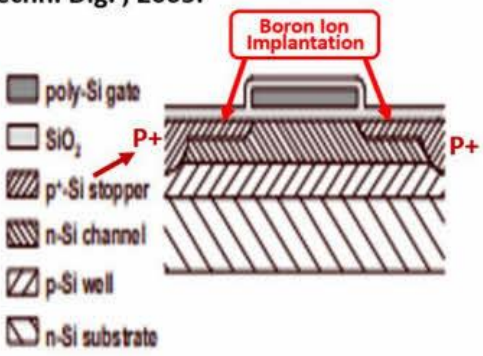


Figure 3. Cross section of a buried-channel CCD on n-Si substrate including light windows and pinned interface potential in the non-covered CCD channels (the cross section is made perpendicular to the CCD channel).

[2] Y. Daimon-Hagiwara et.al., Proc. 10th Conf. on Solid-State Devices, Tokyo, 1978, pp.335-340,

●Eric R. Fossum, Donald D. Hondongwa, “A Review of the Pinned Photodiode for CCD and CMOS Image Sensors,” IEEE Journal of the Electron Devices Society, Vol. 2, No. 3, 2014.

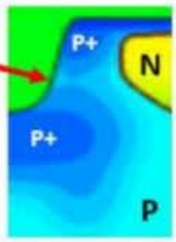
この 2014 年の Fossum の論文の中で、不正確の理解から、萩原の 1975 年の特許と 1978 年の論文には「残像の関する記述がない」と、攻撃しているが、事実無根である。論文に示されている図が間違っている。PPD の発明は寺西であると結論づけているが、攻撃とその結論は間違った理解からなされていると判断される。

Fossum insulted in his 2014 paper Sony and Hagiwara 1975 PPD invention.

Indeed, Hagiwara invented PPD with VOD and the virtual charge transfer in 1975 !!

Sony HAD (PPD+VOD) does not use LOCOS !!!

The surface P+ layer is NOT connected to the LOCOS P+ layer. The surface P+ layer may be floating and this photodiode may have serious image lag.



IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY, VOL. 2, NO. 3, MAY 2014

A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, *Fellow, IEEE*, and Donald B. Hondongwa, *Student Member, IEEE*

Many people now said this is a fake paper !

False

False

C. Other Contributions to the PPD Invention

The PPD structure, while invented for low lag ILT CCD application, shares a strong resemblance to the Hynecek virtual-phase CCD structure, with the exception of the VOD. The two inventions were solving different problems with essentially the same device structure and operating principles.

In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a *pnp* vertical structure was disclosed, among several structures [24]. The top *p* layer was connected by metal to a bias used to control full-well capacity and the *n*-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1996, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called “Hole Accumulation Diode,” or HAD structure [25]. However, the 1975 application did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the NEC paper was published. However, the “narrow-gate” CCD with an open *p*-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

The PPD, as it is most commonly used today, bears the strongest resemblance to the Teranishi et al. ILT CCD device. Thus, these days Teranishi is considered as the primary inventor of the modern PPD [29].

Serious Image Lag ?

NOT connected

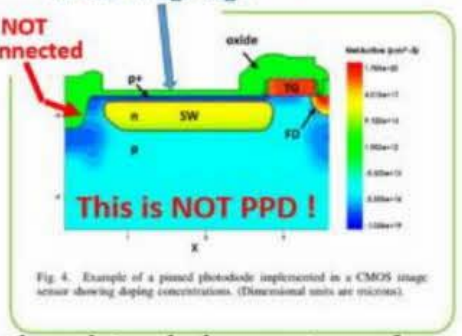


Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

Hagiwara in 1975 invented PPD with VOD and the virtual charge transfer.
Study the Japanese Patents 1975-127646, 1975-127647 and 1975-134985.

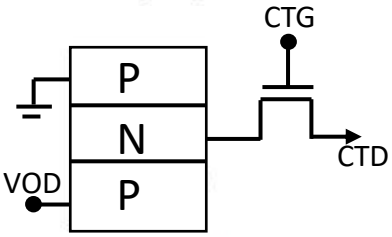
Pinned PhotodiodeとBuried Photodiodeの違いは一般にはいまだに理解されていない。

ELECTRICAL ENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode



In 1975 the first PPD was invented by Hagiwara at Sony and used in ILT CCD PDs by Hamazaki at Sony in 1987.

PPD must have the P+ channel stops nearby to pin the surface P+ layer.

This is a commonly misunderstood misused set of terminologies.

First off these are not PIN Photodiodes - which stands for P - Intrinsic- N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though.

Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space.

You can get surface state pinning from the dangling Si/SiO2 bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The Si/SiO2 surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface.

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

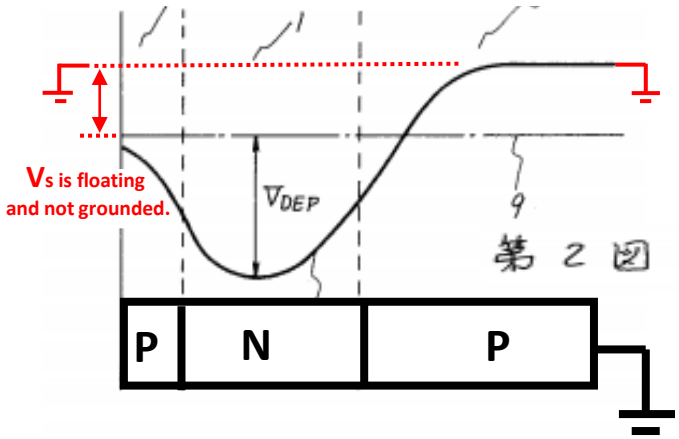
NEC1980年出願特許が　Pinned Photodiodeに関する特許でない証拠は図２と図３から自明である。

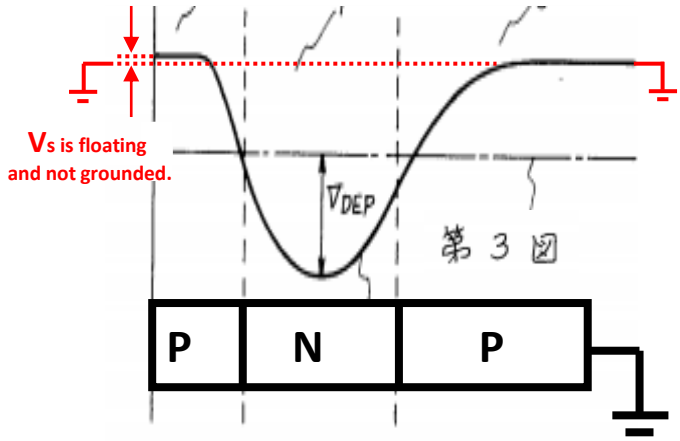
表面P+濃度が濃いだけでは表面はピン留めされない。

実施例図２は表面濃度が薄い場合を示すが
表面電位は固定されておらす浮遊している。

実施例図３は表面濃度が濃い場合を示すが
表面電位は固定されておらす浮遊している。

「図２と図３の違いは表面Ｐ層の濃度である」と特許の説明文に記載されている以外は同一構造。



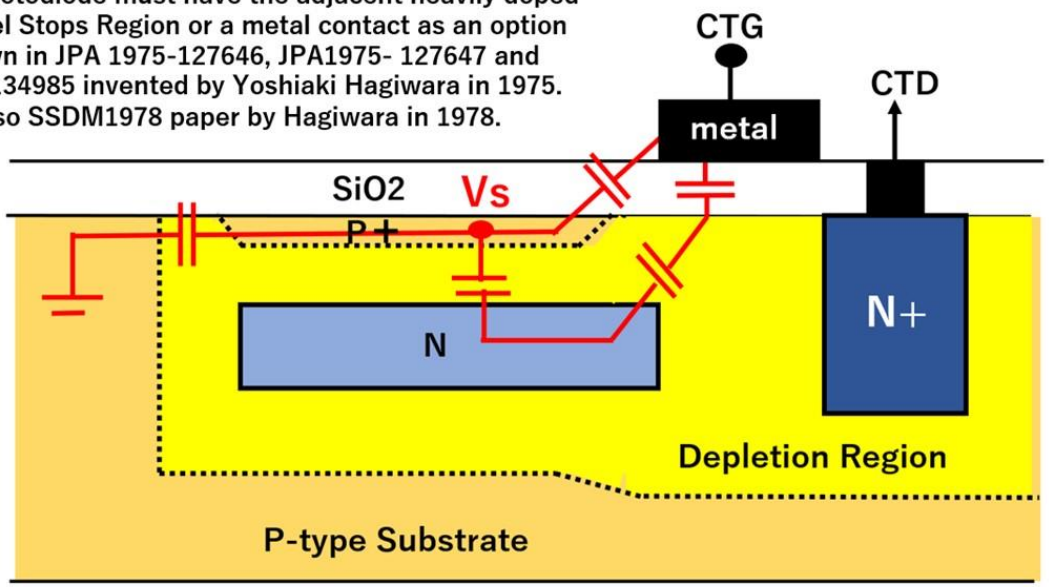


In both figure 2 and 3, the surface potential Vs is not exactly at the substrate grounded voltage level.

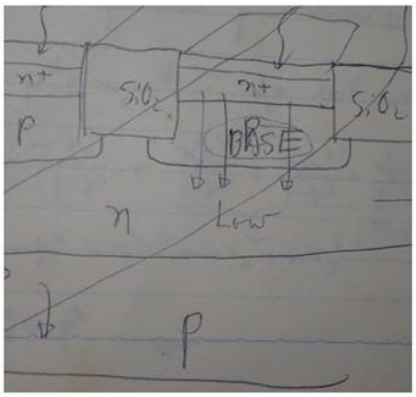
Buried Photodiode with Floating P+ Surface of Serious Image Lag Problem

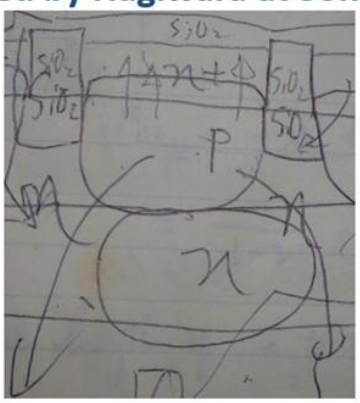
The parasitic capacitance coupling with the surrounding depletion region and the gate oxide.

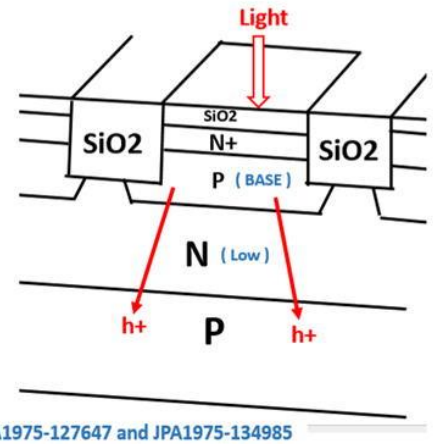
Pinned Photodiode must have the adjacent heavily doped P+ Channel Stops Region or a metal contact as an option as shown in JPA 1975-127646, JPA1975- 127647 and JPA 1975-134985 invented by Yoshiaki Hagiwara in 1975. See also SSDM1978 paper by Hagiwara in 1978.



The N+PNP junction type Dynamic Photo Transistor Structure Pinned Photodiode and Sony Hole Accumulation Diode (HAD) with the vertical overflow drain (VOD) function invented by Hagiwara at Sony in 1975







Hagiwara's Lab Note at Sony in February 1975

In 1975 at Sony, Yoshiaki Hagiwara filed three Japanese patents JPA1975-127646, JPA1975-127647 and JPA1975-134985 on the Pinned Surface Photodiode with the VOD function which is later called as Sony Hole Accumulation Diode (HAD). Hagiwara did not file a patent on the SiO2 device isolation but this lab note shows that Hagiwara had an idea of forming the Shallow Trench Isolation by the Local Oxidation Method, which was hinted by the LOCOS isolation in 1970s.