Imaging Devices

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http://www.isscc.org/isscc/
http://www.ee.ed.ac.uk/ICMTS/
http://www.coolchips.org/
http://www.unf.edu/ccec/ieee/index.html

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Outline

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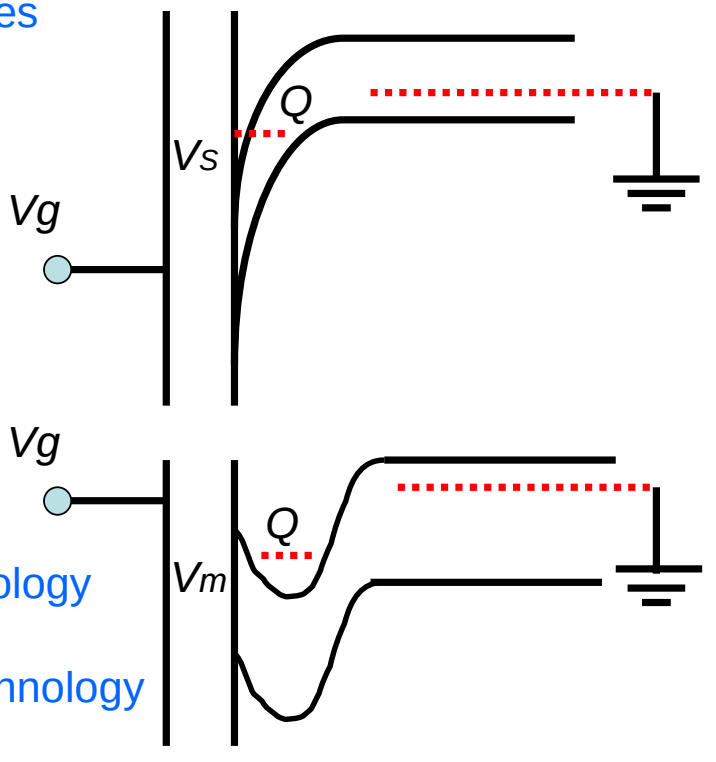
2) Imaging Devices for Digital Consumer Systems
   - 2.1) Digital Information Consumer Products that utilize imaging devices
   - 2.2) Requirements for imaging devices
   - 2.3) Classification of image sensors
3) CCD Technology
   - 3.1) Basic device characteristics
   - 3.2) History of development
   - 3.3) Current topics and future
4) CMOS Sensor Technology
   - 4.1) Basic device characteristics
   - 4.2) History of development
   - 4.3) Current topics and future
5) Circuits and Module Technology
   - 5.1) Role of circuits and module technology
   - 5.2)Technology roadmap
   - 5.3) Impact on device and process technology
6) Summary
7) Reference



Q(1) Obtain $V_S = f_1(Vg,Q)$ and $V_m = f_2(Vg,Q)$

Ref(1-3)

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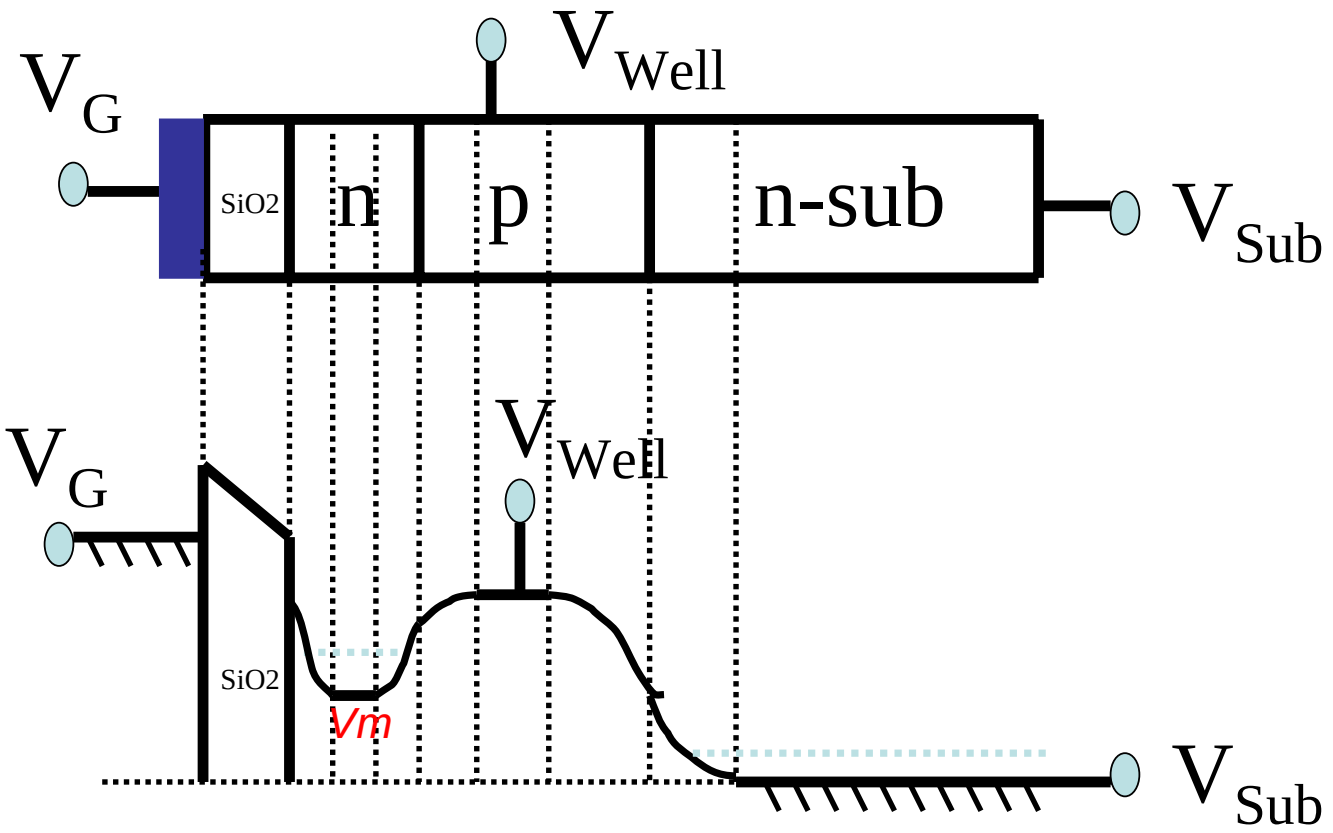


Q(1) Obtain $Vm = f_2 (Vg,Q)$

Buried Channel CCD Structure

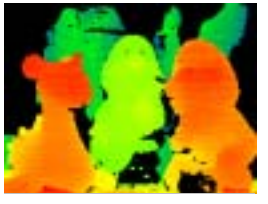
1) Introduction

This lecture will provide an overview of imaging devices. The importance of these devices has increased rapidly due to the tremendous success of digital cameras. Basic characteristics, development history, current topics, and future trend of CCD and CMOS sensor devices will be reviewed.

AIBO 2nd Generation, ERS-210

New AIBO Models,
ERS-210 and SDR-3

Sony Dream Robot, SDR-3



Color Image
at 30fps

Range image at
15Hz scan

Extracted objects

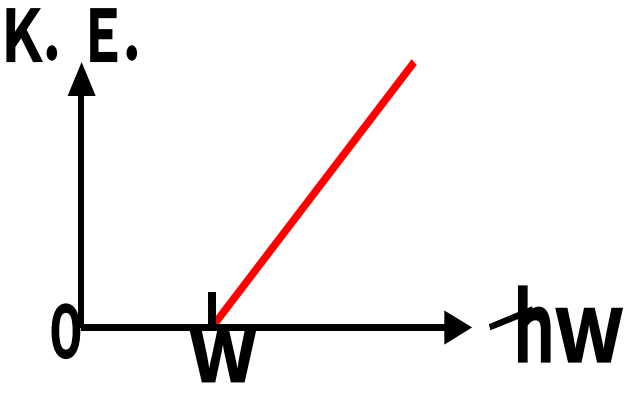
Ref(4-6) M.Fujita,H.Kitano and K.Sabe

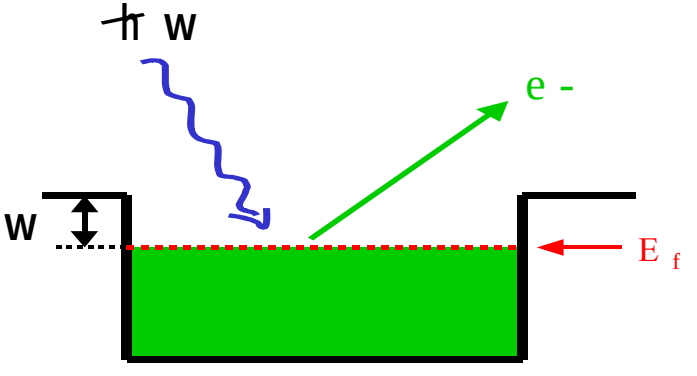
Ref(7) Shin-ichi Yoshimoto

1) Introduction

< Basic Concepts needed to understand Imaging Devices>

Q(2) What is the earliest photo-sensor that converts light information to electrical information ? And how did it evolve ?





Ref(8-9) Photoelectric Effect: The energies of electrons liberated by light from metal depend on the frequency of the light." observed by Heinrich Hertz in 1888 and later explained by Albert Einstein introducing the concept of photon in his Quantum Theory of Light in 1905.

1) Introduction

< Basic Concepts needed to understand Imaging Devices>

Q(3) Explain the following Basic Concepts:

*Semiconductor
*p-n junction
*Bipolar Transistor
*MOS Transistor

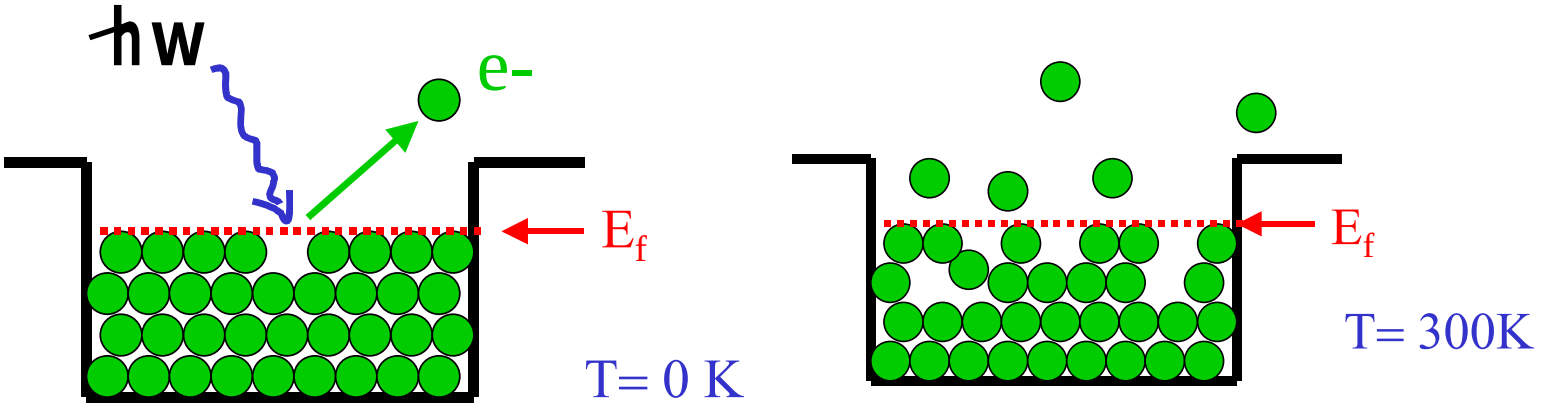
*MOS C-V Measurement
*On-set of Strong Inversion
*Floating MOS Channel region
*Dynamic MOS Shift Register

*Charge Pumping
*Floating Diode Node
*Floating Gate
*Bootstrap Effect

Q(4) What is light ?

Q(5) What is electron ?

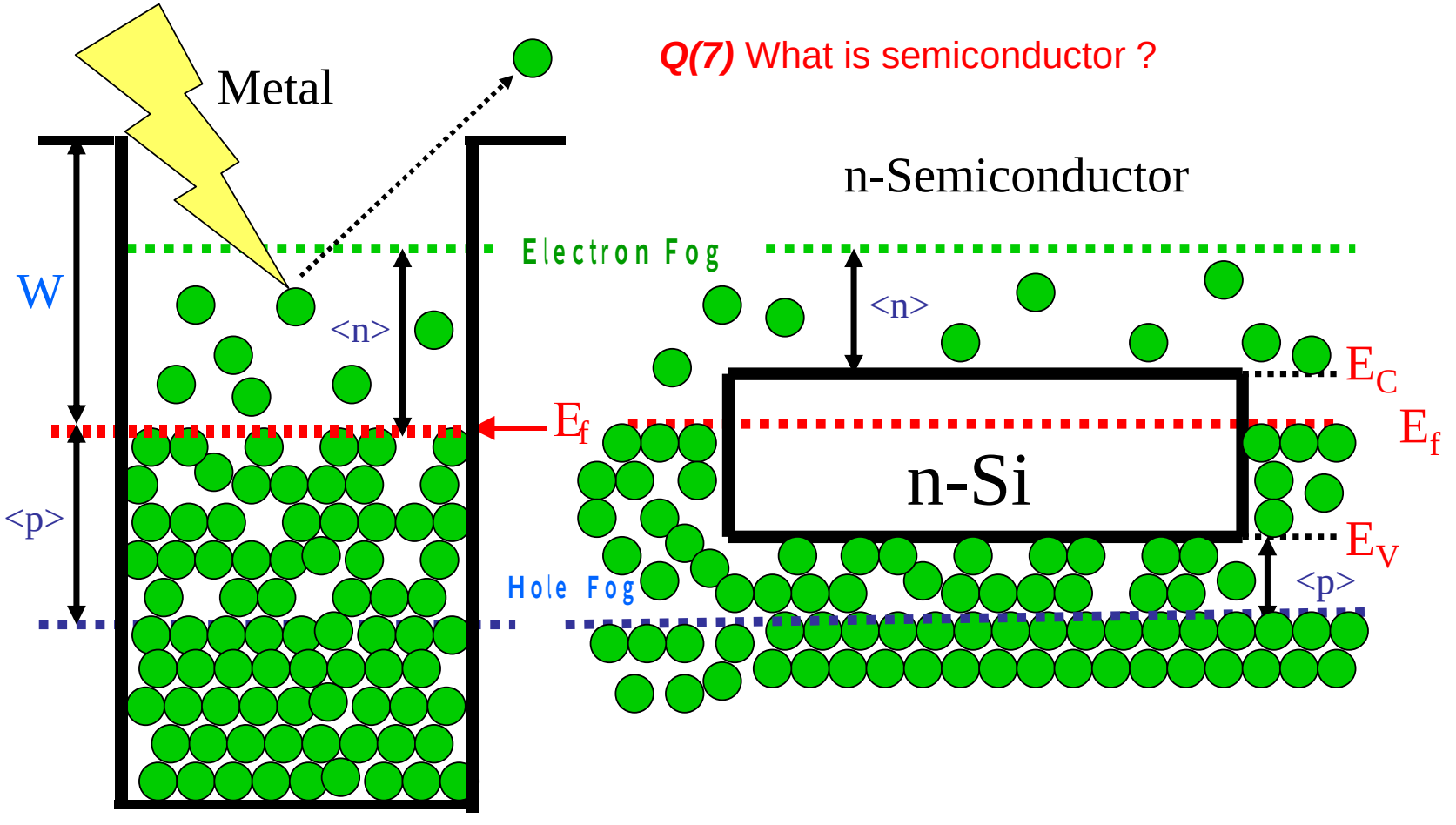
Q(6) What is metal ?



Ref(10-11)

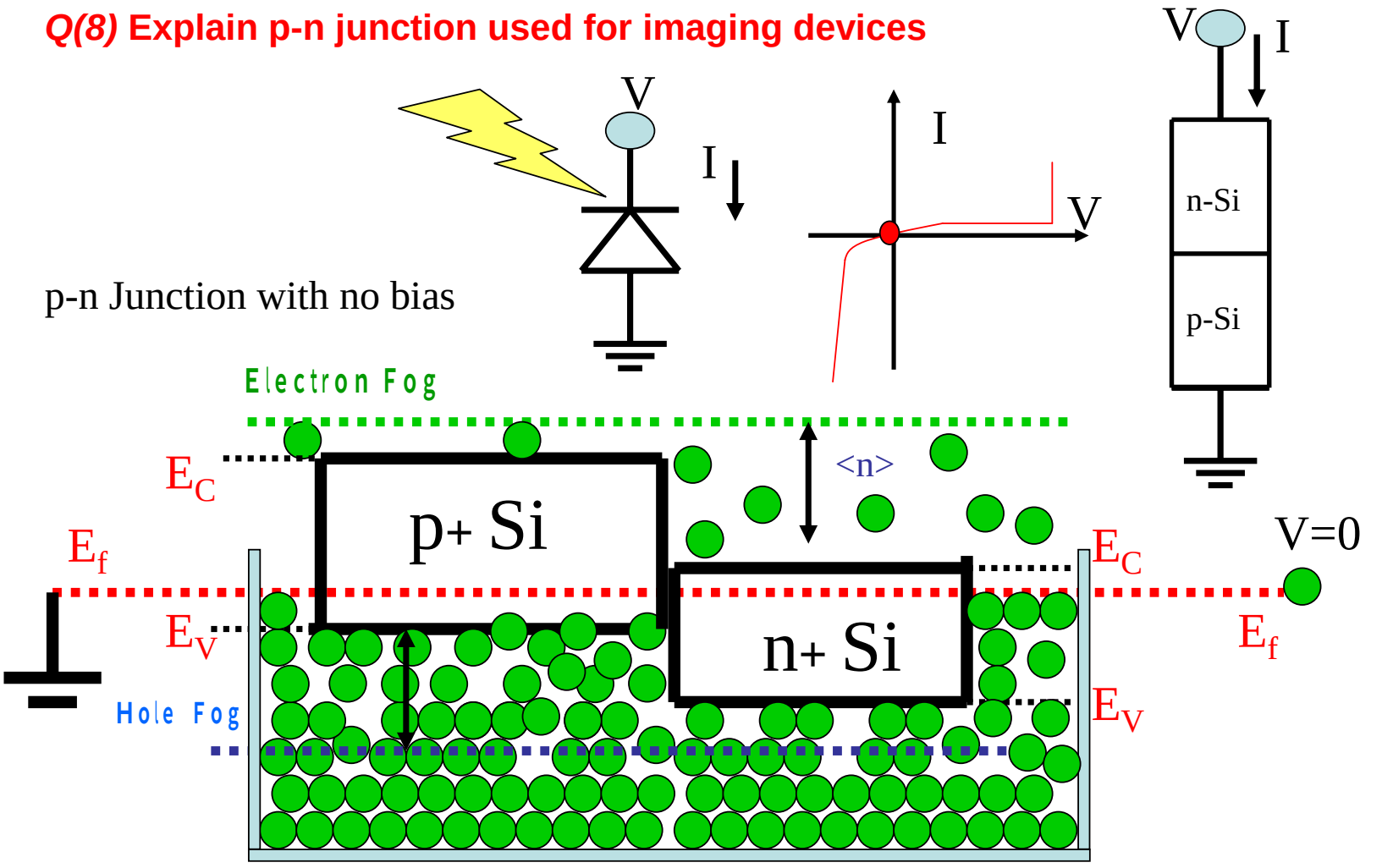
1) Introduction

Q(7) What is semiconductor ?

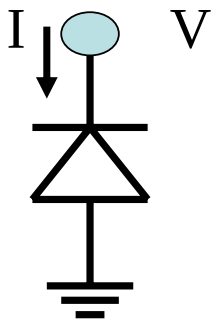


Electron Fog Model in Metal and Semiconductor

Q(8) Explain p-n junction used for imaging devices

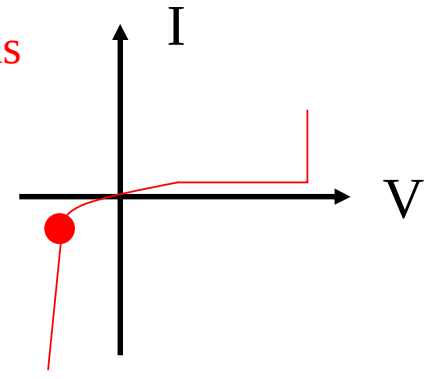


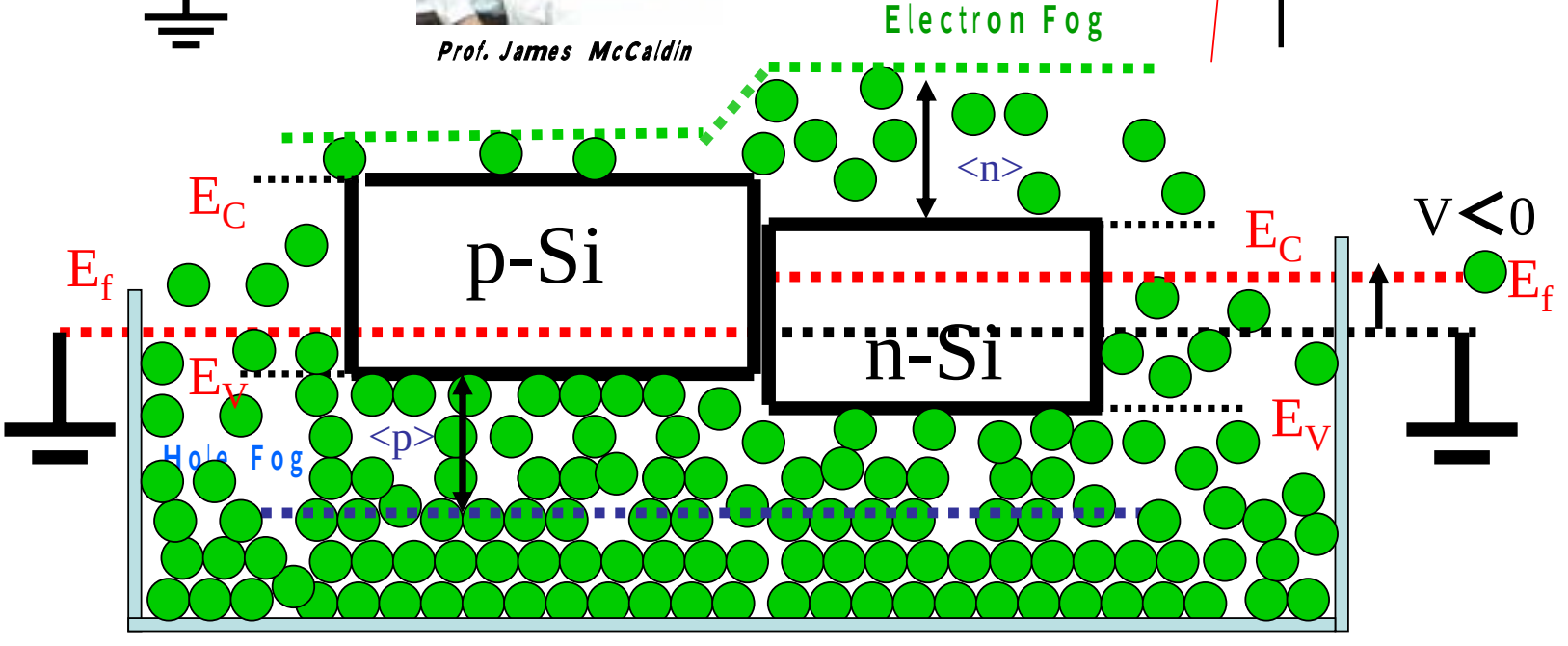
1) Introduction



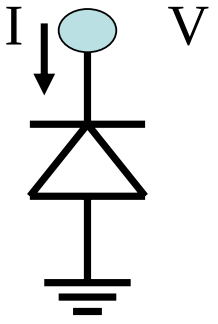
Q(9) Explain p-n Junction with forward bias

Prof. James McCaldin



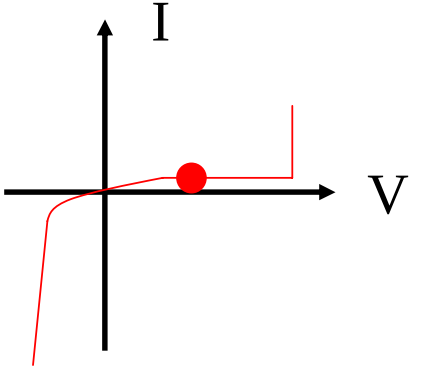


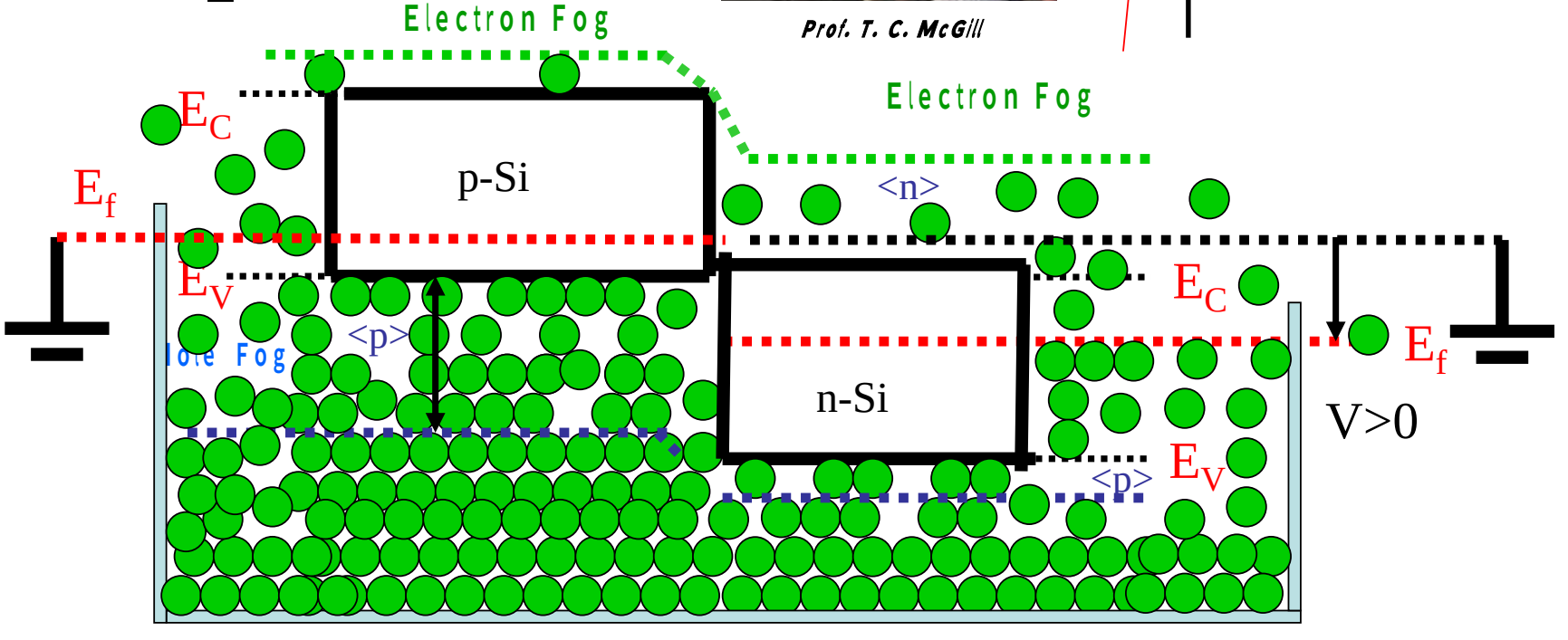
1) Introduction



Q(10) p-n Junction with back bias

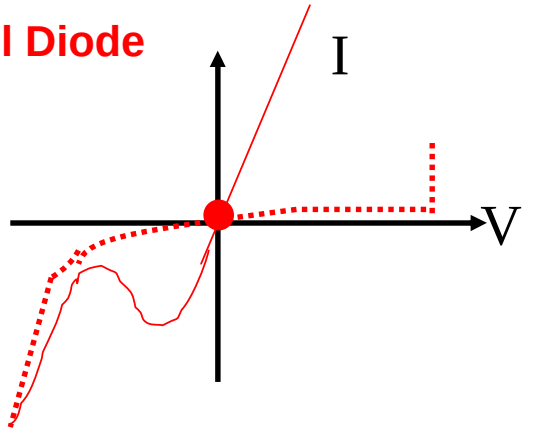
Prof. T. C. McGill





Q(11) Explain Esaki-Tunnel Diode

Prof. C.A. Mead



1) Introduction

<More Basic Concepts needed to understand Imaging Devices>

Q(12) Explain Basic Bip Transistor Action

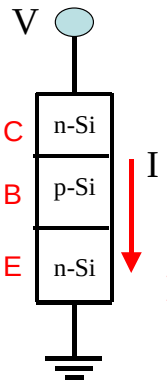
*Bipolar Transistor

$\phi = \phi_i - V_{BE}$

$Q_n = A_E W_B n(0) / 2$

$\tau_t = W_B^2 / 2D_n$

$L_n = \sqrt{D_n \tau_n}$

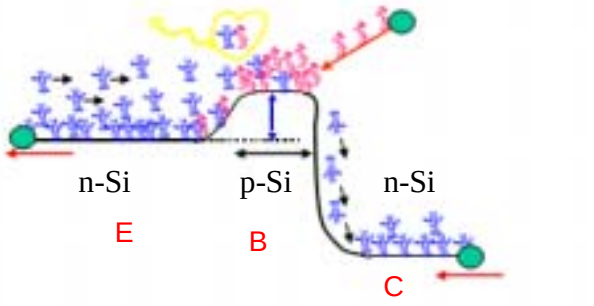


$I_E = \beta I_B$

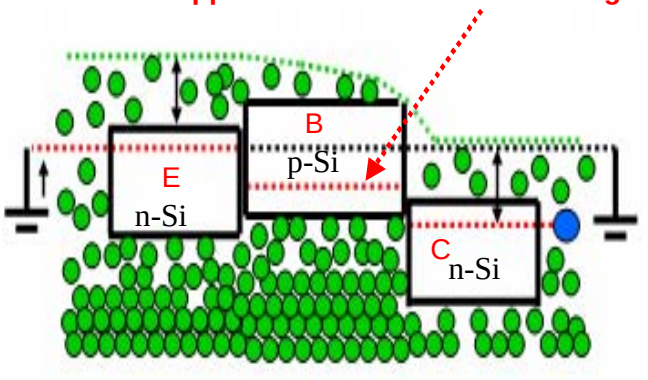
$I_E = I_o \exp(V_{BE}/kT)$

$I_B = Q_n / \tau_n$

$I_o = qA_E D_n \{ n_i^2 / N_a \} / W_B$



What happens when the base is floating ?



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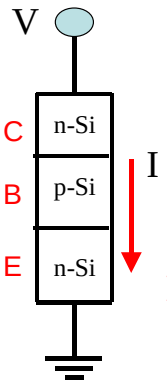


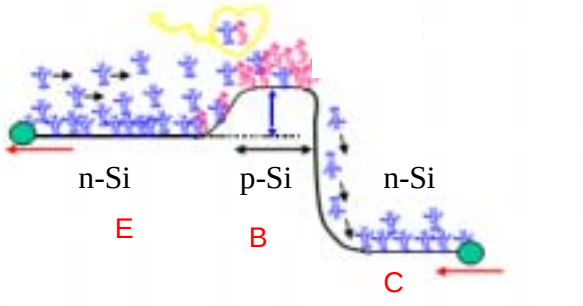
$I_E = \beta I_B$

$I_E = I_o \exp(V_{BE}/kT)$

$I_B = Q_n / \tau_n$

$I_o = qA_E D_n \{ n_i^2 / N_a \} / W_B$

Base Floating Mode



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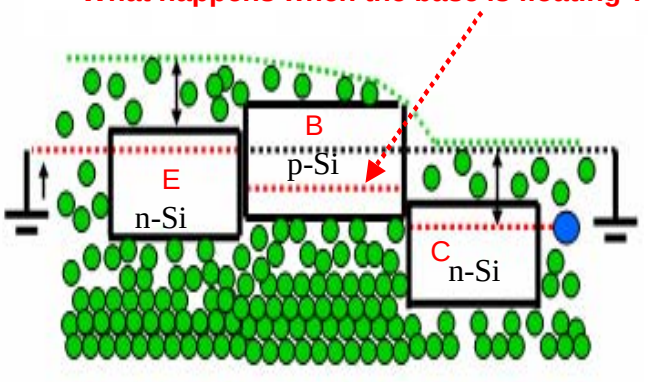

1) Introduction

<More Basic Concepts needed to understand Imaging Devices>

Q(12) Explain Basic Bip Transistor Action

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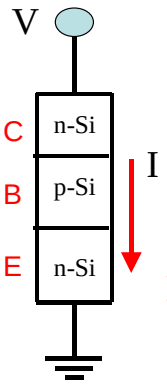


Bip photo Array by M.A.Schuster and G.Strull, Westing House electric Corp. IEEE TED Ed-12 No.12, Dec 1966

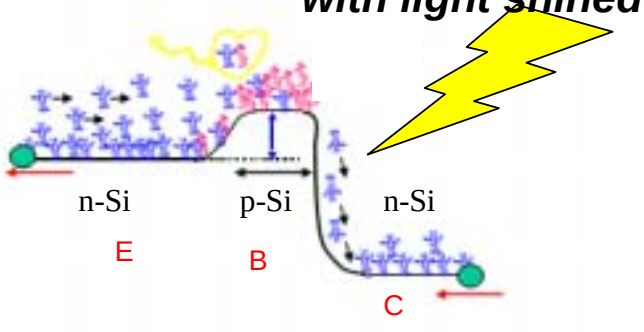
$I_E = \beta I_B$

$I_E = I_o \exp(V_{BE}/kT)$

$I_B = Q_n / \tau_n$

$I_o = qA_E D_n \{ n_i^2 / N_a \} / W_B$

Base Floating Mode with light shined in



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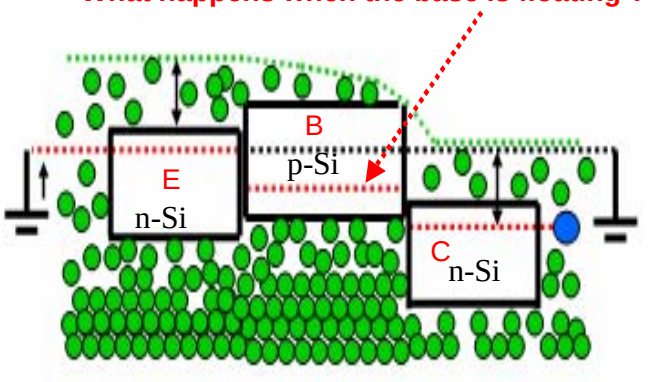
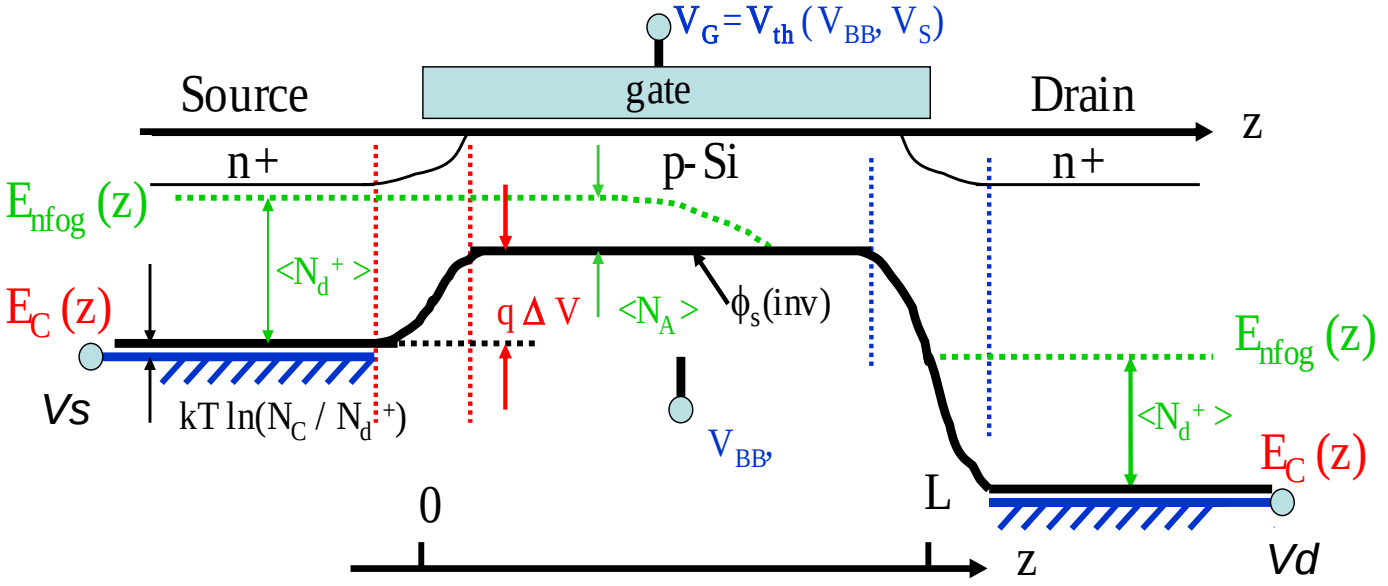


Q(13) Explain a simple MOS Transistor Physical Model and the I V Equation

$$I = w\,\mu\,E\,Q \qquad Q = Co\ (Vch - Vcho) \qquad Vcho = (Vg - Vth)$$

$$E = (Vd - Vs) / L \qquad Vch = (Vd + Vs) / 2$$



MOS FET @ Onset $V_G = V_{th}$

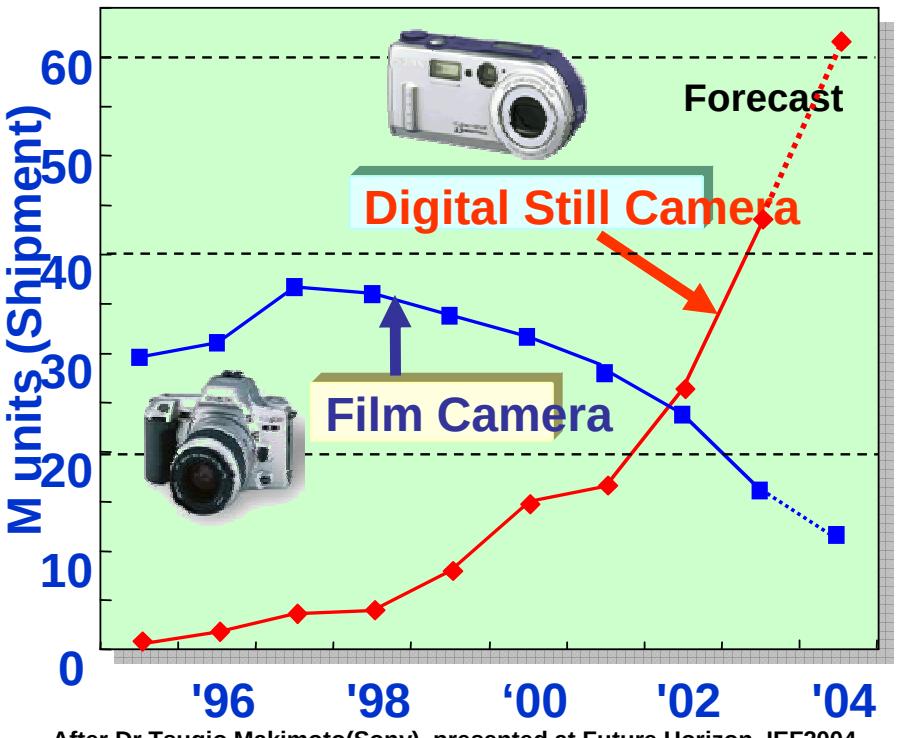
2) Imaging Devices for Digital Consumer Systems:

2.1) Digital information Consumer Products that utilize imaging devices

Q(14) What are they ?

Digital Video Camera
Digital Still Camera
Mobile Phones

Surveillance Camera
Automobile
Robot Eyes



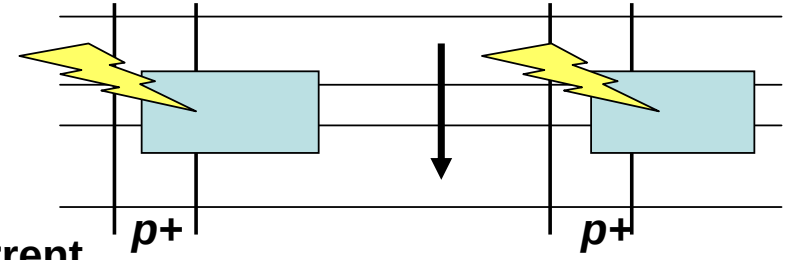
After Dr.Tsugio Makimoto(Sony), presented at Future Horizon, IEF2004

2) Imaging Devices for Digital Consumer Systems:
2.2) Requirements for imaging devices

Q(15) Requirements for image sensors…..What are they ?

(1) High Blue Sensitivity

Ref(12) M.Abe et al 1977



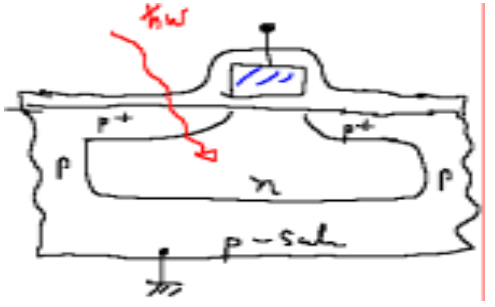
SiO_2 window

(2) Low Dark Current

Block Surface Recombination Current
Hole-Accumulated Pinned Diode

Ref(13) Y.Hagiwara 1977

(3) Image Lag Free



Completely carrier depleted sensing area

(4) Built-in Fast Electrical Shutter

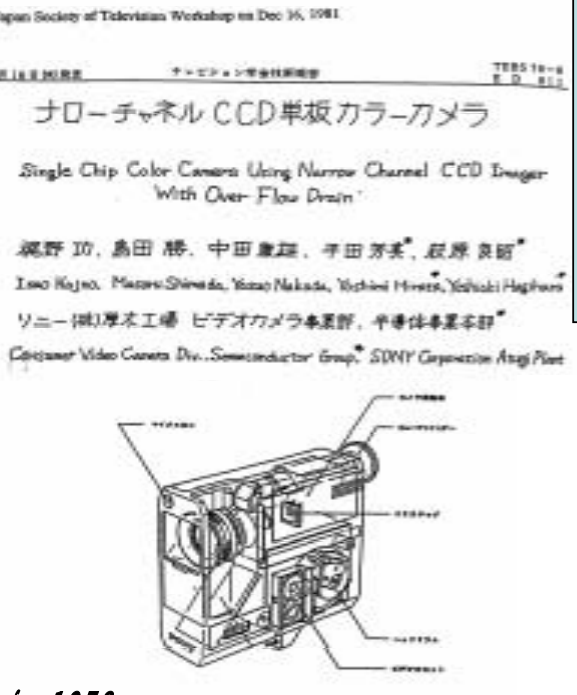
Vertical Overflow Drain Structure

2) Imaging Devices for Digital Consumer System

2.2) Requirements for imaging devices

Q(16) What is the most important ?

Ref(14) Iwao Kajino, 1978



ナローチャネルCCD単板カラーカメラ

Single Chip Color Camera Using Narrow Channel CCD Imager With Over Flow Drain

梶野 功, 島田 勝, 中田 康雄, 平田 芳美*, 萩原 良昭*

Iwao Kajino, Masaru Shimada, Yasuo Nakada, Yoshimi Hirata*, Yoshiaki Hagiwara*

ソニー㈱厚木工場 ビデオカメラ事業部, 半導体事業本部*

Consumer Video Camera Div., Semiconductor Group*, SONY Corporation Atsugi Plant

Kazuo Iwama @ Tokyo Press Conf, 1978

Ref(15-18) More Works On one-chip color camera by

Y.Ishihara 1980

N.Koike 1980

A.Furukawa 1980

N.Teranishi 1982

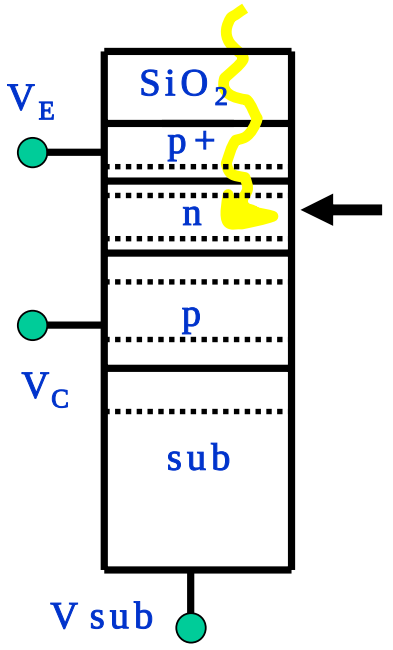
High Sensitivity and Compactness
Easy to carry around with one hand

<FCX016> 570H x 498V One-Chip FT CCD Color Imager, 1978

2) Imaging Devices for Digital Consumer Systems:
2.2) Requirements for imaging devices

Q(17) What is the most ideal structure for photo sensor ?

Ref(19) Hawirara, 1975



A bipolar transistor like p-n-p-sub structure proposed in 1975 with lightly doped base region in dynamic operation with a completely-majority–carrier-depleted base.

This p-n-p-sub sensing element structure is a combination of pinned diode and a vertical OFD sensor structure reported in IEDM 1984. This structure is valid and still very useful both for CCD and current CMOS image sensor.

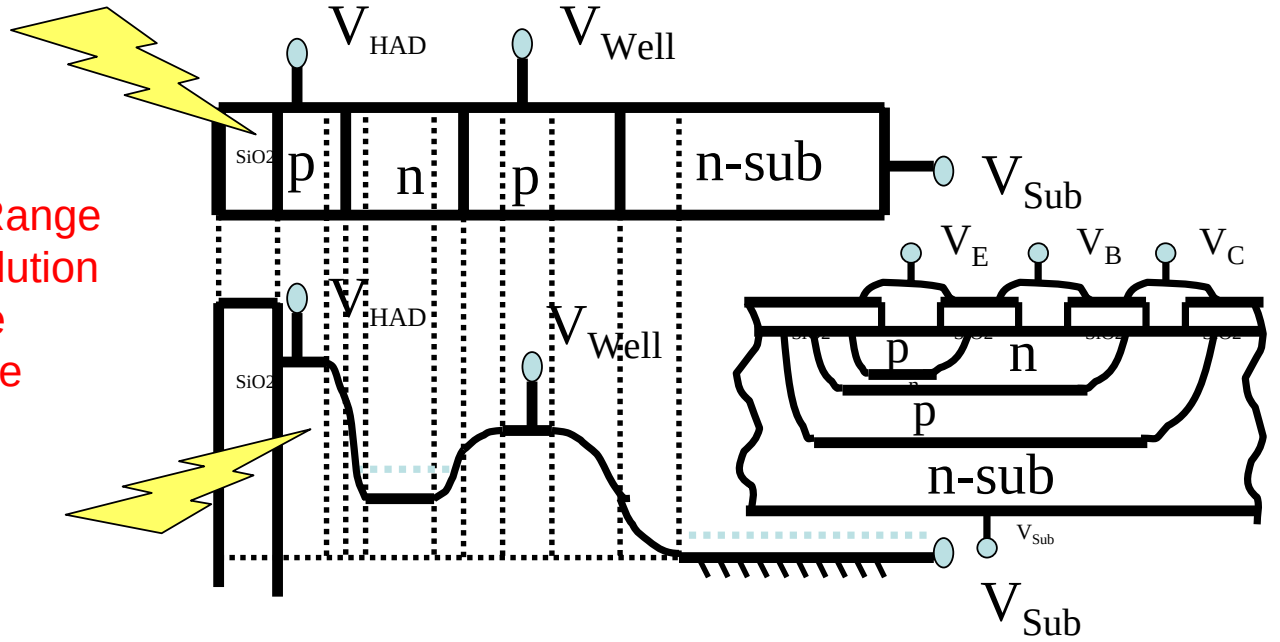
SiO2-P-N-P-Sub Structure : an Ideal Solid State Electrical Eye

2) Imaging Devices for Digital Consumer Systems:

2.2) Requirements for imaging devices

Q(18) What are the important physical parameters for high picture quality ?

Sensitivity
Dynamic Range
High Resolution
Noise Free
Smear Free
No Lag



Output Gain (micro volt / electron)
Charge Capacity (electrons / pixel)

Ref(19) Yoshiaki Hagiwara, 1975

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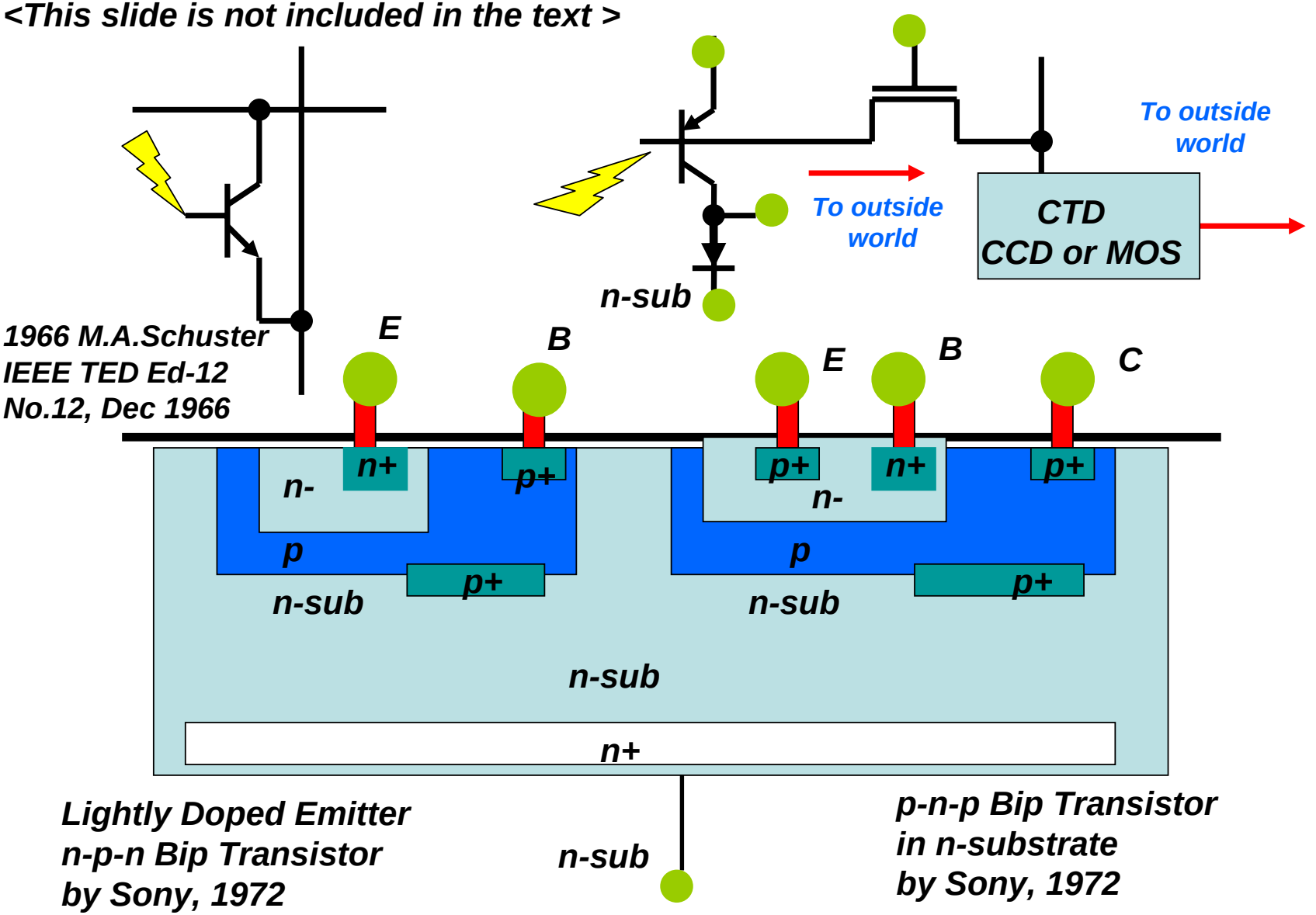


2) Imaging Devices for Digital Consumer Systems:

2.2) Requirements for imaging devices

⑲ 日本国特許庁

公開特許公報

⑪特開昭 52-58414
⑬公開日 昭52.(1977) 5.13
⑳特願昭 50-134985
㉒出願日 昭50.(1975)11.10

特 許 願 (1)

特許庁長官 斎藤英雄殿

1. 発明の名称 固体撮像装置

2. 発明者
住所 神奈川県横浜市保土ケ谷区岩崎町303の153
氏名 萩原義昭 外1名

方式審査 (審査) 50 134985

発明の名称 固体撮像装置

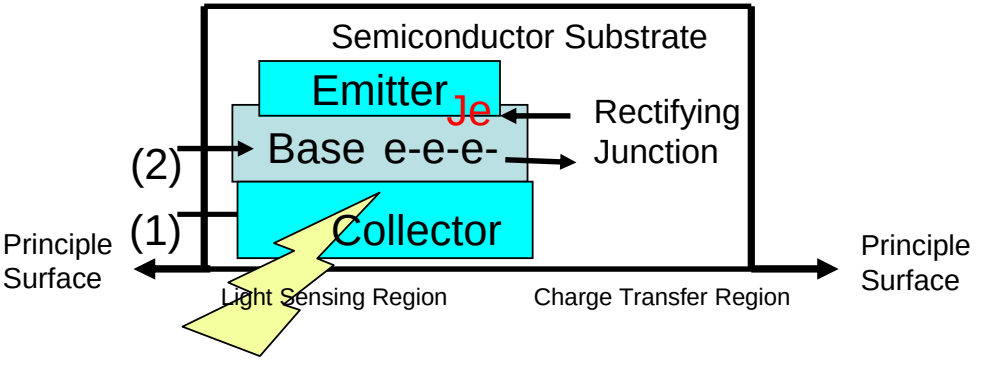
特許請求の範囲

半導体基体に、第1導電型の第1半導体領域と、その上に形成された第2導電型の第2半導体領域とが形成されて光感知部とこよりの電荷を転送する電荷転送部とが上記半導体基体の主面に沿うように配置されてなる固体撮像装置に於いて、上記光感知部の上記第2半導体領域に整流性接合が形成され、該接合をエミッタ接合とし、上記第1及び第2半導体領域間の接合をコレクタ接合とするトランジスタを形成し、該トランジスタのベースとなる上記第2半導体領域に光学像に応じた電荷を蓄積し、ここに蓄積された電荷を上記転送部に移行させて、その転送を行うようにしたことを特徴とする固体撮像装置。

Q(19a) How did the idea come out ?

Claim : In the Semiconductor body, where we have the light sensing region and the charge-transfer region along the principle surface, there is the first conductive region (1) and on top of which there is the second conductive region(2). To the region (2) a rectifying emitter junction is formed while the junction between region(1) and (2) forms a collector junction. Light is emitted to, and the photon generated charge is stored in the base region (2) of the transistor. The stored charge is transferred to the adjacent charge transfer region.

(Pinned diode when sub = p)



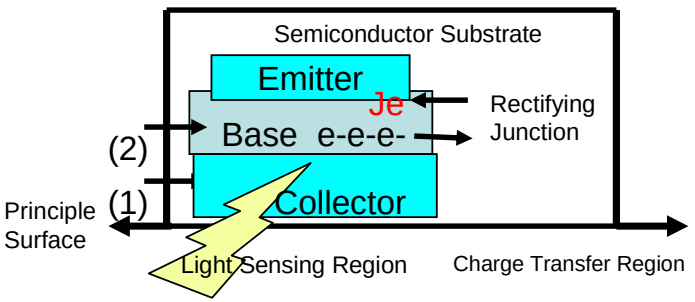
Nov 10, 1975 Japanese Patent 52-58414 “Bipolar Type Sensor Structure for Solid State Imager”

2) Imaging Devices for Digital Consumer Systems:

2.2) Requirements for imaging devices

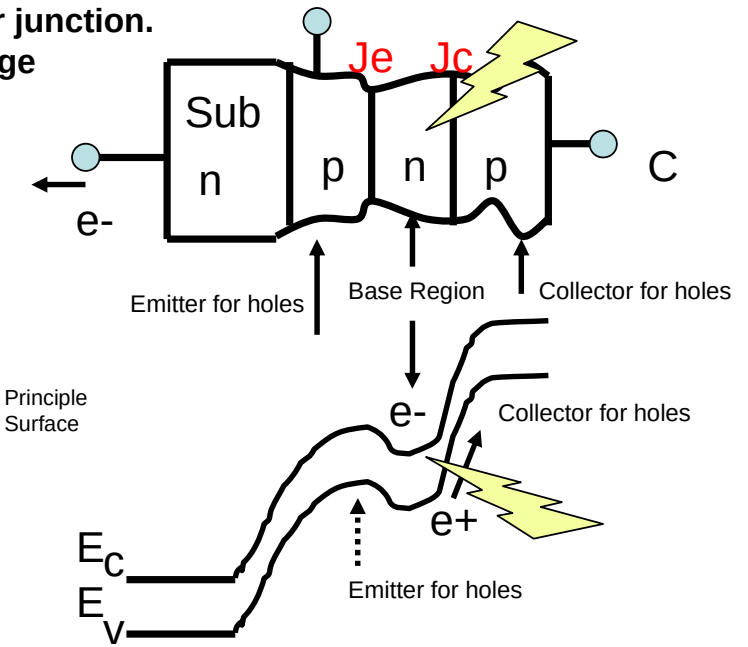
Q(19b) How did the idea come out ?

Claim : In the Semiconductor body, where we have the light sensing region and the charge-transfer region along the principle surface, there is the first conductive region (1) and on top of which there is the second conductive region(2). To the region (2) a rectifying emitter junction is formed while the junction between region(1) and (2) forms a collector junction. Light is emitted to, and the photon generated charge is stored in the base region (2) of the transistor. The stored charge is transferred to the adjacent charge transfer region.



Nov 10, 1975 Japanese Patent 52-58414
"Bipolar Type Sensor Structure for Solid State Imager"

(when sub = n)



Ref(19)Yoshiaki Hagiwara 1975

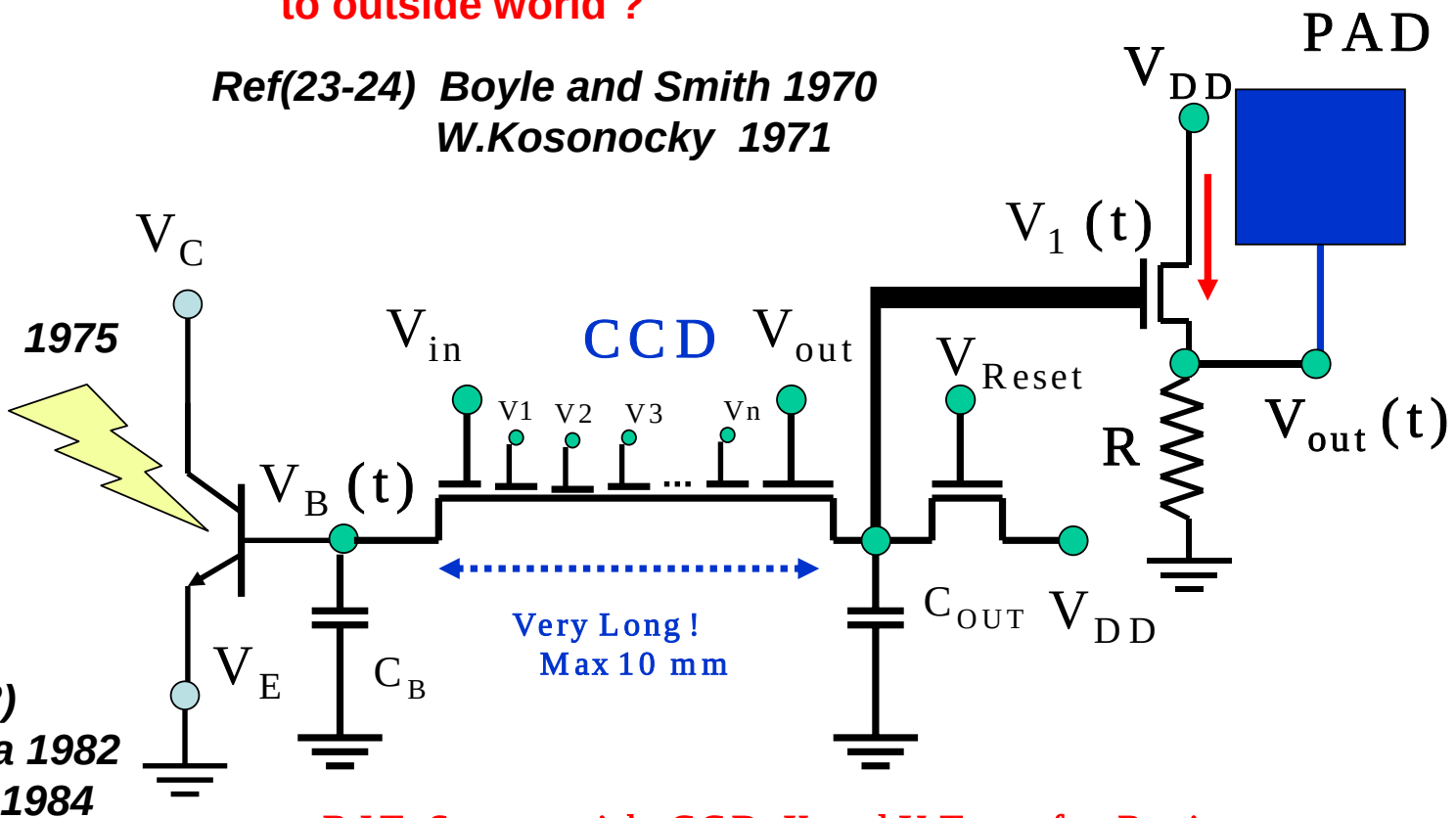
2) Imaging Devices for Digital Consumer Systems:

2.2) Requirements for imaging devices

_Q(20)_ How can we transfer the signal charge to outside world ?

Ref(23-24) Boyle and Smith 1970
W.Kosonocky 1971

Ref(19)
Hagiwara 1975



Ref(20-22)
Y.Ishihara 1982
A.Kohno 1984
B.C. Burkey 1984

BJT Sensor with CCD X and Y Transfer Registers

2) Imaging Devices for Digital Consumer Systems

2.3) Classification of image sensors

Q(21) Explain about the early versions of imagers, such as BBD and CID

BBD(Bucket Brigade Device)
CSD(Charge Sweep Device)
CPD(Charge Priming Device)
CID(Charge Ingjection Device)

CCD (Charge Coupled Device)

MOS (CMOS) Imaging Device

Q(22) Explain Basic CCD Performance parameters

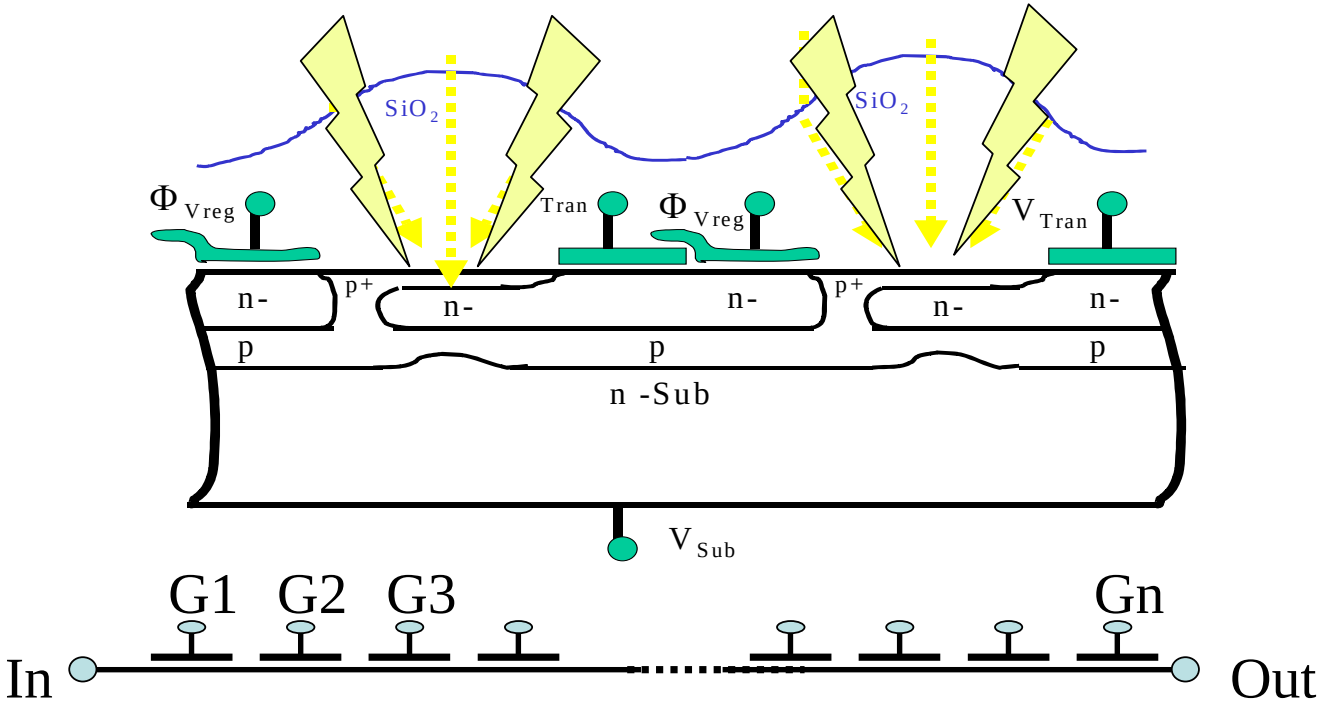
Sensitivity (nA/lx for Color Temperature or volt / lx sec)
Saturation Current (nA)
Dynamic Range (dB)
Smear Reduction Level (dB)
Horizontal & Vertical Limiting
Resolution (TV lines)
Charge Transfer Efficiency (% per Stage)
Dark Signal Output
Signal to Random Noise Ratio (dB)
Signal to Noise Ratio (dB) with or without Fixed Pattern Noise
Output Gain (micro volt / electron)
Charge Capacity (electrons / pixel)

3) CCD Technology

3.1) Basic device characteristics

Q(22) What are the source of contamination and defects in CCD imagers?

Contamination-Free and Defect-Free Clean Process and Device Cares are very, very important.



3) CCD Technology

3.1) Basic device characteristics

Q(23) Discuss about device and process characteristics inherent to CCD imagers to conquer contamination and control defects, such as white-point defects and black-point defects.

AN ANALYSIS OF VIDEO DEFECTS OBSERVED IN AN INTERLINE TRANSFER CCD IMAGE SENSOR

Takashi Shimada and Yasuo Kanoh
SONY CORPORATION Semiconductor Division
4-14-1,Asahi-cho,Atsugi 243,Japan

Junichi Aoyama
SONY CORPORATION Research Center
174 Fujitsuka-cho,Hodogaya-ku,Yokohama 240,Japan

A solid state color camera using two interline transfer CCD chips has been constructed by Sony Corporation. In the CCD image sensor, the overflow drains have been employed to absorb the excess charge overflow in the vertical registers.(Fig.1)(1)

One of the inherent defects in the image sensor is concerned with white points, which are known to be due to the stacking faults in the sensor region. We have investigated the origin of the stacking faults in order to diminish the white points and successfully constructed the CCD image sensor free from the defects.

Reference:
(1) C.Okada, T.Shimada, H.Matsumoto, T.Ando, Y.Kanoh T.Kumesawa, Y.Daimon-Nagiwara, (in Japanese) in Tech. paper, Institute of Electronic and Communication Engineers of Japan, No.SSD78-5, pp31-40, April 1978

Ref(25) Takashi Shimada 1980

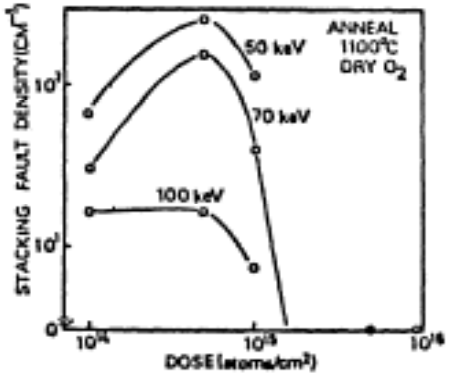


Fig.3 Ion dose and ion energy dependence

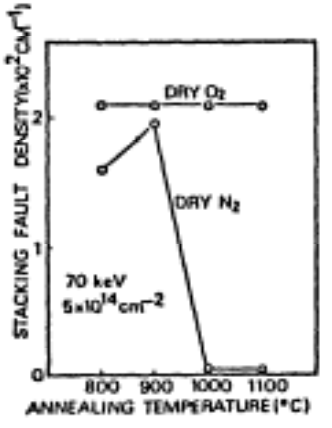


Fig.4 Annealing behavior

3) CCD Technology

3.1) Basic device characteristics

Q(24) What are the next important feature of solid state imager ?

XC-1 1980

Two-Chip Color Video Camera

Technical Report presented at Japan SSD Conference Tokyo, May 1978

SSD78-5

An Interline Transfer CCD Imager With High Density Structure

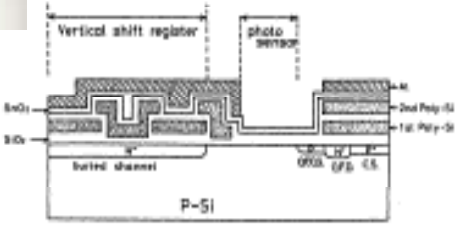
Chikao OKADA, Takeshi SHIMADA, Hiroaki MATSUNOTO, Tetsuo ANDO, Yasuo KANOH, Tatsuaki KINEZAWA, Yoshiaki HAGIWARA

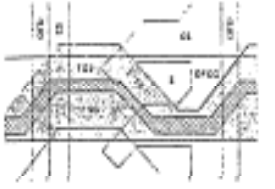
SONY corp. Semiconductor Development Division Research Center

<ICX008>

2/3 Inch 120K Pixcel

IT CCD Imager designed





Ref(26) C.Okada 1978

Answer: Robustness

3) CCD Technology

3.1) Basic device characteristics

***Q(25)* What are the next important feature of solid state imager ?**

Challenge For Higher Resolution

CCD-G5 XC-37 1983

One-Chip Color Video Camera

<ICX016>

2/3 Inch 190K Pixcel
IT CCD Imager designed

Ref(27-28)
H.Murata 1981
T.Kumezawa 1985

VGA	640 x 480
QVGA	320 x 240
SVGA	800 x 600
XGA	1024 x 768
SXGA	1280 x 1024
HD	1280 x 720

Ref(29) K.Ishikawa 1989

		2048 x 1536
		2048(3:2)
		1600 x 1200
		1280 x 960
DSC-P1	2000.1	640 x 480

<This slide is not included in the text >

Higher Performance System

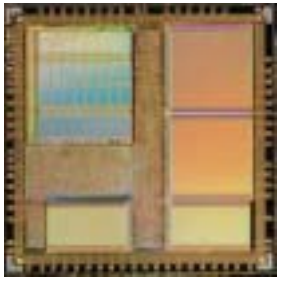
Many Applications/Products

1st EmDRAM Product

0.50μm
1995 MP Start

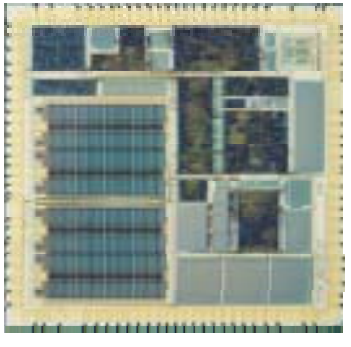
0.35μm
1996 MP Start

0.25μm
1999 MP Start



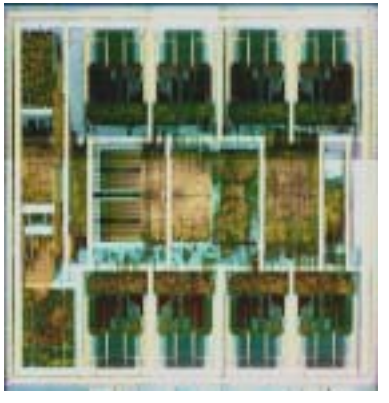
8mm Camcoder LSI

512kbit DRAM+50kG



MD LSI

2Mbit DRAM + 200kG
2.0V Low Voltage Operation



Graphics Synthesizer(PS2)

32Mbit DRAM + 1500KG
DRAM Bandwidth 48GB/S

Embedded DRAM History

3) CCD Technology

3.2) History of development

Proceedings of the 4th Conference on Solid State Devices, Tokyo, 1972
Supplement to the Journal of the Japan Society of Applied Physics, Vol. 42, 1973

6 - 5

AN IMPROVEMENT ON STRUCTURE OF CHARGE COUPLED DEVICES

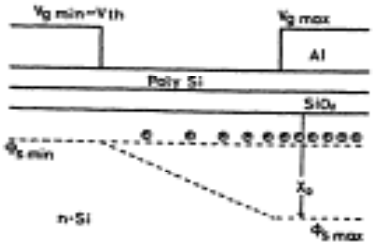
Tadayoshi MIFUNE, Shigeyuki OCHI, Yasuo KANO and Akikazu SHIBATA

SONY CORPORATION Research Center
Yokohama, Kanagawa

A CCD structure having a resistive layer over the oxide film at the interelectrode gaps was studied. Polycrystalline silicon was used as the resistive material. The present structure allowed the use of a gap length of up to 12 μm without appreciable decrease in the charge transfer efficiency. The use of a large gap length removed the severe requirement of the resolution on the photolithographic technology in the conventional CCD structures. The resistivity of the resistive layer was analyzed on the basis of a distributed constant circuit of parallel planes. Test devices of 2- and 3-phase CCDs were fabricated and evaluated based on the present analysis. A 3-phase CCD was used as an image sensor which gave permissible character reproduction.

Ref(30) M.Mifune
S.Ochi
A.Shibata
Y.Kanoh, 1972

Q(26) Explain the common Factors in Transistor Radio and CCD imager development History



The structures of 2- and 3-phase CCDs are illustrated in Fig. 1.

A 3-phase 8-bit unit with a gap length of 5 μm was used as a single line scanner for the image sensing application. The reproduced image is shown in Fig. 4.

Fig. 4. Character display using a 3-phase CCD as a single line scanner.

1972年、エリアあたり4画素のCCDで映し出した「S」の字

3) CCD Technology

3.2) History of development

Q(27) Explain the origin of pinned diode.

Ref(13) Yoshiaki Hagiwara, 1977
Ref(19) Yoshiaki Hagiwara, 1975

Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978;
Japanese Journal of Applied Physics, Volume 18 (1979) Supplement 18-1, pp. 335-340

A 380H × 488V CCD Imager with Narrow Channel Transfer Gates

Yoshiaki Daimon-Hagiwara, Motoaki Abe† and Chikao Okada†

Sony Corporation Research Center, Yokohama 240
†Semiconductor Development Division, Yokohama 240

When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of threshold voltage is observed. This narrow-channel effect has been applied successfully in creating an asymmetric potential well under an electrode for two phase CCD operations. The feasibility of this new structure has been confirmed in a 242 element analog delay line and the application is now extended to a 380H × 488V CCD Imager. In the constructed B/W CCD camera,

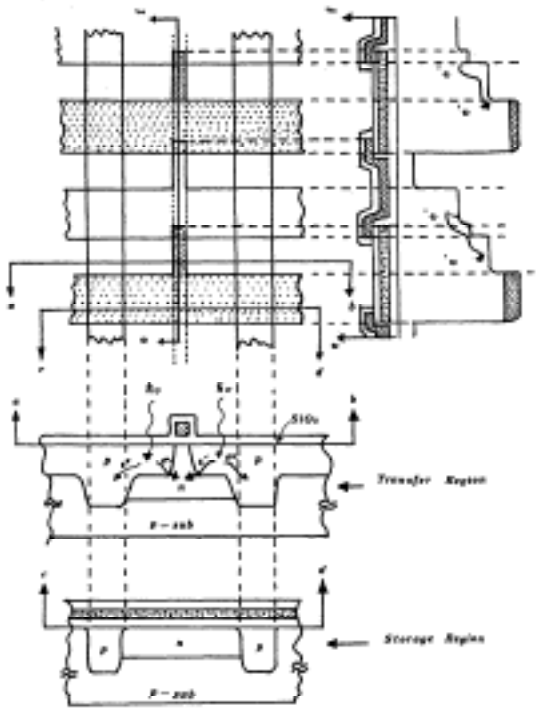
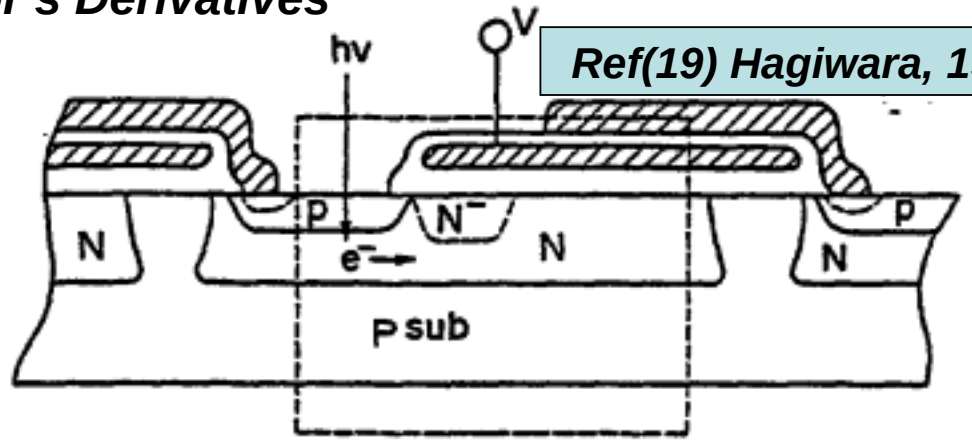
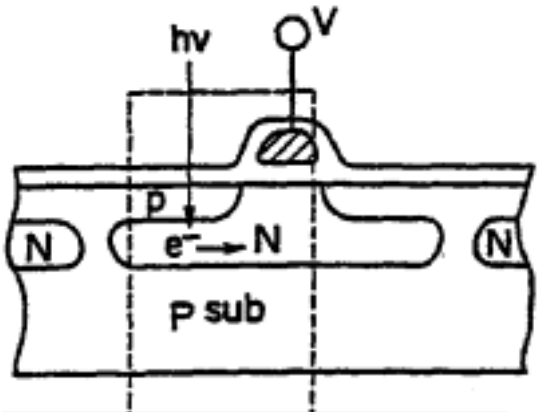


Fig. 2. Top and cross sectional views of the electrode for two phase CCD structure

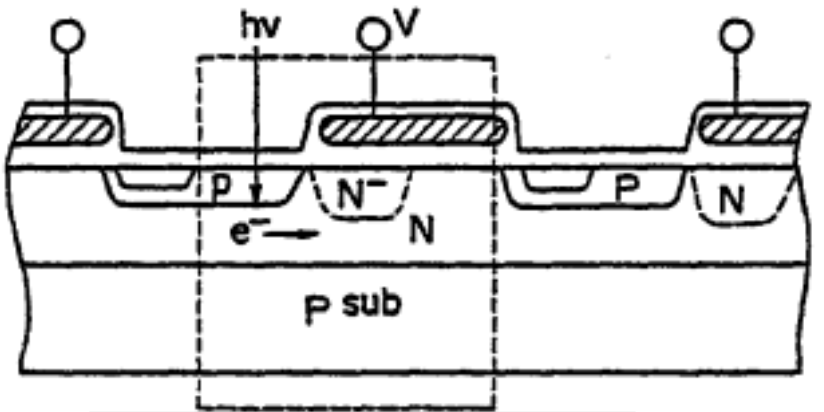
HAD Sensor's Derivatives



Ref(19) Hagiwara, 1975



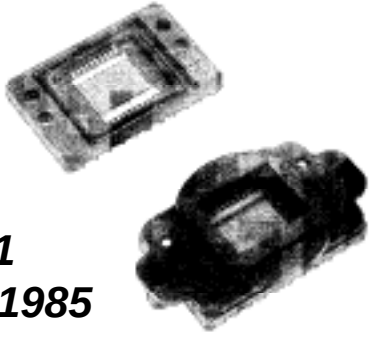
Ref(13) Hagiwara, 1977



Ref(31) Hynecek, 1979

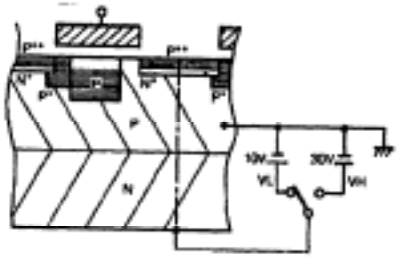
Q(28) Explain the historical development and derivatives of pinned diode.

Challenge for Higher and Higher Resolution



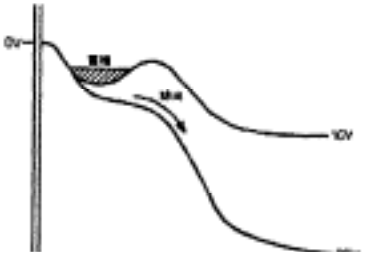
2/3型38万画素 IT（ICX022/024）

Ref(27-28)
H.Murata 1981
T.Kumezawa 1985



Ref(29) K.Ishikawa 1989

CCD-V90



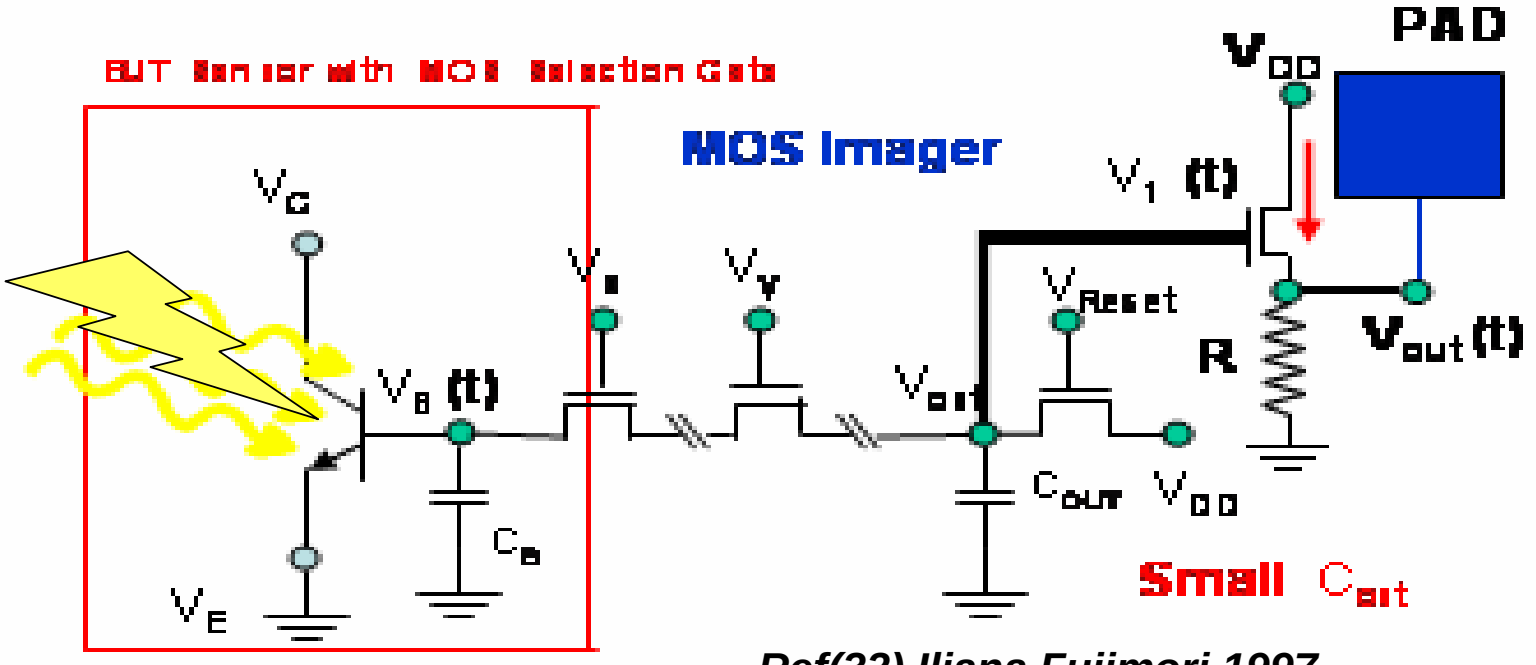
1987 HAD Sensor

Q(29) Why the vertical OFD is needed in CCD ?

4) CMOS Sensor Technology

4.1) Basic device characteristics

***Q(30)* How can we transfer the signal charge to outside world in case of CIS ?**



Ref(32) Iliana Fujimori 1997

Q(31) Explain three types (Current, Voltage. and Charge) of CMOS Image sensors output pixel configurations

4) CMOS Sensor Technology:
4.2) History of development

Q(32) What is the earliest work on MOS Array Sensor ?

Savvas G. Chamberlain,

"Photosensitivity and Scanning of Silicon Image Detector Arrays"
Dec 1969, IEEE Journal of Solid State Circuits, Vol.SC-4,No.6, pp.333-342

Basic Planor Si p+n photo-diode unit,
Principle of operation,
The factors that affect the photodiode and array sensitivity,
Design and layout considerations including the integration time,
Scanning of photo-diode arrays,
Detailed Design Considerations for a static MOST ring counter,
A dynamic shift register with clocked loads for integral scanning,
Design Considerations of an actual photo-sensing matrix

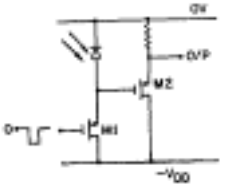


Fig. 1. Array scanning: basic integrating photodiode u

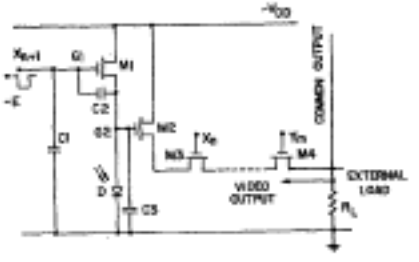
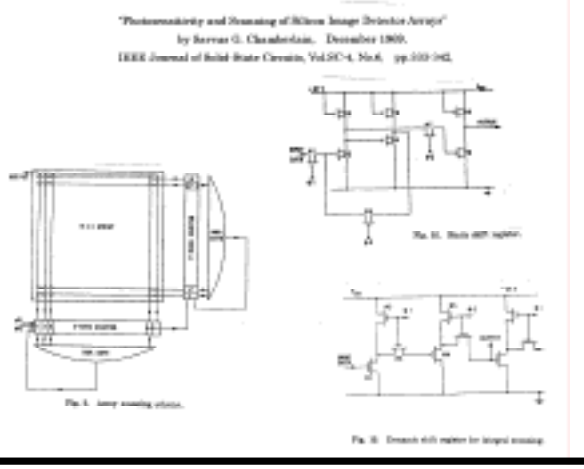


Fig. 8. Array unit for line-time integration.



4) CMOS Sensor Technology:
4.2) History of development

Q(33) Explain the term “quantum efficiency. Why is it important ?

Savvas G. Chamberlain, 1966

IEEE JSSC, Vol.SC-4,No.6, pp.333-342

B. Photocurrent of Planar p⁺-n Diode

For incident monochromatic light of photon flux rate ϕ_0 (photons/s-m²) at wavelength λ, the quantum efficiency η of a photosensor is defined by

$$\eta = \frac{J_p}{e\phi_0} \qquad (9)$$

where J_p = photosensor current density at wavelength λ.

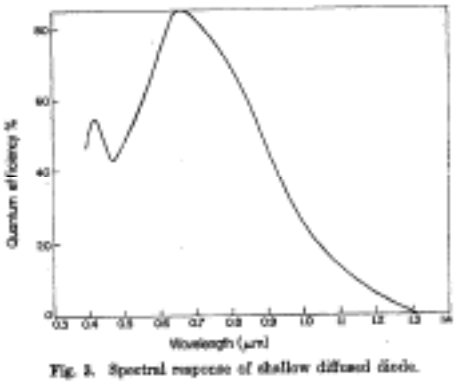


Fig. 3. Spectral response of shallow diffused diode.

C.A.Mead et al , 1972 (1976)

IEEE JSSC, Vol.SC-11,No5, pp.692-695

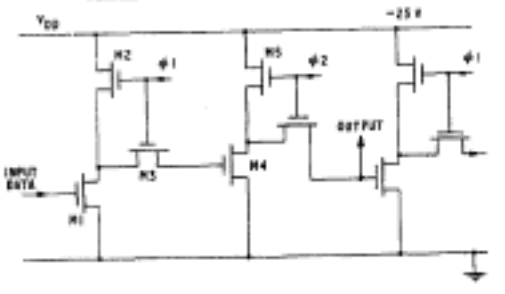


Fig. 13. Dynamic shift register for integral scanning.

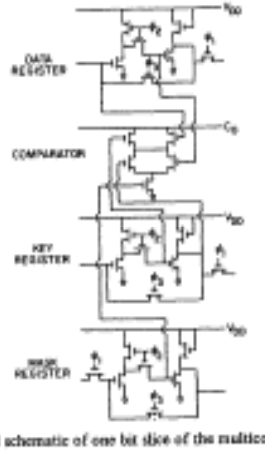


Fig. 5. Full schematic of one bit slice of the multicomparator.

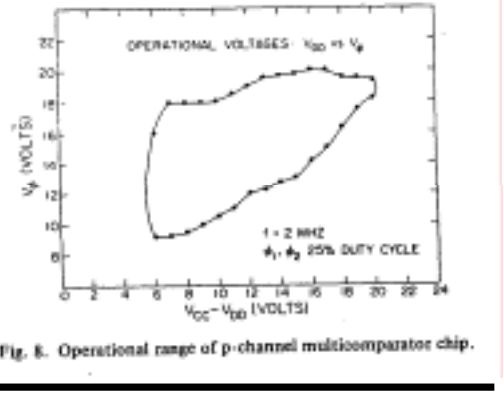
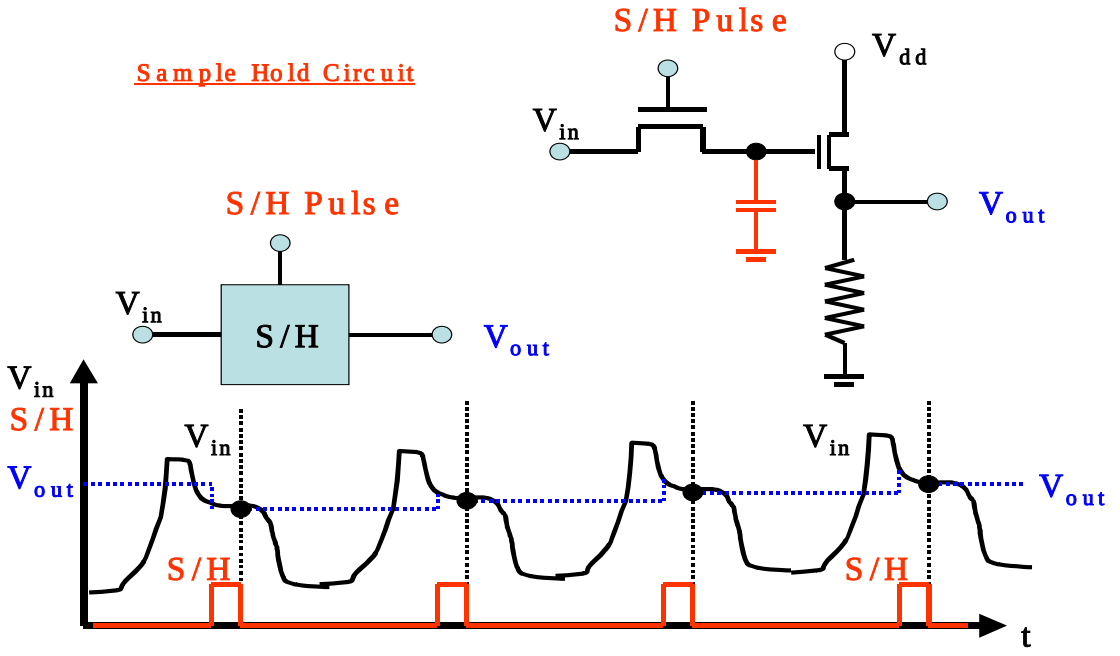


Fig. 8. Operational range of p-channel multicomparator chip.

4) CMOS Sensor Technology:
4.2) History of development

Q(34) Explain S/H circuit for Noise Reduction Cares

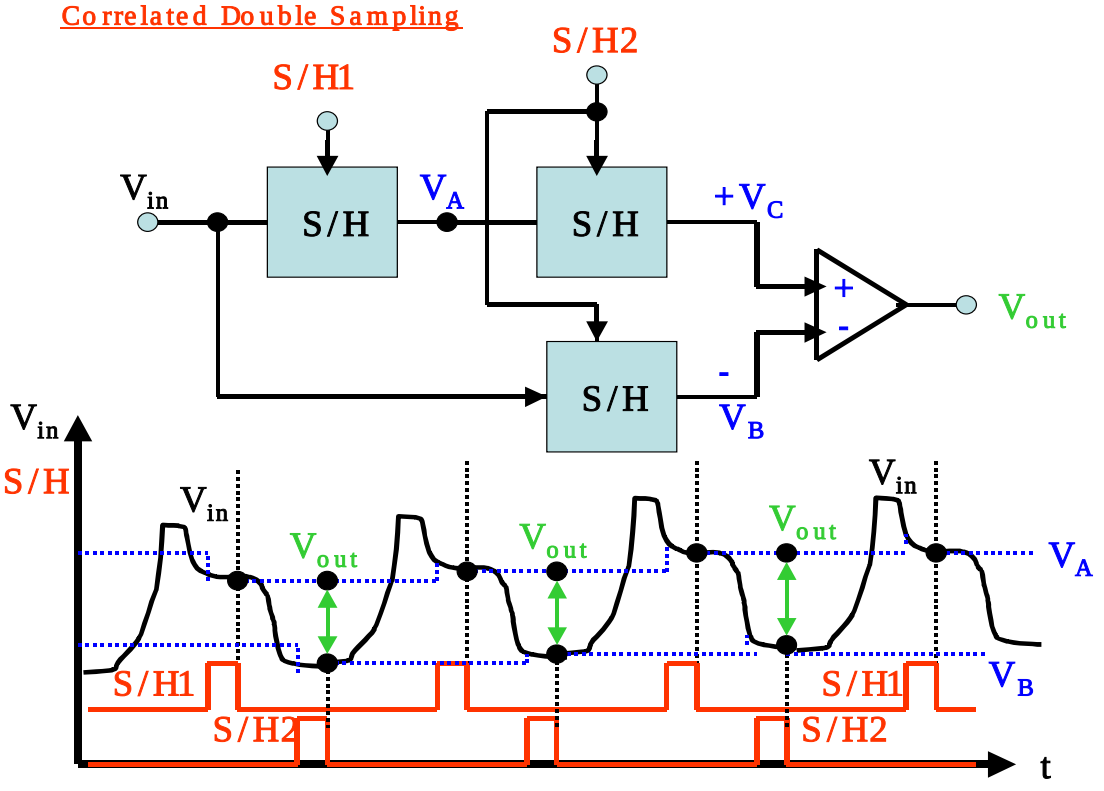
Ref(33) M.Gupta 2004



4) CMOS Sensor Technology:
4.2) History of development

Q(35) Explain CDS technique for effective Noise Reduction Cares

Ref(34) M.H.White 1974



4) CMOS Sensor Technology
4.3) Current topics and future

Q(36) Explain the following features of interest in CMOS image sensors:

Optical Format
Chip Size
Image Area
Number of Pixels
Unit Cell Size
Clock Drivers
Timing Generator
Output Circuits
Sample-and-hold circuits
Power Supply Voltages
Power Supply Currents
On-chip Micro Lens
Color Filters
Package

PRESENT STATE OF THE ART *(PROBLEMS)*

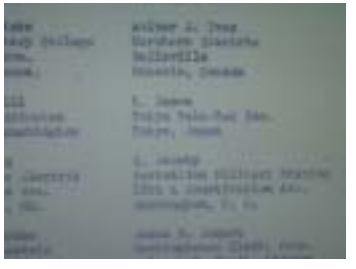
- CMOS image-sensor pixel-pitch reduction is presently done only by technology shrinking
- Basic 3-Transistor/pixel CMOS active-pixel sensors in standard CMOS technology suffer from readout noise and dark current problems.
- Conventional use of a buried pinned photodiode to improve the image quality (for reducing KTC noise and dark current) requires an extra transistor and wire.

4) CMOS Sensor Technology
4.3) Current topics and future

Q(37) Compare the performance, the merits & demerits of CCD Imager v.s. MOS Imager and their future trend.

Process	*Sensitivity*
Substrate&Well Formation	*S/N*
Isolation	*Dark Current*
Gate Oxide	*Smear*
Gate Electrode	*Dynamic Range*
Passivation Layer	*Color Mix*
Light Shield	*Supply Voltage*
	Power

Kazuo Iwama in ICTC(ISSCC) 1954 Attendee List @ University of Pennsylvania, Philadelphia



Smaller and Smaller CMOS Pixels seen in ISSCC2004

Paper# 6.1 *Canon. Japan "* **A 3.9×3.9μm2 Pixel VGA-Format 10b Digital CMOS Image Sensor with 1.5 Transistors/Pixel Architecture**

Paper# 6.2, *Matsushita, Japan,* **"A ¼ inch 2M pixel CMOS Image Sensor with 1.75 Transistors/Pixel Architecture"**

Paper#6.3 *Sony, Japan* **"A CMOS Image Sensors using Floating Diffusion Driving"**

Paper# 6.4 **A CMOS Image Sensor Uses a Dynamic Reset Current Source for Noise Suppression**

Paper# 6.5 **Combined Liner-Logarithmic CMOS Image Sensor**

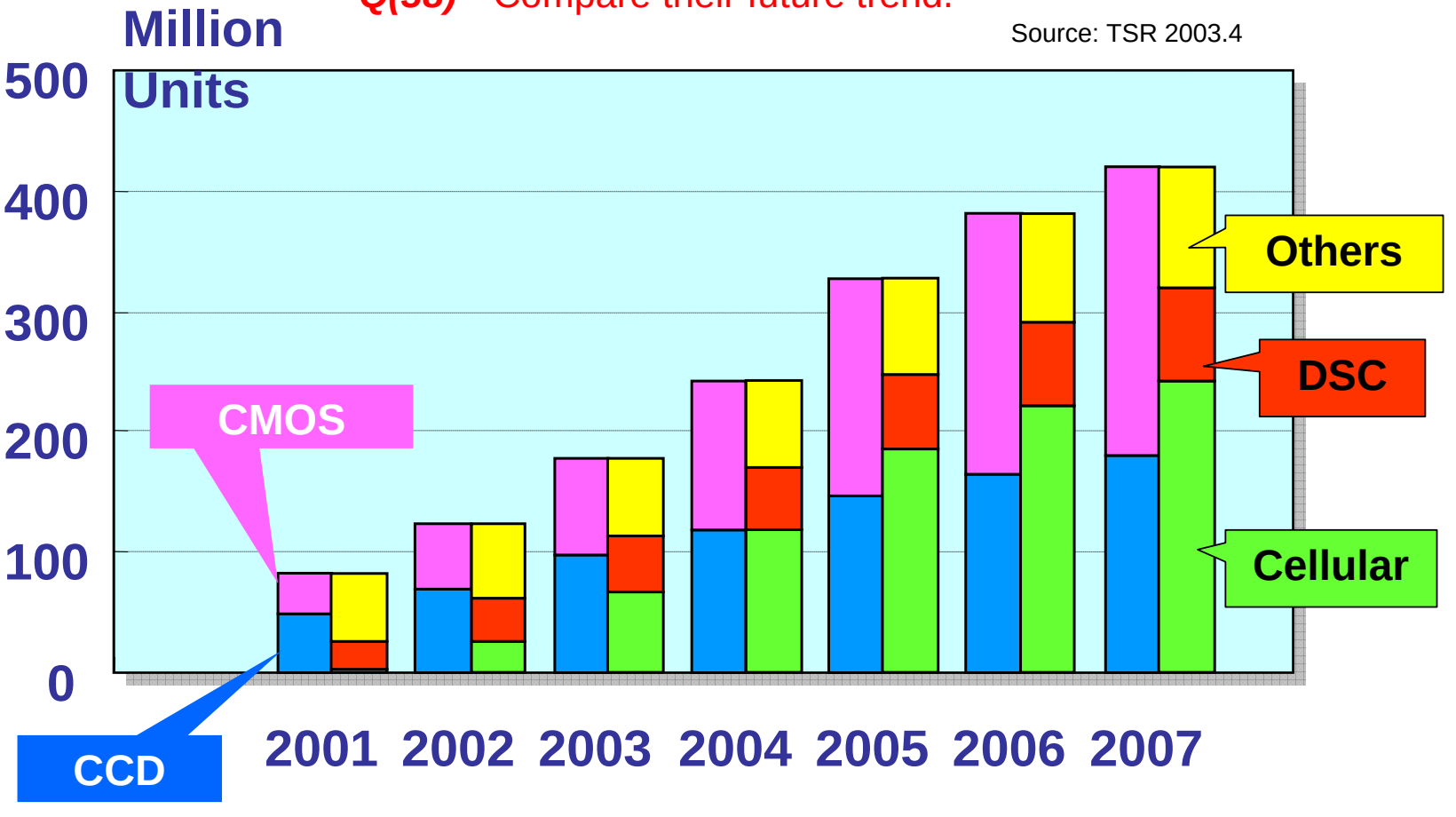
Paper# 6.6 **A 375×365 3D 1Kframe/s Range-finding Image Sensor with 394.5 kHz Access Rate and 0.2 Sub-Pixel Accuracy**

4) CMOS Sensor Technology

4.3) Current topics and future

Q(38) Compare their future trend.

Source: TSR 2003.4

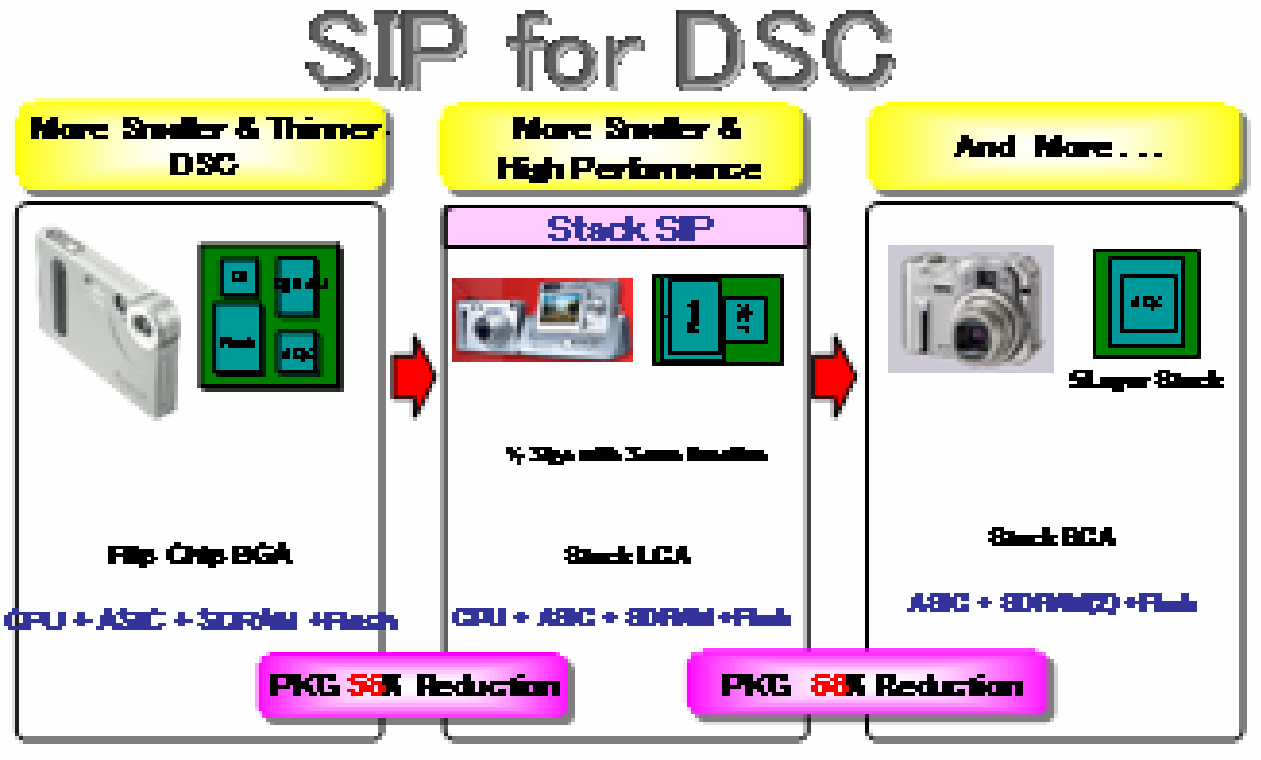


After Dr.Tsugio Makimoto(Sony), presented at Future Horizon, IEF2004

5) Circuits and Module Technology

5.1) Role of circuits and module technology

***Q(39)* Is it important ?**

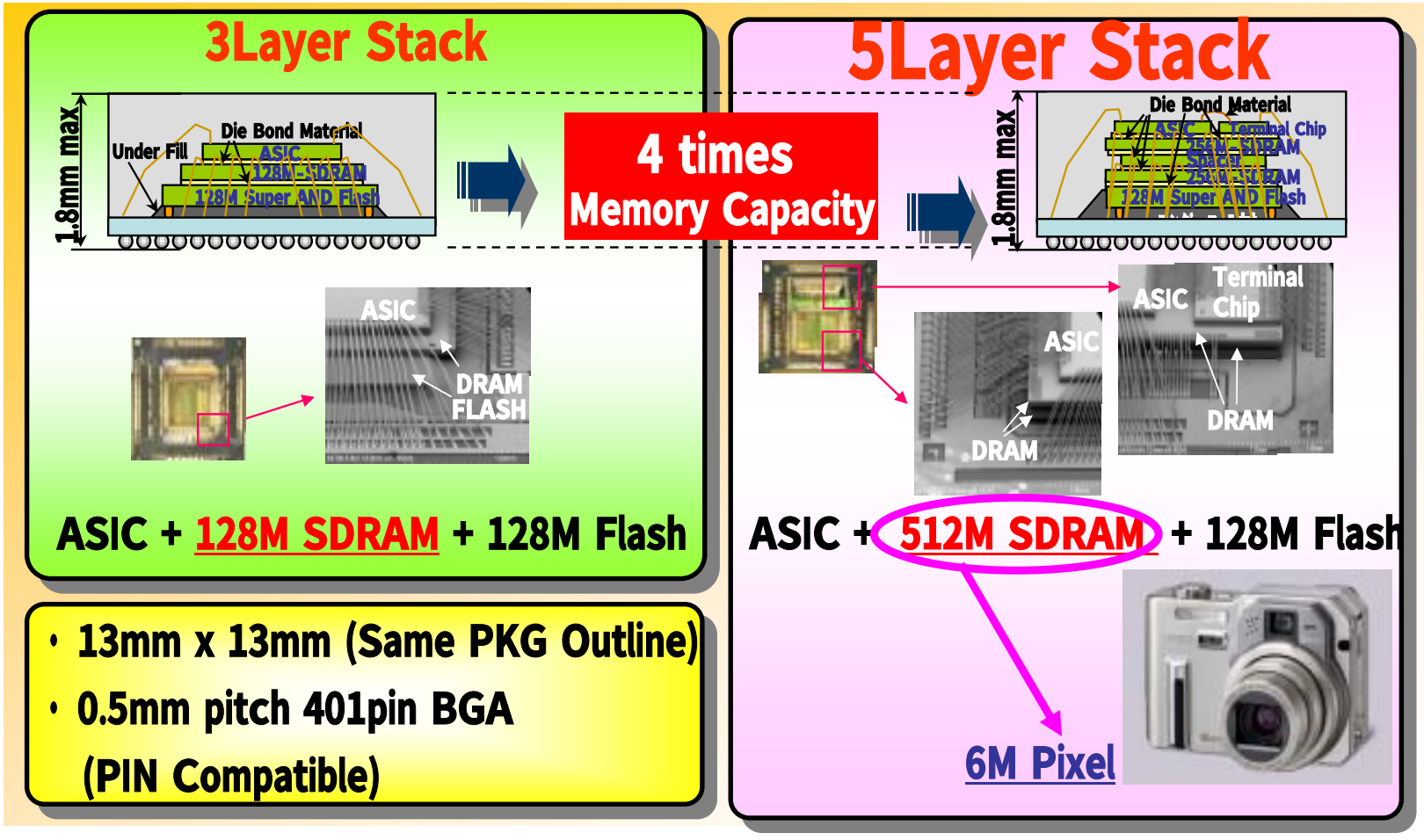


Courtesy of Dr.Toshihisa Sato, Renesas(1/4)
SSDM2004, Short Course, Sept 14 2004, Tokyo Japan

5) Circuits and Module Technology

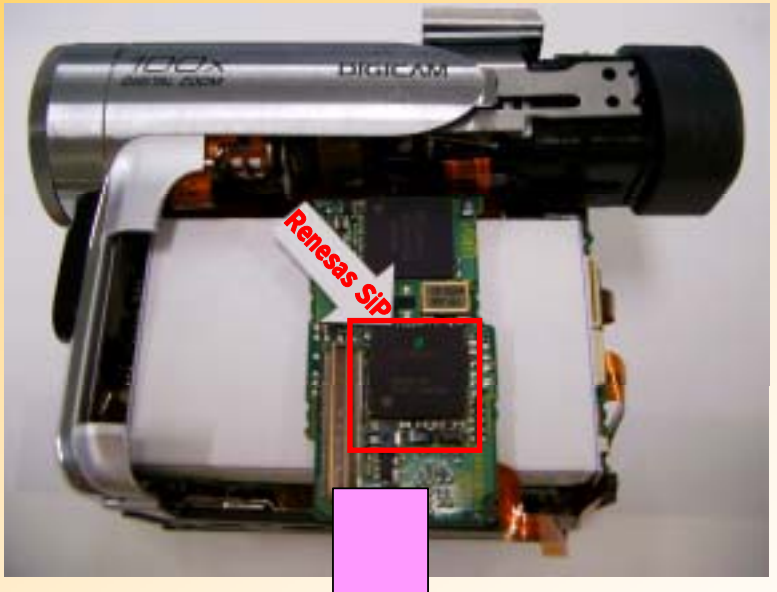
5.1) Role of circuits and module technology

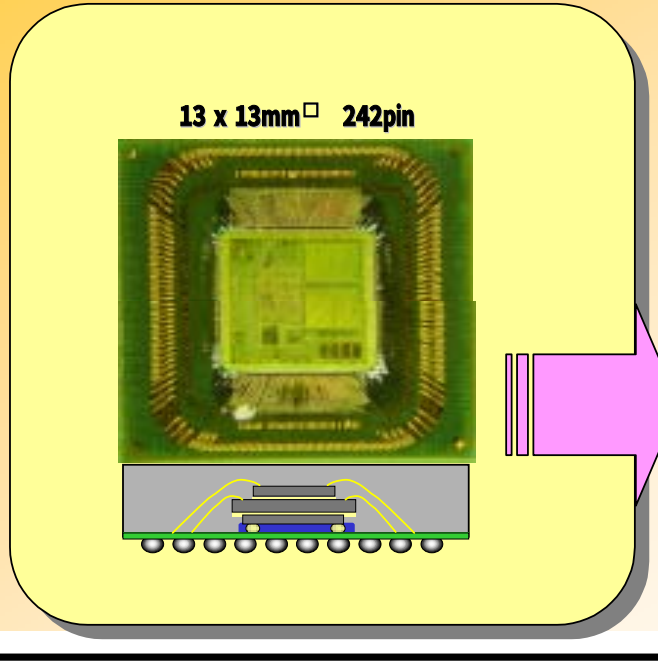
Courtesy of Dr.Toshihisa Sato, Renesas(2/4)

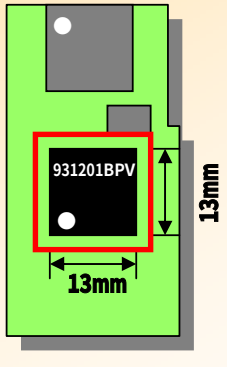


5) Circuits and Module Technology

5.1) Role of circuits and module technology







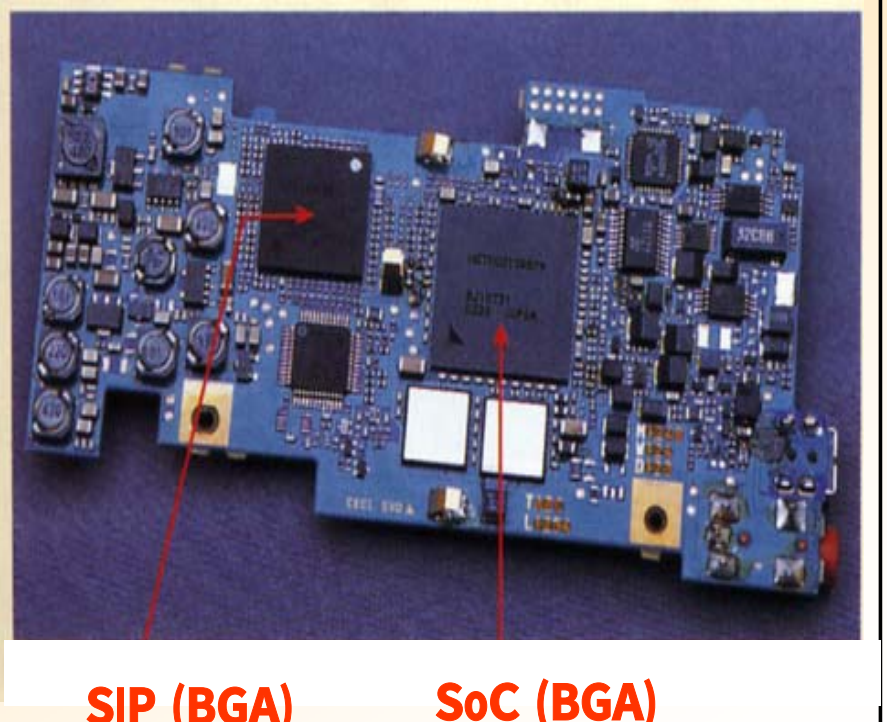
Courtesy of Dr.Toshihisa Sato, Renesas(3/4)

5) Circuits and Module Technology

5.1) Role of circuits and module technology

Courtesy of Dr.Toshihisa Sato, Renesas(4/4)

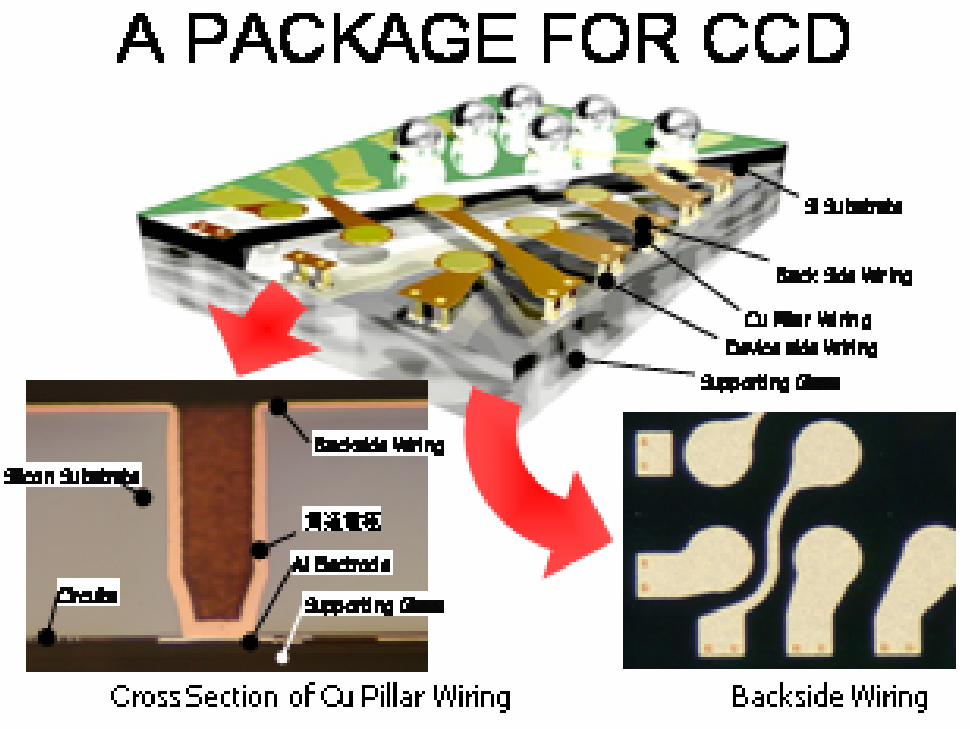
Stack Type SIP



SIP (BGA) SoC (BGA)

5) Circuits and Module Technology

5.1) Role of circuits and module technology

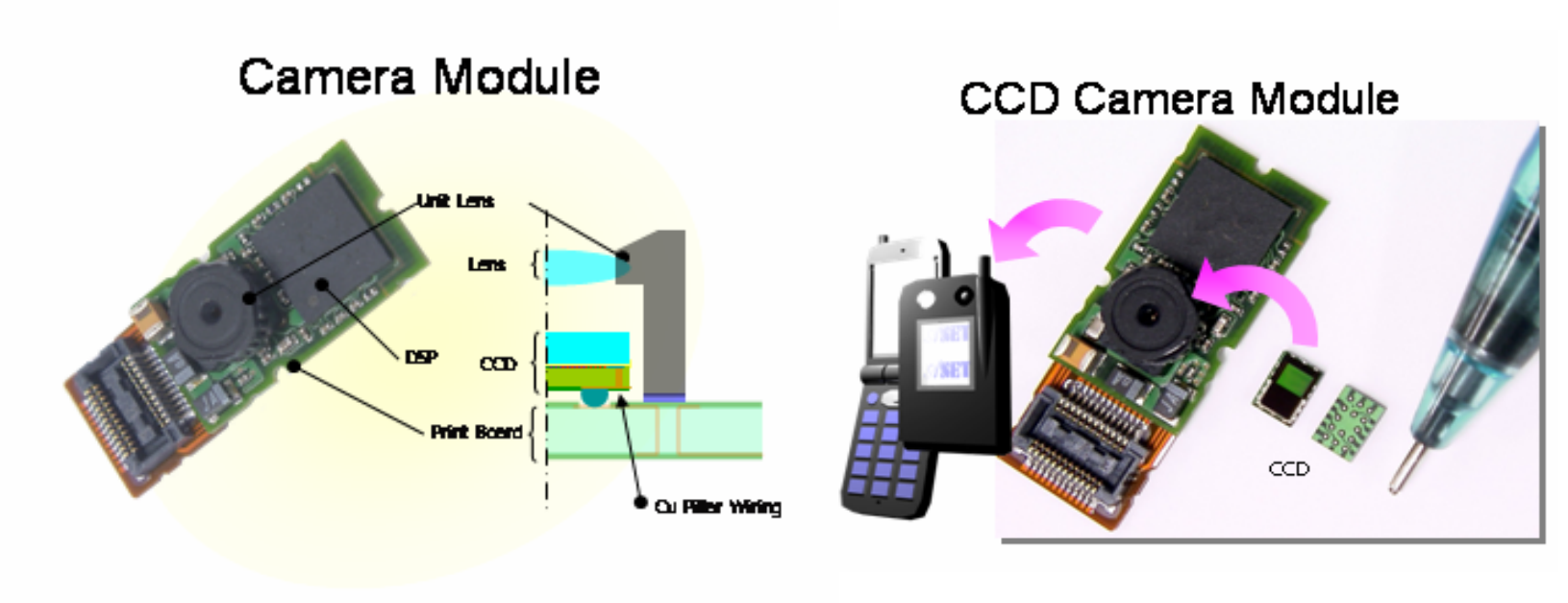


Courtesy of Dr.Kenshi Takahashi, ASET

Ref(40) SSDM2004, Short Course, Sept 14 2004, Tokyo Japan

5) Circuits and Module Technology

5.1) Role of circuits and module technology



Courtesy of Dr.Kenshi Takahashi, ASET
Ref(40) SSDM2004, Short Course, Sept 14 2004, Tokyo Japan

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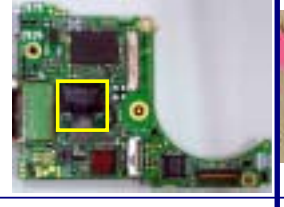
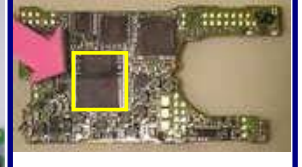
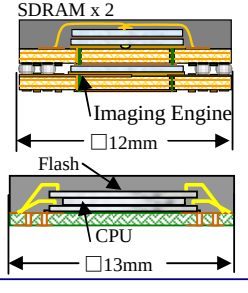
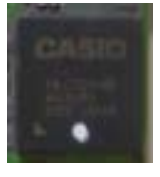
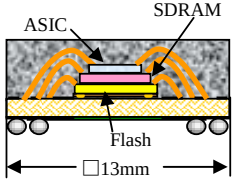
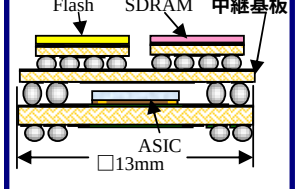
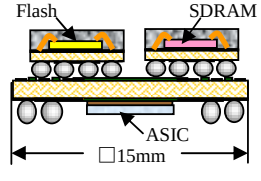
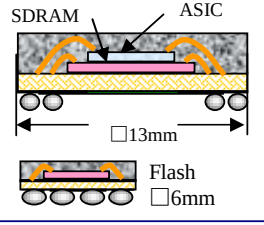
	SONY	CASIO	Canon	KYOCERA	FUJIFILM
set	DSC-T1 	EXILIM CARD S-100 	IXY DIGITAL 40/50 	Contax i4R 	FinePix A340 
brd					
SiP	 	 	 	 	 
	313mm2	169mm2	169mm2	225mm2	205mm2

SiP RoadMap

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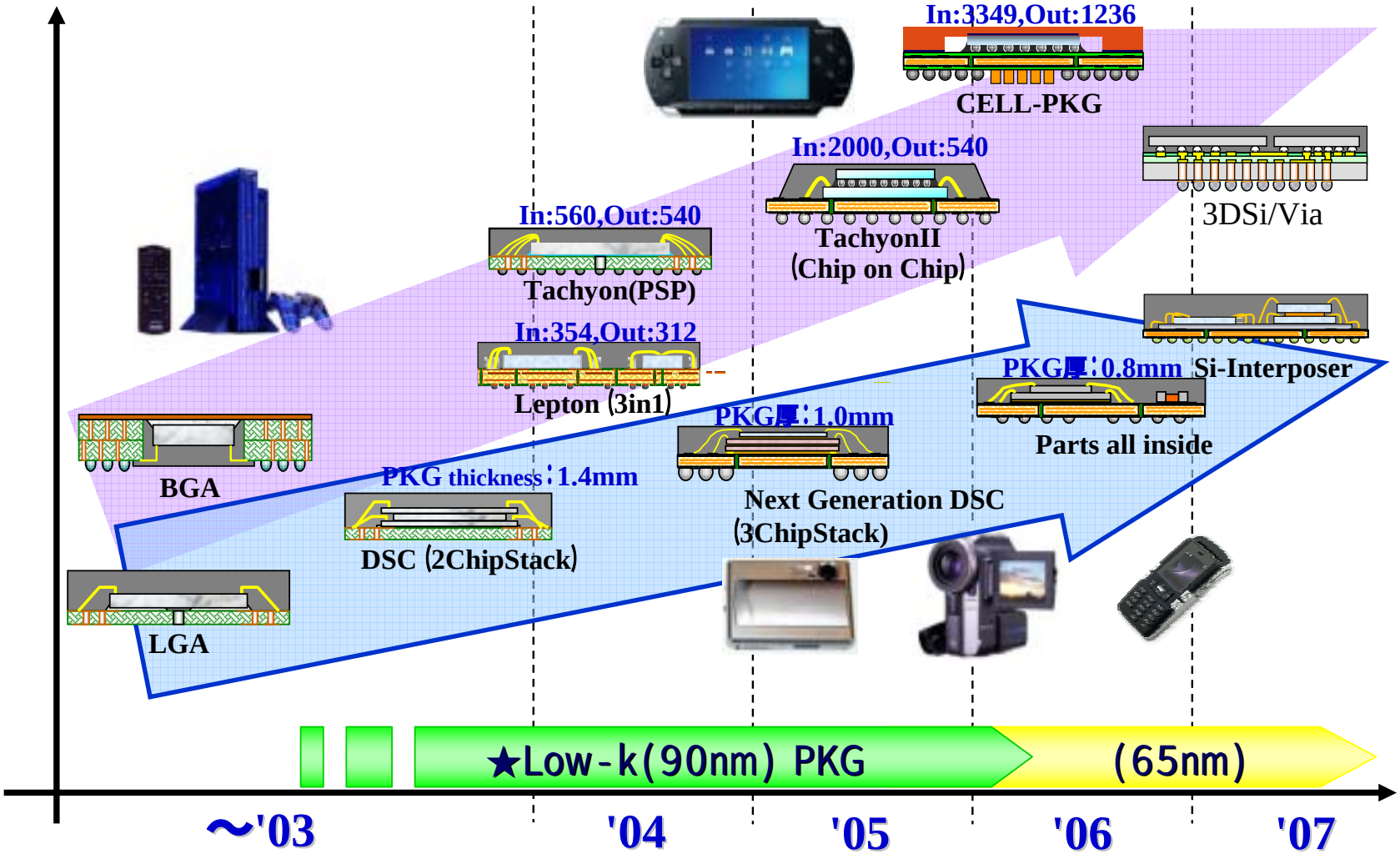

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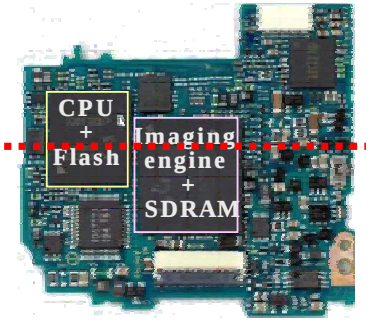
SiP Mother-board Less

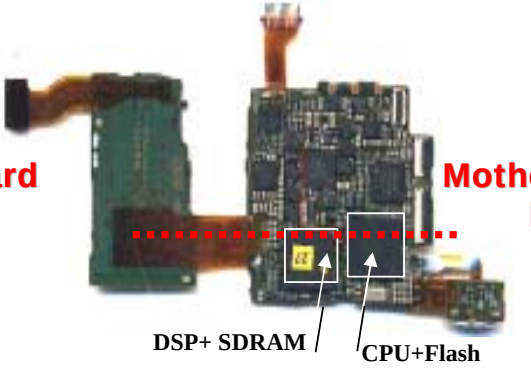
'03 Model (P10)

'04Model (T1)

Ultra-thin type DSC

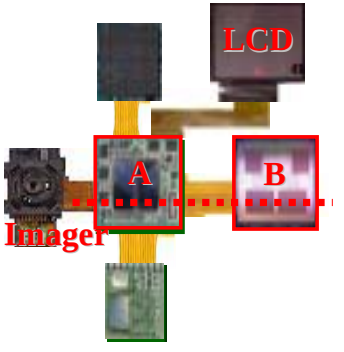


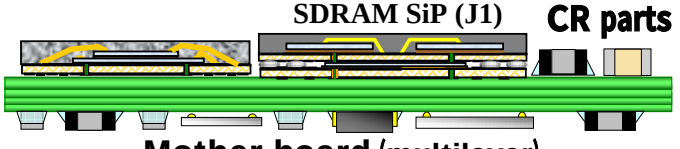
Mother board shrink



Mother board less

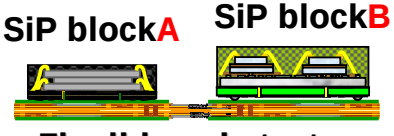
※ SiP Function block





Mother board (multilayer)

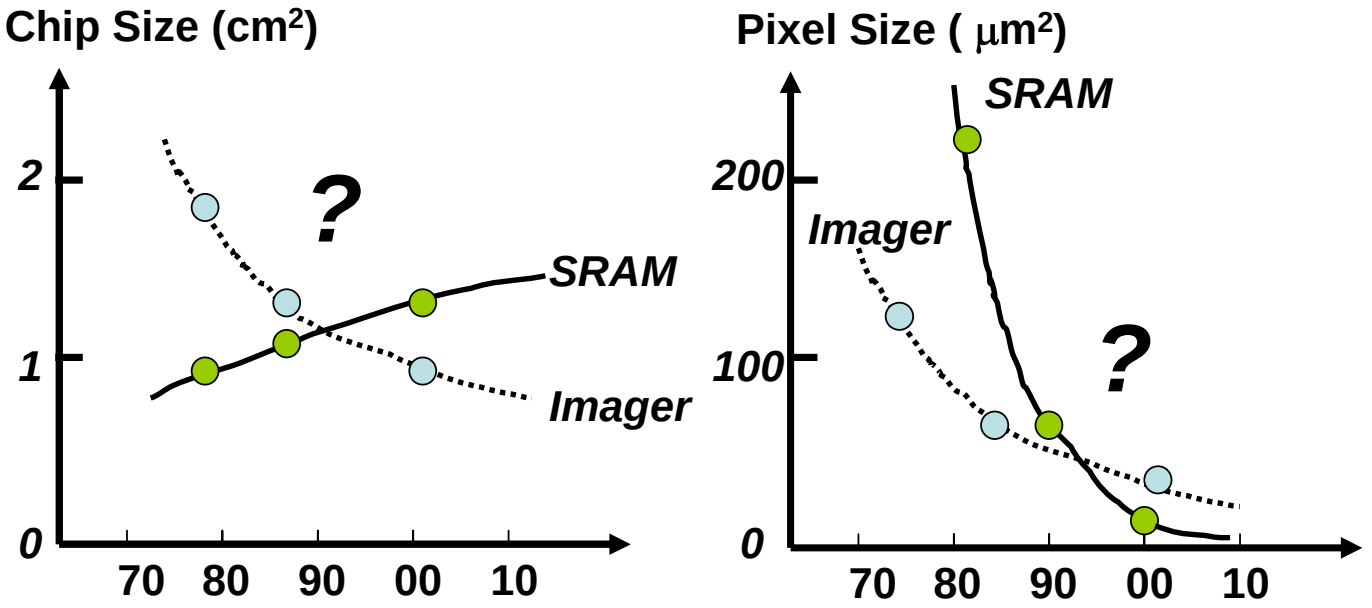
Mother board (multilayer)



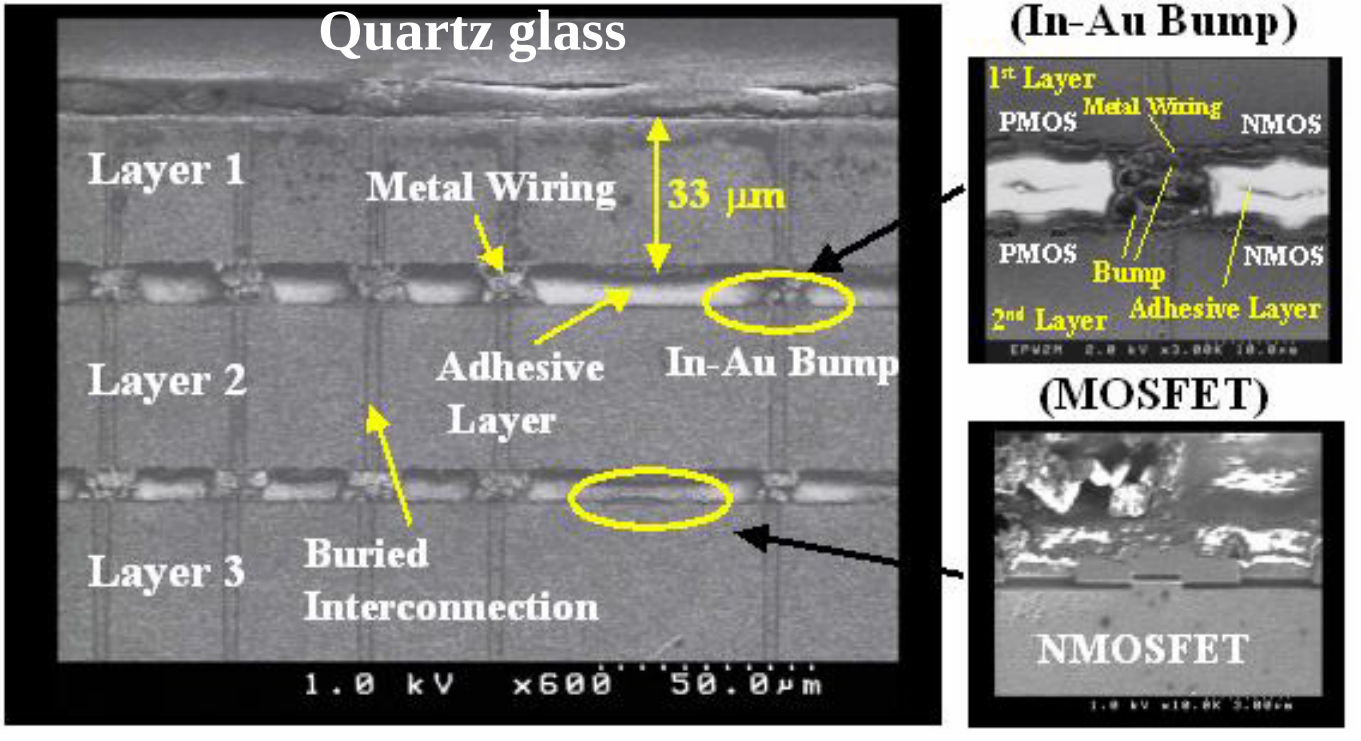
Flexible substrate

Q(40) Explain imager and LSI technology Scaling Trends

Ref(35) Yoshiaki Hagiwara, CCD79, Edinbough Sept 18-19, 1979
Ref(36) Yoshiaki Hagiwara, 1983-1996

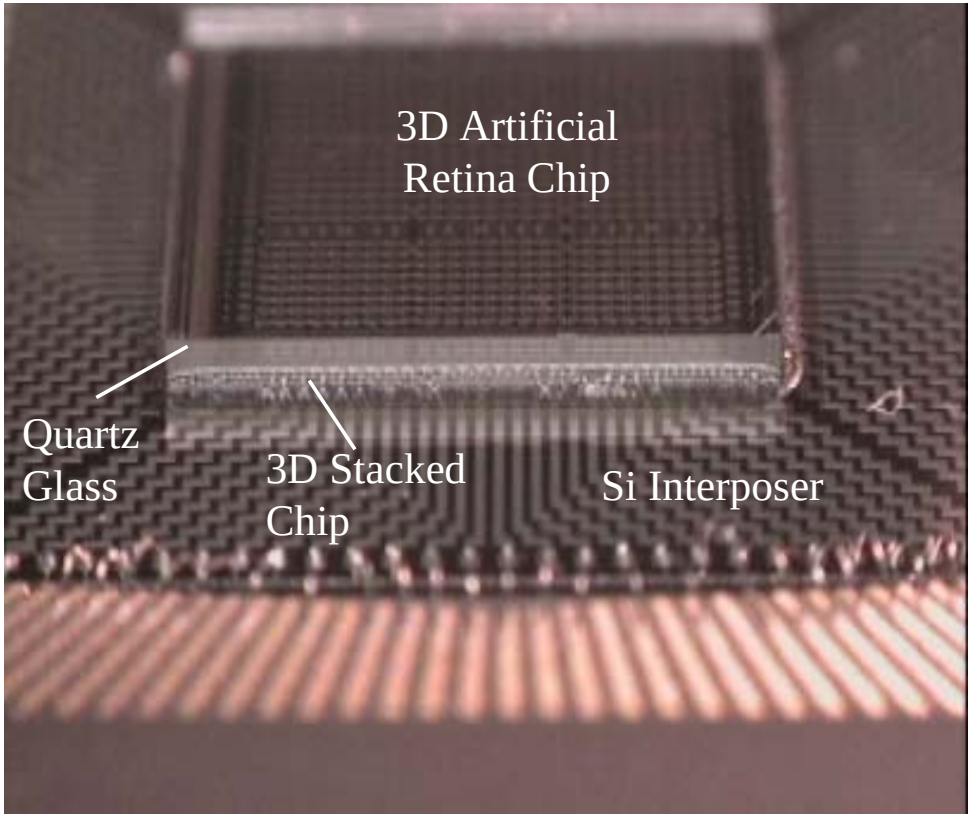


SEM Cross Section of 3D Artificial Retina Chip



Source: Prof.M.Koyanagi @ Tohoku University

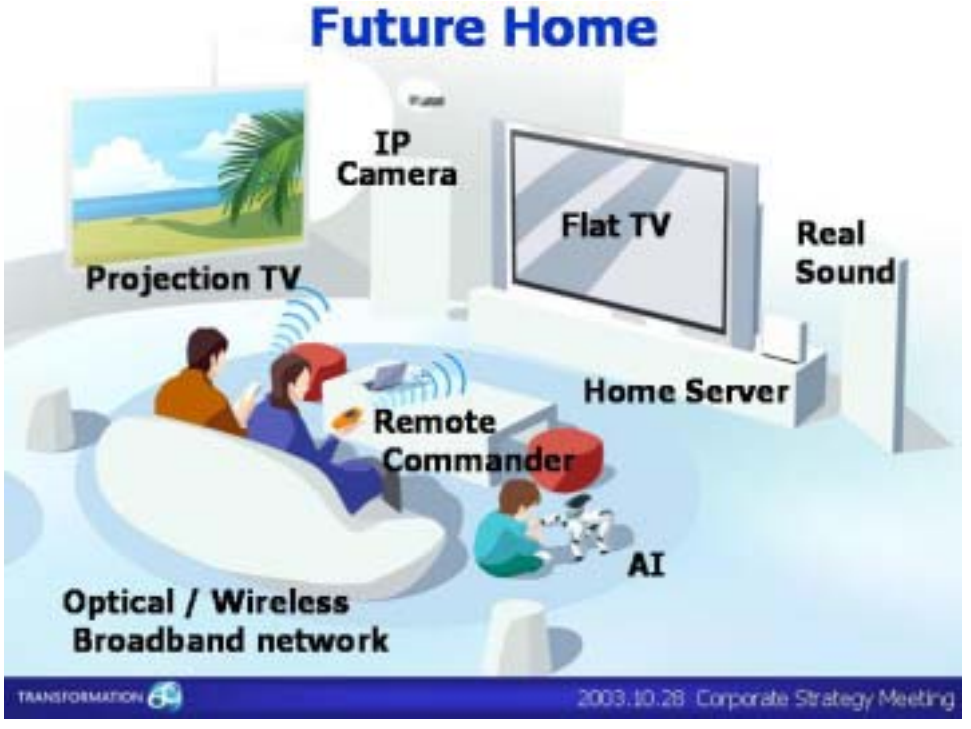
Three-Dimensional Artificial Retina Chip



Source: Prof.M.Koyanagi @ Tohoku University

Image sensors in CMOS achieving CCD pixel pitches and quality will continue to drive the technology into the emerging mass markets for cell phones and Digital Still Cameras with analog design techniques to reduce readout noise in conventional CMOS Extended dynamic range image sensing, that does not sacrifice the low light or other imaging performance parameters for eventual use in non-machine vision applications.

And 3D imaging is a potential enabling technology for the virtual world, with impact on human- interface technologies, robotics, and metrology . Sight-restoration electronics will likely provide enormous medical and economic opportunities.



7) Reference

Ref(1) Yoshiaki Daimon-Hagiwara et al, “A 380H x 488V CCD Imager with Narrow Channel Transfer Gate", p.335-340, Proceeding of the 10th Conference on Solid State Devices, Tokyo, 1978.

Ref(2) Yoshiaki Daimon (Hagiwara) et al, "Final Stage of Charge Transfer Process in Charge Coupled Devices", IEEE Transaction on Electron Devices, Vol.Ed-21,No.4,April 1974, pp.266-272

Ref(3) Yoshiaki Daimon (Hagiwara) et al, "Charge Transfer in Buried Channel Charge Coupled devices, ISSCC1974, Dig. Tech. Paper, Philadelphia,PA, Feb 1974,pp.146-147

Ref(4) M. Fujita and H. Kitano:"{{D}evelopment of and {A}utonomous {Q}uadruped {R}obot for {R}obot {E}ntertainment}", Autonomous Robots vol.5, pp.7-8, Kluwer Academic Publishers, 1998.

Ref(5) Kohtaro Sabe, ” Architecture of Entertainment Robot - Development of AIBO ?”, IEEE Computer Element MESA Workshop 2001, Mesa Arizona, Jan 14-17, 2001

Ref(6) Yoshiaki Hagiwara, “ Measurement technology for Home Entertainment LSI Chips”, a key note presentation at the tutorial session in ICMTS2001, Kobe Japan, March 19-22, 2001

Ref(7) Shin-ichi Yoshimoto et al, "A 48kframes/sec CMOS Image Sensor for Real-Time 3-D Sensing and Motion Detection", ISSCC2001, Tech Dig Paper pp.76-77

Ref(8) See for example pp.58-65 of Authur Beiser “Concepts of Modern Physics” ISBN 0-07-004814-2. On Page 62, Sony‘s 8mm Video Camera is taken as a modern tool to change photons to electrons !

Ref(9) Iconoscope by Zworykin, RCA Report 1933 in Vacuum Tube Era

Ref(10) Andy Grove "Physics and Technology of Semiconductor Devices“ that I studied in 1969-1971 in APh181 taught by Prof.James McCaldin, my life- long Mentor.

Ref(11) Feymann Physics Course I learned in 1967-1969 at CalTech Pasadena Calif as an undergraduate student for my freshman and sophomore years.

Ref(12) Motoaki Abe, et al "A CCD Imager wih SiO2 Exposed Photosensor Arrays", IEDM 1977

7) Reference

Ref(13) Yoshiaki Daimon-Hagiwara, "Two Phase CCD with narrow-channel transfer regions", Proc. 9th Conference Soild State Devices, Tokyo Japan,1977 pp.255-261

Ref(14) I.Kajino,M.Shimada,Y.Nakata,Y.Hirata, and Y.Hagihara(Hagiwara),"Single Chip Color Camera Using Narrow Channel CCD Imager with Overflow Drain", Technical Report at Japan Society of Television Workshop on Dec 16, 1981, TED 76-6, ED 611 (in Japanese)

Ref(15) Y.Ishihara,E.Takeuchi,N.Teanishi,A.Kohono,T.Aizawa,K.Arai,H.Shiraki,"CCD Imager for Single Sensor Color Camera," ISSCC1980 Tech Dig Paper pp.24-25

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Ref(17) A 492 x 400 IT CCD with OFD stripes for a Single Sensor 2/3 Color Camera by A.Furukawa et al, Toshiba, pp.346 IEDM 80

Ref(18) No Image Lag Photo Diode Structure in the IT CCD Imager by Nobukazu Teranishi et al pp.324, IEDM 82

Ref(19) JP 1215101 (a Japanese Patent #58-46905), Nov 10, 1975 by Yoshiaki Hagiwara

Ref(20) Interline CCD Image Sensor with an Vertical Anti Blooming Structure by Yasuo Ishihara, et al pp.168, ISSCC82

Ref(21) A.Khono,N.Teranishi and Y.Ishihara, "A Design consideration on p-well structure for solid-state image sensors",IEDM 1984, pp.24-27

Ref(22) B.C.Burkey, W.C.Chang,J.Littlehale,T.H.Lee,T.J.Tredwell, J.P.Lavine, E.A.Trabka, "The pinned photodiode for an interline-transfer CCD Image Sensor", IEDM 1984, pp.28-31

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Ref(25) Takashi Shimada, Yasuo Kakno and Junichi Aoyama “An Analysis of Video Defects observed in an Interline Transfer CCD Imager”, Abstract No.153, The Electrochemical Society Spring Meeting at St.Louis, May 1980

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Ref(27) ICX016 2/3 inch 190K pixel IT imager, a long seller imager for 15 years developed Oct 1981, for one chip color camera also used in XC-37, a servaillance camera pioneered by Hiroshi Murata and Takashi Shimada.

Ref(28) T.Kumezawa et al, "High Resolution CCD Image Sensors with Reduced Smear," in IEEE Transactions on Electron Device, vol.ED-32, no/8, pp.1451-1456, Aug 1985

Ref(29) K.Ishikawa,M.Hamasaki,T.Suzuki,H.Kanbe,Y.Kagawa,K.Miyata, and K.Yonemoto "IT CCD Imaging Sensor with Variable Speed Electric Shutter", Proc of SPIE, Vol.1107, March 1989

Ref(30) M.Mifune,S.Ochi,A.Shibata and Y.Kanoh, "An Improvement on Structure of Charge-Coupled Devices", the 4th Conference on Solid State Device, Tokyo Aug 1972

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Ref(34) M.H.White "Characterization of Surface Channel CCD Image Arrays at Low Light Levels" IEEE J. Solid State Circuits, Vol.SC-9, No.1, pp.1-12, 1974

Ref(35) Yoshiaki Daimon-Hagiwara "Advances in CCD Imagers", an invited talk at CCD79, Edinbough, Scotland, September 18-19, 1979

Ref(36) Yoshiaki Hagiwara, "High Density and High Quality Frame Tansfer CCD Imager with Very Low Smear, Low Dark Current, and Very High Blue Sensitivity", IEEE Transaction on Electron Devices, Vol.43, no.12, Dec 1996. This 800H x 492 Narrow-channel Frame Transfer CCD Imager was actually developed in 1983.

Imaging Devices

Thank You !

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http://www.isscc.org/isscc/ http://www.coolchips.org/
http://www.ee.ed.ac.uk/ICMTS/ http://www.unf.edu/ccec/ieee/index.html

Thank You !

Imaging Devices

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http://www.isscc.org/isscc/
http://www.ee.ed.ac.uk/ICMTS/
http://www.coolchips.org/
http://www.unf.edu/ccec/ieee/index.html