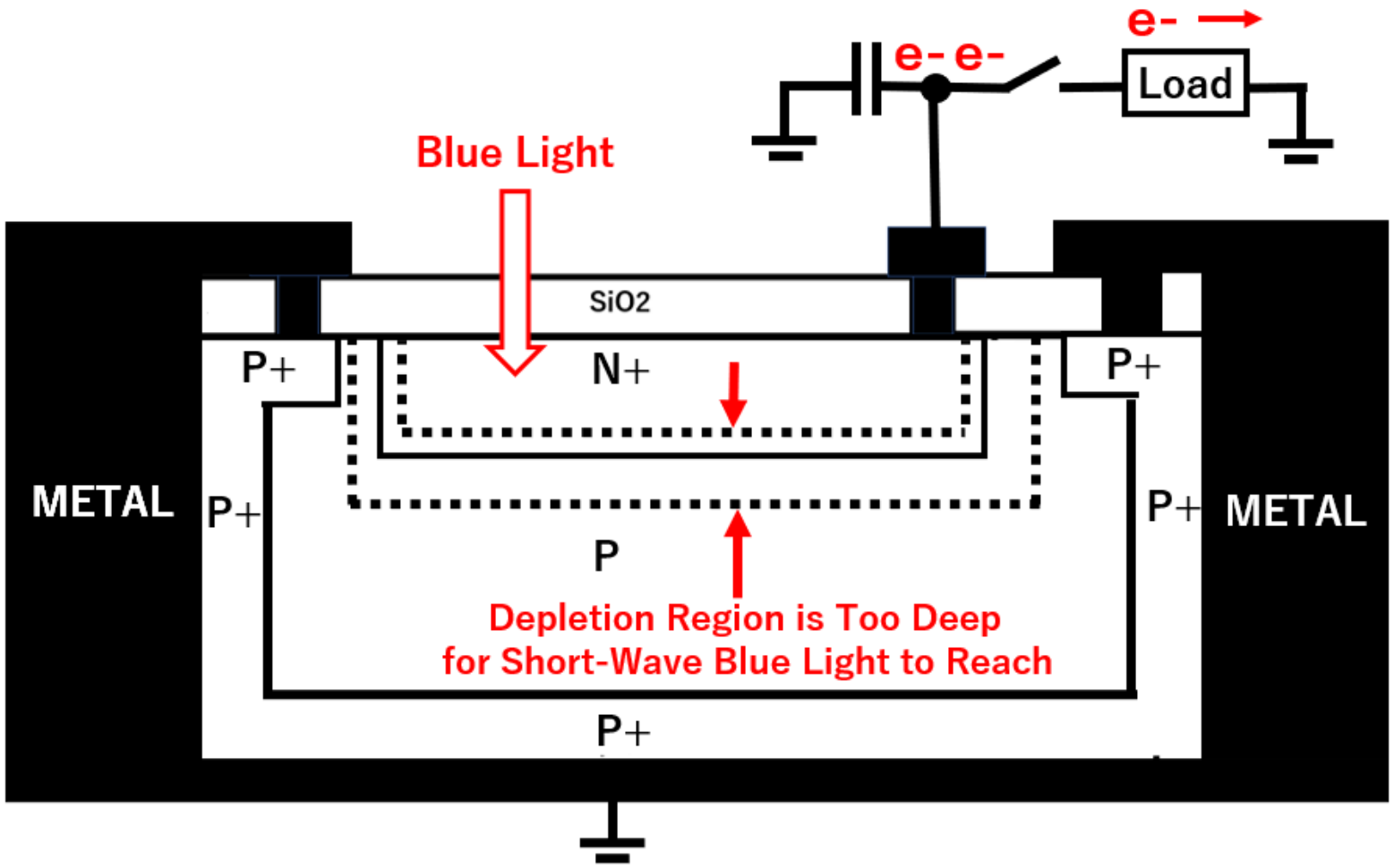
Conventional N+P Single Junction Structure type Solar Cell

Yoshiaki Hagiwara (AIPS), 2021.08.14

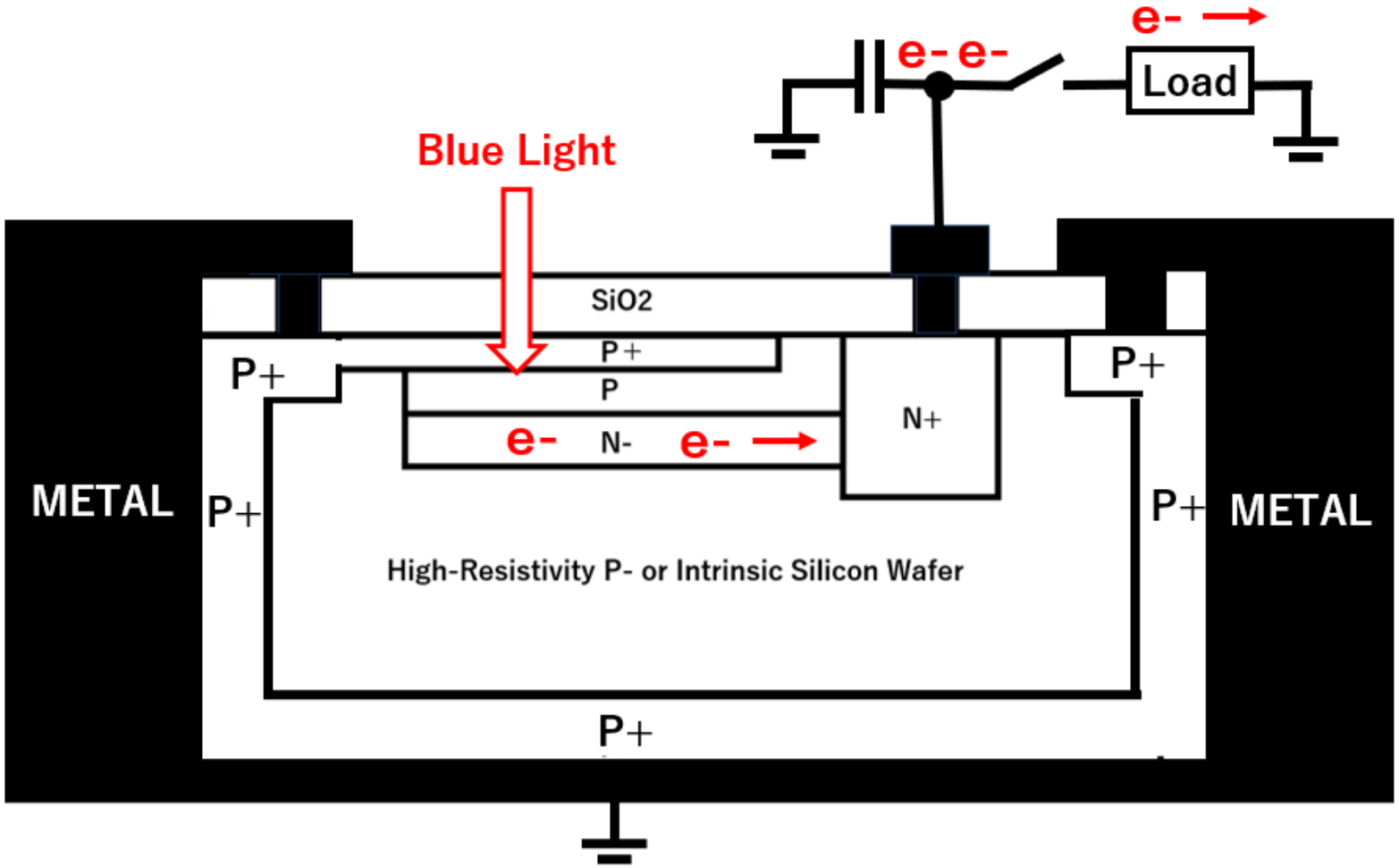
Short-Wave Blue Light does not penetrate more than 500 Å in depth thru the silicon crystal surface.
Most of the electron hole pairs generated at the silicon surface are recombined with no contribution.



Metallic Packaging with Grounded Metal Side-Walls

Pinned Buried P+PNIP+ Photodiode Structure type Solar Cell

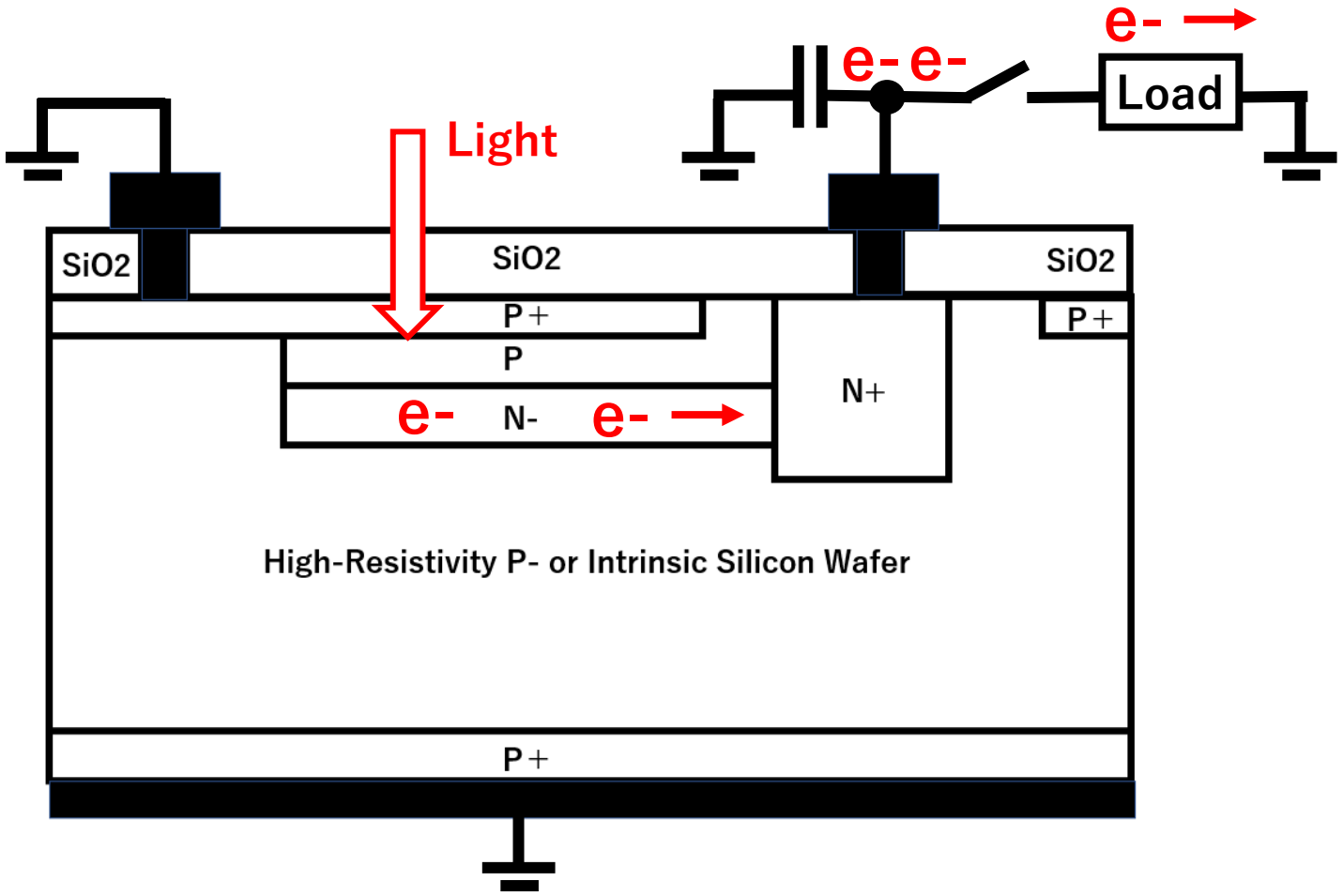
Short-Wave Blue Light does not penetrate more than 500 Å in depth thru the silicon crystal surface. However, the electron hole pairs generated at the silicon surface can be efficiently separated by the surface `P+P Barrier Electric Filed formed by Clever double Gaussian Doping-Engineering.

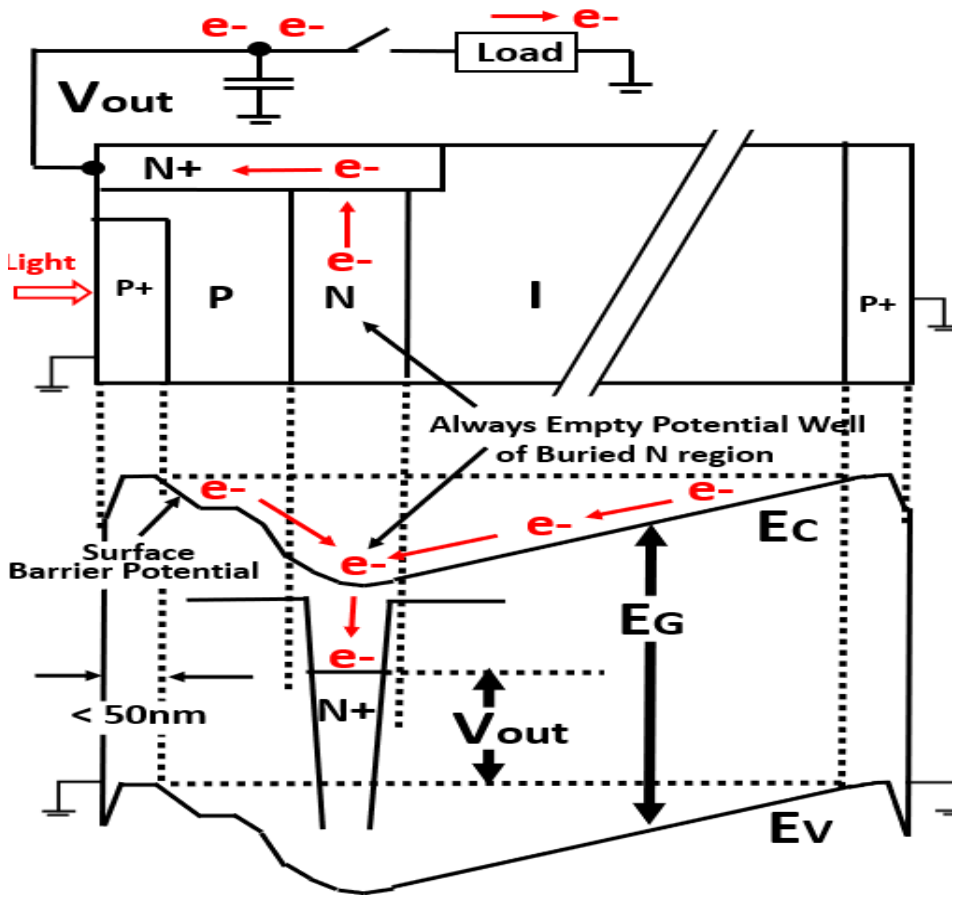


Metallic Packaging with Grounded Metal Side-Walls

Pinned Buried P+PNIP+ Photodiode Structure type Solar Cell

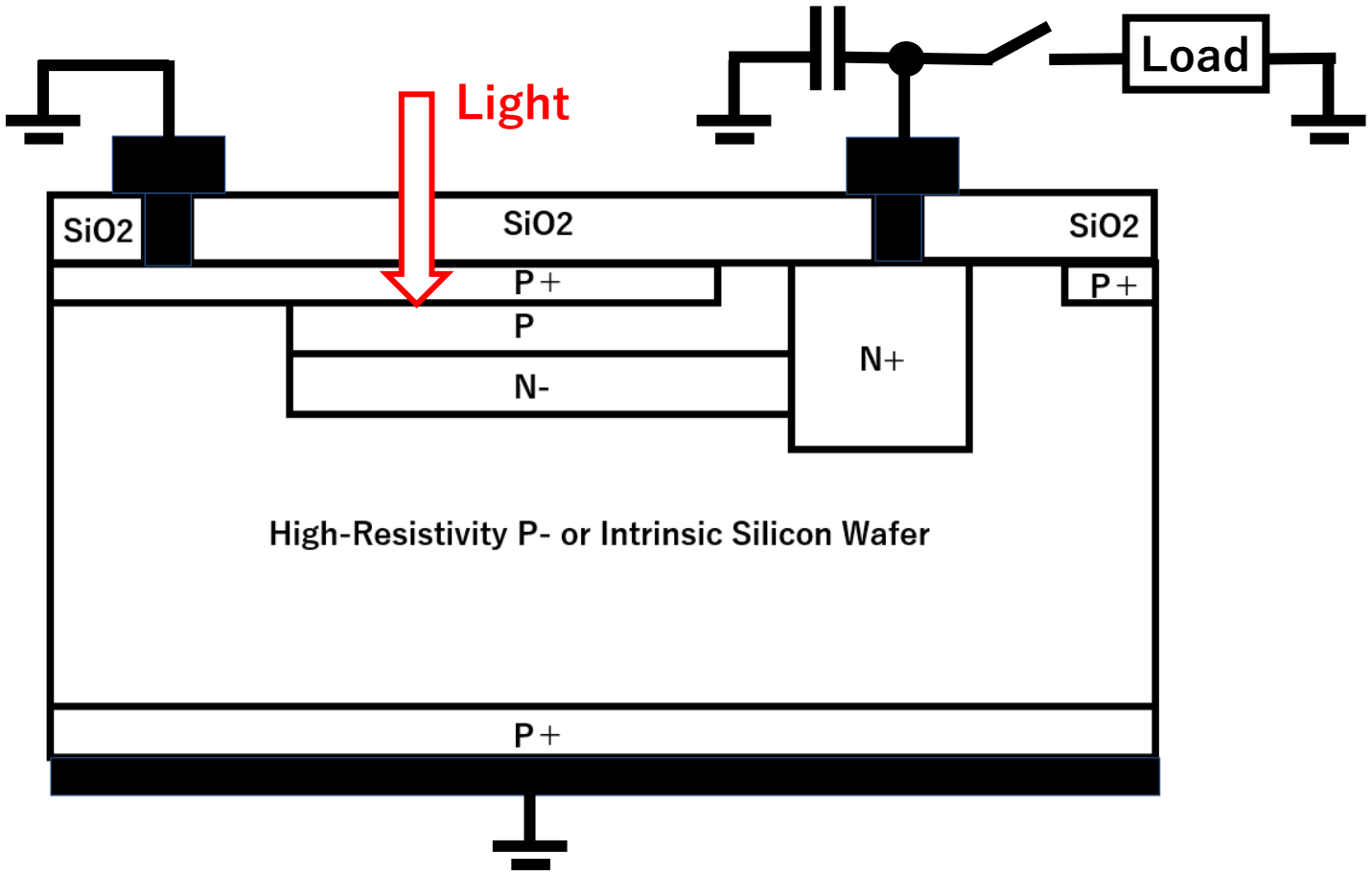
Yoshiaki Hagiwara (AIPS), 2021.08.11　（今作成しました）





Process Flow of P+PNIP+ Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021



MASK_01 is used at Step(3) to form a window for the photo charge collecting Buried PN junction region

MASK_02 is used at Step(7) of to form the surface heavily doped P+ region

MASK_03 is used at Step(9) to form the oxide window for the heavily doped N+ charge storage region

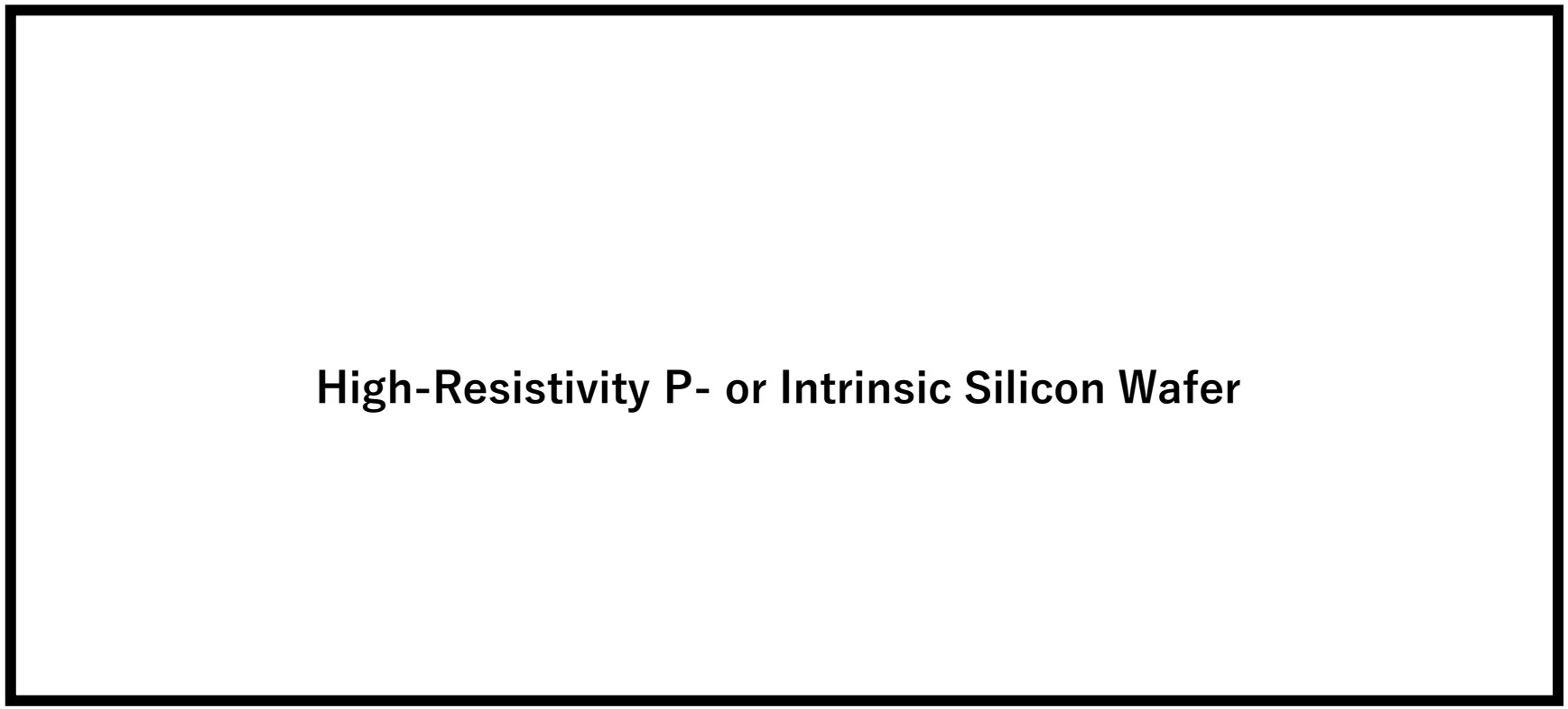
MASK_04 is used at Step(14) to form the metal contact windows

MASK_05 is used at Step(15) to form the metal wiring patterns.

Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

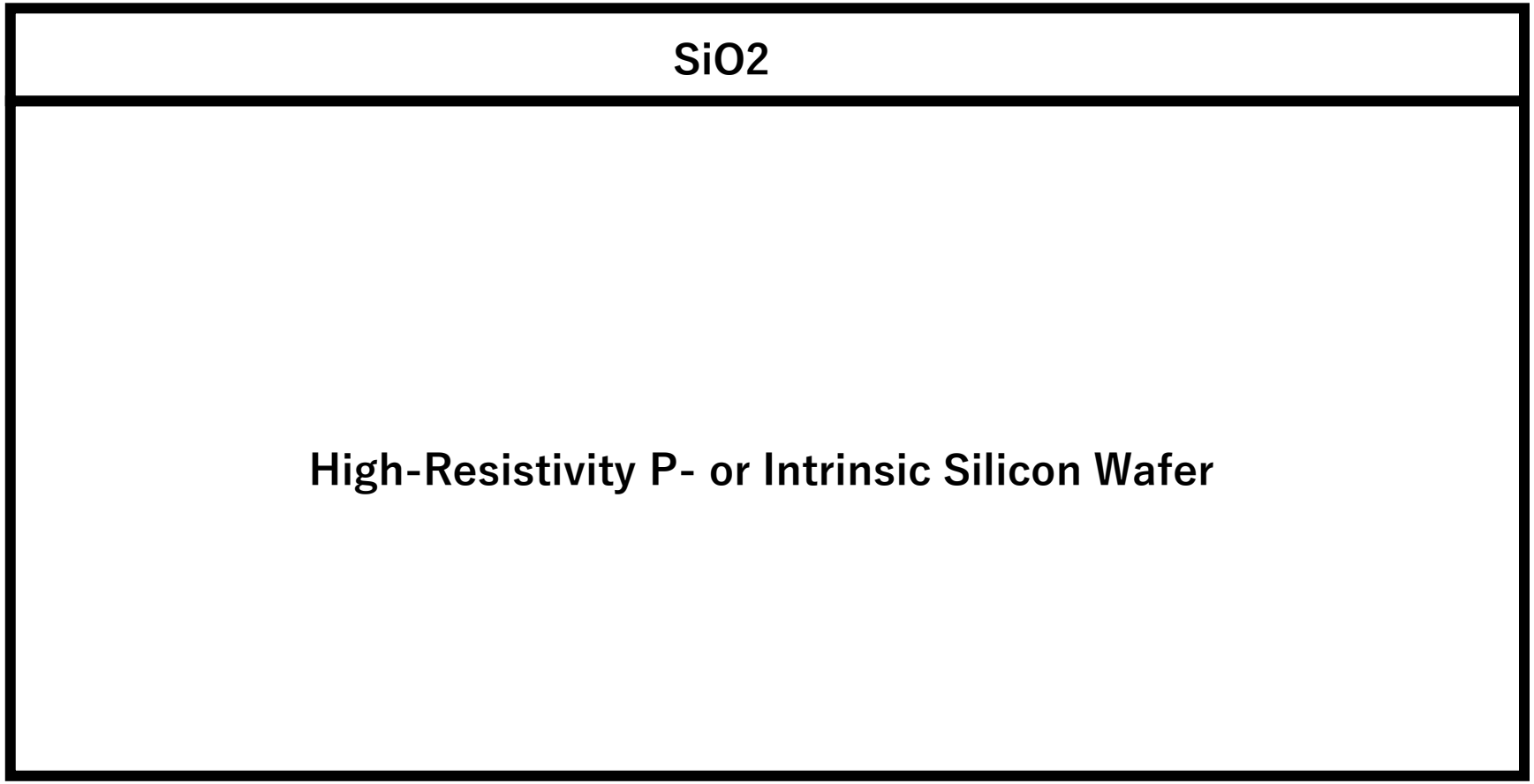
(1) Start with a very high-resistivity P- type or Intrinsic Silicon Wafer



Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

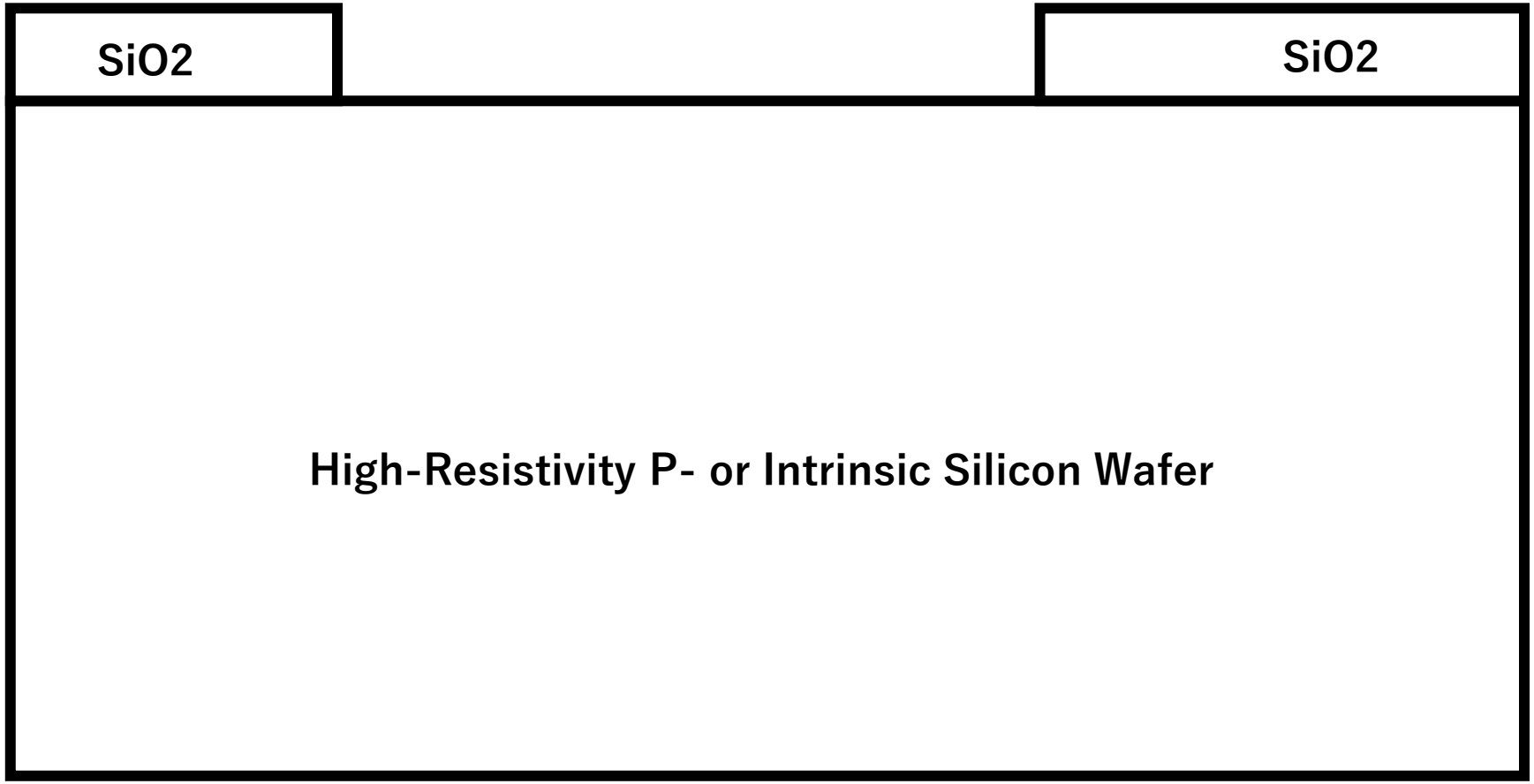
(2) Form the first thick protection SiO2 layer on the top surface



Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

(3) Form a window for the photo charge collecting Buried PN junction region

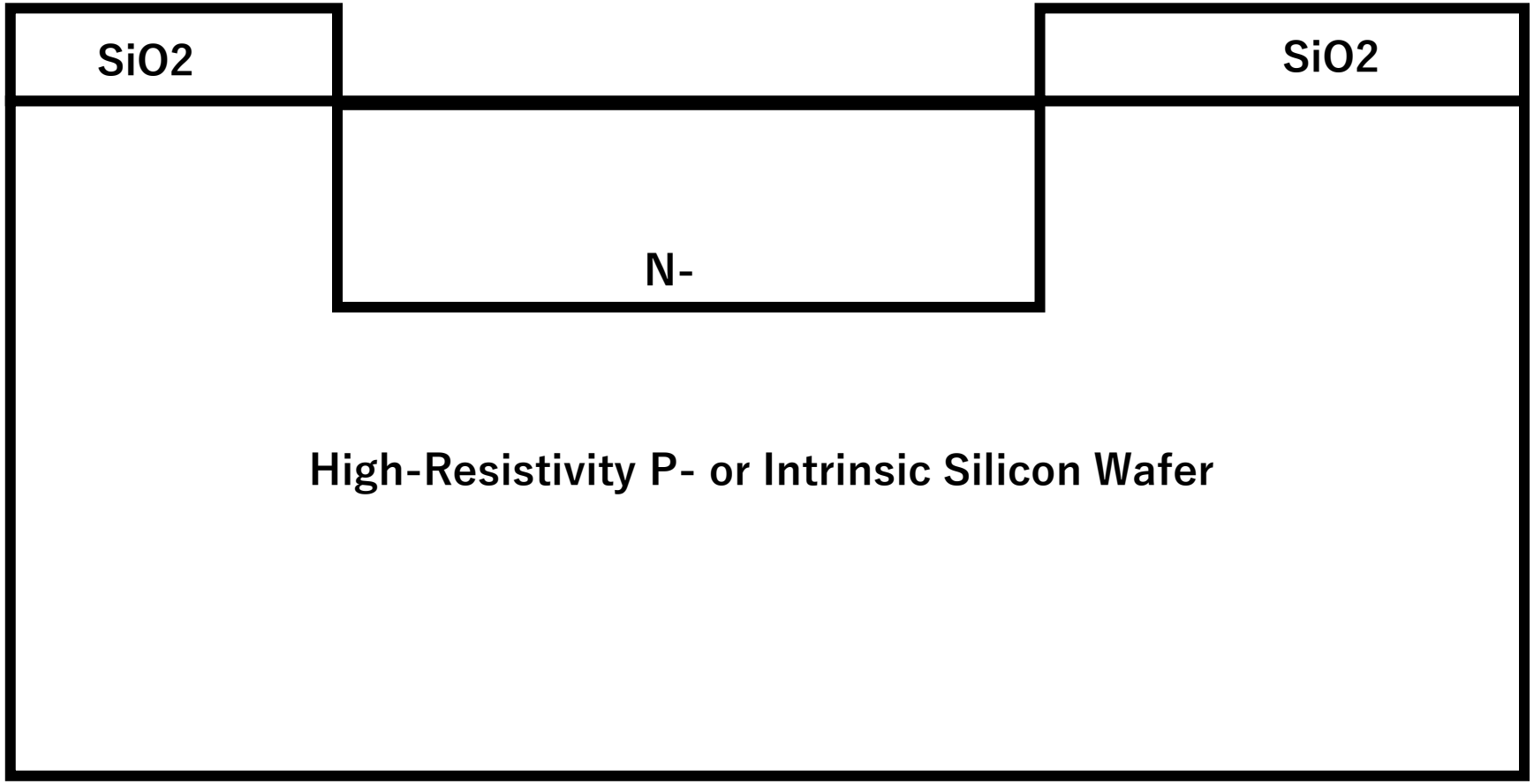


MASK_01

Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

(4) Form the photo charge collecting junction region by ion implantation.

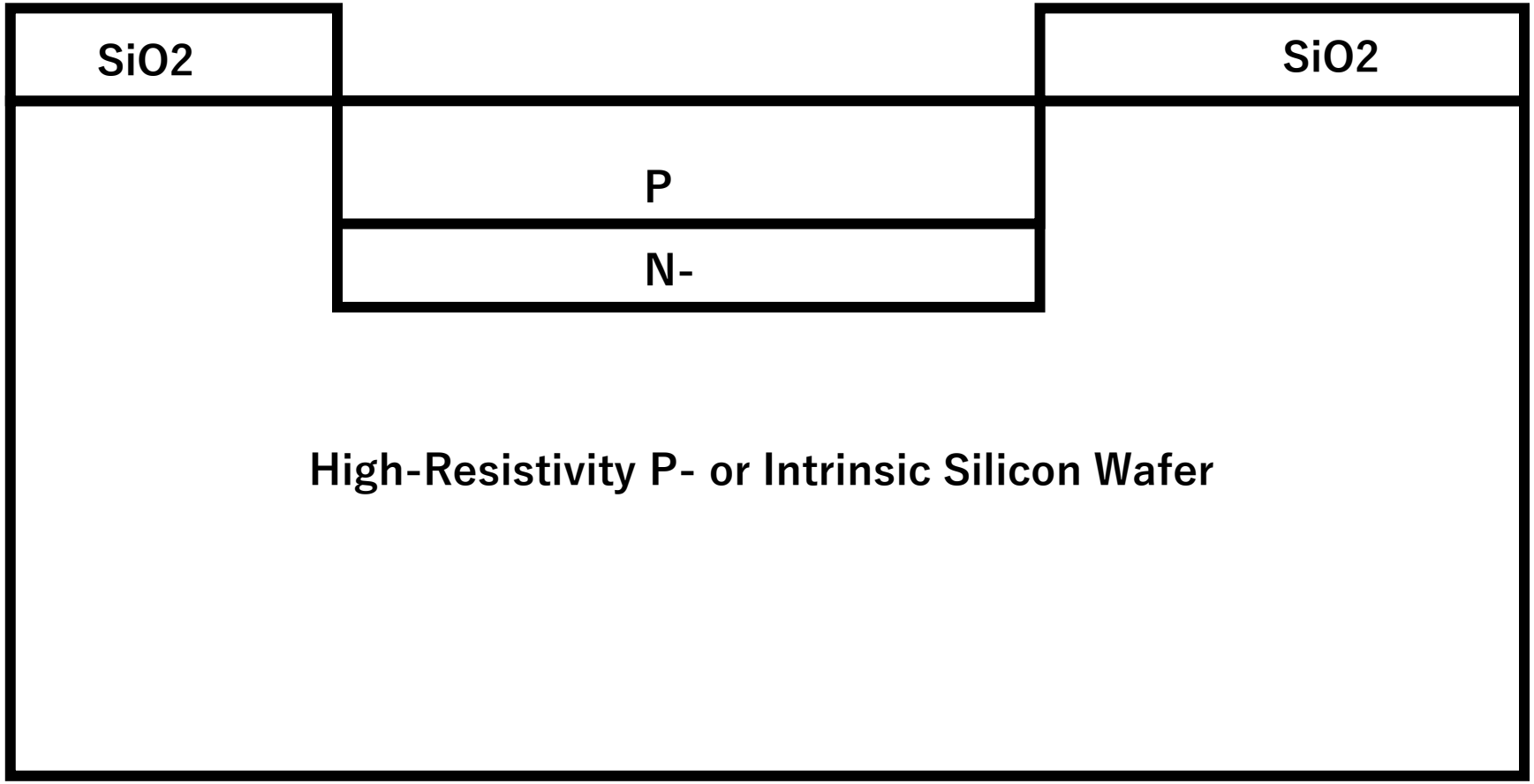


MASK_01

Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

(5) Form the surface P region by ion implantation.

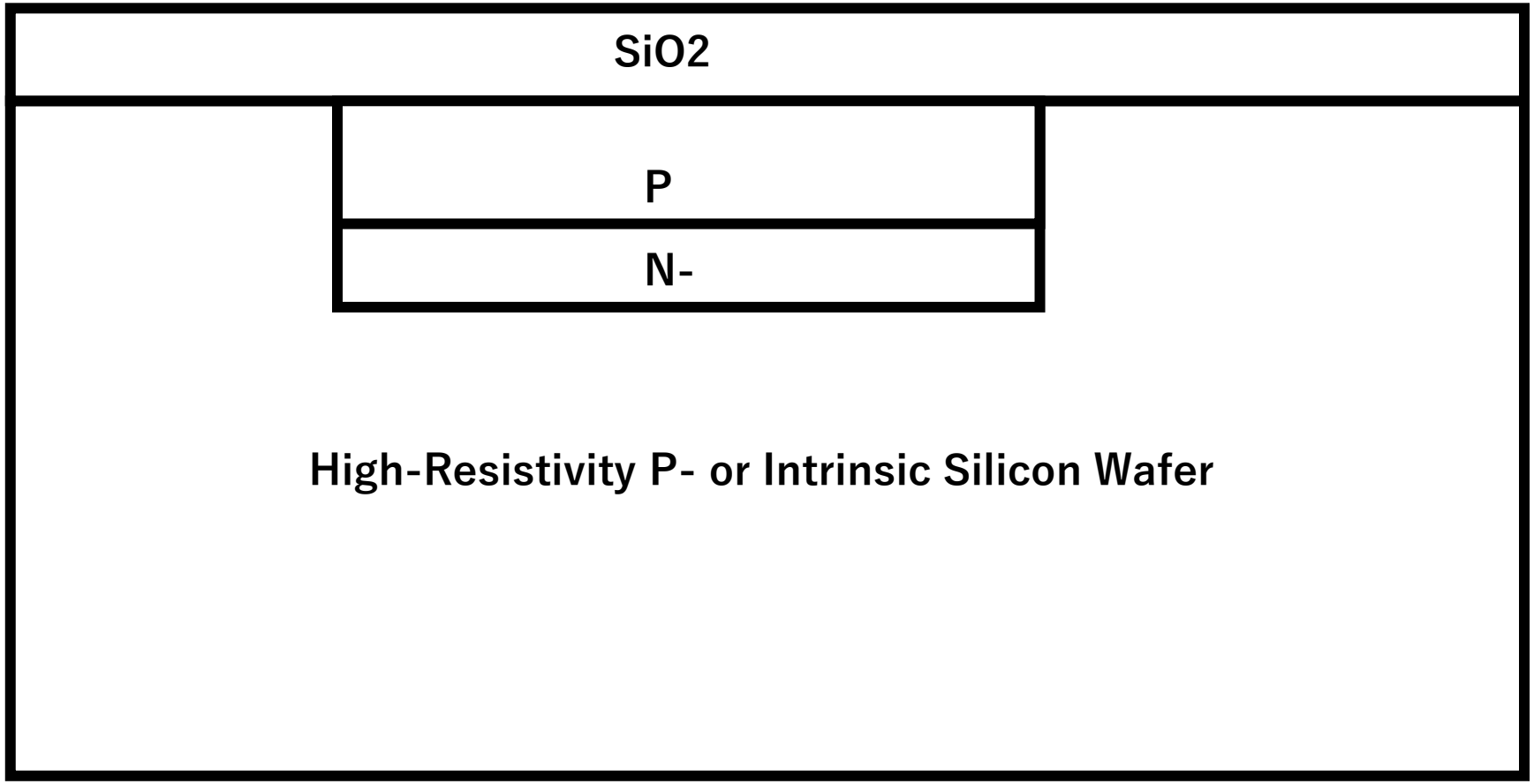


MASK_01

Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

(6) Form the second protection oxide layer

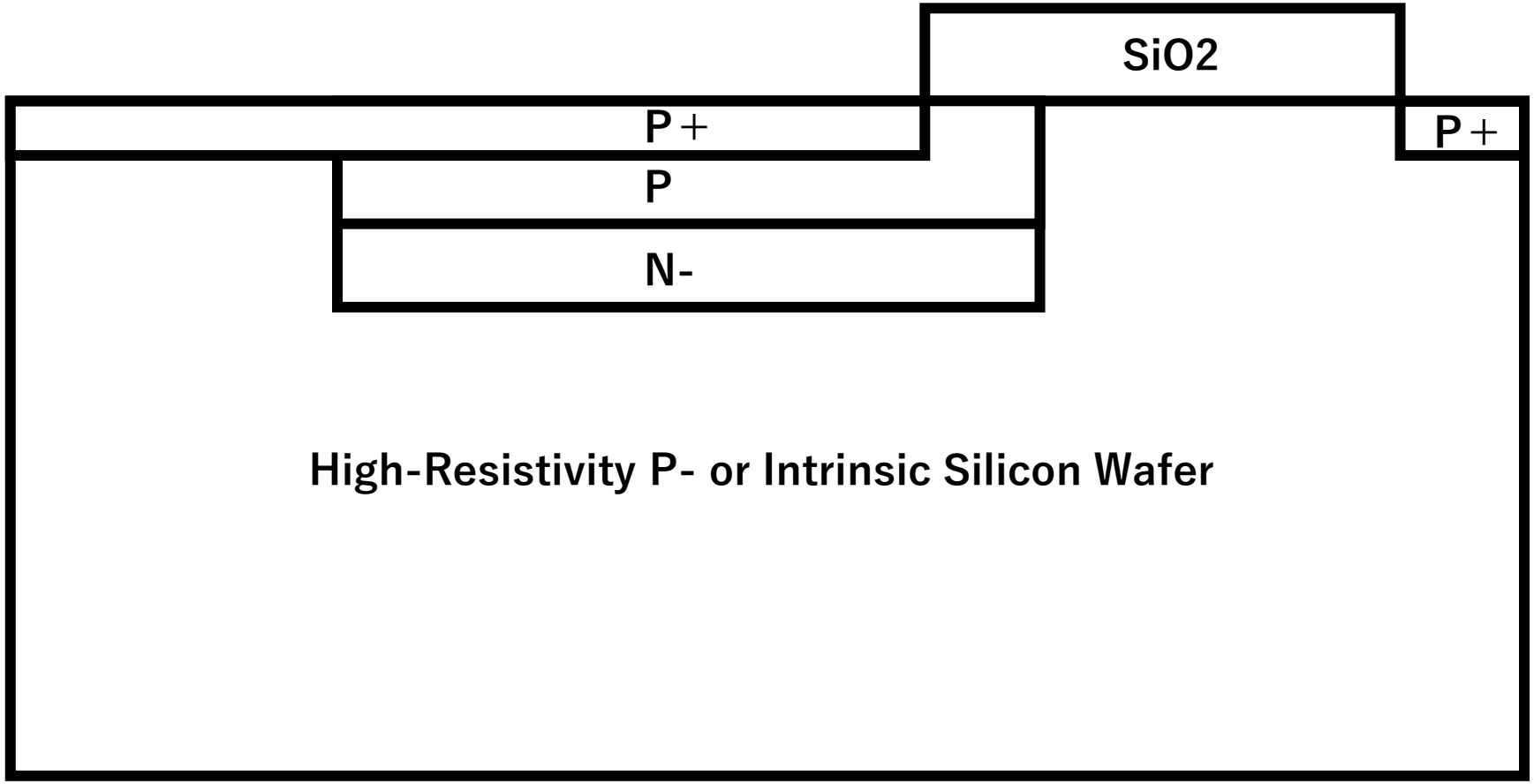


MASK_01

Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

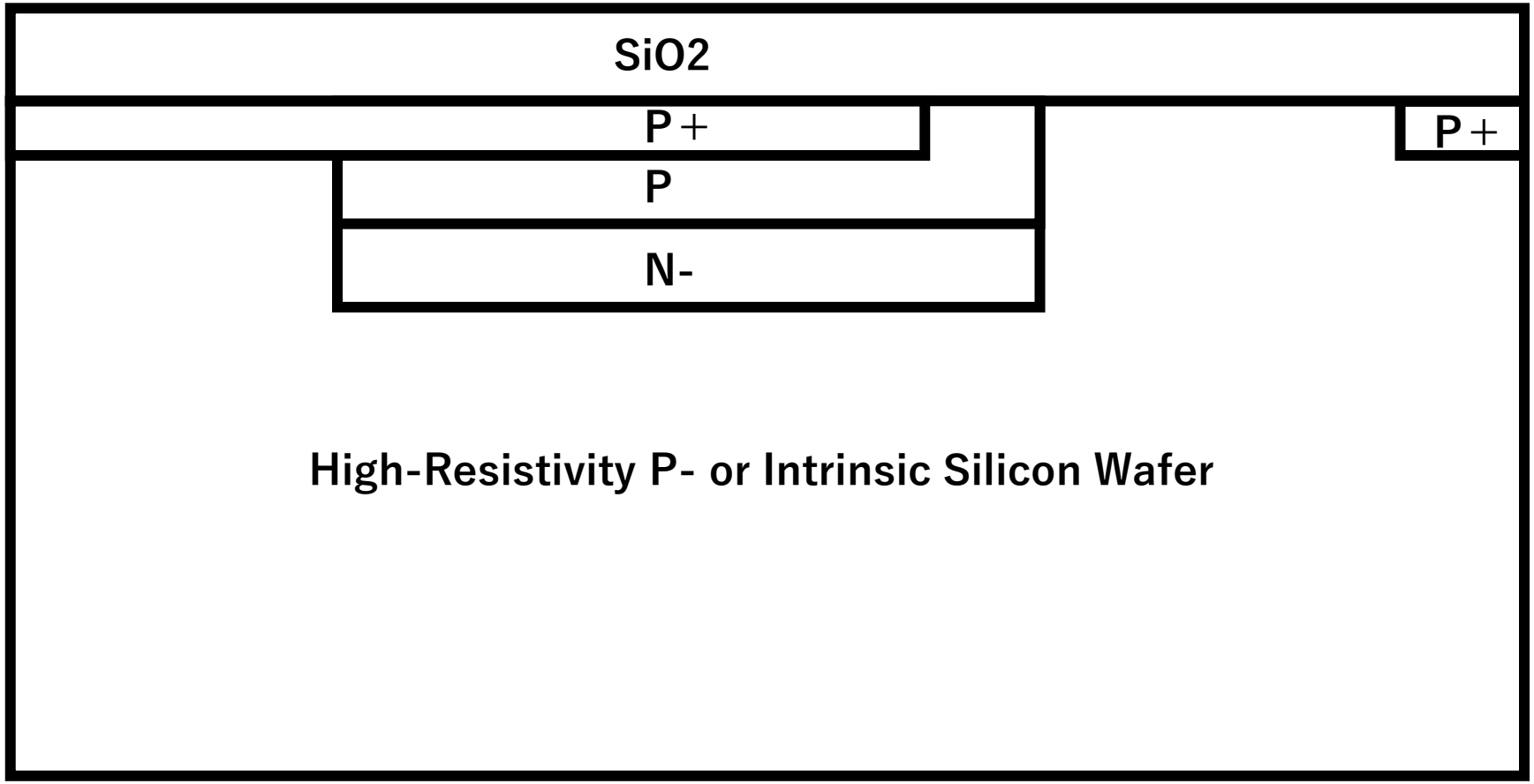
(7) Form the surface heavily doped P+ region



Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

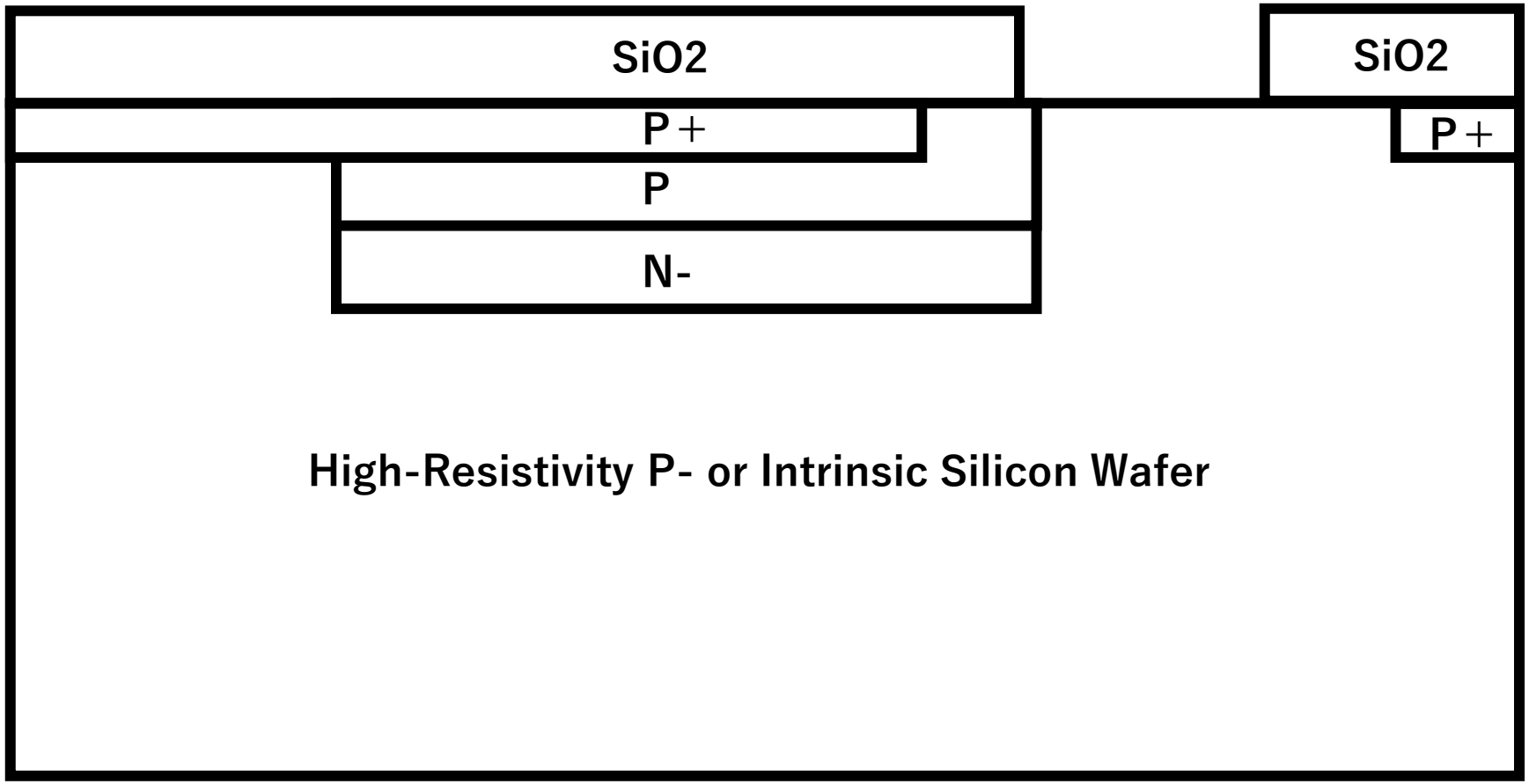
(8) Form the third protection oxide layer



Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

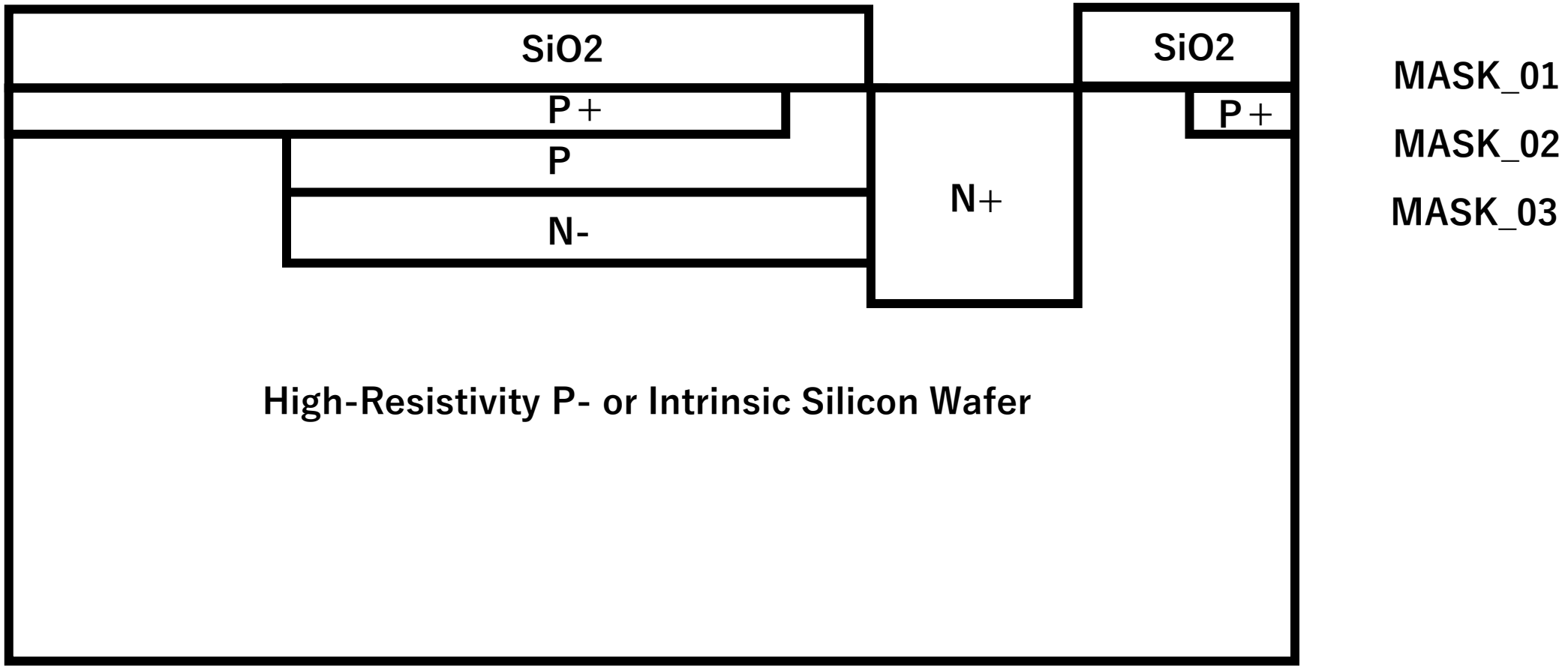
(9) Form the oxide window for the heavily doped N+ charge storage region



Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

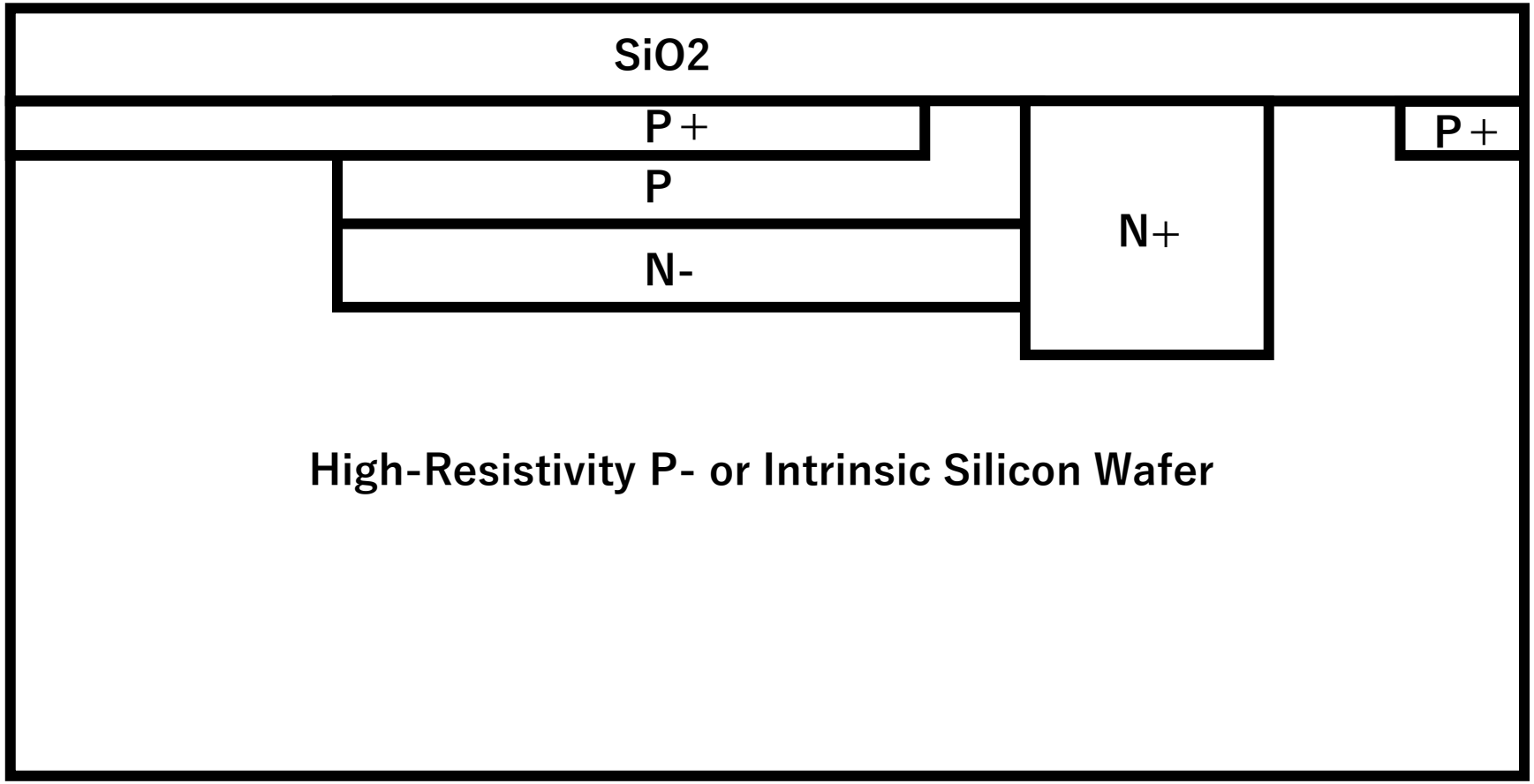
(10) Form the heavily doped N+ charge storage region by high energy deep ion implantation.



Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

(11) Form the fourth protection oxide layer



MASK_01

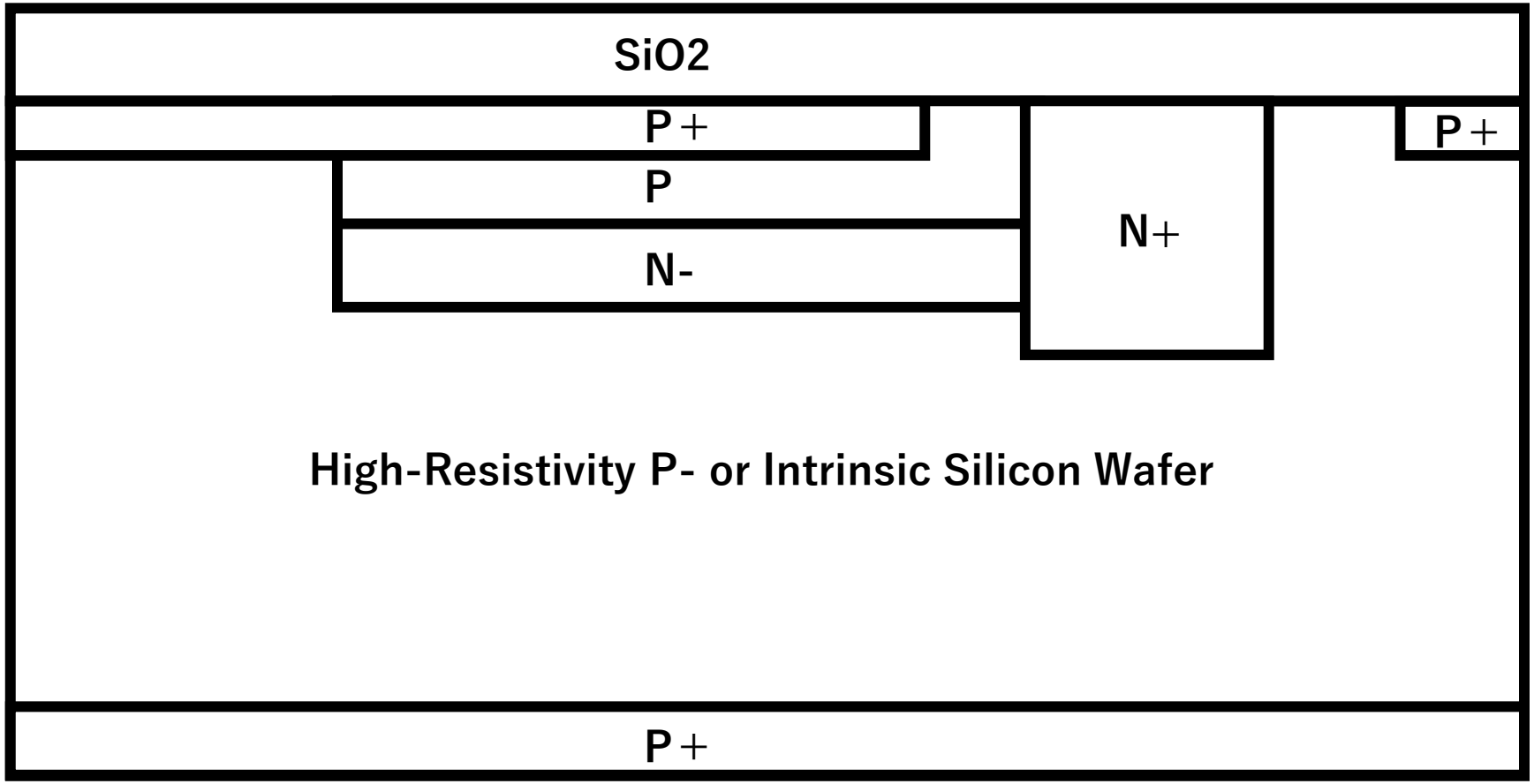
MASK_02

MASK_03

Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

(12) Form the P+ heavily doped back side region



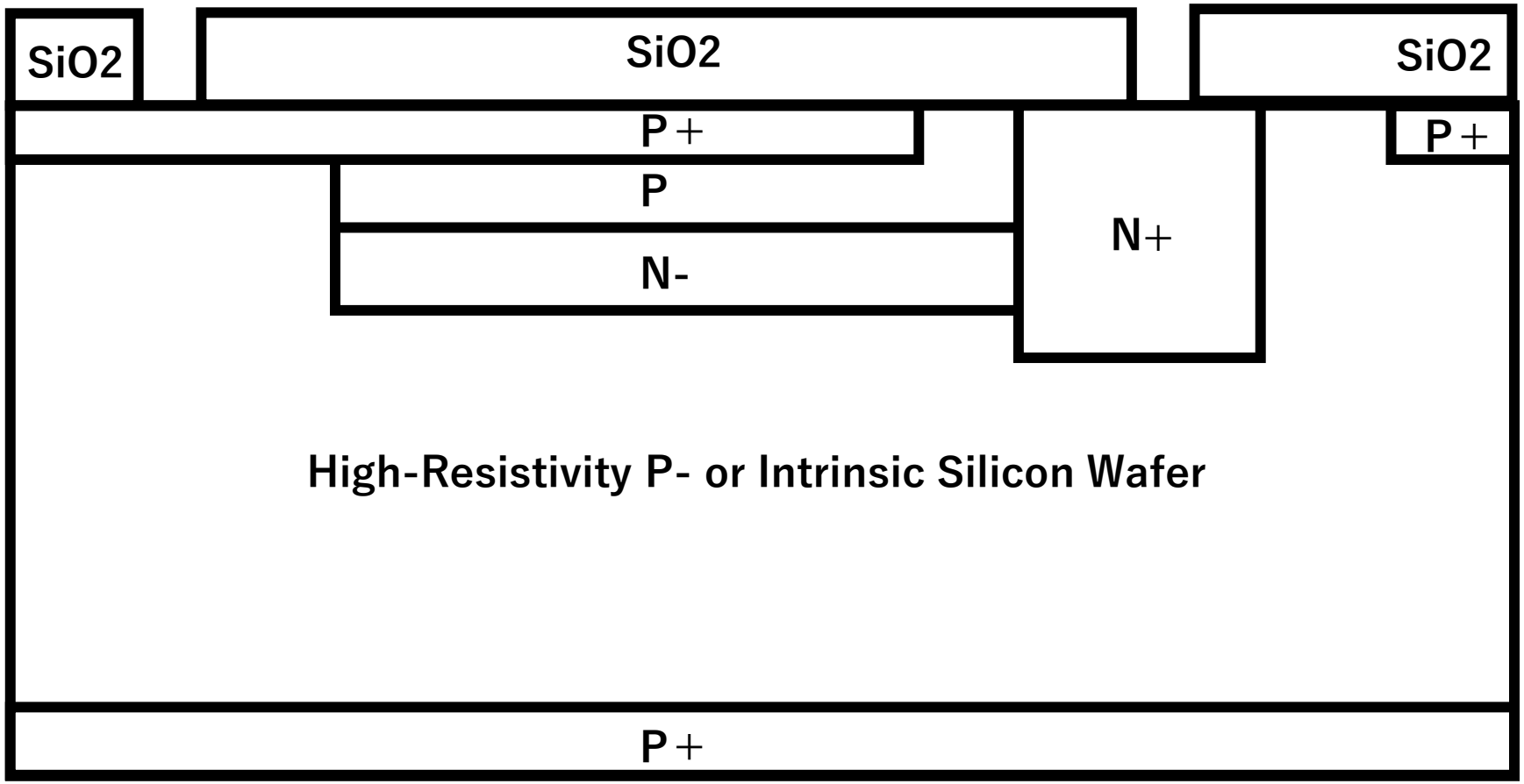
MASK_01

MASK_02

MASK_03

Simple Process Flow of Pinned Buried PIN Photodiode

(13) Form the metal contact windows

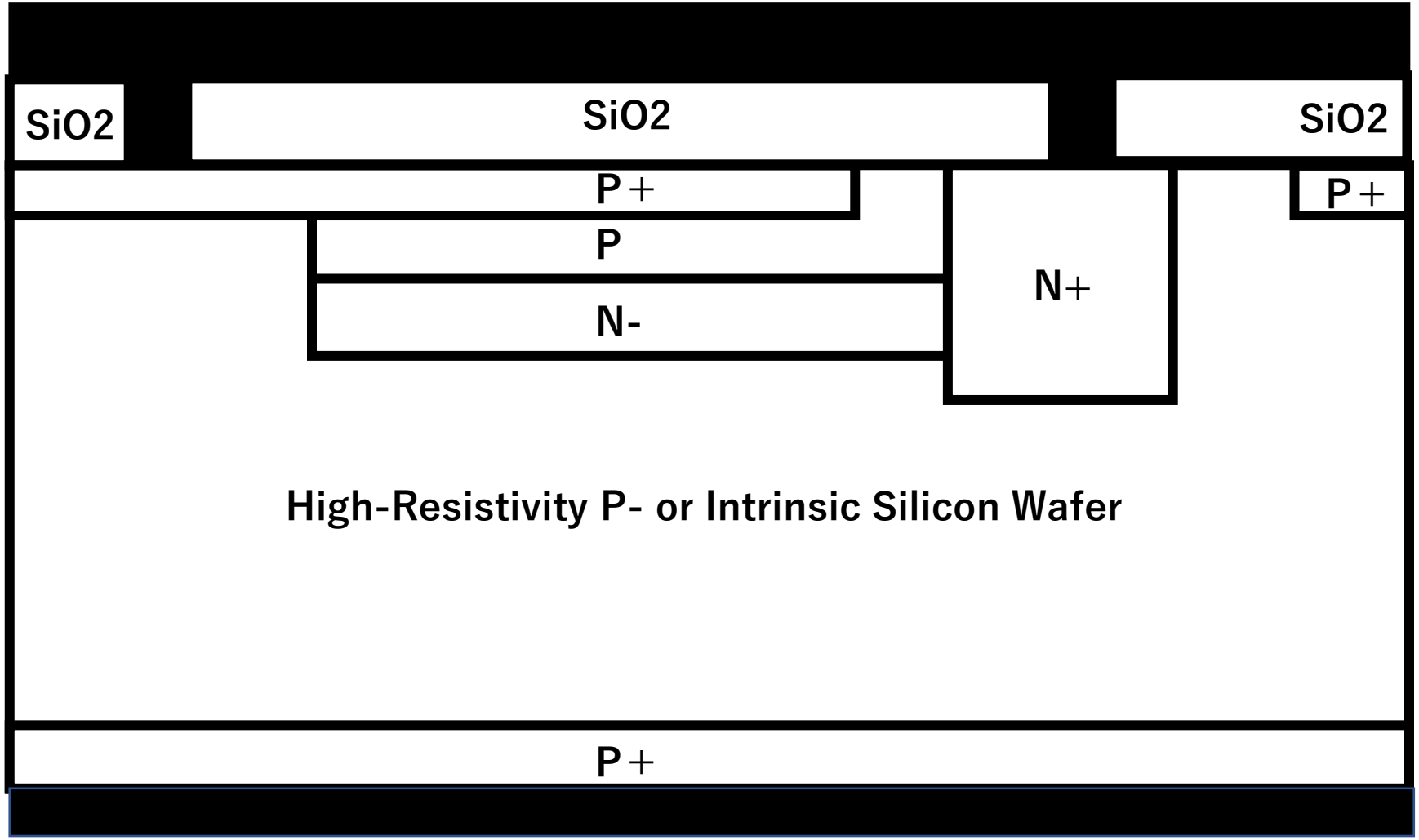


MASK_01
MASK_02
MASK_03
MASK_04

Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

(14) Cover the metal layers on the front and back wafer surface.



MASK_01

MASK_02

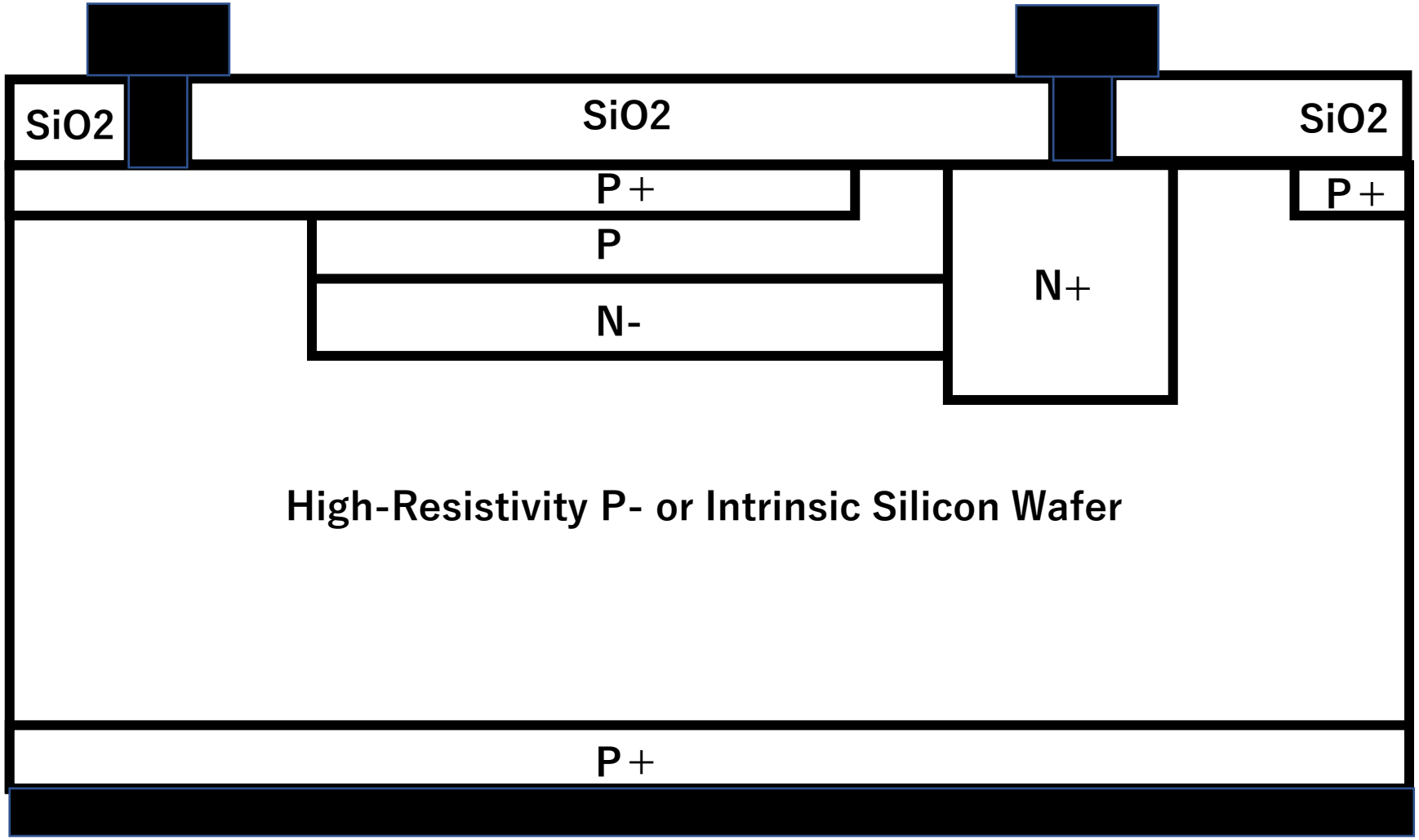
MASK_03

MASK_04

Simple Process Flow of Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021

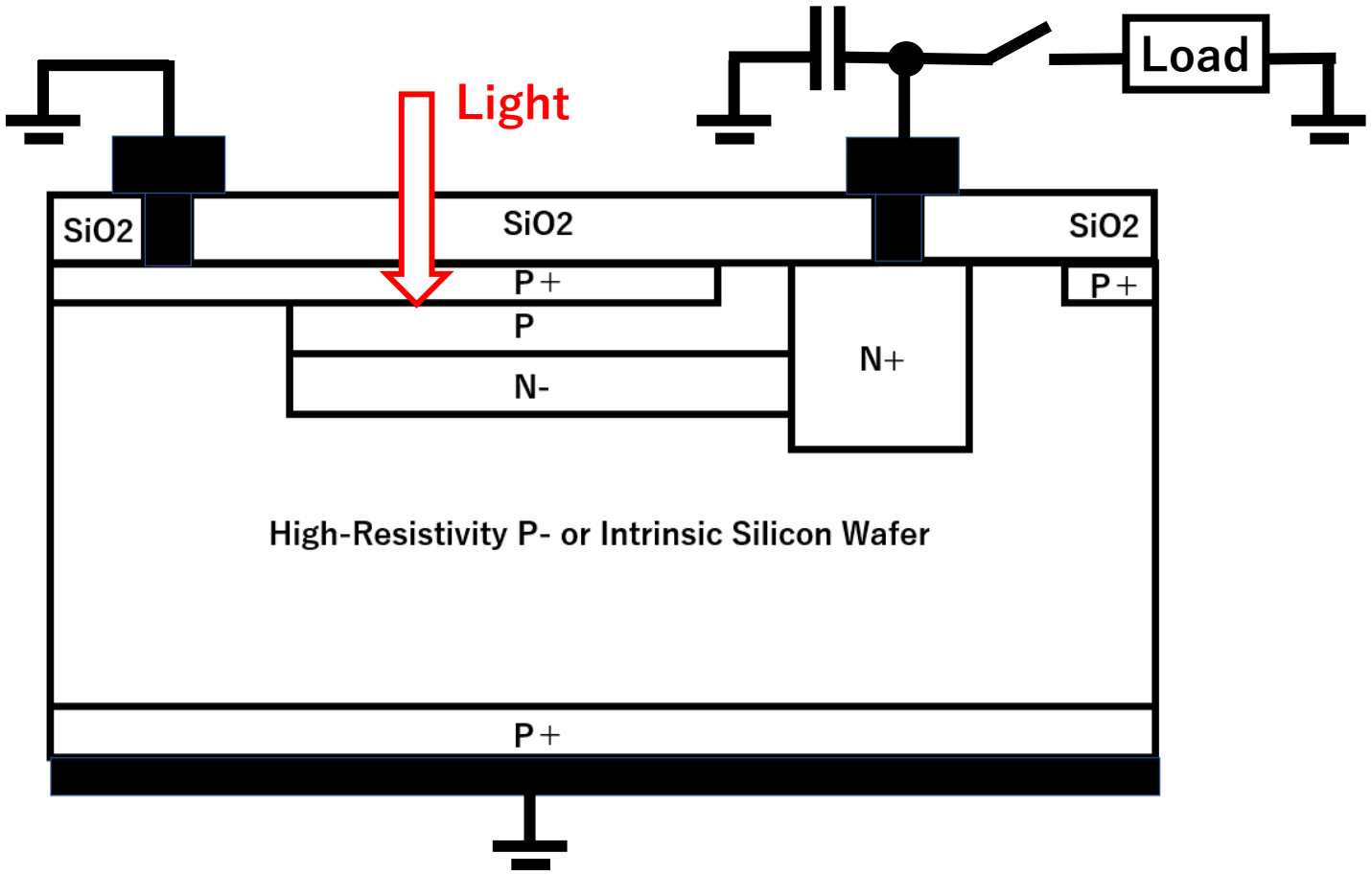
(15) Form the metal wiring patterns



MASK_01
MASK_02
MASK_03
MASK_04

Process Flow of P+PNIP+ Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021



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Process Flow of P+PNIP+ Pinned Buried PIN Photodiode

Yoshiaki Hagiwara (AIPS), 2021