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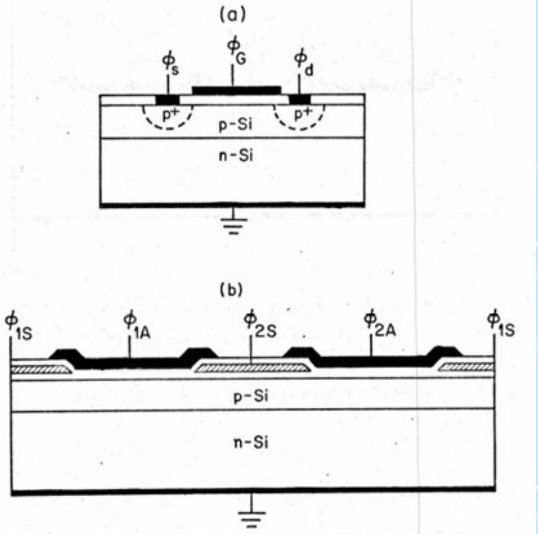

Fig. 4.1a The structure of a surface field effect transistor with a metalurgical channel. The channel is p-type, epitaxially grown.

Fig. 4.1b One unit cell of overlapping gate buried channel CCD.

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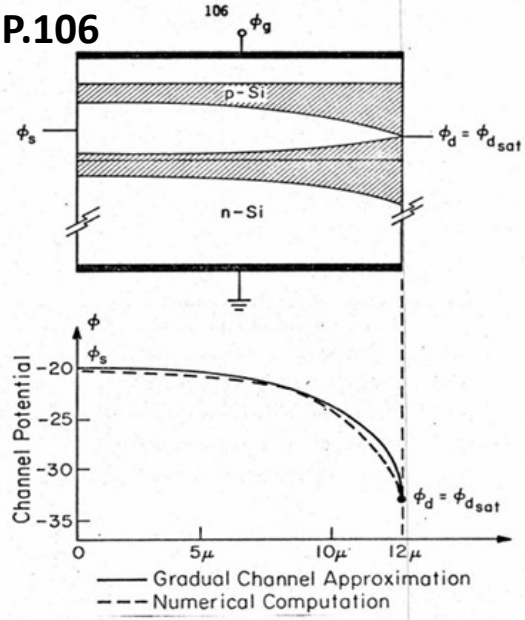

Fig. 4.2a The ideal condition at the onset of saturation is illustrated. $\phi_d = \phi_{d_{sat}} = -32.8$ volt and $\phi_s = -20$volt.

Fig. 4.2b The channel potentials computed by the gradual channel approximation and the numerical computation are compared. The gate length L is 12μ. $\phi_{sF} = -13$ volt.

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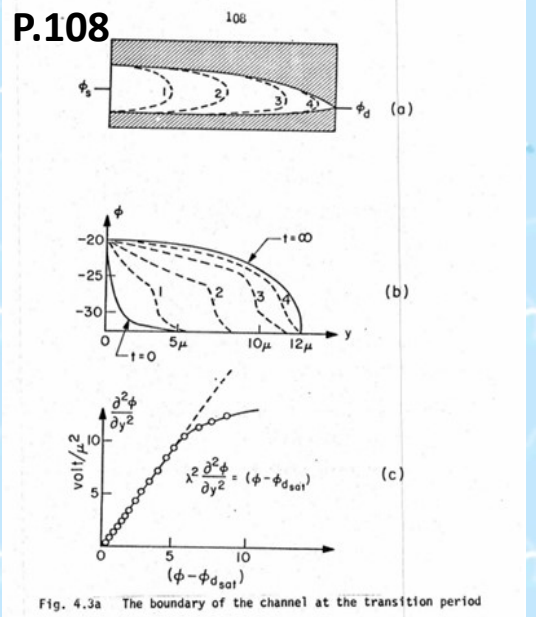

Fig. 4.3a The boundary of the channel at the transition period when the drain voltage changes suddenly from ϕ_s to $\phi_{d_{sat}}$.

Fig. 4.3b The channel potential at transit times. The profiles at t = 0 and t = ∞ are calculated exactly.

Fig. 4.3c The curvature of the channel potential.

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