How_Sony_won_the_Farichild_Patent_War (1990 to 2020)

Fairchild, NEC and KODAK attacked SONY Hole Accumulation DIODE (SONY TRADE MARK) which is the P+NPN triple junction type Pinned and Buried Photodiodes invented by Hagiwara at Sony in 1975. The evidences are given in the Japanese Patent Applications JPA1975-127646, JPA1975-127647, and JPA1975-134985.

Patent Claim in Original Japanese

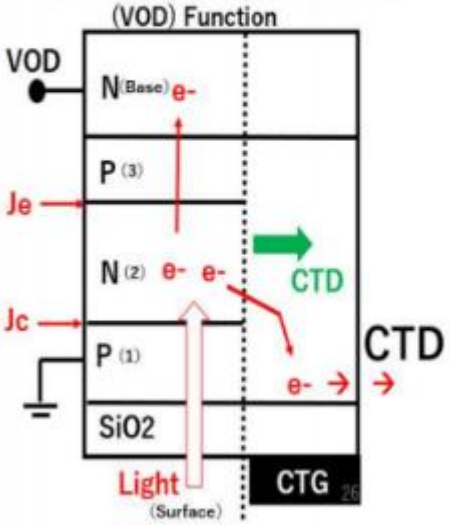
1) 半導体基体(N)に、第１導電型の第１半導体領域（P)と、之の上に形成された第２導電型の第２半導体領域（N)とが形成されて
2) 光感知部(NP)と之よりの電荷を転送する電荷転送部（CTD)とが上記半導体基体の主面に沿う如く配置されて成る個体撮像装置に於いて
3) 上記光感知部(NP)の上記第２半導体領域（N)に整流性接合が形成され、該接合をエミッタ接合(Je)とし、
4) 上記第１及び第２半導体領域間の接合をコレクタ接合(Jc)とするトランジスタ(PNP)を形成し、
5) 該トランジスタ(PNP)のベースとなる上記第２半導体領域(N)に光学像に応じた電荷を蓄積し
6) ここ(N) に蓄積された電荷を上記転送部に移行させて、その転送を行うようにしたことを特徴とする個体撮像装置

Patent Claim in English Translation

1) In the semiconductor basic body (N), the first region (P) of the first impurity is formed, and on which the second region (N) of the second impurity type is formed.
2) On the photo sensor (NP) so defined as a solid state image sensor with Charge Transfer Device (CTD) placed along the surface of the semiconductor basic body,
3) a rectifying emitter junction (Je) is formed on the photo sensor (NP).
4) The junction between the first region (P) and the second region (N) being as the collector junction (Jc) of the transistor (PNP),
5) the second region (N)becomes the base region of the transistor (PNP) which stores the photo charge according to the photo image.
6) And the charge stored in this region (N) is transferred to the Charge Transfer Device (CTD).

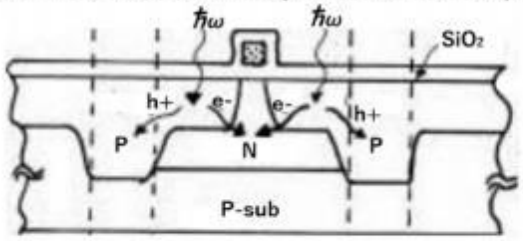
File 1975-134985 Filed 1975/11/10
Public 1977-058414 on 1977/05/13

Buried Pinned Photodiode Patent the PNP Double Junction type Dynamic Photo Transistor with the Vertical Overflow Drain (VOD) Function

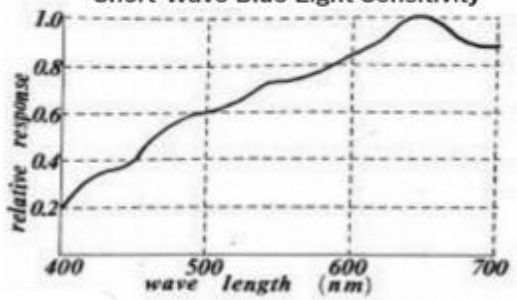


Patent Claim of JPA1975-134985 on the PNPN Dynamic Photo Thyristor with Pinned P+ surface (HAD).

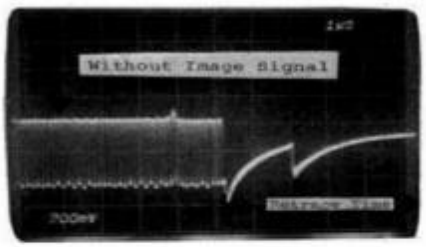
(A) Pinned-Surface and Buried-Storage PNP Photodiode with Adjacent Channel Stops



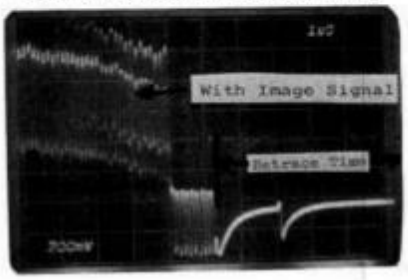
(B) Spectral Response with Very High Short-Wave Blue Light Sensitivity



(C) Signal Output with No Light showing Very Low Dark Current Feature



(D) Signal Output with Input Light showing No Image Lag Feature



The Spectral Response and Signal Outputs reported in Hagiwara SSDM1978 Paper [6-7] showing the No Image Lag Feature.

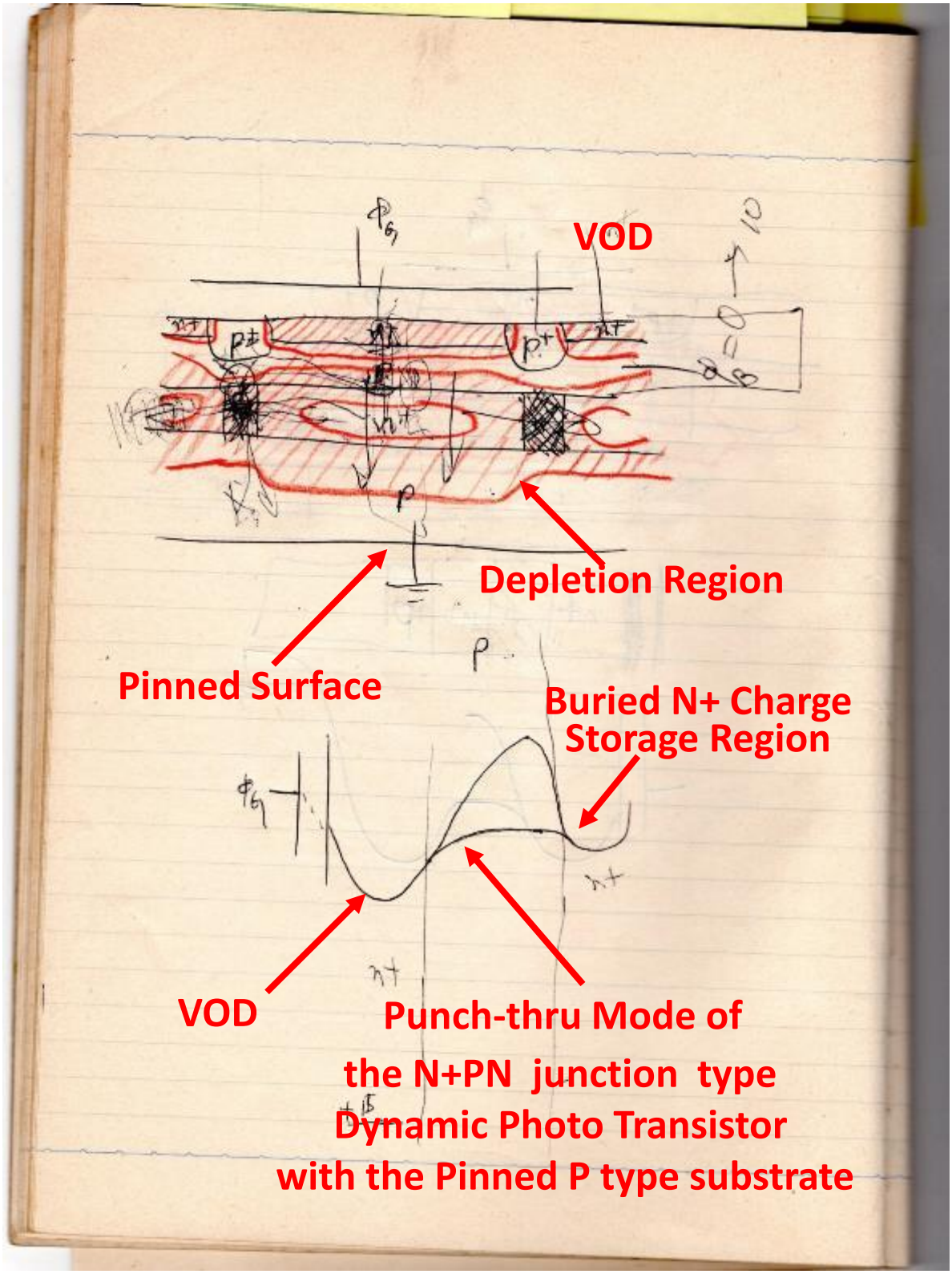
Yoshiaki Hagiwara, Motoaki Abe and Chikara Okada, "A 380H X 488V CCD Imager with Narrow Channel Transfer Gates", Proceeding of the 9th Conference on Solid State Devices, Tokyo 1977, Japanese Journal of Applied Physics Volume 18 Sup 18-1, pp. 335-340 November 1979.

Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Yokohama Central Research Center

Yoshiaki Daimon Hagiwara

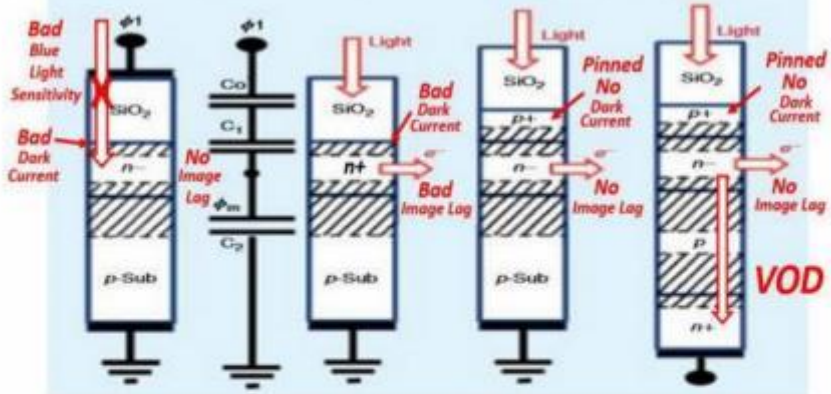
Page41, Back Light PNPN junction type Pinned Photodiode



January 22, 1975

JPA1975-134985

History of dynamic Solid State image sensing structure from BCCD type MOS capacitor to the P+NPN junction Pinned Photodiode capacitor

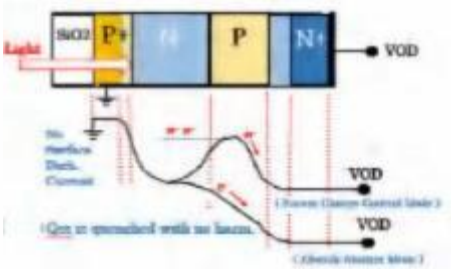


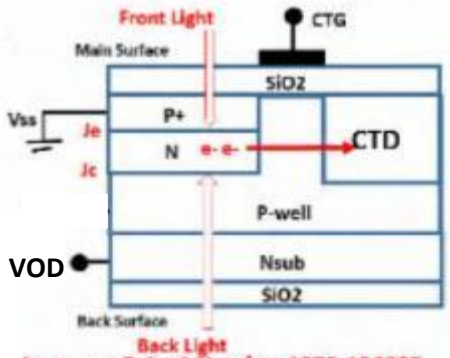
(1) CCD type invented by Bell Lab in 1968

(2) N+P type The classical photodiode with serious image lag

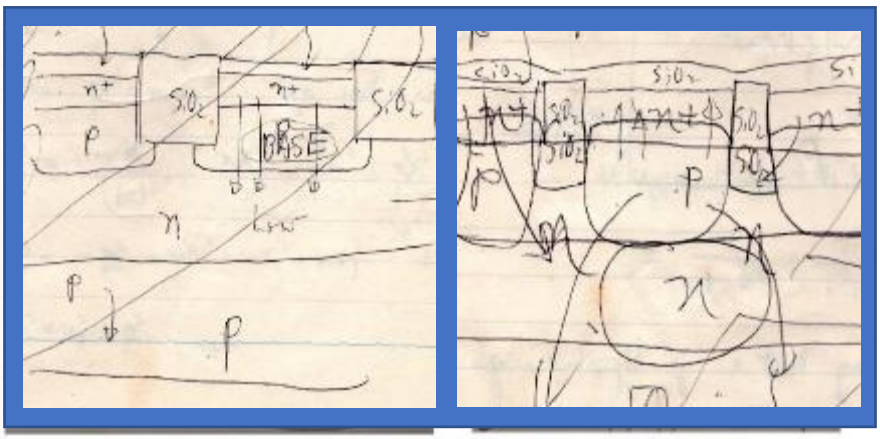
(3) P+NP type (4) P+NPN type (3) and (4) are the P+NP junction type Pinned Photodiode invented by Yoshiaki Hagiwara, 1975

In Japanese patent 1975-134985, Hagiwara at Sony invented the Pinned photodiode with very low dark current, which is also the completely depleted Buried Photodiode with image lag free picture quality, and also with the built-in vertical overflow drain (VOD) function.

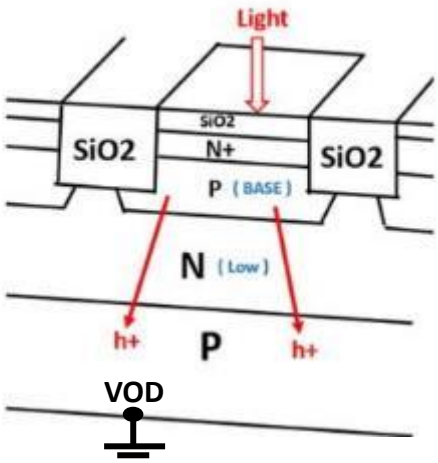




Japanese Patent Number 1975-134985

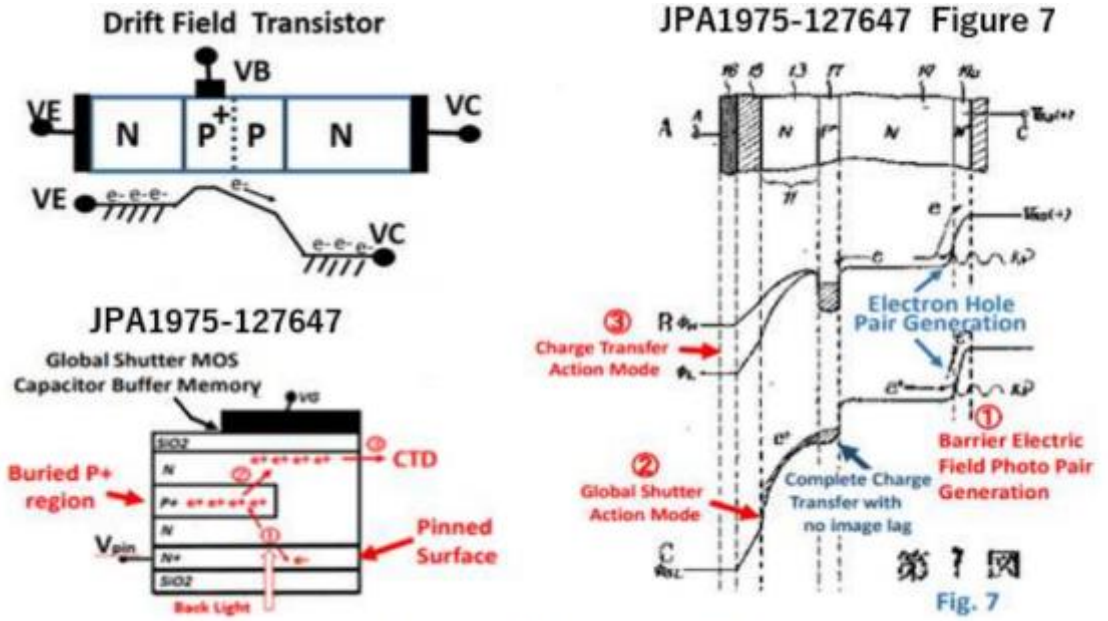


Hagiwara's Lab Note at Sony in February 1975

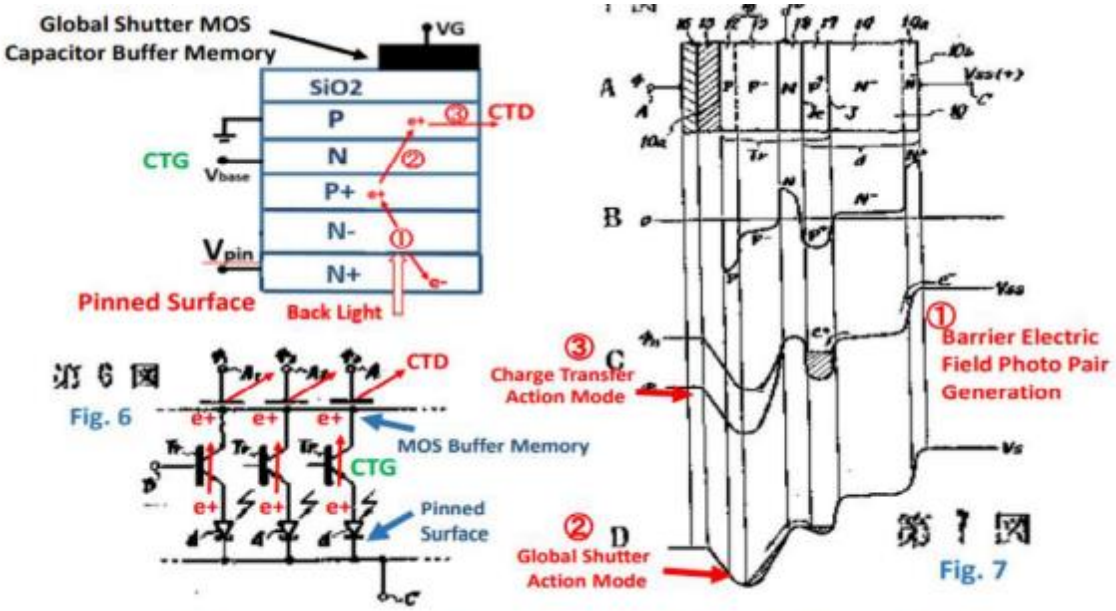


Comparison of Various Light Detecting Photo Sensor Structures

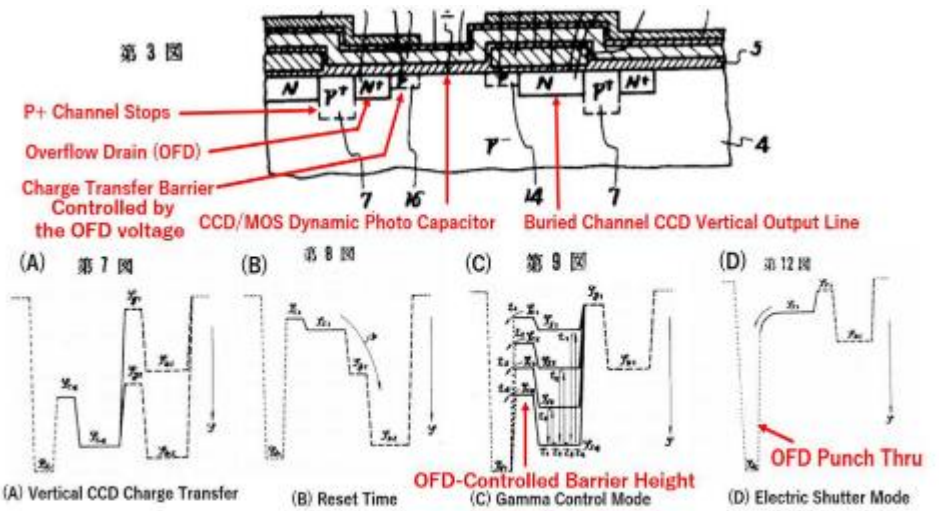
feature \ type	Classical N+Psub Photodiode	Surface Channel CCD	Buried Channel CCD	Yamada 1978 NPNsub	Teranishi 1980 PNPsub	Hagiwara 1975 PNPNsub
Blue Light Sensitivity	△	X	X	○	○	○
Low Image Lag	X	○	○	X	○	○
Surface Dark Current	○	X	X	X	○	○
Surface Trap Noise	○	X	○	X	○	○
Vertical OFD (VOD)	X	X	X	○	X	○
Electrical Shutter	X	X	X	X	X	○



The N+NP+N type Pinned Photodiode defined in Figure 7 of JPA1975-127647 patent by Hagiwara.



The N+NP+N type Pinned Photodiode defined in JPA1975-127647 patent by Hagiwara.

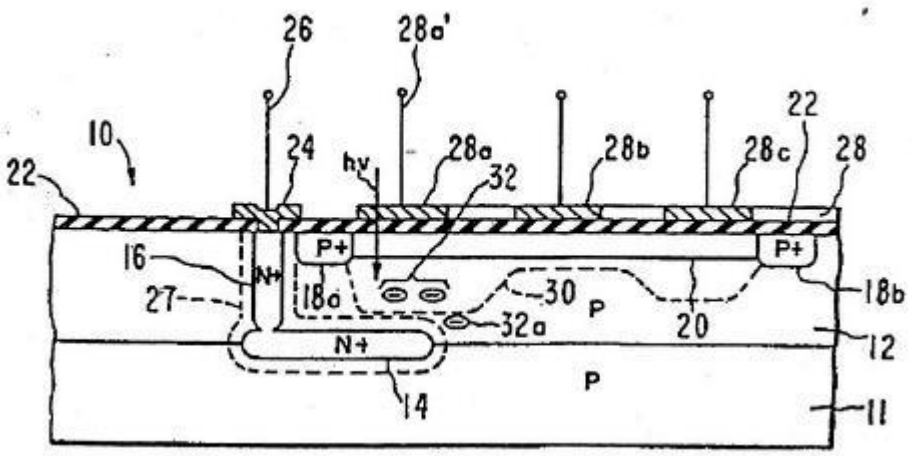


Electric Shutter Function and Gamma Control defined in JPA1977-126885 patent proposed by Hagiwara in 1977.

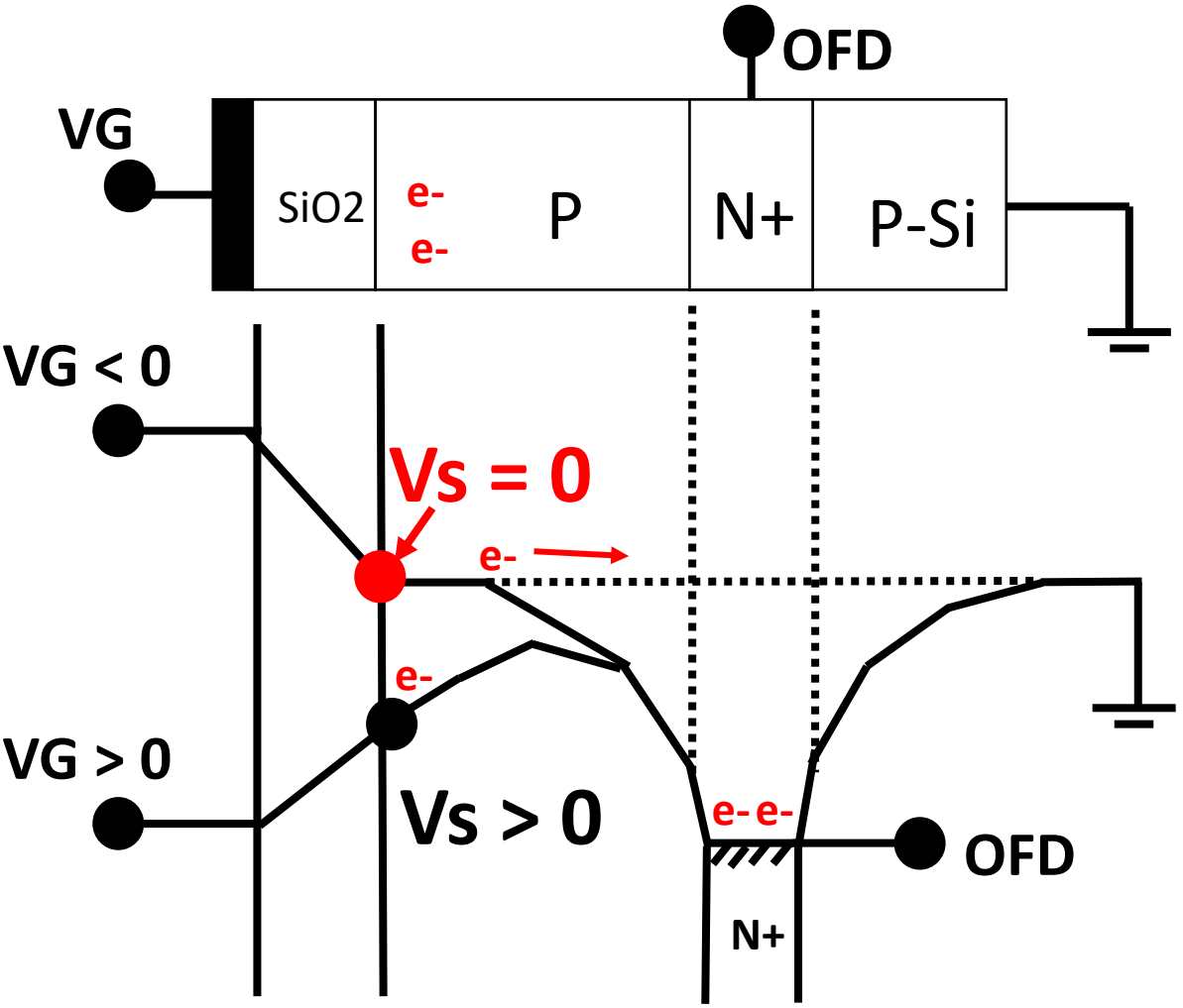
Floating Surface N+NPP+ Single Junction Photodiode JPA1975-134985 Figure 6

Early Patent United State Patent 3,896,485 July 22,1975

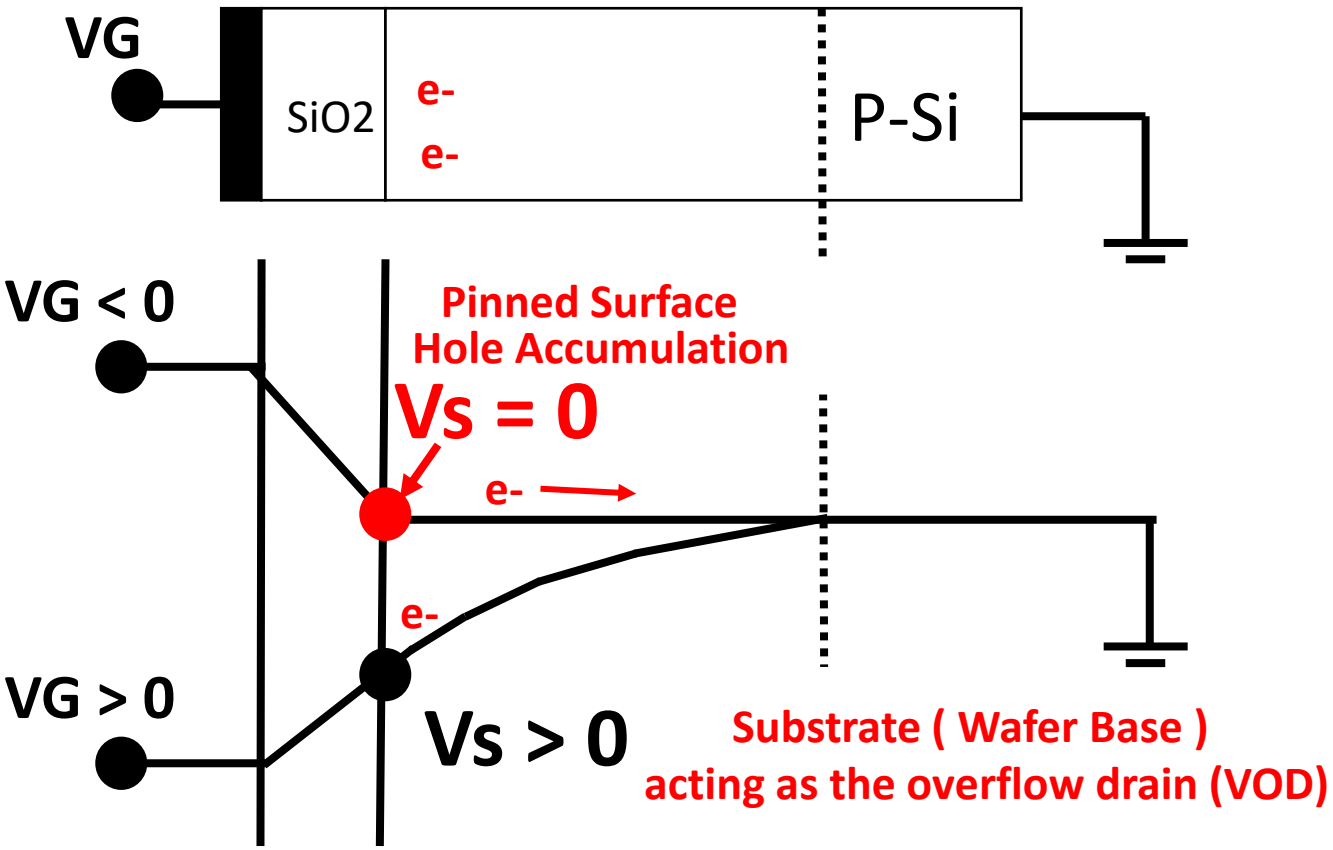
James M. Early (Fairchild Camera and Instrument Corporation):
Charge-Coupled Device with Overflow Protection



Fairchild claimed that the vertical overflow drain (VOD) structure with the punch thru operation mode of N+ overflow drain (OFD) region as the Fairchild original idea. The excess charge is drained to the silicon surface instead of the silicon substrate in this case.



However, the idea of the in-pixel overflow drain (OFD) function was already well known in the case of the Frame Transfer Type CCD image sensors with CCD/MOS dynamic capacitors.



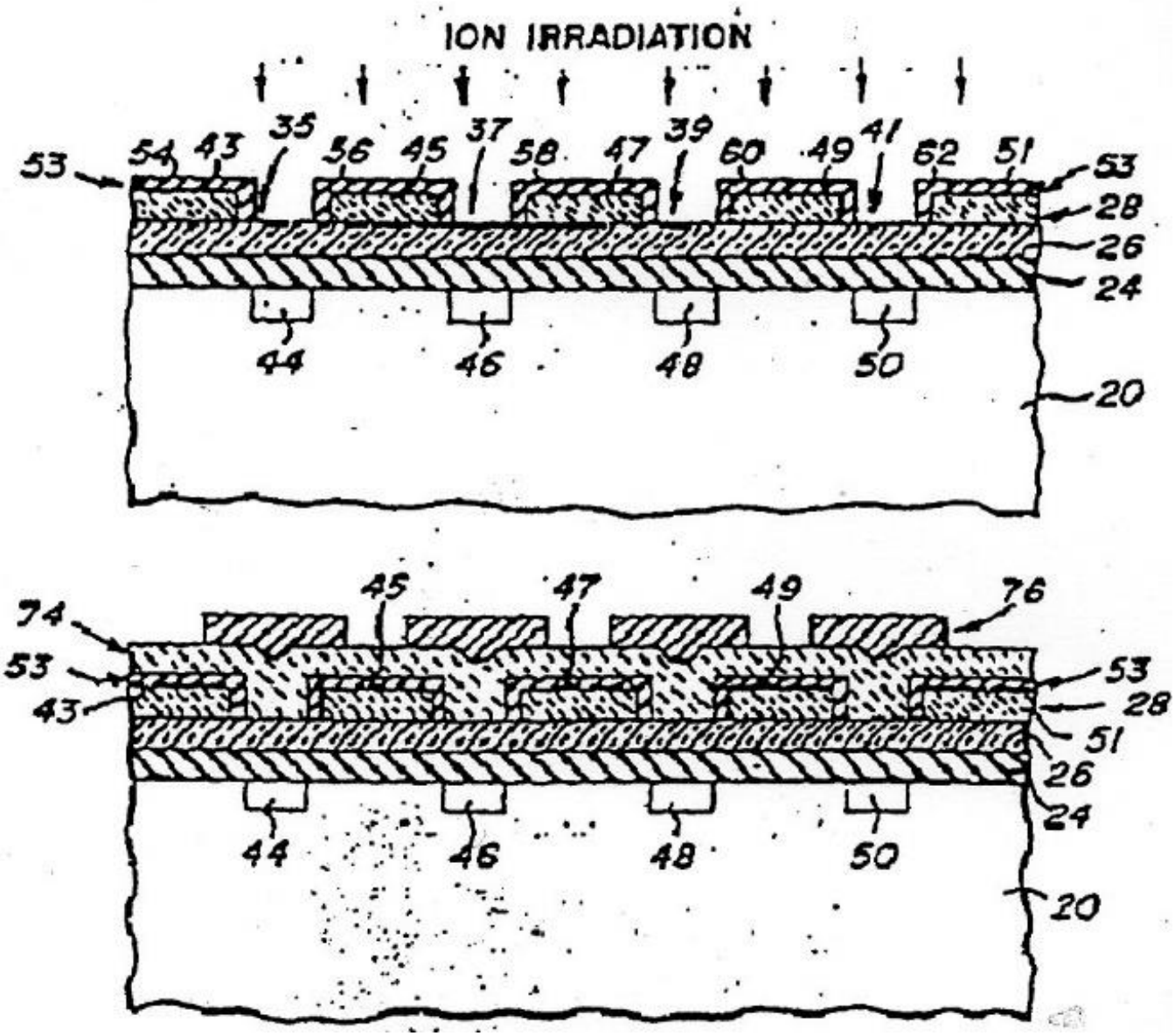
Hagiwara proposed in JPA 1975-134985 the P+NP double junction type Pinned Photodiode with the N type substrate in 1975 , which is not of the CCD/MOS dynamic capacitor type proposed by Fairchild.

SONY HAD sensor is a triple junction type Dynamic photo sensor with the bult-in overflow drain (OFD) function. The OFD is no a region, the OFD is the substrate itself in case of Sony HAD Sensor.

The excess charges are drained to the substrate which was widely well known and very similar to the conventional OFD action which is being applied in case of the Frame Transfer Type CCD image sensors. Besides, in case of Sony HAD sensors, there is another transfer base P type region in-between the buried N charge storage region and the substrate (wafer base) acting as the vertical overflow drain (VOD).

Amelio Patent United States Patent 3,931,674 Jan.13,1976

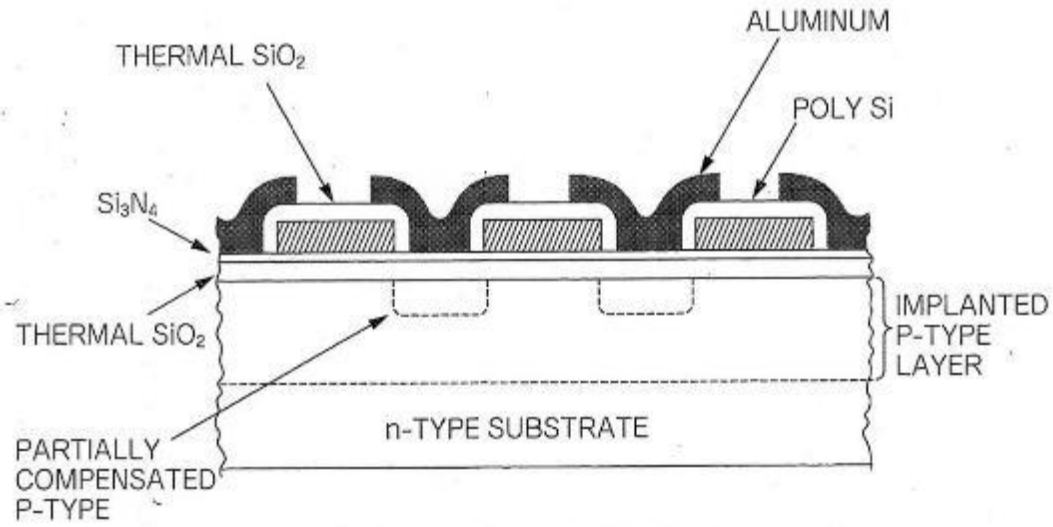
Gilbert F. Amelio (Fairchild Camera and Instrument Corporation) : Self Aligned CCD Element including Two Levels of Electrodes and Method of Manufacture therefor



Fairchild claimed the Vth adjustment method of the overlapped Buried Channel CCD electrodes was the Fairchild original. But the truth is that the Hughes Aircraft reported in 1973 already the Vth adjustment method of the overlapped Buried Channel CCD in the IEEE IEDM1973 conference.

The SONY Process was found identical to the one reported by Hughes Aircraft at the IEEE IEDM1973 conference.

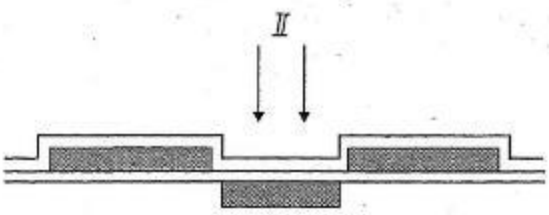
IEDM1973 Paper by Hughes Aircraft Company,
D.M. Erb, W. Kotyczka, S.C. Su, C. Wang and G. Clough,
"An overlapped Electrode Buried Channel CCD", IEDM1973,
reporting the ion implantation of the Vth
adjustment of electrodes of Charge Coupled Devices



D.M. Erb, S.C. Su

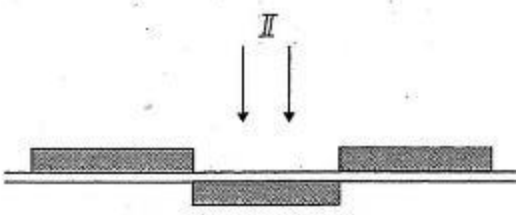
Difference of Fairchild (Amelio) 1976 Process and Sony 1987 Process

Ion Implantation Vth Adjustment
after oxidation of
the first polysilicon electrodes



Amelio 674 Pat.

Ion Implantation Vth Adjustment
before oxidation of
the first polysilicon electrodes



Sony Process

Besides Fairchild (Amelio) 1976 Process and Sony 1987 Process
had a big difference for manufacturability and yield considerations.

Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Atsugi Tech Center , Summer 1971

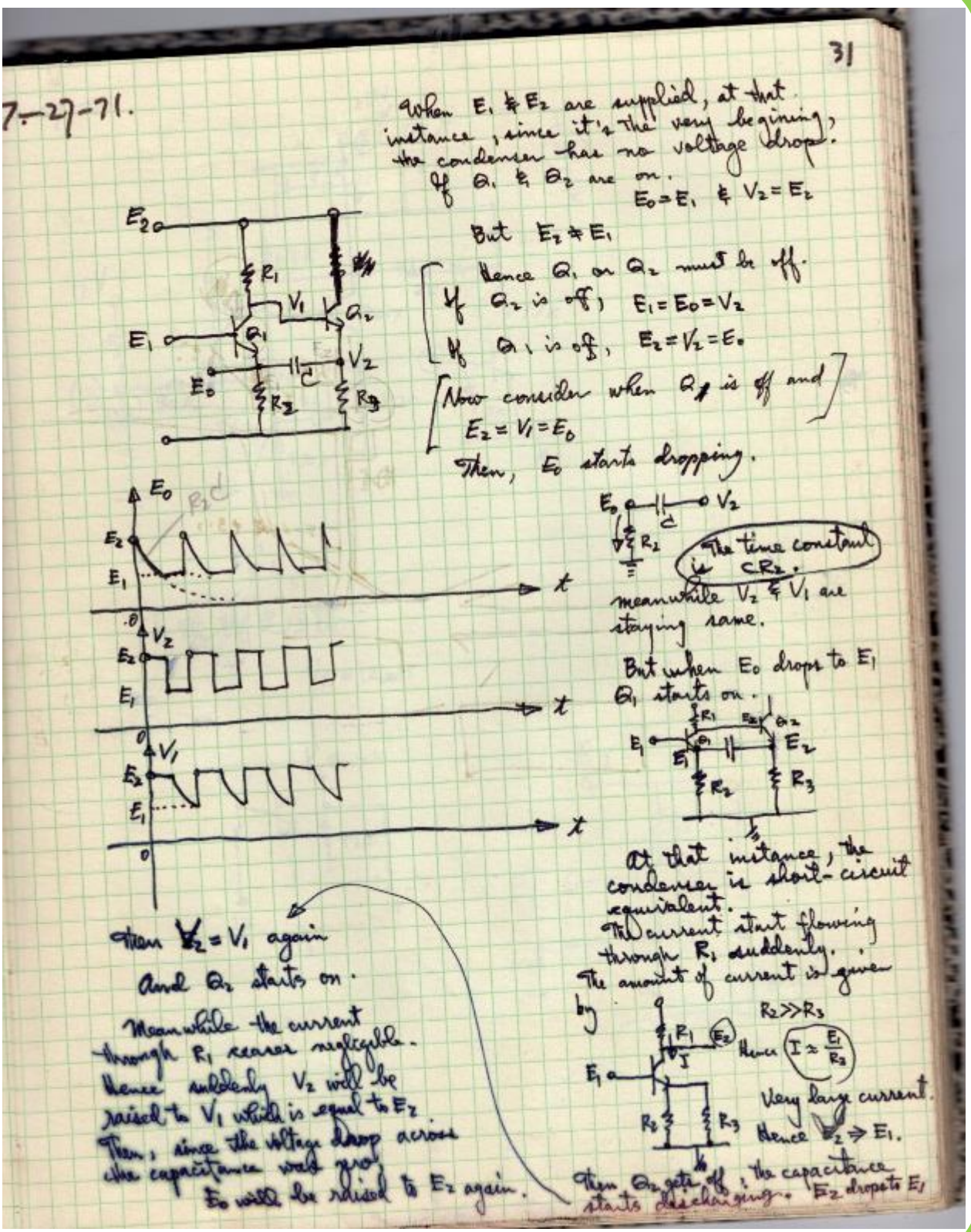
Yoshiaki Daimon Hagiwara

Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Atsugi Tech Center , Summer 1971

Yoshiaki Daimon Hagiwara

Sony CX083F/CX087B Bipolar IC Basic Circuit Memo

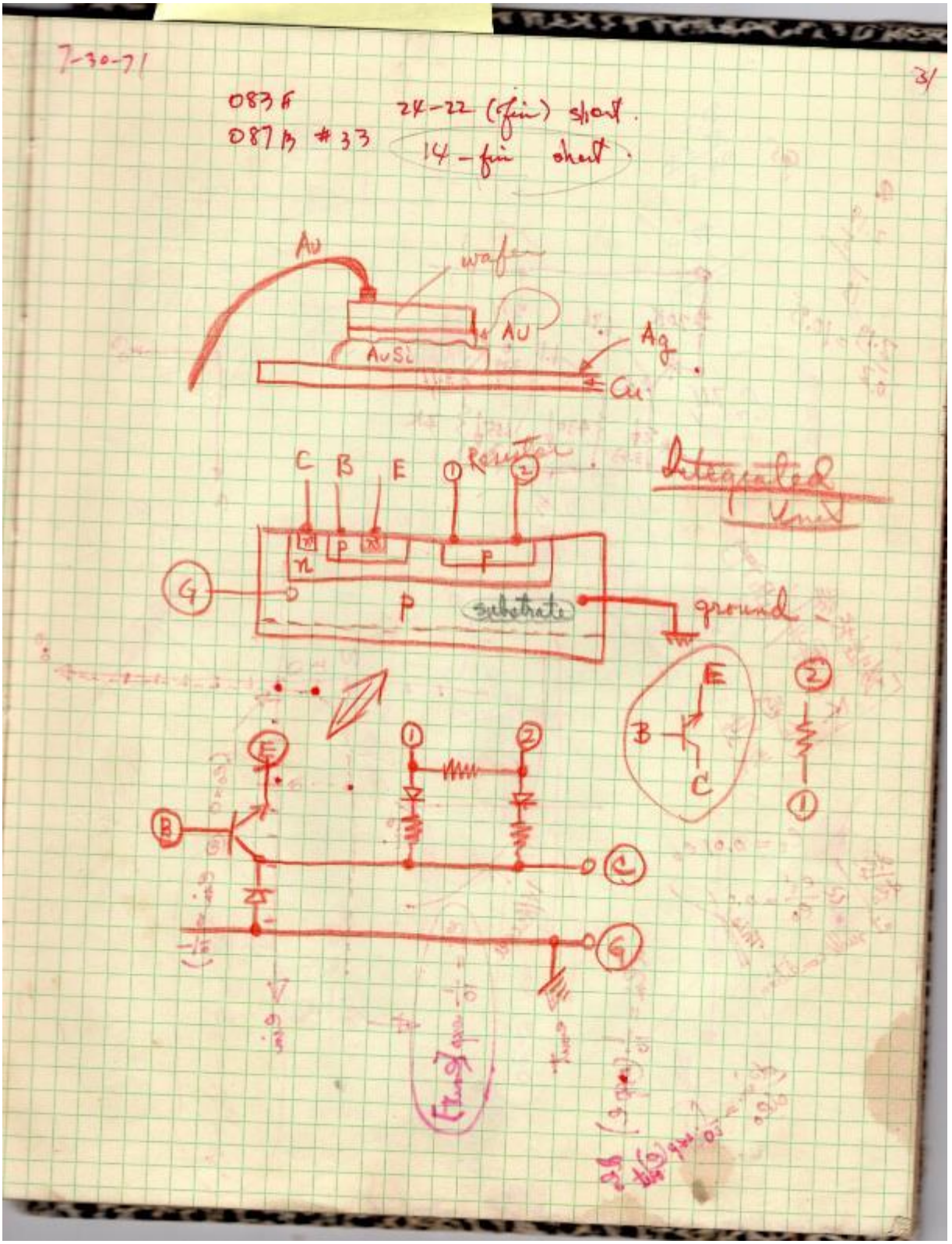


Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Atsugi Tech Center , Summer 1971

Yoshiaki Daimon Hagiwara

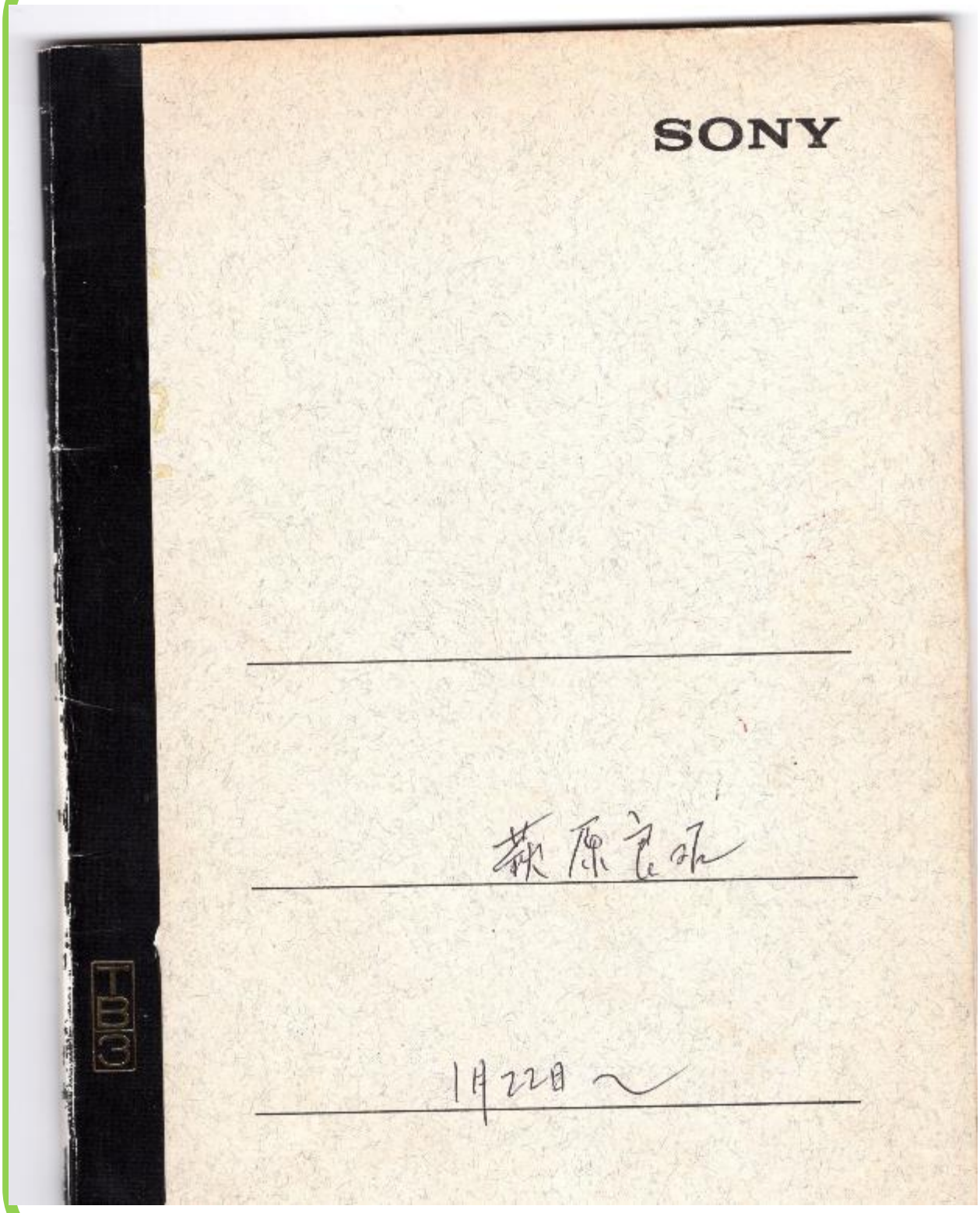
Sony CX083F/CX087B Bipolar Process Memo



Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Yokohama Central Research Center

Yoshiaki Daimon Hagiwara

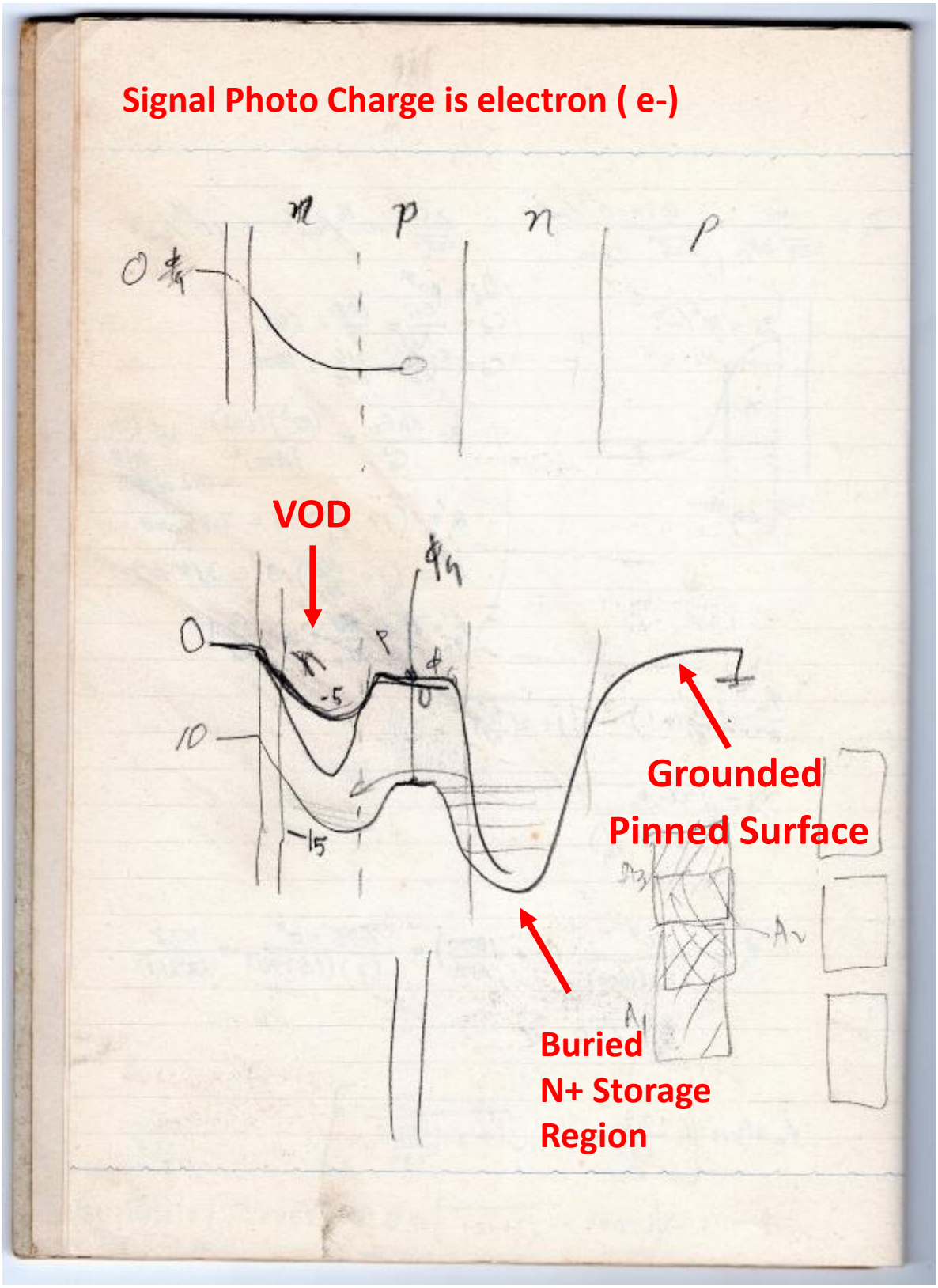


January 22, 1975

Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Yokohama Central Research Center
Yoshiaki Daimon Hagiwara

Page2, Back Light PNPN junction type Pinned Photodiode

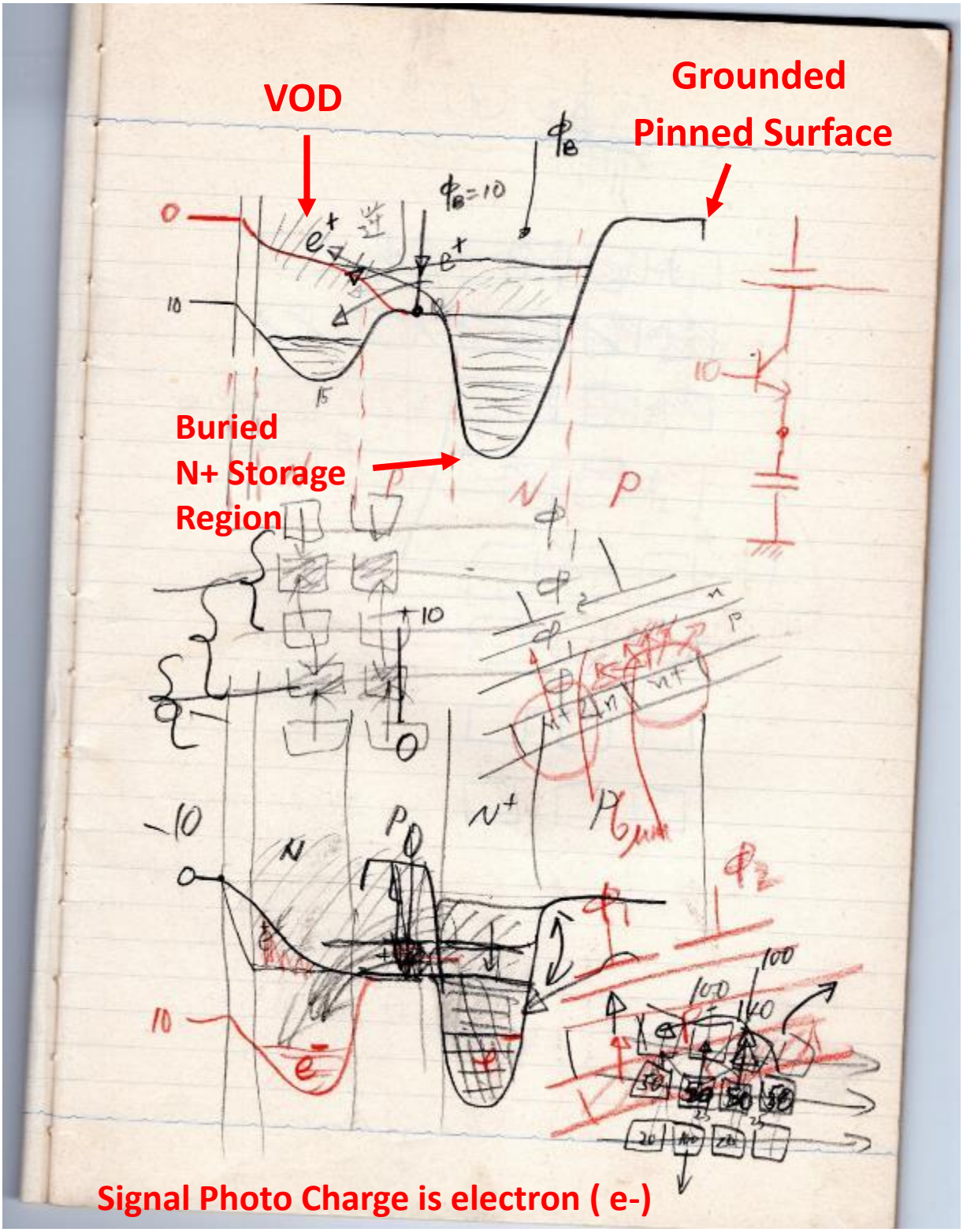


January 22, 1975

Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Yokohama Central Research Center
Yoshiaki Daimon Hagiwara

Page3, Back Light PNPN junction type Pinned Photodiode



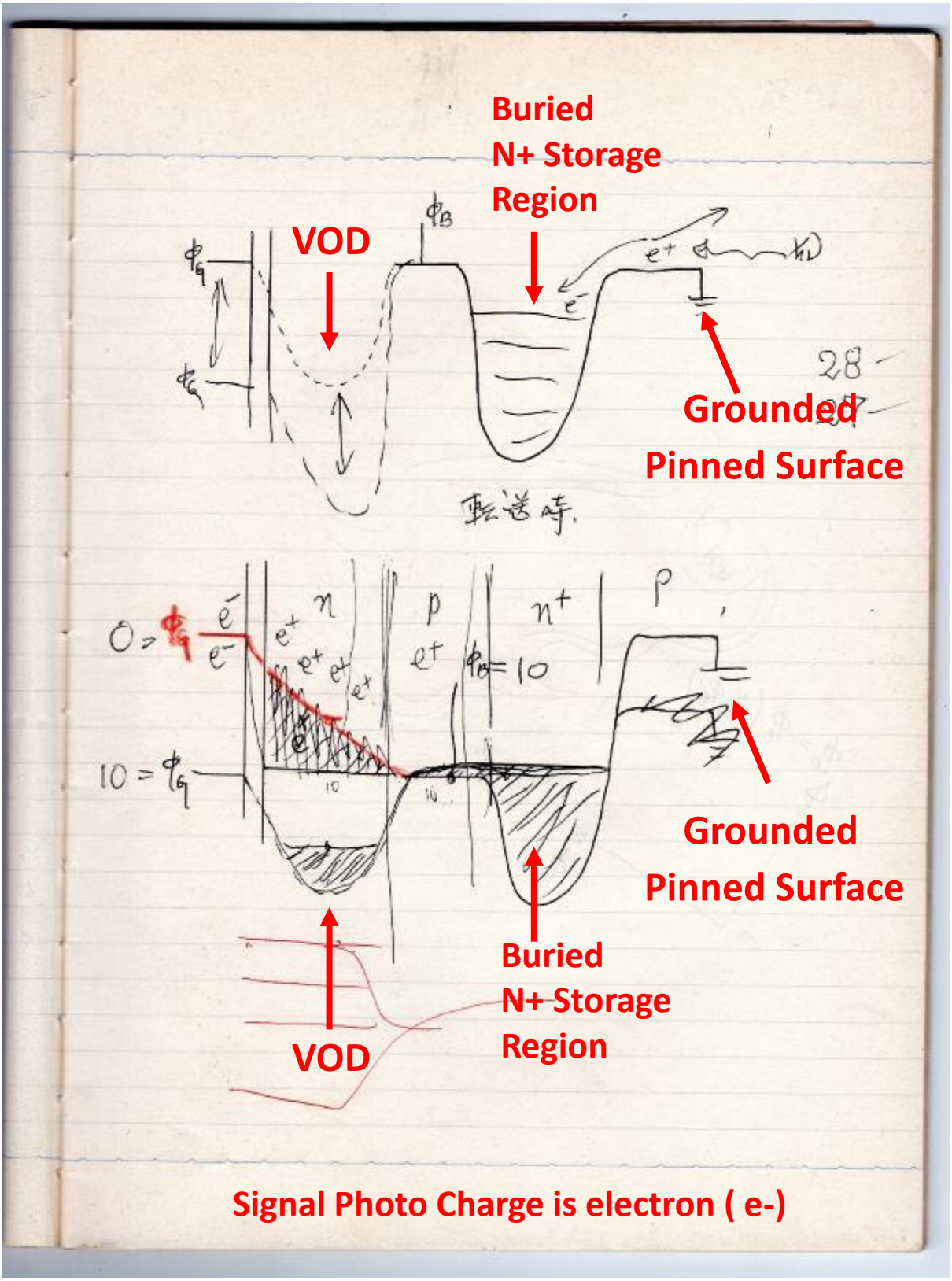
January 22, 1975

Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Yokohama Central Research Center

Yoshiaki Daimon Hagiwara

Page7, Back Light PNPN junction type Pinned Photodiode

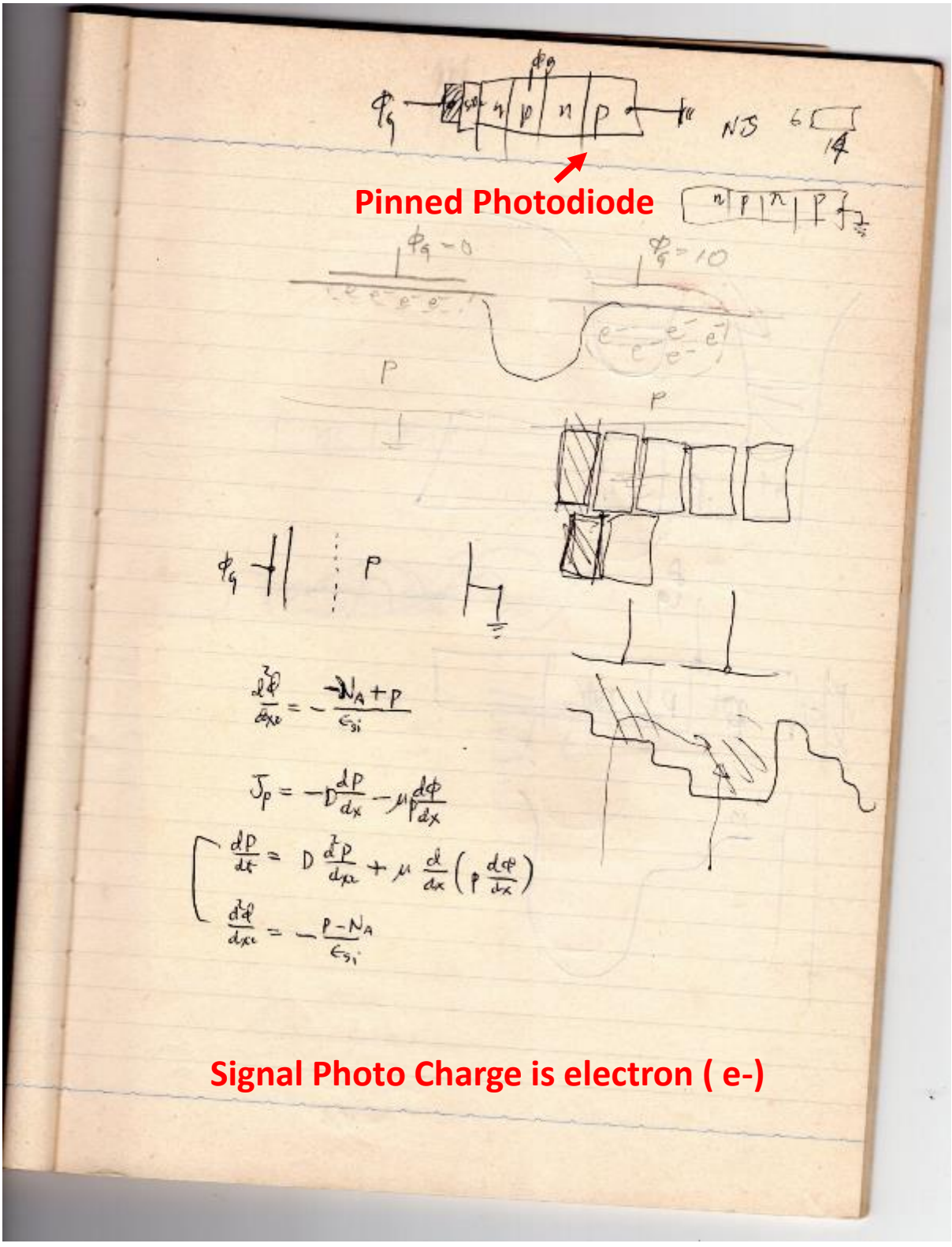


January 22, 1975

Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Yokohama Central Research Center
Yoshiaki Daimon Hagiwara

Page19, Back Light PNPN junction type Pinned Photodiode



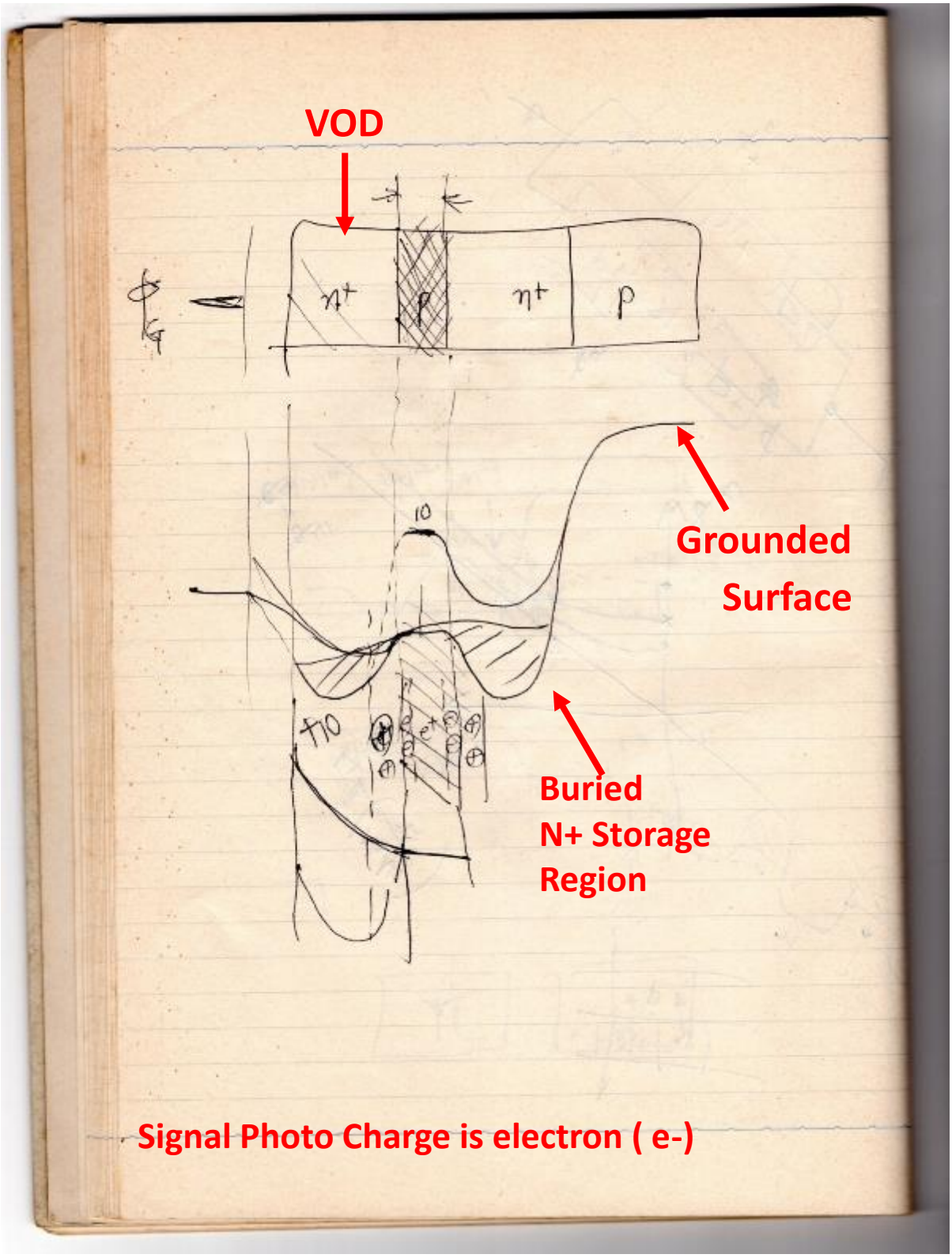
January 22, 1975

Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Yokohama Central Research Center

Yoshiaki Daimon Hagiwara

Page37, Back Light PNPN junction type Pinned Photodiode

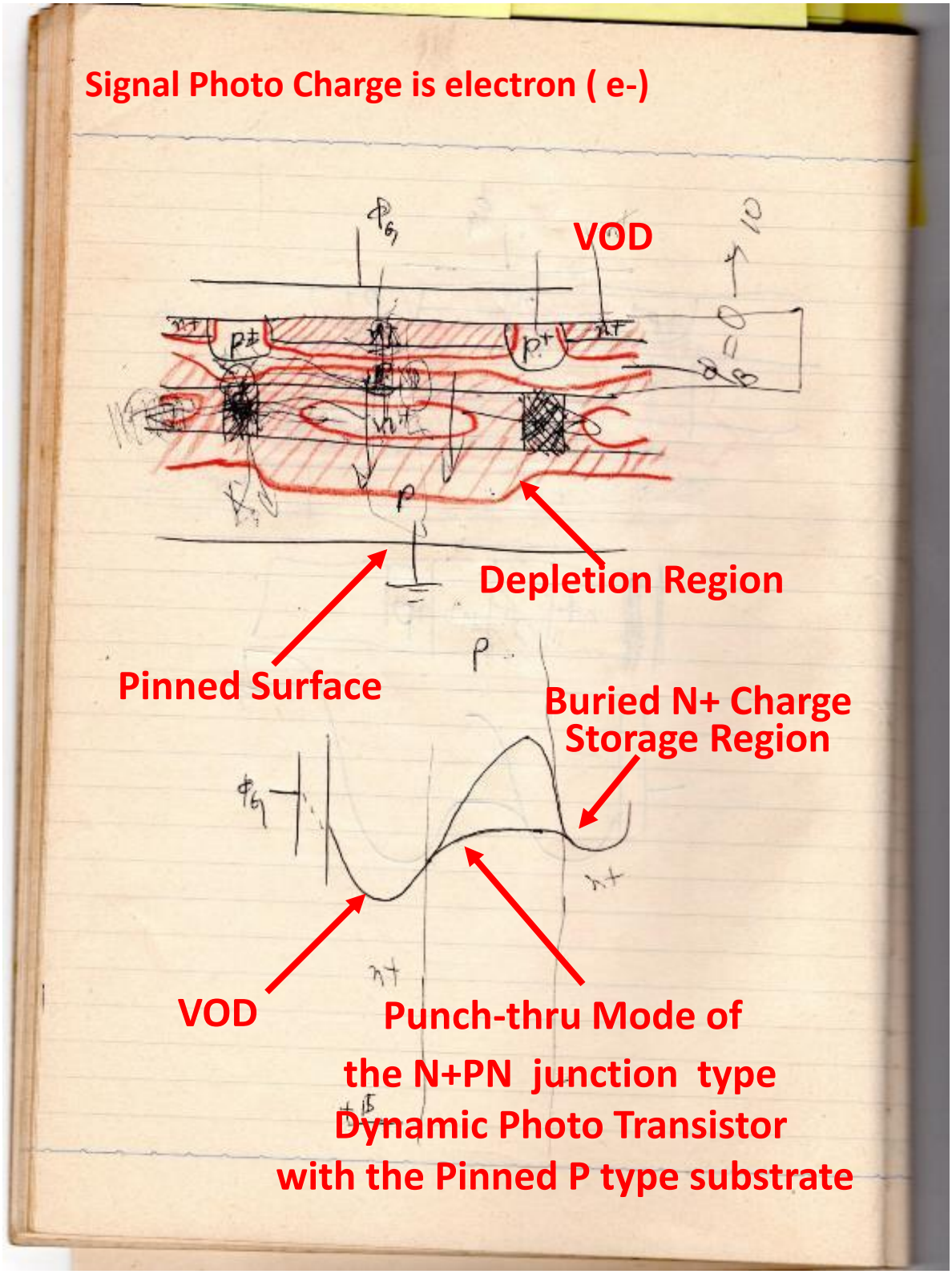


January 22, 1975

Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Yokohama Central Research Center
Yoshiaki Daimon Hagiwara

Page41, Back Light PNPN junction type Pinned Photodiode



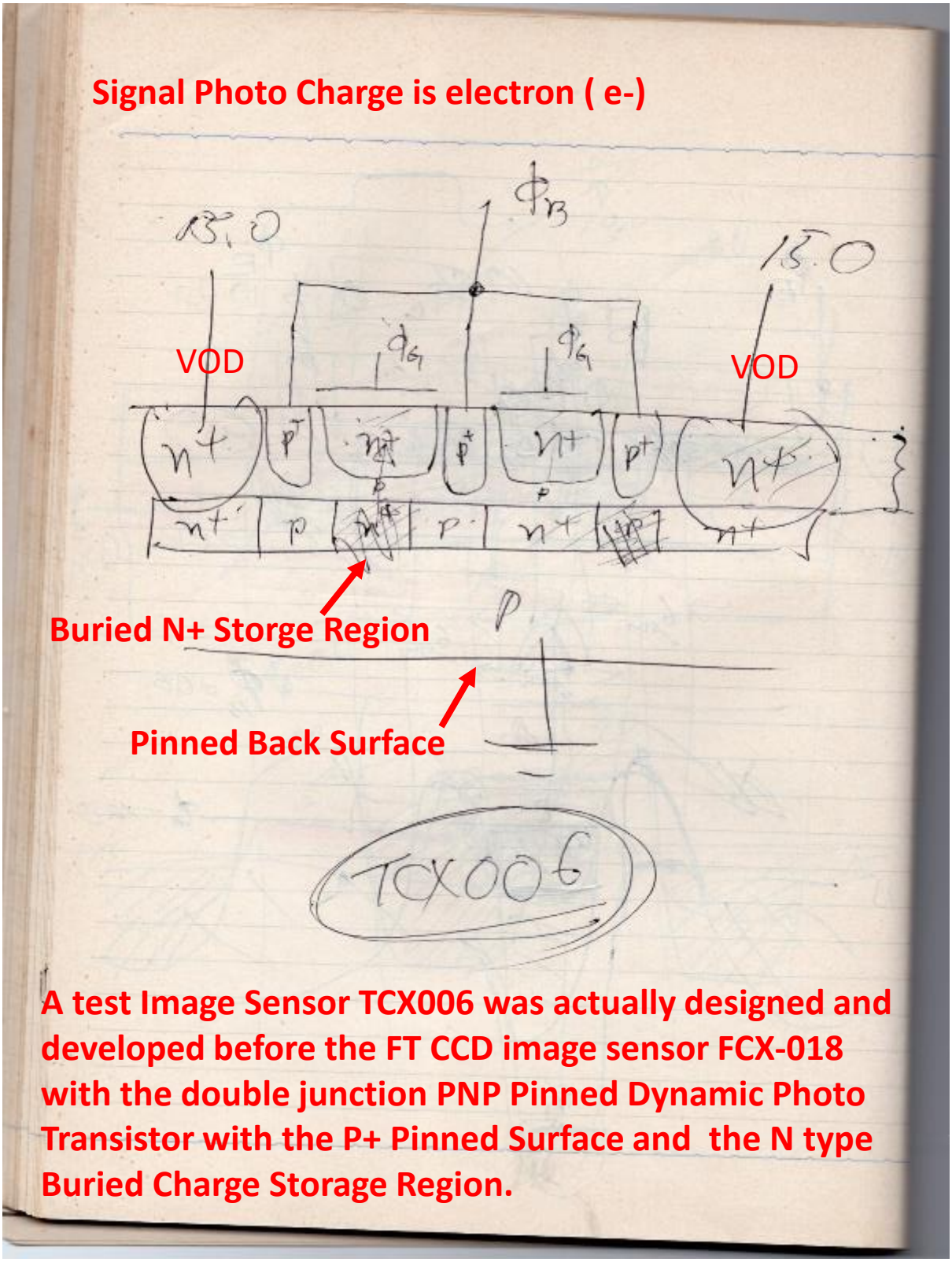
January 22, 1975

Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Yokohama Central Research Center

Yoshiaki Daimon Hagiwara

Page51, Back Light PNPN junction type Pinned Photodiode



A test Image Sensor TCX006 was actually designed and developed before the FT CCD image sensor FCX-018 with the double junction PNP Pinned Dynamic Photo Transistor with the P+ Pinned Surface and the N type Buried Charge Storage Region.

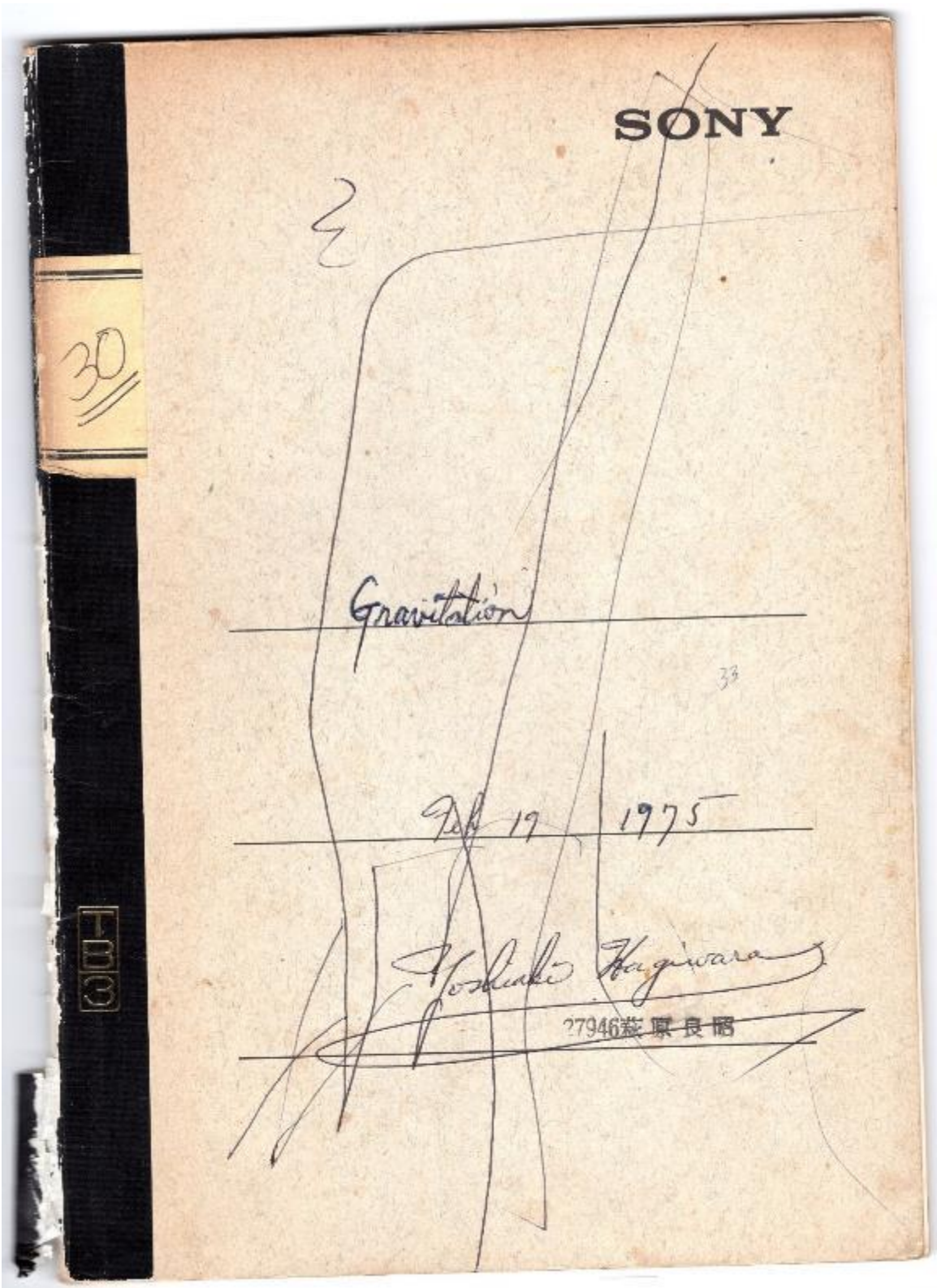
.

January 22, 1975

Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Yokohama Central Research Center

Yoshiaki Daimon Hagiwara

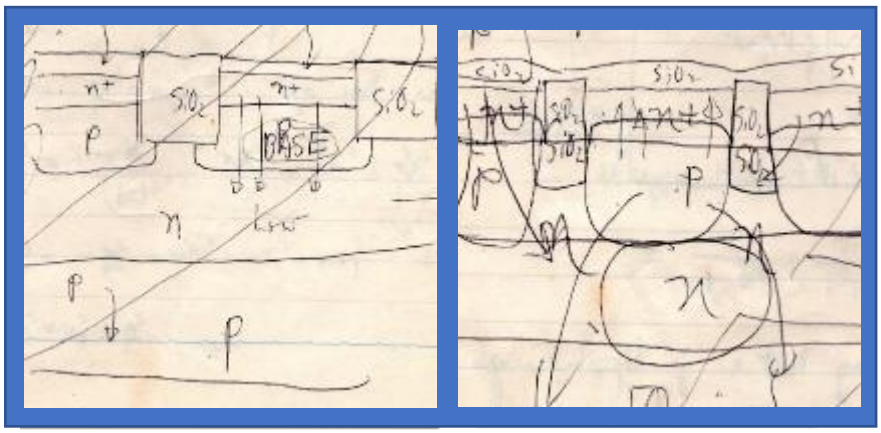


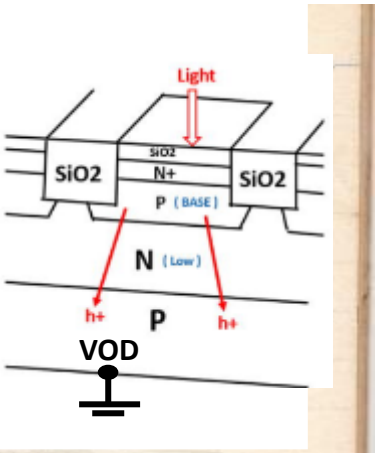
February 17, 1975

Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Yokohama Central Research Center
Yoshiaki Daimon Hagiwara

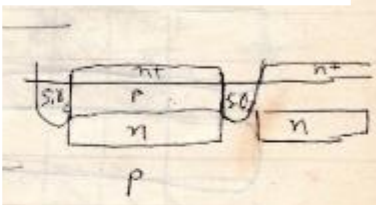
Page21, N+PNPsub junction type Pinned Photodiode

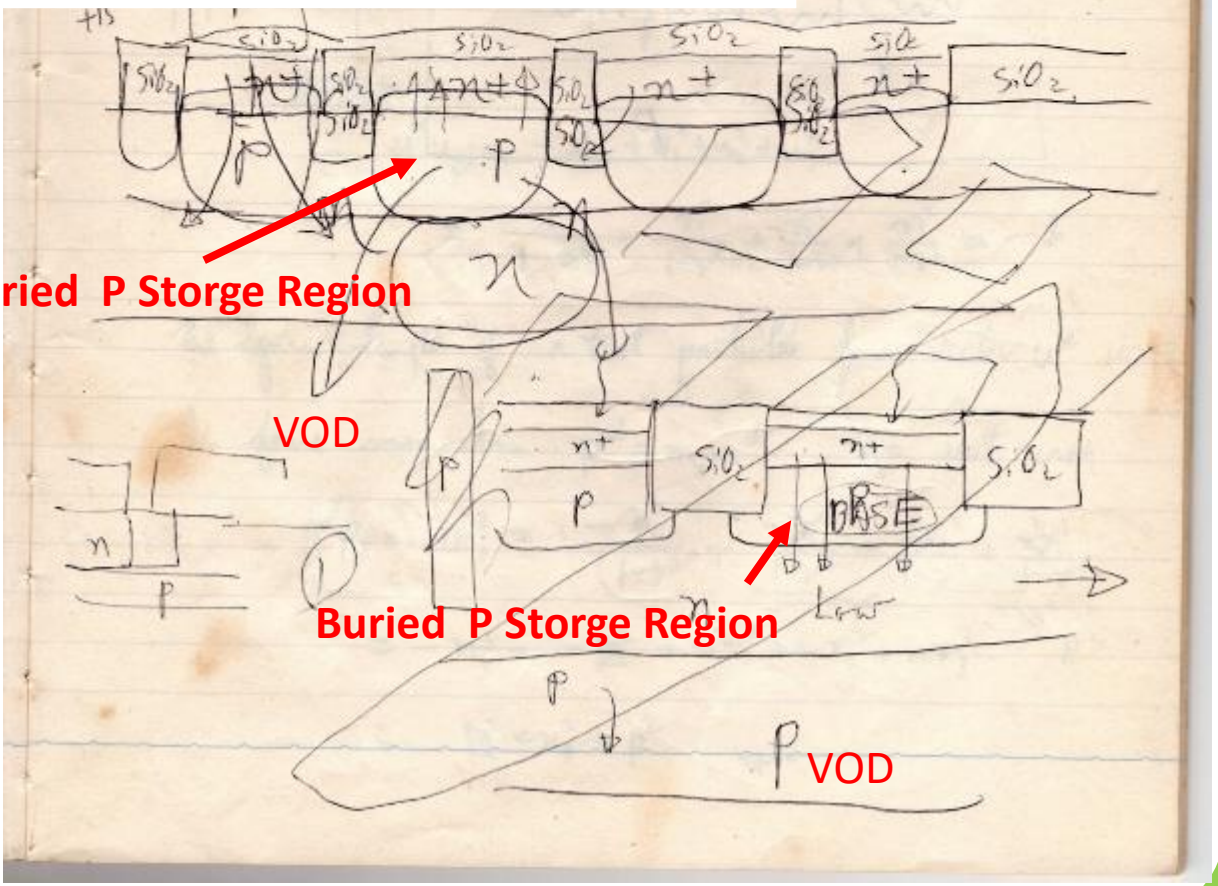




Hagiwara's Lab Note at Sony in February 1975

Signal Photo Charge is hole (e+)





February 17, 1975

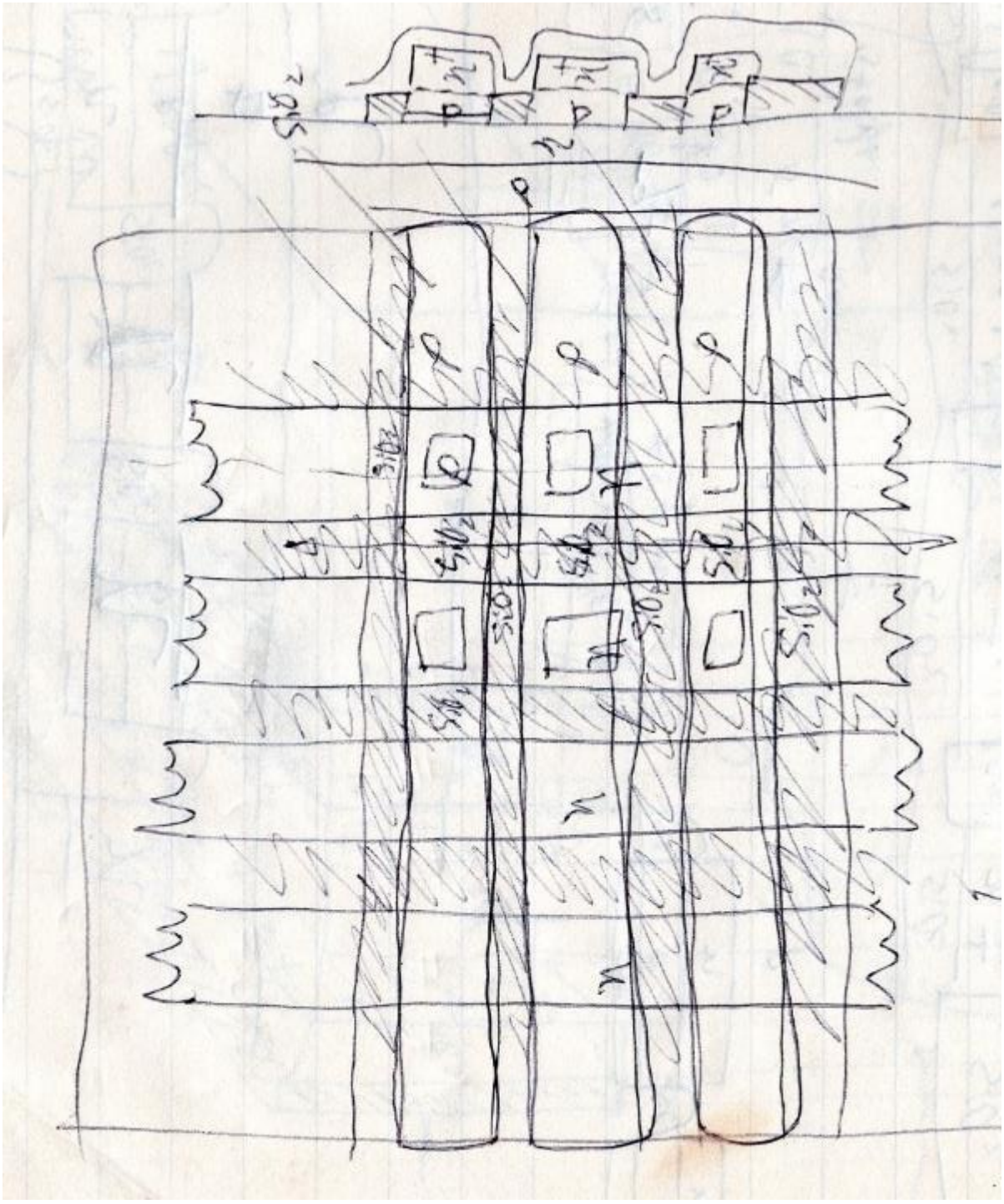
Sony Bipolar Transistor Hinted the invention of Pinned Photodiode

Lab Note at Sony Yokohama Central Research Center

Yoshiaki Daimon Hagiwara

Page22, N+PNPsub junction type Pinned Photodiode

Signal Photo Charge is hole (e+)



February 17, 1975

Japanese News Paper reporting that Sony defended the Patent War between Fairchild and Sony on Image Senor Basic Patent on Sony Hole Accumulation Diode (HAD) which is identical to Pinned Photodiode with VOD.

1996年7月　日刊工業新聞記事から
（2000年1月米国最高裁で最終決着ソニー勝訴）

CCD特許侵害訴訟

ソニー、逆転勝訴

NY東部地裁

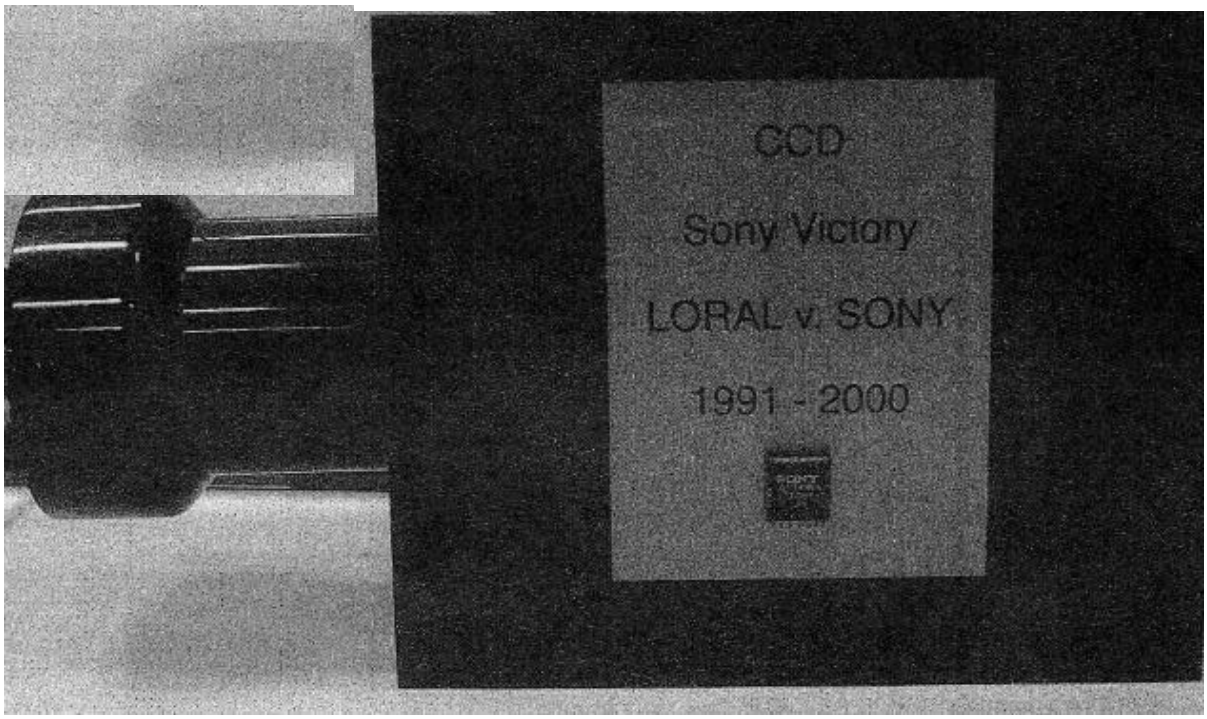
日刊 7/16

電子機器の基幹部品である電荷結合素子（CCD）の特許侵害訴訟を審理していた米ニューヨーク東部地裁は、ソニー（社長出井伸之氏）を訴えていた米ローラル・フェアチャイルド社の主張を退け、ソニー勝訴の判決を下した。同訴訟はソニーが特許を侵害しているとの陪審員評決が二月に出ていたが、ソニーが逆転勝訴した。フェアチャイルドは日立製作所、東芝など日韓の大手電機メーカー二十社以上を同様の趣旨で訴えており、ソニーの勝訴は他社の審理にも影響も与えそうだ。

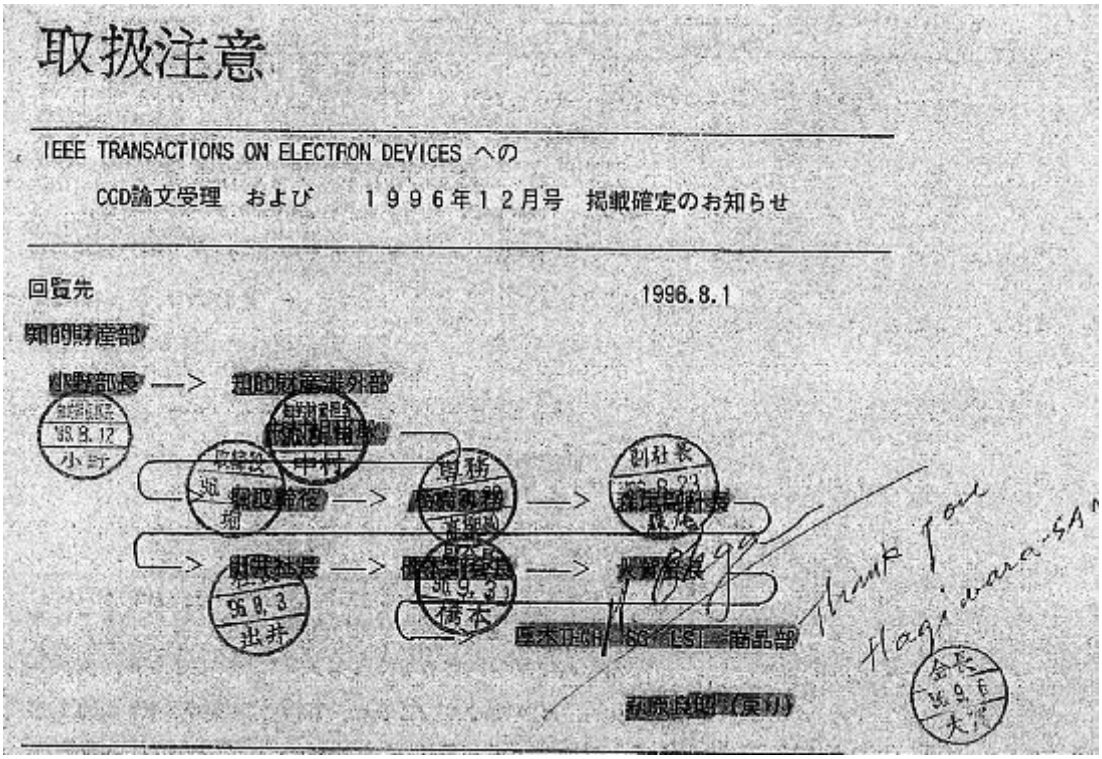
ソニーが十五日明らかにしたところによると、ニューヨーク東部地裁は「ソニー製のCCDはローラル・フェアチャイルド社の二件の特許に抵触しない」との判決を下し、陪審員の評決を破棄した。フェアチャイルドは控訴するかどうかの態度をまだ表明していないという。

CCDはカメラ一体型VTRやファクスなどの電子機器に使われる光学部品で「電子の目」と呼ばれる重要部品。フェアチャイルドは自社が保有するCCDの製造プロセスと構造に関する二件の特許を侵害しているとして九一年九月、ソニーのほか日立、東芝、沖電気工業、松下など日韓の大手各社を訴えていた。ソニーは「当社のCCDはフェアチャイルドの特許とは異なる製造プロセスと構造を採用していると主張してきたが、その正当性が認められた」としている。ただフェアチャイルドが控訴すれば、裁判が再び長期化する可能性も残っている。

Sony celebrated the victory of the long Patent War (1991 to 2000) between Fairchild and Sony on Image Senor Basic Patent of Pinned Photodiode with the vertical overflow drain (VOD) function.



Thank You Note from Mr. Ohga (Sony Chairman) to Yoshiaki Hagiwara for his contribution to the patent war.


取扱注意

IEEE TRANSACTIONS ON ELECTRON DEVICES への
CCD論文受理 および 1996年12月号 掲載確定のお知らせ

回覧先 1996.8.1

知的財産部

Thank You
Hagiwara-SAN

Sony Semiconductor Company 1999 President Award Certificate to Yoshiaki Hagiwara for his contribution in defending for Sony at the Image Sensor Patent War (1991-2000) against Fairchild.

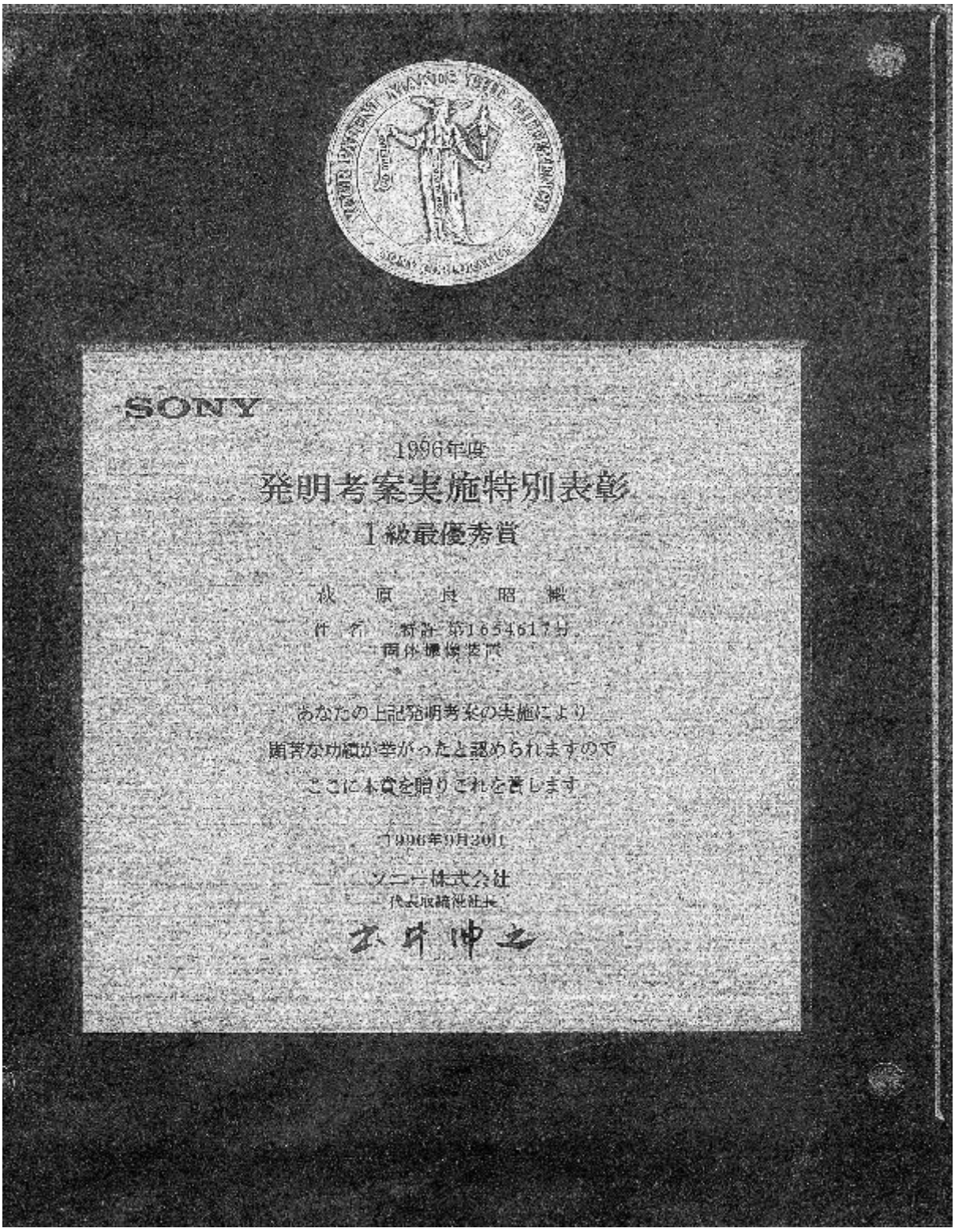
1999
SC President Award
プロセスマネジメント賞
個人賞
ＣＣＤビジネス特許紛争へのサポート

半導体戦略室　萩原良昭殿

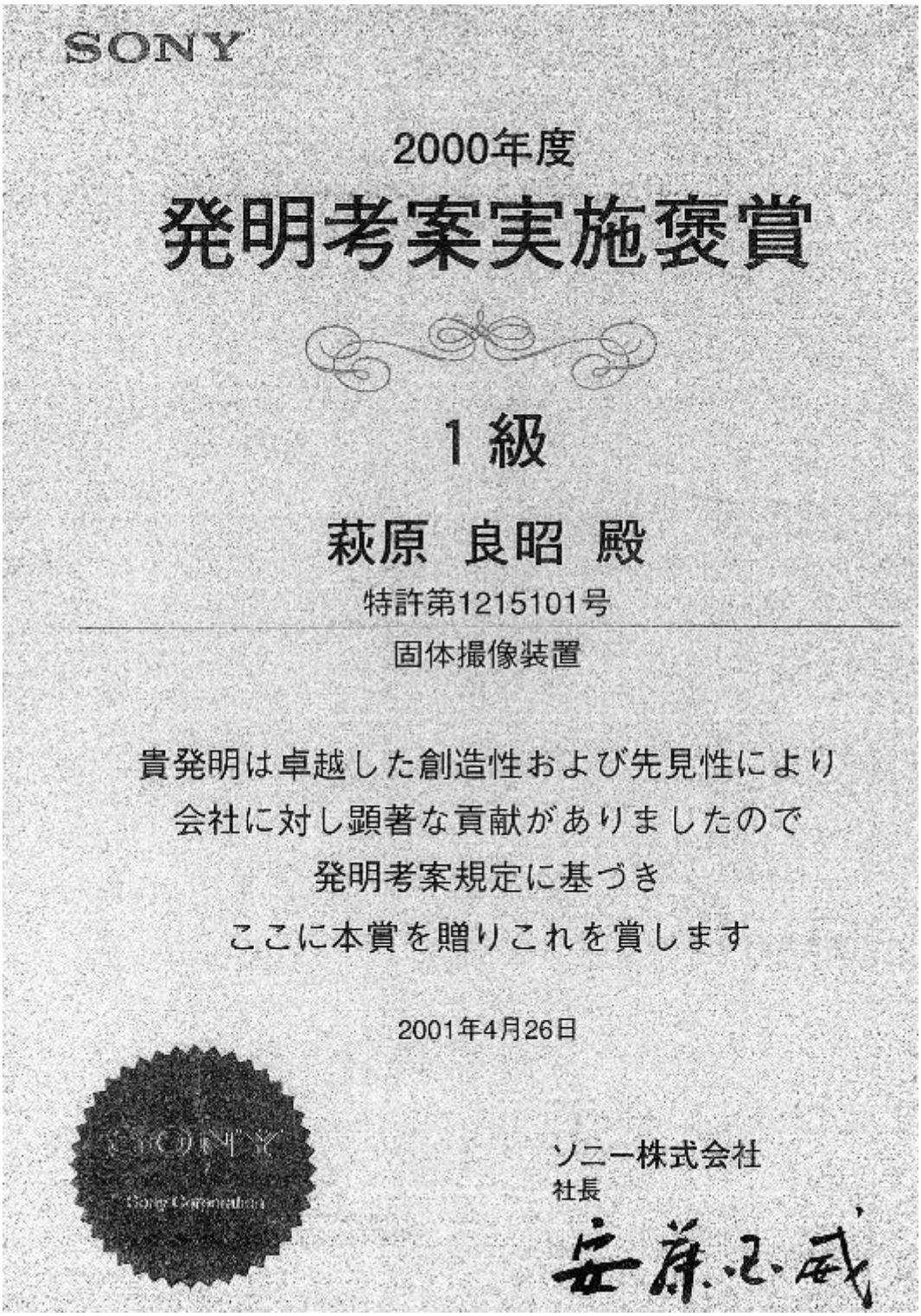
あなたはＣＣＤに関しての長年のローラルとの
特許紛争において最高裁判所での
ソニー勝利の判決に多大な貢献をされました
また７５年以来人材育成・特許Defenseに
おいても重要な役割を果たされてきました
その成果はＳＣビジネスへの貢献において
高く評価されます
よって ここにその功績を称え表彰致します

２０００年４月１０日
ソニー株式会社 常務
コアテクノロジー＆ネットワークカンパニー
セミコンダクタカンパニープレジデント

Sony President 1996 Award Certificate of Patent 1654617 on the electrical shutter clocking scheme of image sensors with the in-pixel overflow drain (OFD) punch-thru modulation.



Sony President 2000 Award Certificate of Patent 1215101 on the PNPN triple junction dynamic photo transistor which is called as Sony Hole Accumulation Diode (HAD) and also as Pinned Photodiode with the vertical overflow drain (VOD) with the in-pixel overflow drain (OFD) punch-thru modulation.



SONY

2000年度

発明考案実施褒賞

1級

萩原 良昭 殿

特許第1215101号

固体撮像装置

貴発明は卓越した創造性および先見性により
会社に対し顕著な貢献がありましたので
発明考案規定に基づき
ここに本賞を贈りこれを賞します

2001年4月26日

ソニー株式会社
社長