History of Semiconductor Devices

MOSFETの発明
Al/Al2O3/Cu2S
1926,1928 Lilienfield

Si MOSFETの発明
1960 Kahng

Si CMOSの発明
1963 Wanlass

④ 1T1C 型DRAMの発明
1966 NEC 樗本、一条

1T1C 型DRAM の開発と Scaling 則
1967 IBM Dennard

初の3T1C DRAM 製品
1970 Intel

初の1T1C DRAM 動作実証
1971 GI

1T1C DRAM 用 Sense Amp回路
1972 GI

初の1T1C DRAMの製品化
1975 TI

① Bipolar Transistorの発明
1948年 Schocley et al

Wire Bond 型 集積回路の発明 1958 Kilby at TI

世界初の集積回路 1961 TI

MOS 集積回路 商品化
1963 RCA

Bipolar 集積回路商品化
1963 Fairchild

TI JAPAN 設立 (TI and SONY)

1970 SONY カラーTV用 Bipolar IC

Mooreの法則(original)
1965 Intel

All MOS Transistor Memory Computer
1970 IBM

初の MPUの商品化
1971 Intel

MOS Scaling 則
1972, 1974 Dennard et al,

② コンデンサー容量メモリー発明
1948年 Norbert Wiener

③ Photo Transistorの 発明
1950年 John Northrop Shive

Bipolar 型電荷転送装置(CTD)
1967年 G.Krause

MOS imager with Pixel 3 Tr Active AMP
by Peter Noble in 1966

磁気コア Bubble Memoryの発明
1967年 F.L.J. Sanster

MOS BBD 型電荷転送装置(CTD)
1970年 F.L.J. Sanster

⑦ 1975 Philips PNP Buried Photodiode

⑧ 1975 Sony HAD Sensor
PNPN Pinned Photodiode
with Anti-Blooming VOD

⑤ SCCD 型電荷転送装置(CTD)
1970年 Boyle and Smith

⑥ BCCD 型電荷転送装置(CTD)
1974年 Boyle and Smith

⑨ 1978 Sony PNP Pinned Photodiode
with adjacent P+ channel stops

⑩ NEC Buried Photodiode (= SONY HAD) @IEDM1982
KODAK Pinned Photodiode (= SONY HAD) @IEDM1984
SONY HAD Interline Transfer CCD Imager with VOD
の 商品化で市場制覇 1987 SONY

SONY HAD CMOS Imager 2019
with Back Light Illumination and Global Shutter Function

Hagiwara 1975 patents showed Features of No Image Lag , Empty Potential Well and Complete Charge Transfer of the double junction Pinned Buried Photodiodes.

(a) Pinned Photodiode defined in Fig. 7 of JPA1975-127647

Fig. 7A

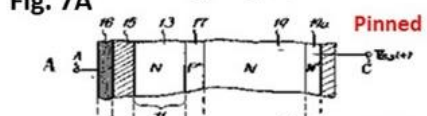


Fig. 7B

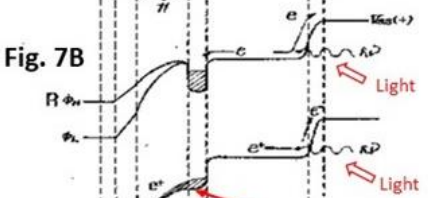


Fig. 7C

(b) Pinned Photodiode defined in Fig. 5 and 6 of JPA1975-134985

Metal Contact is optional

Fig. 5

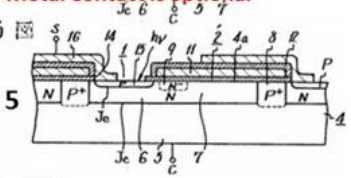


Fig. 6A

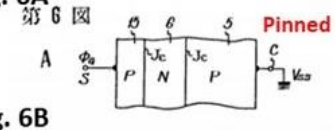
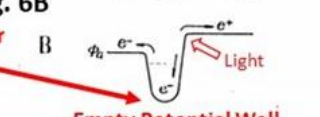


Fig. 6B

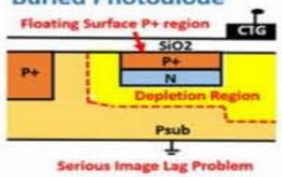


NEC IEDM1982 paper was not Pinned Photodiode by definition.

Difference of Buried Photodiode and Pinned Photodiode

Figure 5 does not have the P+ channel stop nearby.

Buried Photodiode



Serious Image Lag Problem

NEC IEDM1982 Paper

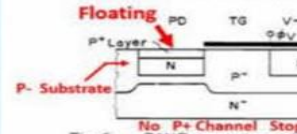


Fig.5. P+NP- structure photodiode
(a) Unit cell cross sectional view

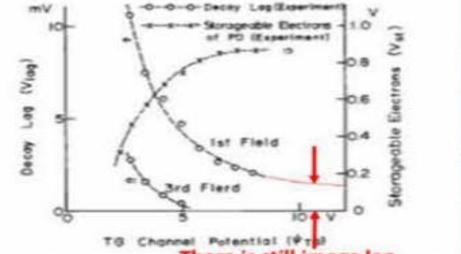


Fig.6. Storagenable electrons vs. transfer gate channel potentials, and decay lag vs. transfer gate channel potential in the P+NP- structure photodiode

NEC IEDM1982 Paper reported Image Lag

Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 volt.