History_of_Invention_and_Development_of_Pinned_Photodiode

Yoshiaki Hagiwara

To Whom It May Concern,
Dear Sir,

July 23, 2021

My name is Yoshiaki Hagiwara. I used work at Sony and developed semiconductor LSI chip sets for consumer and industrial applications from 1975 till 2008. My first work at Sony since 1975 till 1980 was the development of solid state image sensors. I would like to explain here the details of my 1975 invention of Pinned Photodiode and the subsequent pioneering development efforts of the first Pinned Photodiode, which was reported at SSDM1978 Tokyo Conference in 1978 by Sony.

I believe that I am the inventor of Pinned Photodiode, as defined in the three Japanese Patent Applications, JPA1972-127646, JPA1975-127647 and JPA1975-134985, and also I am the person who developed the first Pinned Photodiode as reported in the SSDM1978 Tokyo Conference.

The following slides explained the details. Please look at these slides and if possible kindly let me know what you think about them. Do you agree with my point of view on the history of invention and development of Pinned Photodiode ? Please feel free to e-mail me (hagiwara@aiplab.com) .

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History_of_Invention_and_Development_of_Pinned_Photodiode

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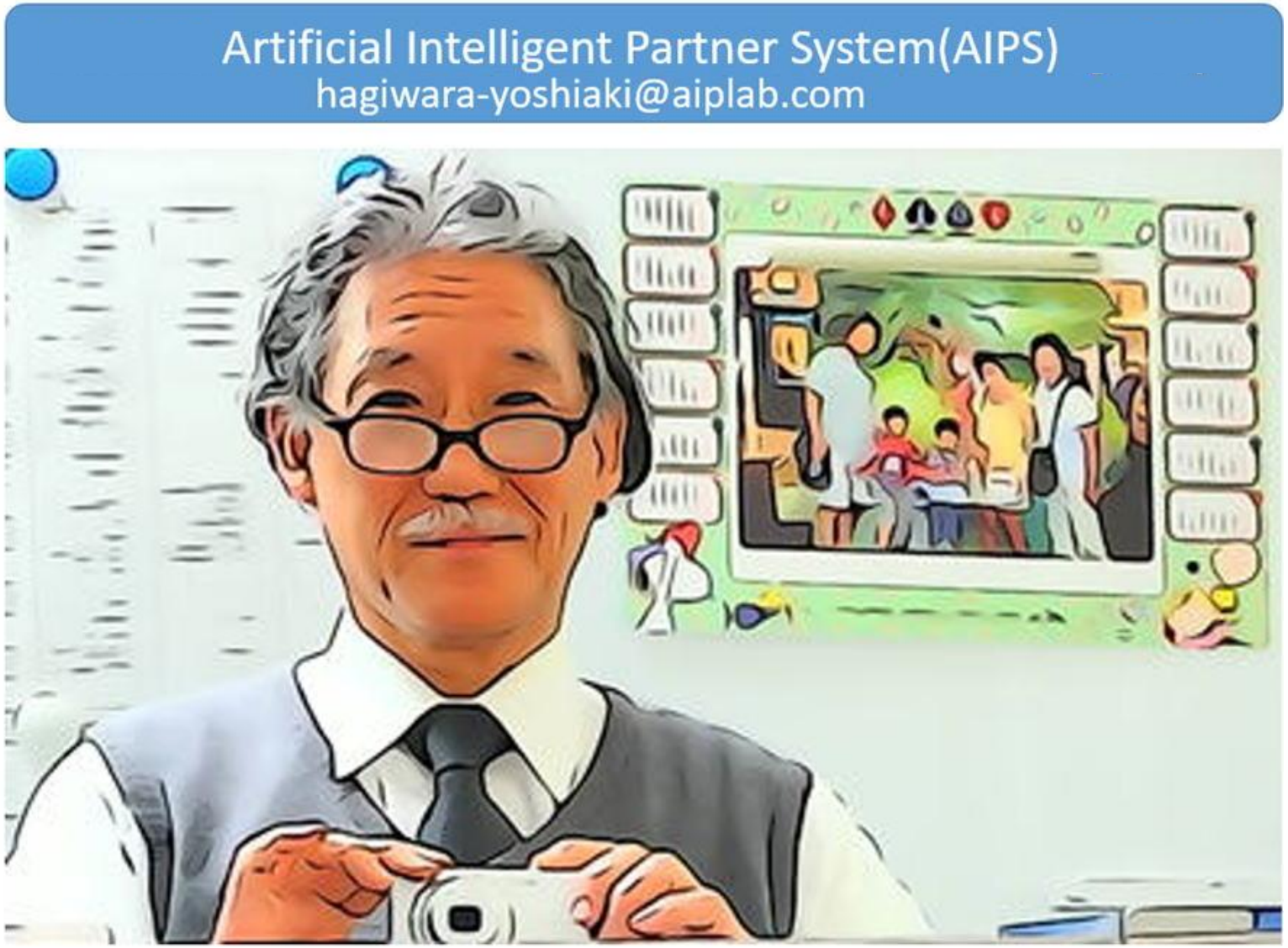

by Yoshiaki (Daimon) Hagiwara
IEEE Life Fellow

Born on July 4, 1948 in Kyoto Japan.
Moved to USA in 1965 for studying.
Graduated Riverside Polytechnic High School, Calif USA in June, 1967.
Graduated Caltech in Pasadena Calif. USA with the degrees of BS in 1971, MS in 1972 and PhD in 1975.
Worked for Sony Tokyo Japan from Feb 1975 till July 2008.
Worked as a professor at Sojo University in Kumamoto, Japan from April 2009 till March 2017.
Currently serving as the chair of the Education Committee of Society of Semiconductor Industry Specialists (http://www.ssis.or.jp).

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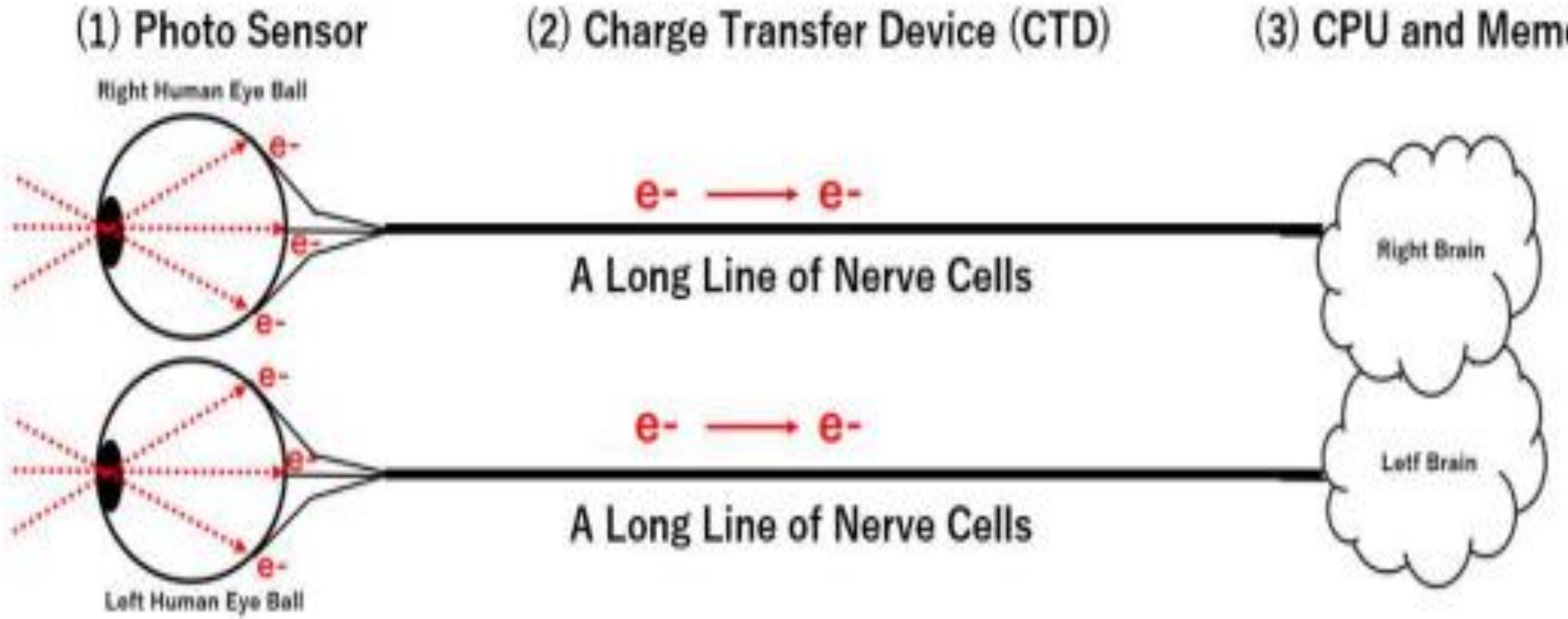

Basic Three Components of Intelligent Image Sensor

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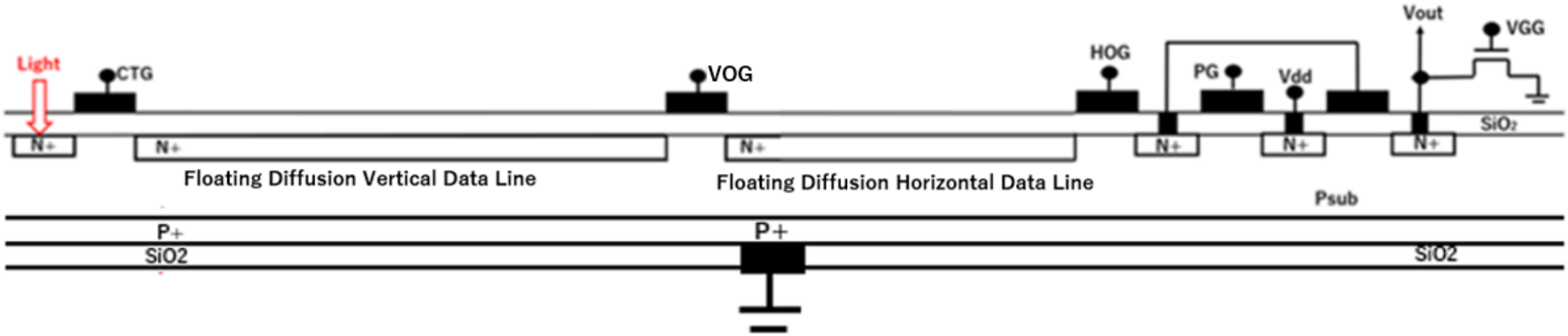
(1) A classical MOS image sensor has a single junction type Photodiode with the N+ Floating Surface Diffusion. It has a long floating diffusion output read-out data line as the charge transfer device (CTD).



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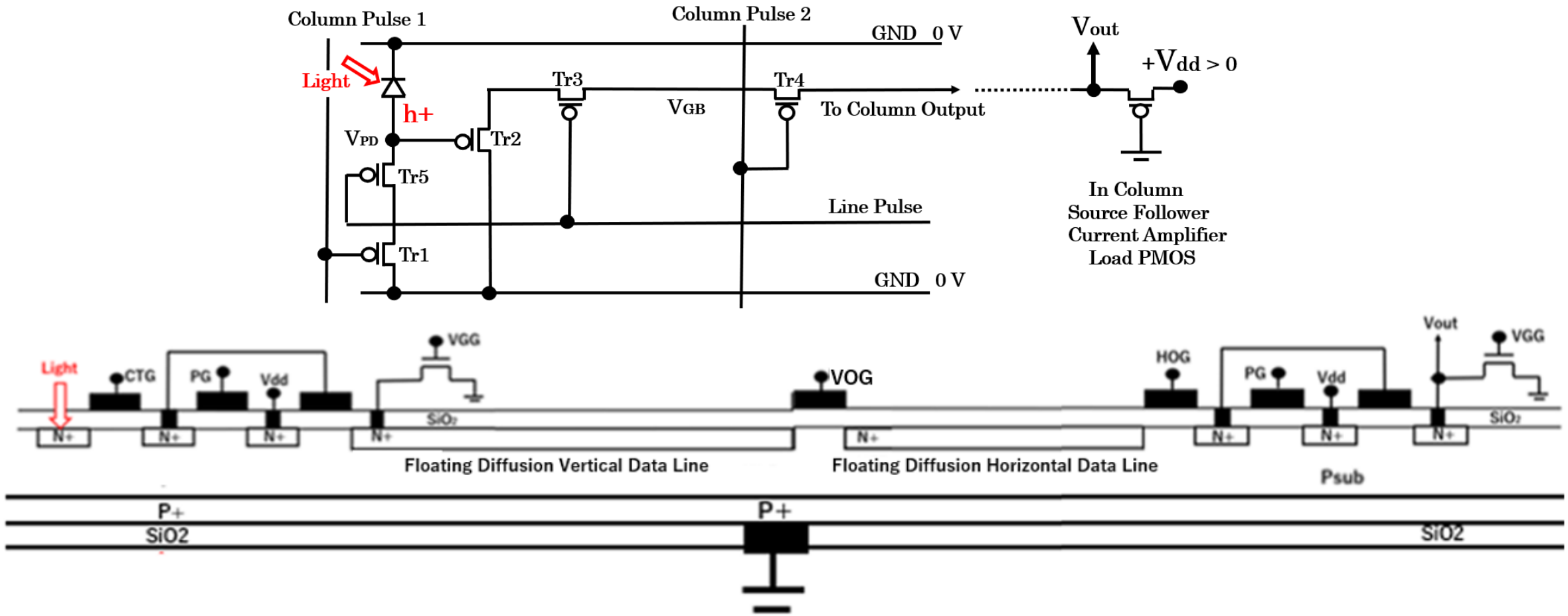
(2) Peter Noble proposed in 1968 to use an in-pixel source amplifier circuit for each picture element.

Peter Nobel, IEEE Transaction of Electron Devices 15-4 (1968) pp. 202-209



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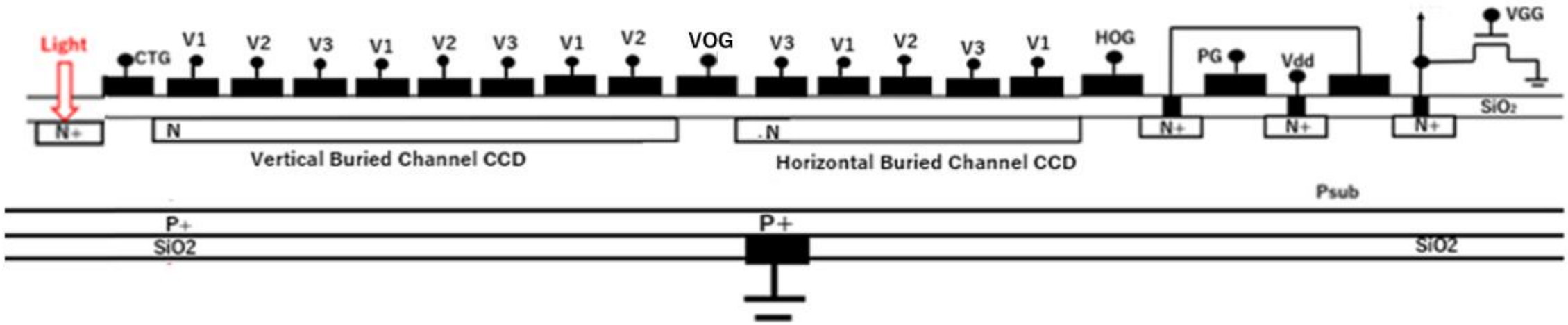
(3) Boyle and Smith in 1970 proposed the concept of charge couple device (CCD).

W. S. Boyle and G. E. Smith, “Charge Coupled Semiconductor Devices, ”
B. S. T. J., 49, No. 4 (April 1970) pp. 587-593.



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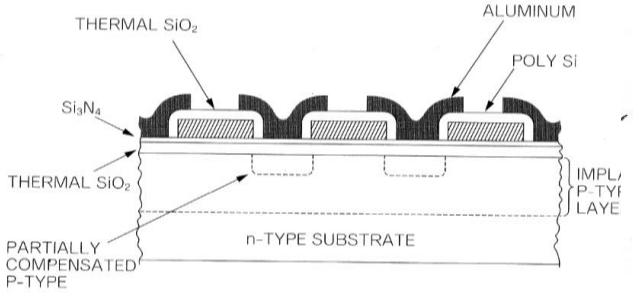
(4) Hughes Aircraft Company reported at IEDM1973 the Overlapped Electrode Structure to enhance the charge transfer efficiency of Buried Channel CCD in 1973.

D. M. Erb, W. Kotcyczka, S. C. Su, C. Wang, and G. Clough,
“An Overlapped Electrode Buried Channel CCD” IEDM1973, Dec 3-5 (1973)

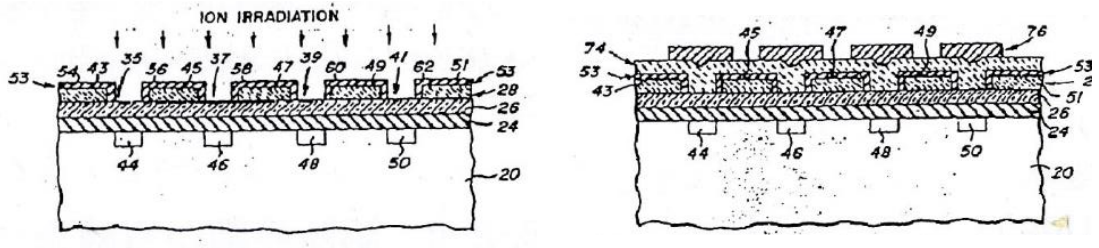
Gilbert F. Amelio, USP3931674, Jan 13, 1976,
"Self Aligned CCD Elementincluding Two Levels Electrodes..."

Sony CCD process is very similar to the Overlapped Electrode Structure reported at IEDM1973
Sony process used self-aligned ion implantation before the oxidation of the first electrode.

D.M.Erb, 1973

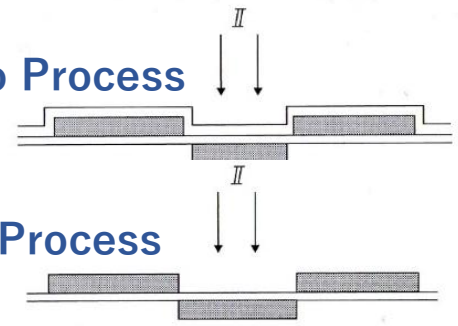


Gilbert F. Amelio, 1976



Amelio Process

Sony Process



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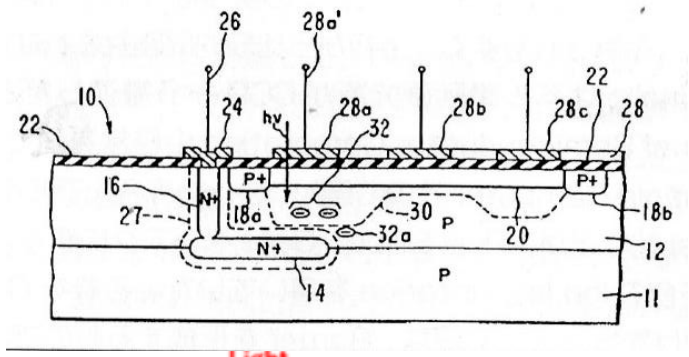
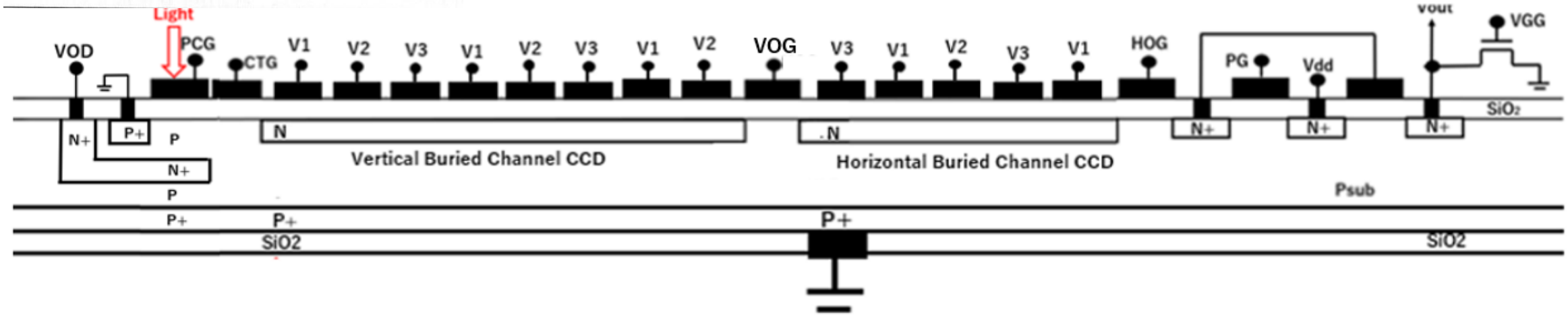
(5) James M. Early on July 22 in 1975 proposed the concept of in-pixel vertical overflow drain (VOD).

James M. Early , “Charge Coupled Device with Overflow Drain Protection”, USP3896485, July 22, 1975.





History_of_Invention_and_Development_of_Pinned_Photodiode

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(6) Yoshiaki Hagiwara on October 23 in 1975 proposed the concept of the triple junction type Pinned Photodiode with back light illumination mode with the in-pixel CCD/MOS type dynamic capacitor buffer memory for Global Shutter Operation needed critically for CMOS image sensors.

Yoshiaki Hagiwara, Japanese Patent Application JPA 1975-127646, October 23, 1975.

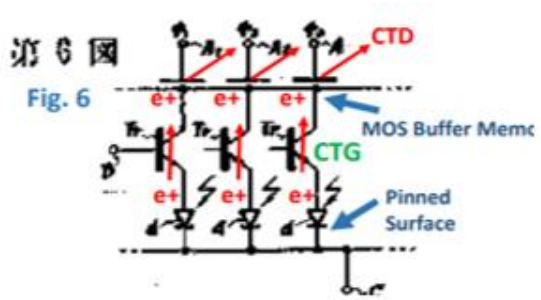
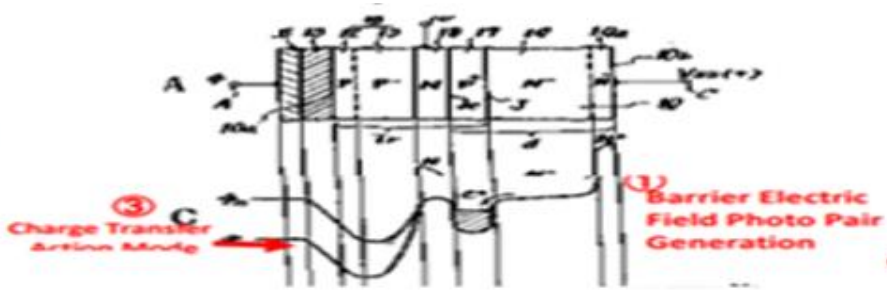


Fig. 6



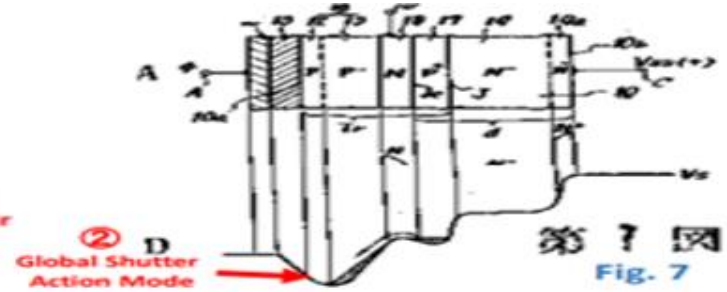
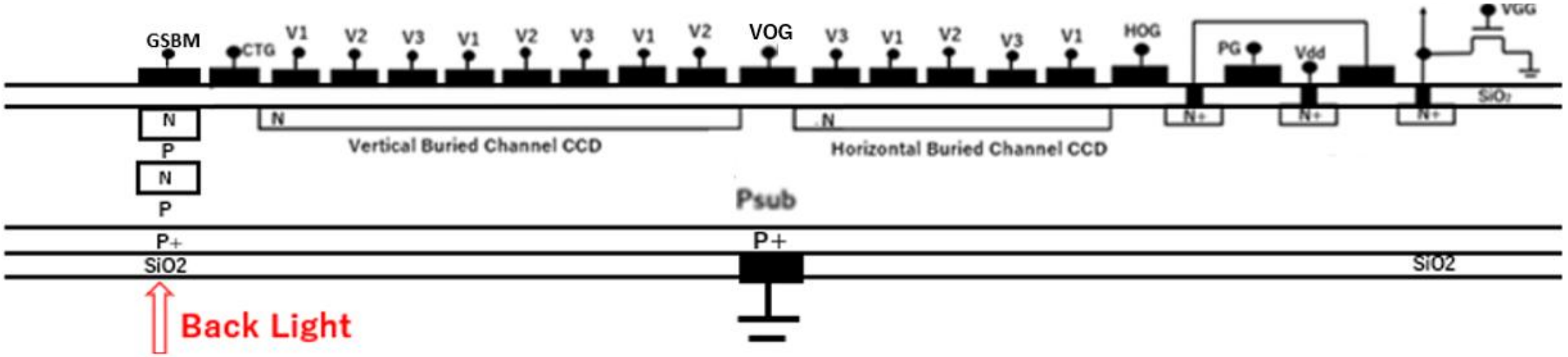


Fig. 7



History_of_Invention_and_Development_of_Pinned_Photodiode

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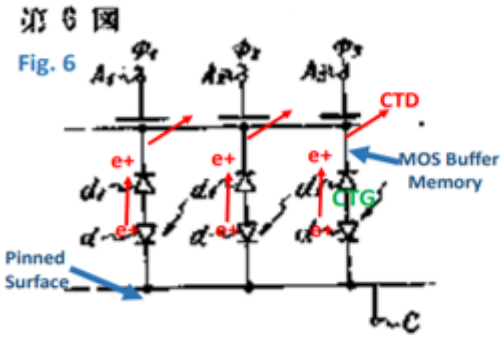
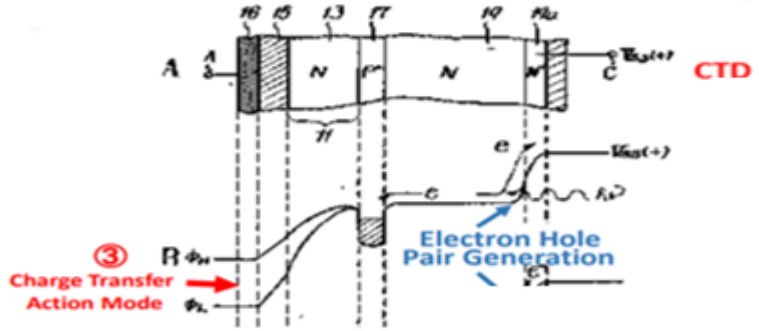
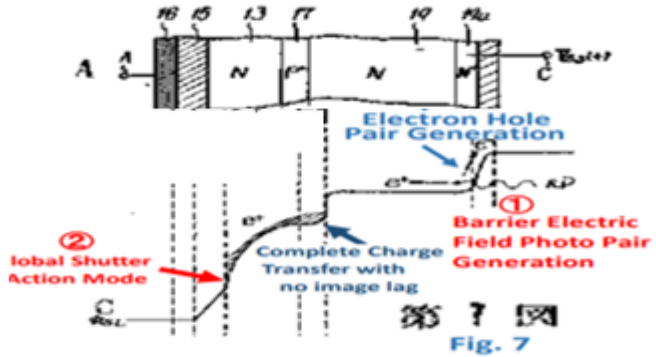
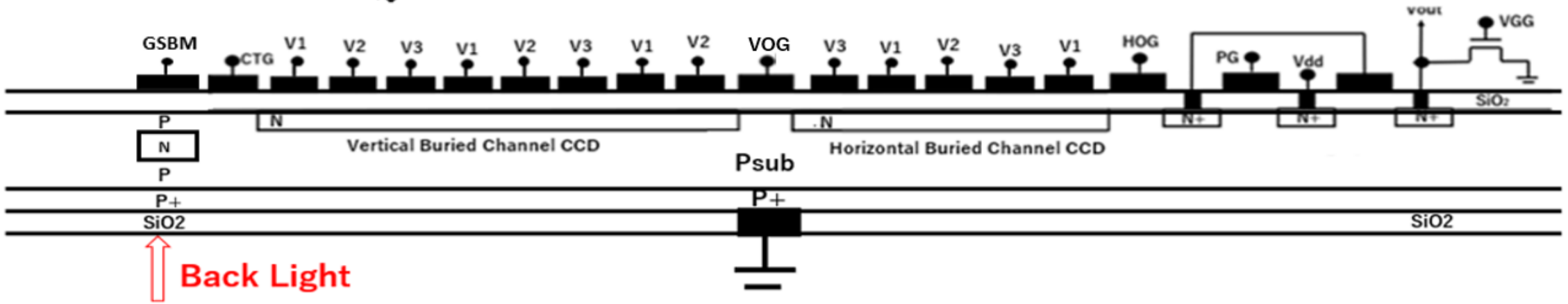
(7) Yoshiaki Hagiwara on October 23 in 1975 proposed the concept of the double junction type Pinned Photodiode with back light illumination mode with the in-pixel CCD/MOS type dynamic capacitor buffer memory for Global Shutter Operation needed critically for CMOS image sensors.

Yoshiaki Hagiwara, Japanese Patent Application JPA 1975-127647 , October 23, 1975.









History_of_Invention_and_Development_of_Pinned_Photodiode

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(8) Yoshiaki Hagiwara on November 10 in 1975 proposed the concept of the double junction type Pinned Photodiode with the front-side built-in vertical overflow protection capability

Yoshiaki Hagiwara, Japanese Patent N. 1215101 (Japanese Patent Application JPA1975-134985)

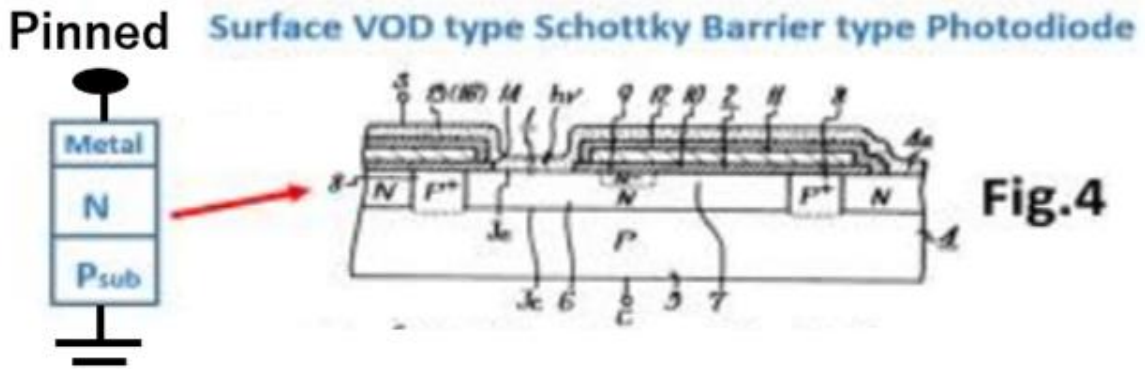


Fig.4

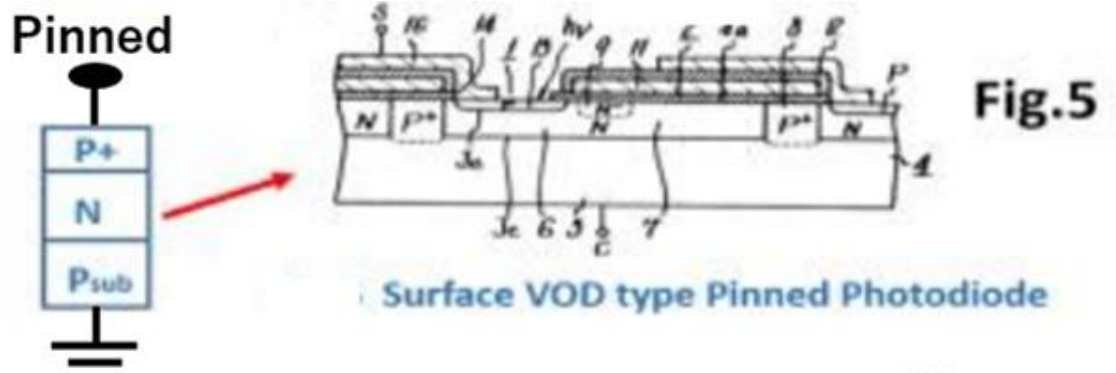
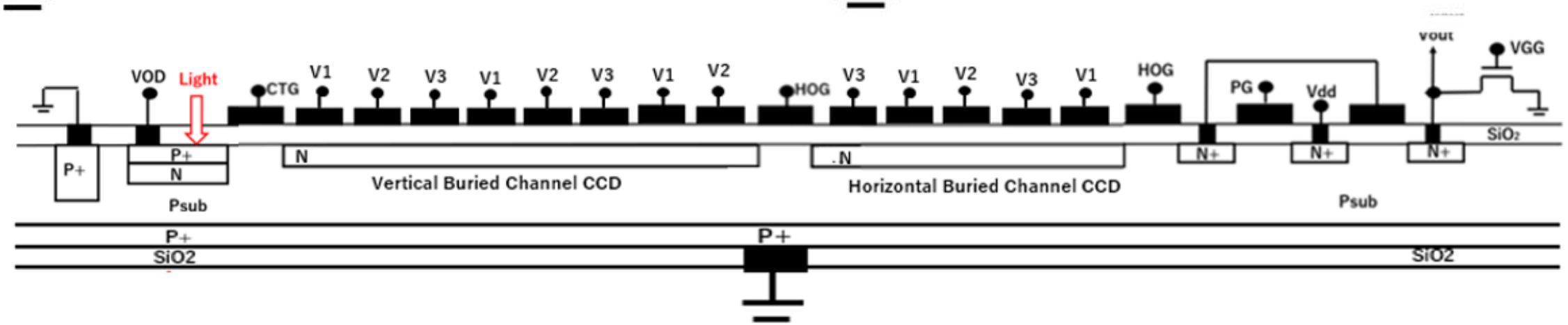


Fig.5

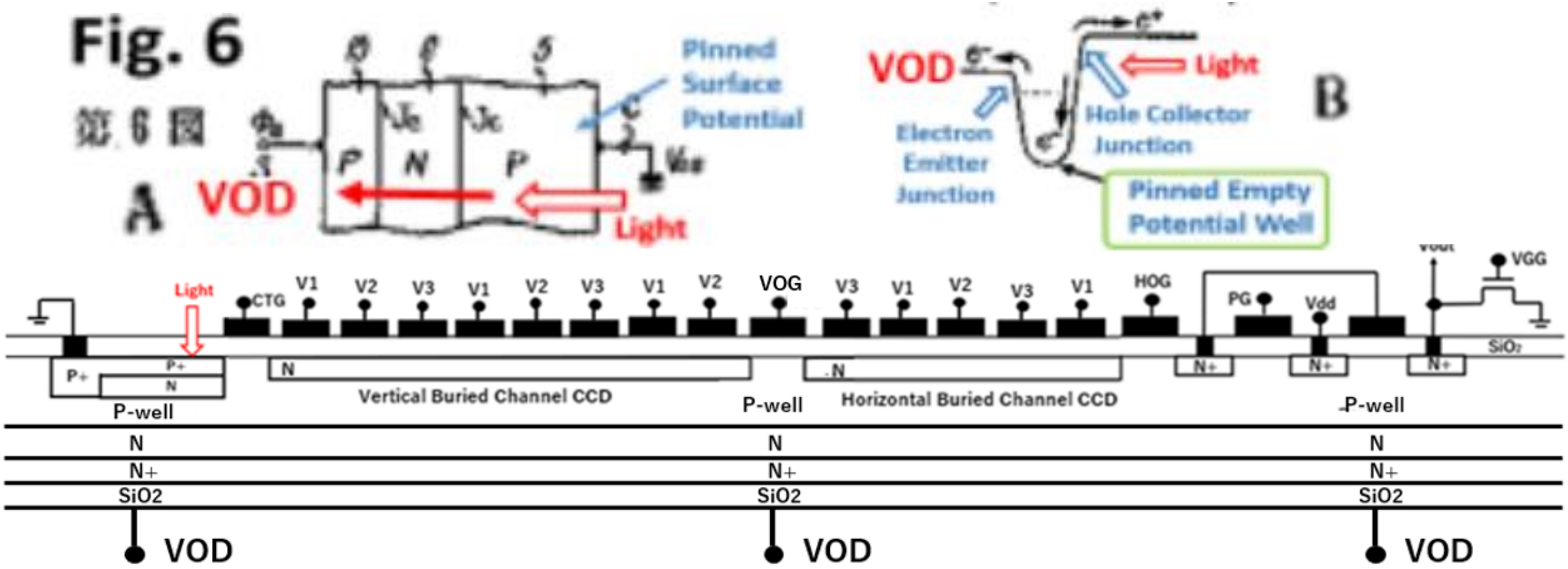


History_of_Invention_and_Development_of_Pinned_Photodiode

Yoshiaki Hagiwara

(9) Yoshiaki Hagiwara on November 10 in 1975 proposed the concept of the triple junction type Pinned Photodiode with the back-side built-in vertical overflow protection capability.

Yoshiaki Hagiwara, Japanese Patent No. 1215101（Japanese Patent Application JPA1975-134985)



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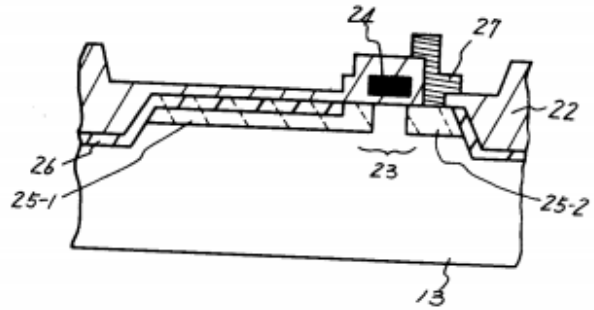
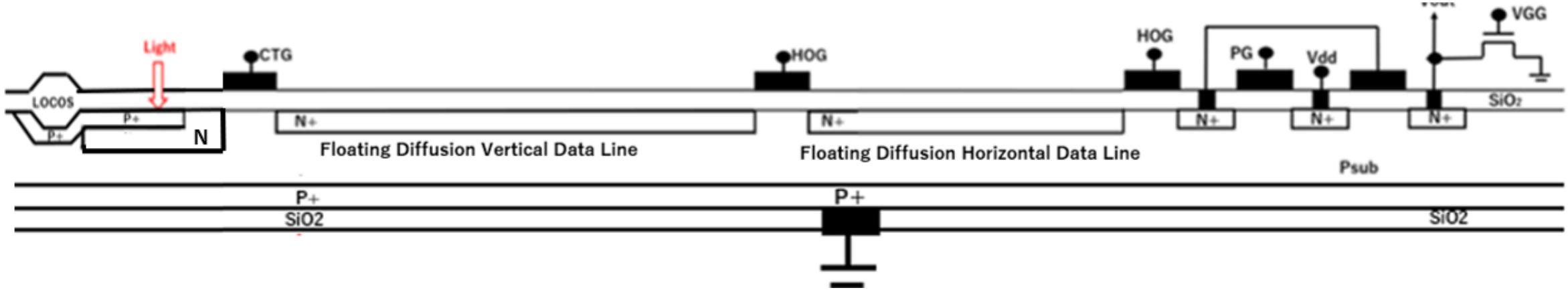
(10) Koike and Takemoto used P+NP Pinned Photodiode for MOS image sensor with overflow protection scheme by draining the excess signal charge thru the charge transfer gate (CTG) to the output diffusion data lines during the photo signal integration time.

Koike and Takemoto, Japanese Patent Application JPA1977-837, Jan 10, 1977
on P+NP Pinned Photodiode with Overflow Protection Scheme.



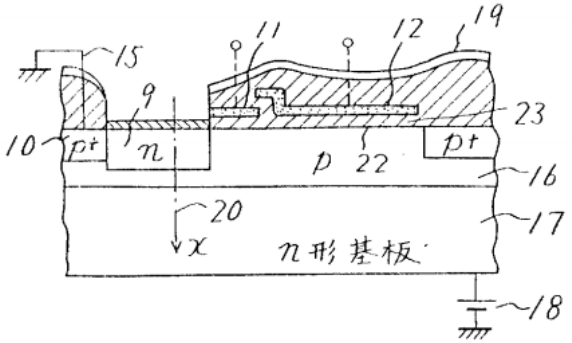


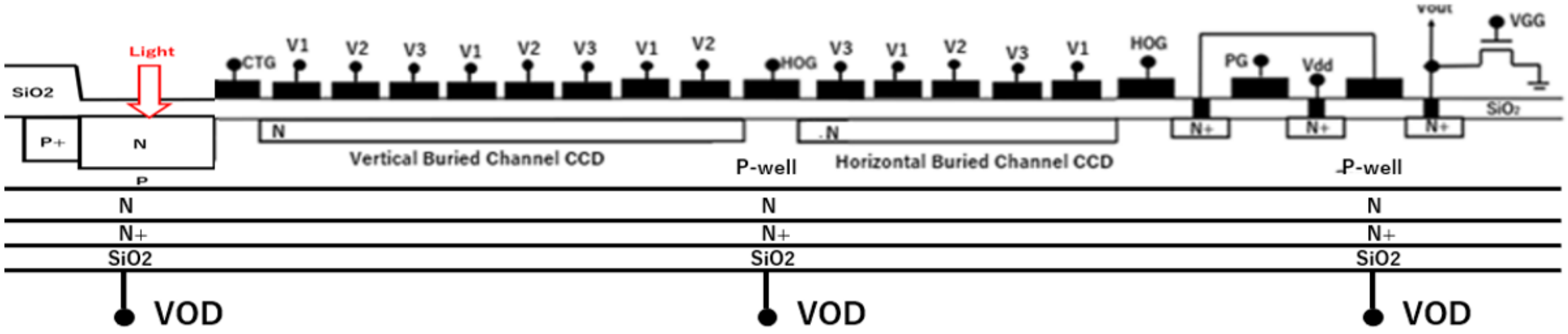
History_of_Invention_and_Development_of_Pinned_Photodiode

Yoshiaki Hagiwara

(11) Yamada at Toshiba proposed in 1988 the NPN double junction type Photodiode with the floating surface N diffusion storage region with the vertical overflow protection.

T. Yamada, Japanese Patent Application JP1978-1971
on NPN double junction type photodiode
with overflow protection, filed on Jan 13, 1978





History_of_Invention_and_Development_of_Pinned_Photodiode

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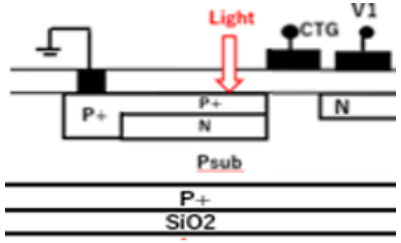
(12) Sony developed in 1978 the P+NP double junction type Pinned Photodiode with the complete charge transfer capability to realize the excellent feature of no image lag for fast action pictures.

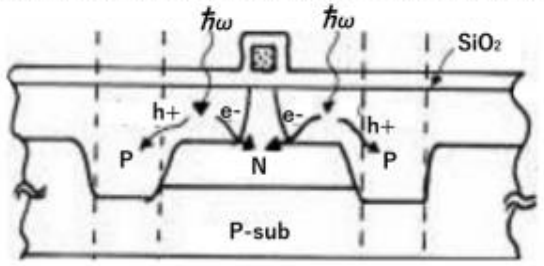
The pinned surface P+ hole accumulation region was formed by self-aligned ion implantation. Total dark current was measured to be less than 5 nA/cm^2. And the dark current level was less than 3 % of the maximum signal level at room temperature of 20 ℃. Very low surface dark current was observed since there is no electric field in the Pinned P+ surface region,

Yoshiaki Hagiwara, SSDM1978 `Paper and Japanese Patent No. 1215101 (Japanese Patent Application JPA 1975-134985)

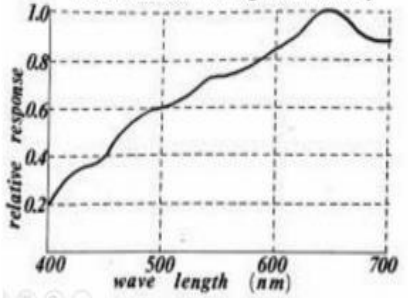
Yoshiaki Hagiwara, Motoaki Abe and Chikara Okada, “A 380H x 488V CCD Imager with Narrow Channel Transfer Gates”.
Proceeding of the 10th Conference on Solid State Devices, Tokyo 1978;
Japanese Journal of Applied Physics, Volume 18(1979) Supplement 18-1, pp. 335-340.



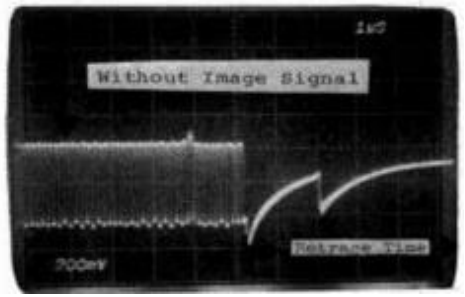
(A) Pinned-Surface and Buried-Storage PNP Photodiode with Adjacent Channel Stops



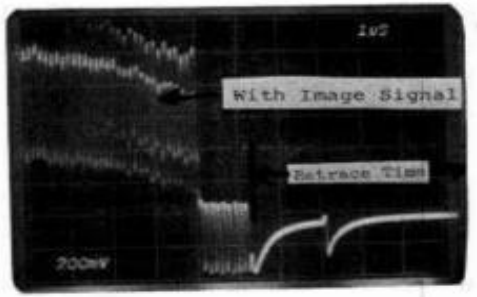
(B) Spectral Response with Very High Short-Wave Blue Light Sensitivity



(C) Signal Output with No Light showing Very Low Dark Current Featu



(D) Signal Output with Input Light showing No Image Lag Feature

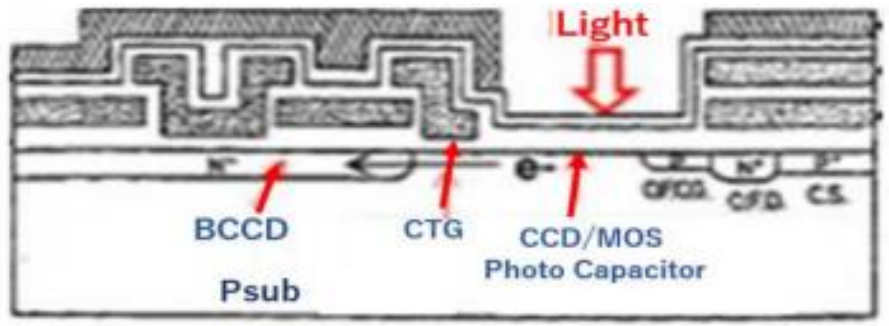


History_of_Invention_and_Development_of_Pinned_Photodiode

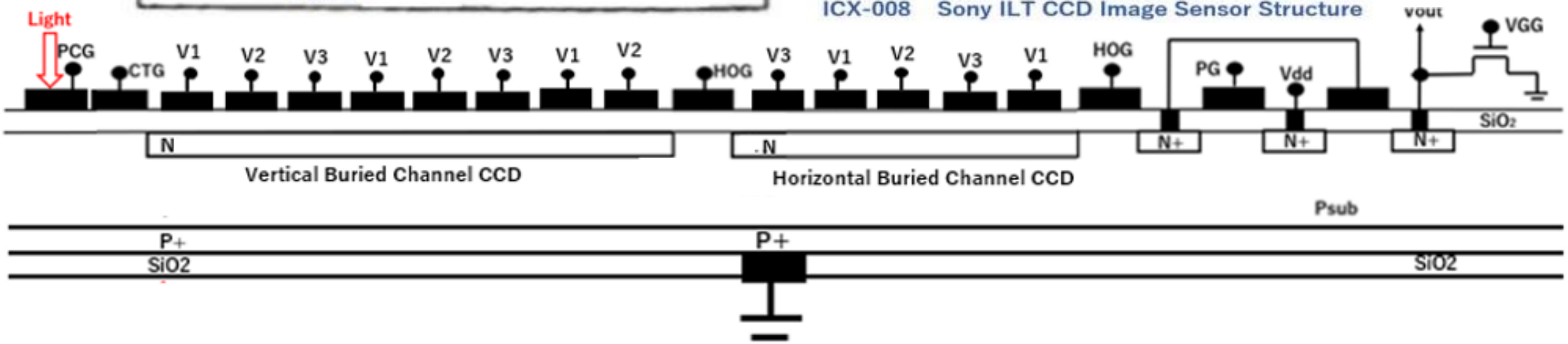
Yoshiaki Hagiwara

(13) Sony developed the CCD/MOS dynamic photo capacitor type photon detecting device and the CCD type Charge Transfer Device (CTD) for an interline CCD image sensor in 1980 with the complete charge transfer of no image lag feature for fast action pictures.

Y. Kanoh, T. Ando, H. Matsumoto, Y. Hagiwara and T. Hashimoto, "Interline Transfer CCD Image Sensor", Technical Journal of Television Society, ED 481, pp. 47-52, Jan 24, 1980.



ICX-008 Sony ILT CCD Image Sensor Structure



History_of_Invention_and_Development_of_Pinned_Photodiode

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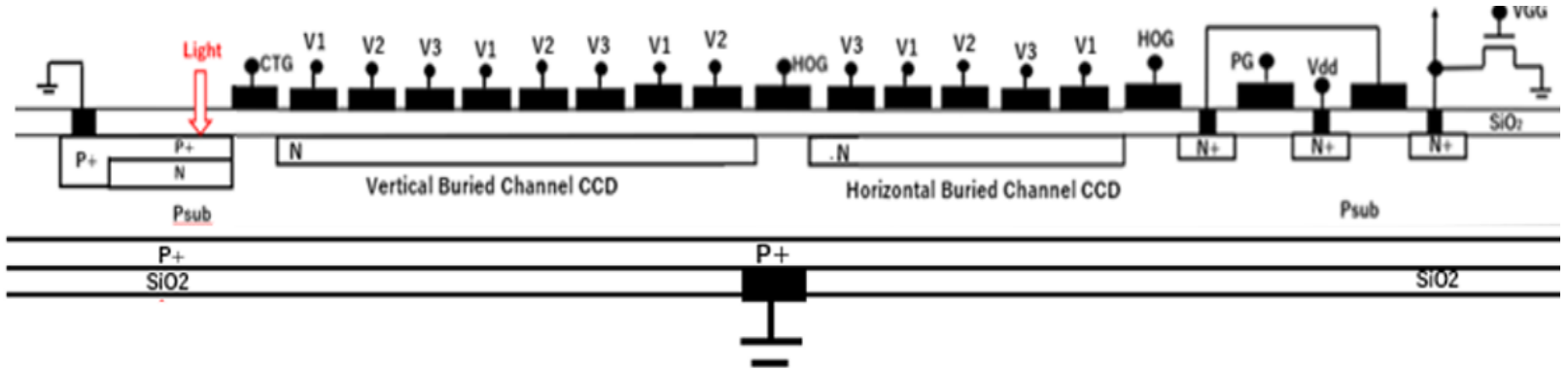
(14) Sony used the P+NP double junction type Pinned Photodiode for 380H x 488V in 1978 and 570H x488V one chip color FT CCD Image Sensors in 1980.

Yoshiaki Hagiwara, SSDM1978 `Paper and Japanese Patent No. 1215101 (Japanese Patent Application JPA 1975-134985)

Yoshiaki Hagiwara, Motoaki Abe and Chikara Okada, “A 380H x 488V CCD Imager with Narrow Channel Transfer Gates”.
Proceeding of the 10th Conference on Solid State Devices, Tokyo 1978;
Japanese Journal of Applied Physics, Volume 18(1979) Supplement 18-1, pp. 335-340.

I. Kajino, M. Shimada, Y. Nakada, Y. Hirata and Y. Hagiwara,”
Single Chip Color Camera Using Narrow channel CCD Imager with Over Flow Drain”,
Technical Report of The Institute of Image Information and Television Engineers,
vol. 5, no. 29, pp. 32-3S, (1981).



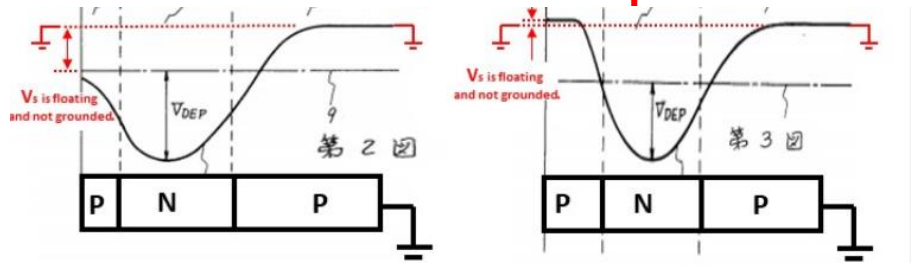
Sony 1980 Video Movie has in one body
an 8 mm VTR and One Chip FT CCD Image Sensor
with the PNP Double Junction type Pinned Photodiode
developed by Hagiwara in 1978

History_of_Invention_and_Development_of_Pinned_Photodiode

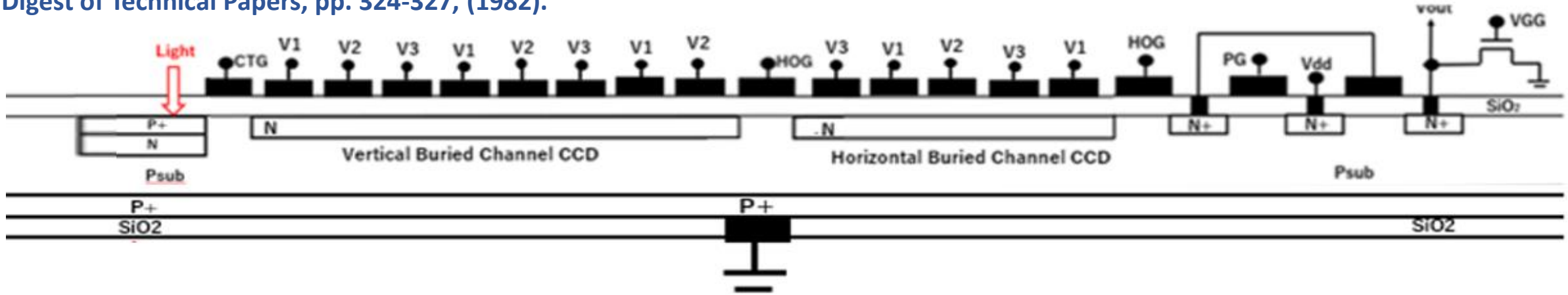
Yoshiaki Hagiwara

(15) NEC used Buried Photodiode for the ILT CCD image sensor for the first time in the world. However, the P+NP double junction type Buried Photodiode did not have any adjacent P+ channel stops region. The NEC IEDM1982 reported the details of the serious image lag problems. This is NOT Pinned Photodiode. The buried N storage region of this Buried Photodiode is floating since the surface P+ is not pinned. There is a large RC delay constant and the long P+ surface diffusion stripe would be floating.

The surface P+ is not pinned.



N. Teranishi, Y. Ishihara and H. Shiraki, Japanese Patent Application JPA1980-138026.
N. Teranishi, A. Kohono, Y. Ishihara, E. Oda, and K. Arai,
"No image lag photodiode structure in in the interline CCD image sensor",
1982 International Electron Devices Meeting (IEDM1982)
Digest of Technical Papers, pp. 324-327, (1982).



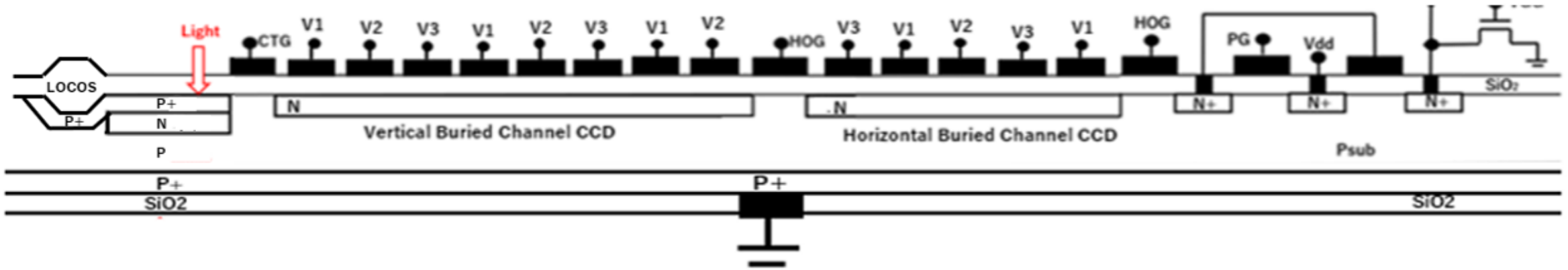
History_of_Invention_and_Development_of_Pinned_Photodiode

Yoshiaki Hagiwara

(16) KODAK developed in 1984 the P+NP double junction type Pinned Photodiode, which has the adjacent P+ channel stops under the LOCOS region. Consequently, the buried N storage region has the pinned empty potential well when the signal charge is completely drained.

B. C. Burkey, W. C. Chang, J. Littlehale, T. H. Lee, T. J. Tredwell, J. P. Lavine, E. A. Trbk,
"The Pinned Photodiode for an Interline-transfer CCD Image Sensor",
IEDM1984, Digest of Technical Papers, paper (2.3), (1984).

Yoshiaki Hagiwara invented Pinned Photodiode In 1975.
Sony used Pinned Photodiode for the FT CCD image sensor for the first time in the world in 1978.
NEC used Buried Photodiode for the ILT CCD image sensor for the first time in the world in 1982.
Kodak used Pinned Photodiode for the ILT CCD image sensor for the first time in the world in 1984.

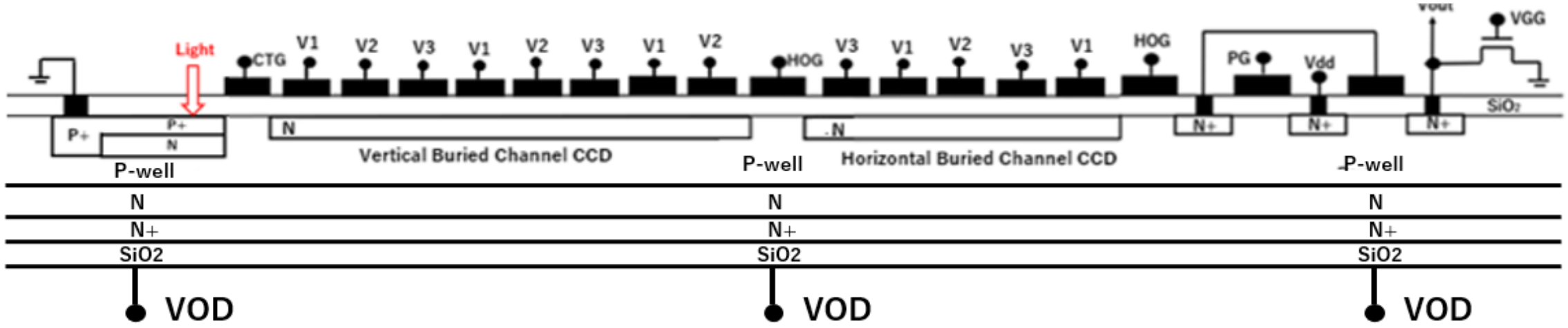


History_of_Invention_and_Development_of_Pinned_Photodiode

Yoshiaki Hagiwara

(17) Sony developed in 1987 the P+NPN triple junction type Pinned Photodiode with the pinned surface P+ hole accumulation region formed by high energy ion implantation without LOCOS with the overflow protection and the electrical shutter function for fast action pictures.

M. Hamasaki, T. Suzuki, Y. Kagawa, K. Ishikawa, K. Miyata and H. Kambe,
"An IT-CCD image with electronically variable shutter speed",
Technical Report of The Institute of Image Information and Television Engineers. vol. 12, no. 12, pp. 31-36, (1988).



History_of_Invention_and_Development_of_Pinned_Photodiode

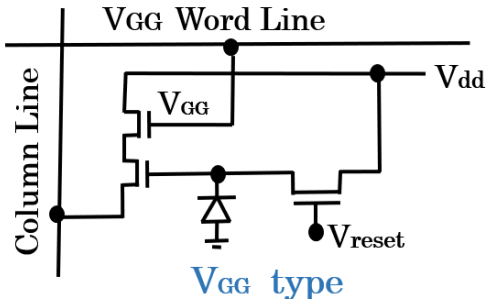
Yoshiaki Hagiwara

(18) NHK developed in 1987 the active in-pixel current amplifier circuit used in MOS image sensor.

Peter Nobel, IEEE Transaction of Electron Devices 15-4 (1968)

Ando et al, "Amplified MOS Intelligent Imager ", TV Society Technical Report, Vol. 11 No. 41 pp. 1075-1082 (1987)

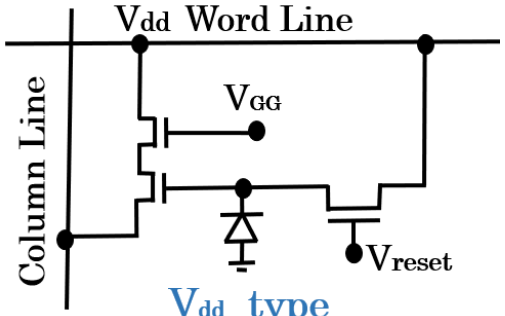
Peter Noble, 1968



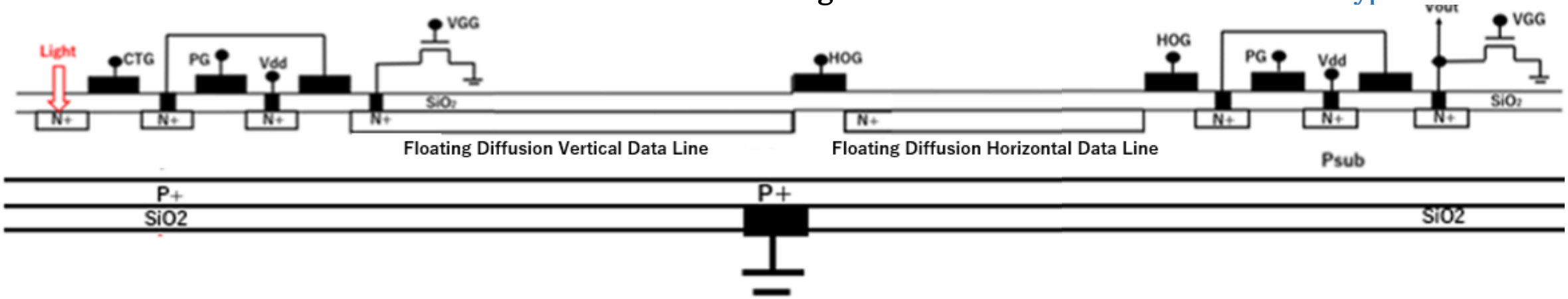
V_{GG} type

The first active pixel 3T1C large scale MOS image sensor of Vdd word line type was developed in 1987 by Ando team at NHK and was called as Amplified MOS Intelligent Imager (AMI) while Peter Noble proposed the V_{GG} word line type Active Pixel MOS image sensor in 1968.

Ando Team at NHK, 1987



V_{dd} type



History_of_Invention_and_Development_of_Pinned_Photodiode

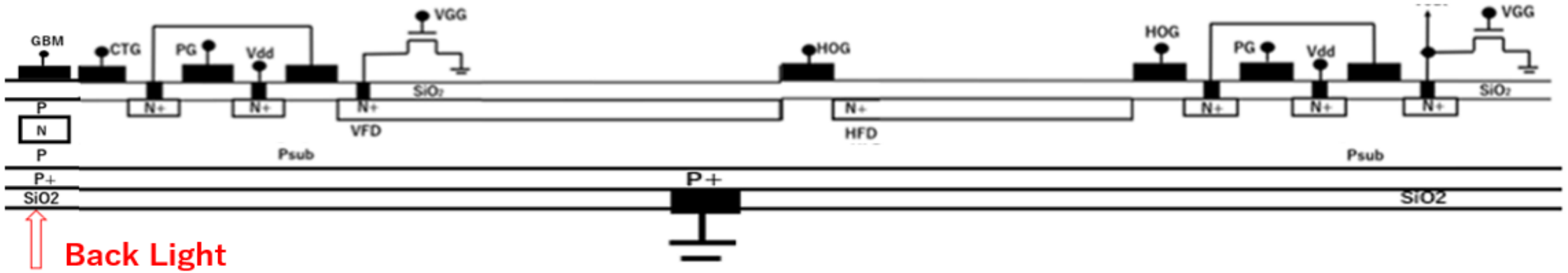
Yoshiaki Hagiwara

(19) Hagiwara proposed Multi-chip 3D CMOS Image Sensor for Flash Image Acquisitions in 2019 using the original P+PNP double junction Pinned Photodiode invented in 1975 by Hagiwara.

Peter Nobel, IEEE Transaction of Electron Devices 15-4 (1968)

Yoshiaki Hagiwara, Japanese Patent Application JPA 1975-127647 , October 23, 1975.

Yoshiaki Hagiwara, "Multichip CMOS Image Sensor Structure for Flash Image Acquisition", IEEE 2019 International 3D Systems Integration Conference (3DIC2019), Sendai, Japan.

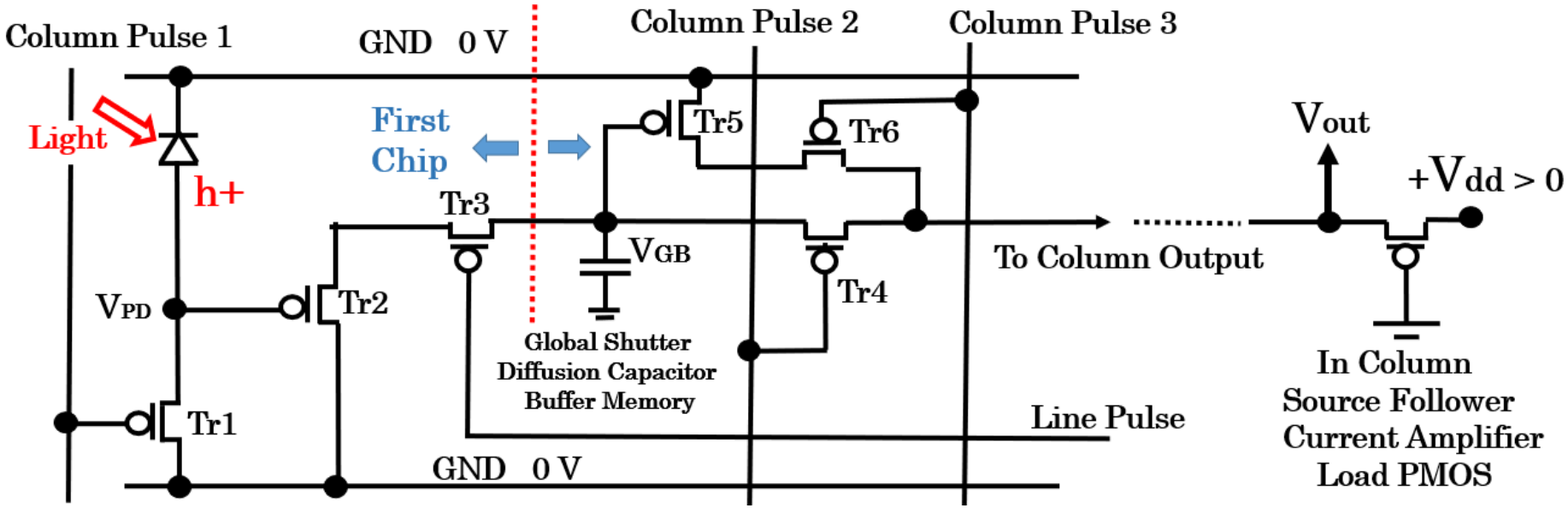


History_of_Invention_and_Development_of_Pinned_Photodiode

Yoshiaki Hagiwara

(20) An example of 1C6T type active pixel with the double source follower current amplifier circuits with Global Shutter function which is suitable to be used for the multi-chip 3D integration.

Yoshiaki Hagiwara, "Multichip CMOS Image Sensor Structure for Flash Image Acquisition", IEEE 2019 International 3D Systems Integration Conference (3DIC2019), Sendai, Japan.

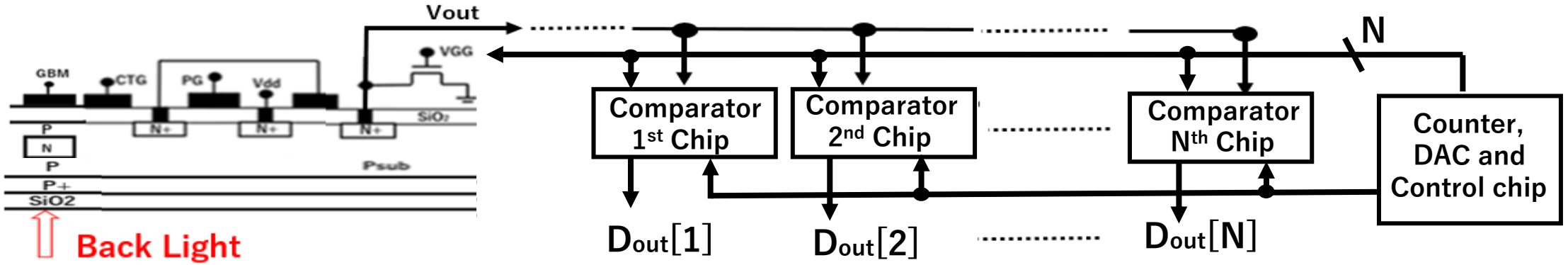


An example of 1C6T active pixel source follower current amplifier circuit proposed by Hagiwara 2021.

History_of_Invention_and_Development_of_Pinned_Photodiode

Yoshiaki Hagiwara

(21) Sony proposed Multi-chip 3D CMOS Image Sensor for Flash Image Acquisitions in 2019.



Peter Nobel, IEEE Transaction of Electron Devices 15-4 (1968)

Yoshiaki Hagiwara, Japanese Patent Application JPA 1975-127647 October 23, 1975.

Yoshiaki Hagiwara, "Multichip CMOS Image Sensor Structure for Flash Image Acquisition", IEEE 2019 International 3D Systems Integration Conference (3DIC2019), Sendai, Japan.

Taku Umebayashi, Hiroshi Takahashi, Japanese Patent Number 5773379 on the invention of the Cu-to-Cu direct contact technique to achieve the 3D stacked multi-chip LSI system.

Ryoji Suzuki, Keiji Mabuchi, Tomonori Mori, Japanese Patent Number 3759435 on the invention of the fabrication method to achieve back illuminated image sensors.

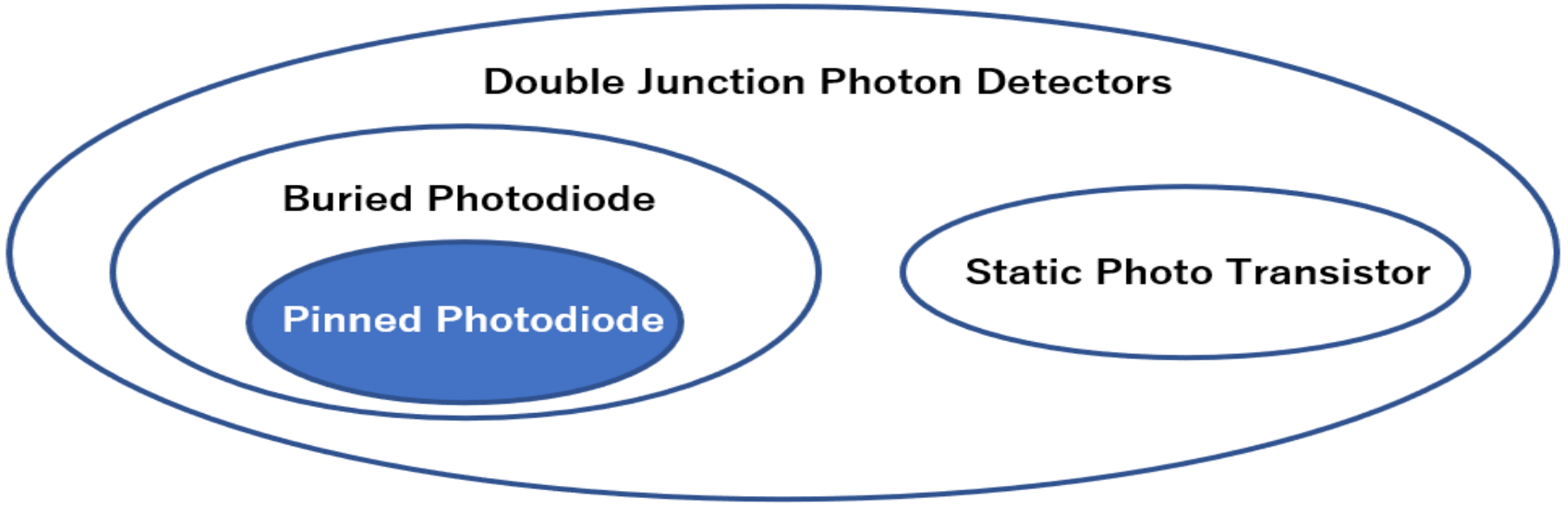
History_of_Invention_and_Development_of_Pinned_Photodiode

Yoshiaki Hagiwara

(22) Difference of Buried Photodiode and Pinned Photodiode.

Buried Photodiode is not always Pinned Photodiode.
But Pinned Photodiode is always Buried Photodiode.
Pinned Photodiode does not have the serioous image lag problem.
But Buried Photodiode may have the seriour image lag problem.

Buried Photodiode and Pinned Photodiode are the double junction dynamic photodiodes.



History_of_Invention_and_Development_of_Pinned_Photodiode

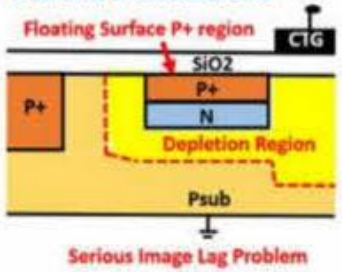
Yoshiaki Hagiwara

(23) Difference of Buried Photodiode and Pinned Photodiode.

Difference of Buried Photodiode and Pinned Photodiode

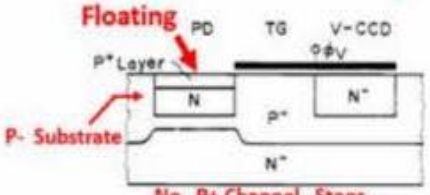
Figure 5 does not have the P+ channel stop nearby.

Buried Photodiode



Serious Image Lag Problem

NEC IEDM1982 Paper



No P+ Channel Stops

Fig.5. P+NP+ structure photodiode
(a) Unit cell cross sectional view

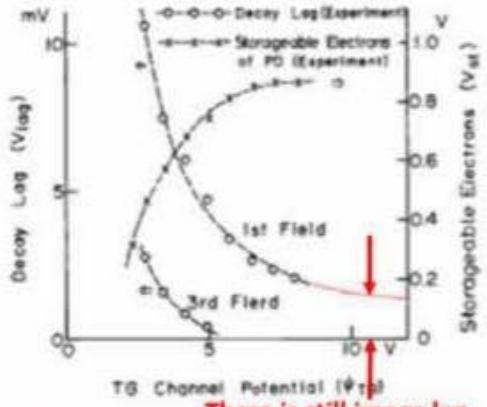


Fig.6. Storageable electrons vs. transfer gate channel potential, and decay lag vs. transfer gate channel potential in the P+NP+ structure photodiode

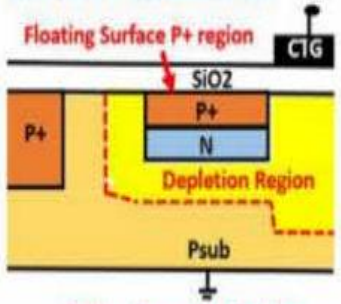
There is still image lag
at the CTD gate voltage more than 10 volt.

NEC IEDM1982 Paper reported Image Lag

Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 volt.

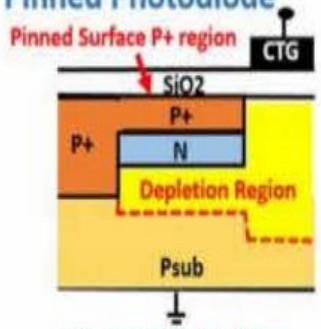
Pinned Photodiode Must Have the Grounded P+ Channel Stops Nearby.

Buried Photodiode



Serious Image Lag Problem

Pinned Photodiode



No Image Lag Problem

The resistivity ρ of the P+ hole accumulation layer is given by

$$\rho = R * W * d / L$$

In the 2/3 inch optical lens system, we have the optical image size of 8.8 mm (H) x 6.6 mm (V) which was a common size in 1980s. Hence, we then have L = 6.6 mm = 6600 μm

The short wave blue light cannot penetrate more than d = 0.2 μm into the silicon crystal in depth. Hagiwara reported in SSDM1978 paper $Qd = 2 \times 10^{13} cm^{-2}$ which gives $Nd = Qd/d = 1 \times 10^{18} cm^{-3}$

For $Nd = 1 \times 10^{18} cm^{-3}$ we have ρ = 0.04 ohm cm = 400 ohm μm

$$RC = \{L\rho / (W*d)\} \{\varepsilon W*L / Xo\} = \varepsilon \rho L^2 / (d\,Xo)$$

We have ε = 216 e/volt μm for silicon oxide and $e = 1.6 \times 10^{-19}$ Coulomb

$$RC = (216)(1.6 \times 10^{-19})(400)(6600)(6600) / (0.2)/(0.1)\ \text{sec}$$

RC = 30.1 μsec while one frame is 1/60 sec = 16.7 msec and the Vertical CCD register clock period is 16.7/500 = 33.4 μsec

Hence RC delay time may not be ignored and surface P+ may be floating ?

History_of_Invention_and_Development_of_Pinned_Photodiode

Yoshiaki Hagiwara

(24) Difference of Buried Photodiode and Pinned Photodiode.

ELECTRICALENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

This is a commonly misunderstood misused set of terminologies.

First off these are not PIN Photodiodes - which stands for P - Intrinsic- N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though.

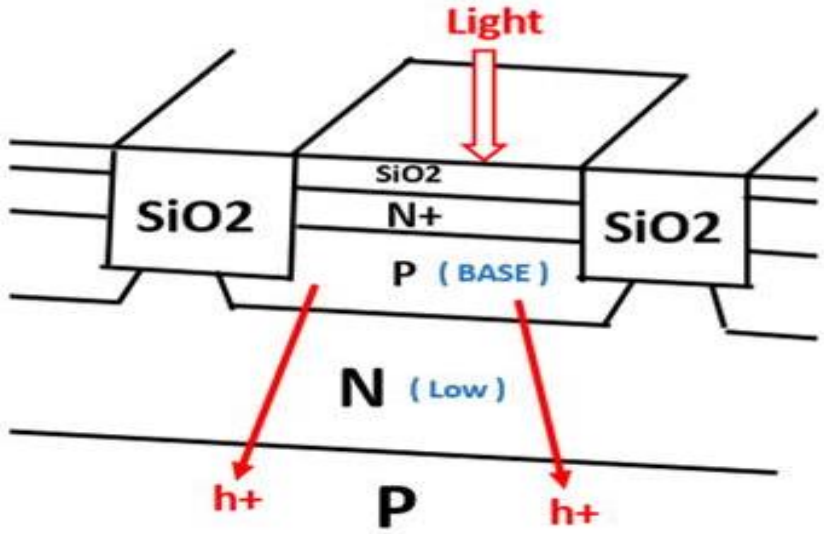
Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space.

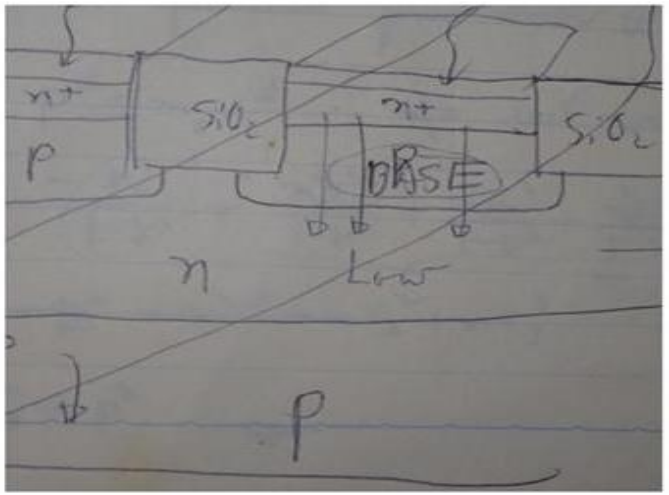
You can get surface state pinning from the dangling Si/SiO2 bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The Si/SiO2 surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface.

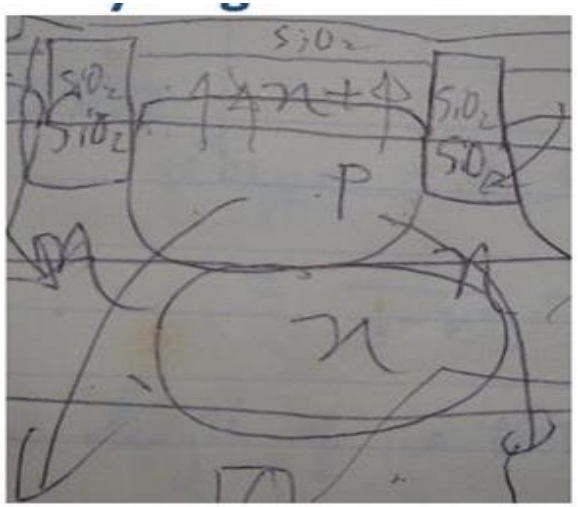
A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)







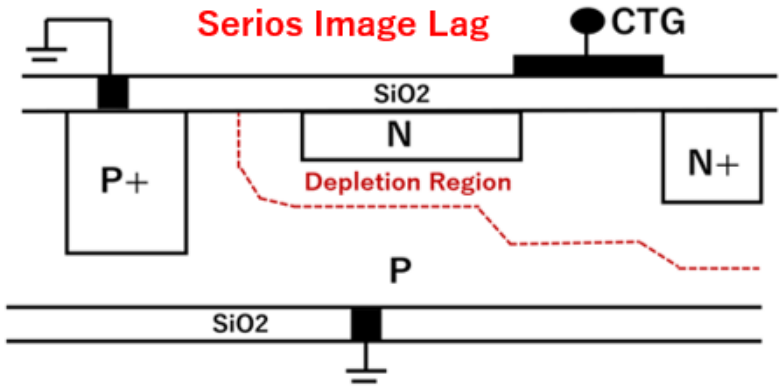
Hagiwara's Lab Note at Sony in February 1975

History_of_Invention_and_Development_of_Pinned_Photodiode

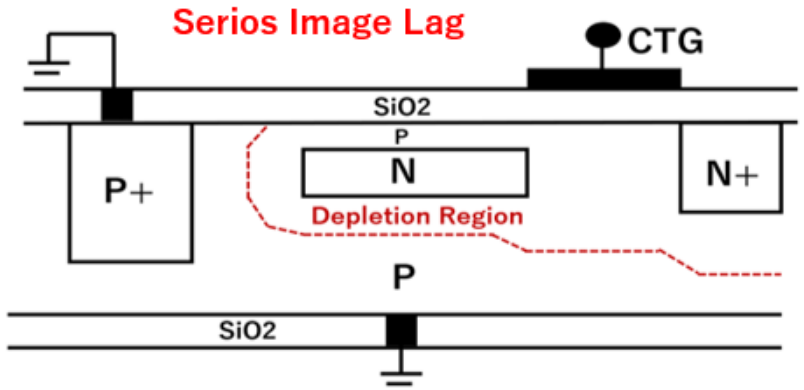
Yoshiaki Hagiwara

(25) Four Types of Basic Photo Sensor Structures

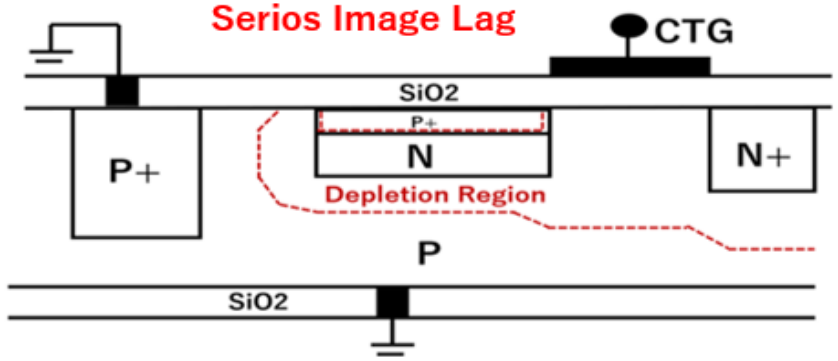
(A) Classical N+P Single Junction type Photodiode with the floating surface N storage region



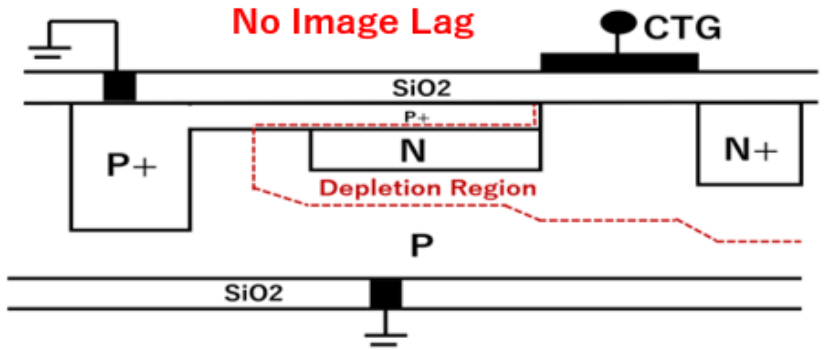
(B) Double Junction PNP type Buried Photodiode with the floating surface P region and the floating buried N storage region

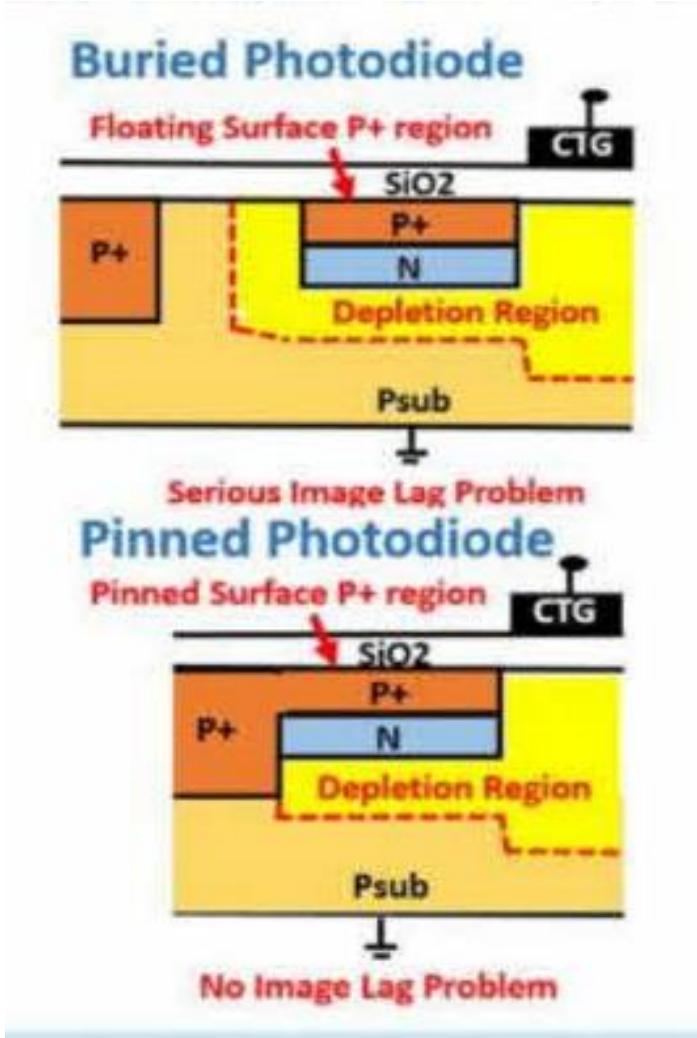


(C) Double Junction P+NP type Buried Photodiode with the floating surface P+ hole accumulation region and the floating N Storage Region.



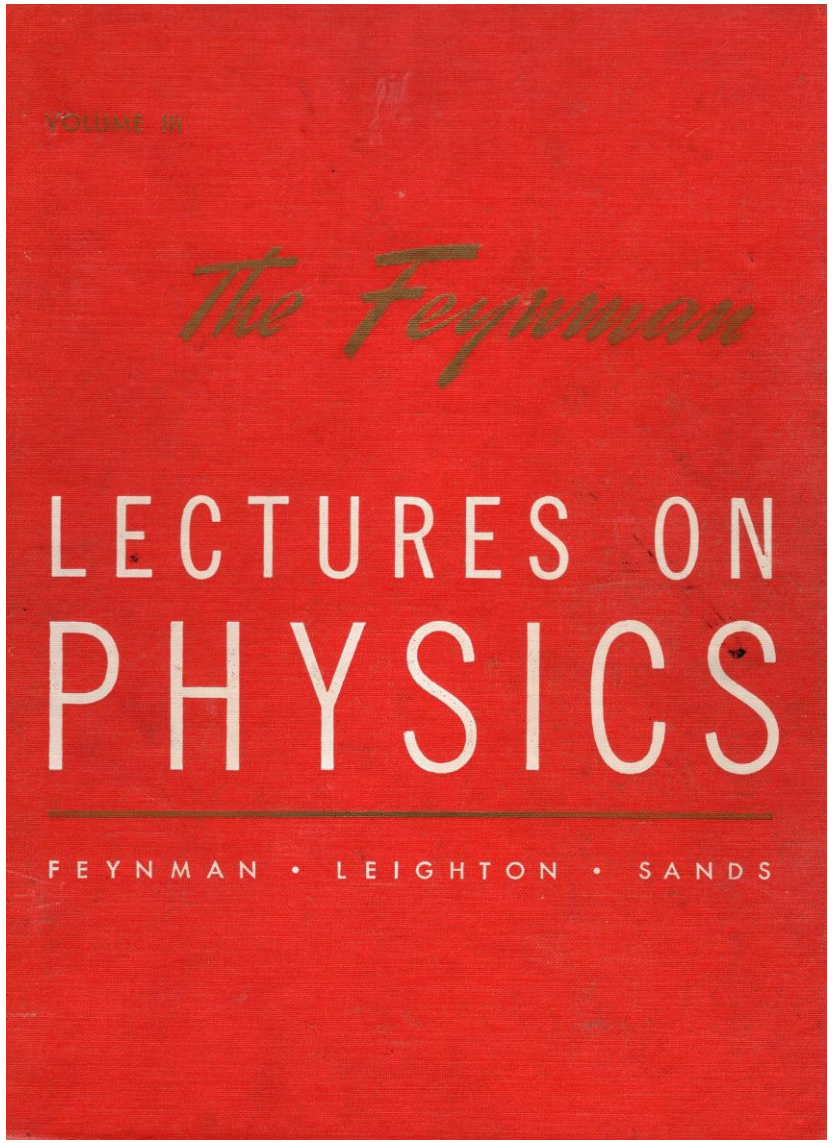
(D) Double Junction P+NP type Pinned Photodiode with the pinned surface P+ hole accumulation region and the pinned N Storage Region





History_of_Invention_and_Development_of_Pinned_Photodiode

Yoshiaki Hagiwara



After studying the quantum theory of hydrogen atom, Hagiwara learned for the first time the physics of semiconductor devices, including the crystal band thery of the single junction type PN diode and the double junction type PNP bipolar transistor at the 2nd year in college.

constant so long as ΔV is not too large. When they approach the barrier, these carriers will still find a downhill potential and will all fall down to the p-side. (If ΔV is larger than the natural potential difference V, the situation would change, but we will not consider what happens at such high voltages.) The net current I of positive carriers which flows across the junction is then the difference between the currents from the two sides:

$$I = I_0(e^{+q\Delta V/kT} - 1). \tag{14.14}$$

The net current I of holes flows into the n-type region. There the holes diffuse into the body of the n-region, where they are eventually annihilated by the majority n-type carriers—the electrons. The electrons which are lost in this annihilation will be made up by a current of electrons from the external terminal of the n-type material.

When ΔV is zero, the net current in Eq. (14.14) is zero. For positive ΔV the current increases rapidly with the applied voltage. For negative ΔV the current reverses in sign, but the exponential term soon becomes negligible and the negative current never exceeds I_0—which under our assumptions is rather small. This back current I_0 is limited by the small density of the minority carriers on the n-side of the junction.

If you go through exactly the same analysis for the current of negative carriers which flows across the junction, first with no potential difference and then with a small externally applied potential difference ΔV, you get again an equation just like (14.14) for the net electron current. Since the total current is the sum of the currents contributed by the two carriers, Eq. (14.14) still applies for the total current provided we identify I_0 as the maximum current which can flow for a reversed voltage.

The voltage-current characteristic of Eq. (14.14) is shown in Fig. 14–10. It shows the typical behavior of solid-state diodes—such as those used in modern computers. We should remark that Eq. (14.14) is true only for small voltages. For voltages comparable to or larger than the natural internal voltage difference V, other effects come into play and the current no longer obeys the simple equation.

You may remember, incidentally, that we got exactly the same equation we have found here in Eq. (14.14) when we discussed the "mechanical rectifier"—the ratchet and pawl—in Chapter 46 of Volume I. We get the same equations in the two situations because the basic physical processes are quite similar.

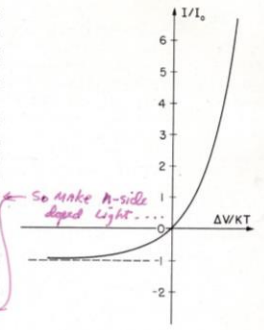


Fig. 14–10. The current through a junction as a function of the voltage across it.

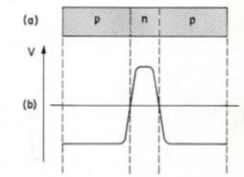


Fig. 14–11. The potential distribution in a transistor with no applied voltages.

14–6 The transistor

Perhaps the most important application of semiconductors is in the transistor. The transistor consists of two semiconductor junctions very close together. Its operation is based in part on the same principles that we just described for the semiconductor diode—the rectifying junction. Suppose we make a little bar of germanium with three distinct regions, a p-type region, an n-type region, and another p-type region, as shown in Fig. 14–11(a). This combination is called a p-n-p transistor. Each of the two junctions in the transistor will behave much in the way we have described in the last section. In particular, there will be a potential gradient at each junction having a certain potential drop from the n-type region to each p-type region. If the two p-type regions have the same internal properties, the variation in potential as we go across the crystal will be as shown in the graph of Fig. 14–11(b).

Now let's imagine that we connect each of the three regions to external voltage sources as shown in part (a) of Fig. 14–12. We will refer all voltages to the terminal connected to the left-hand p-region so it will be, by definition, at zero potential. We will call this terminal the *emitter*. The n-type region is called the *base* and it is connected to a slightly negative potential. The right-hand p-type region is called the *collector*, and is connected to a somewhat larger negative potential. Under these circumstances the variation of potential across the crystal will be as shown in the graph of Fig. 14–12(b).

Let's first see what happens to the positive carriers, since it is primarily their behavior which controls the operation of the p-n-p transistor. Since the emitter is

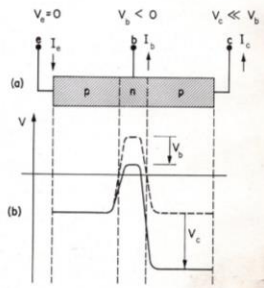


Fig. 14–12. The potential distribution in an operating transistor.

History_of_Invention_and_Development_of_Pinned_Photodiode

Yoshiaki Hagiwara

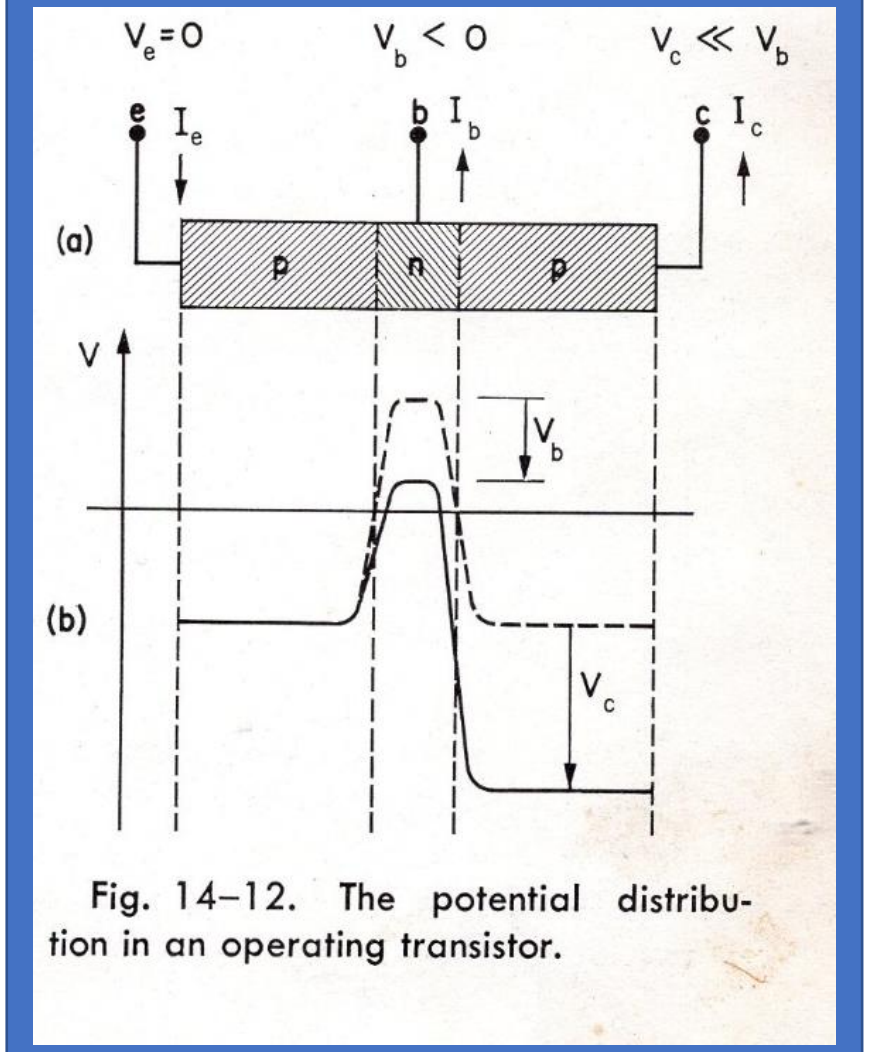
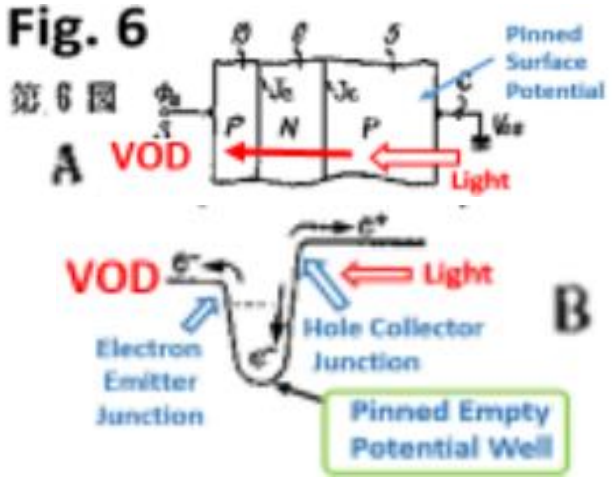
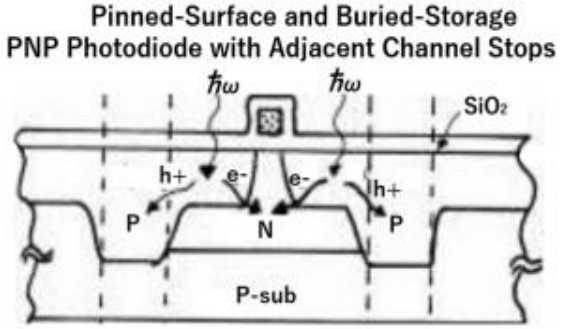


Fig. 14–12. The potential distribution in an operating transistor.

Yoshiaki Hagiwara,
Japanese Patent No. 1215101
(Japanese Patent Application JPA1975-134985)



Yoshiaki Hagiwara, Motoaki Abe and Chikara Okada, “A 380H x 488V CCD Imager with Narrow Channel Transfer Gates”. Proceeding of the 10th Conference on Solid State Devices (SSDM1978), Tokyo 1978;



constant so long as ΔV is not too large. When they approach the barrier, these carriers will still find a downhill potential and will all fall down to the *p*-side. (If ΔV is larger than the natural potential difference V, the situation would change, but we will not consider what happens at such high voltages.) The net current I of positive carriers which flows across the junction is then the difference between the currents from the two sides:

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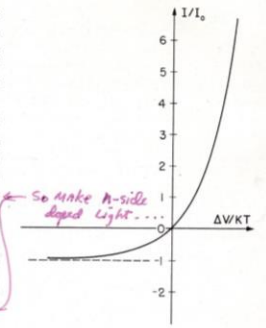

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Perhaps the most important application of semiconductors is in the transistor. The transistor consists of two semiconductor junctions very close together. Its operation is based in part on the same principles that we just described for the semiconductor diode—the rectifying junction. Suppose we make a little bar of germanium with three distinct regions, a *p*-type region, an *n*-type region, and another *p*-type region, as shown in Fig. 14–11(a). This combination is called a *p-n-p* transistor. Each of the two junctions in the transistor will behave much in the way we have described in the last section. In particular, there will be a potential gradient at each junction having a certain potential drop from the *n*-type region to each *p*-type region. If the two *p*-type regions have the same internal properties, the variation in potential as we go across the crystal will be as shown in the graph of Fig. 14–11(b).

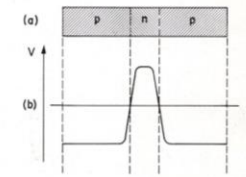


Fig. 14–11. The potential distribution in a transistor with no applied voltages.

Now let’s imagine that we connect each of the three regions to external voltage sources as shown in part (a) of Fig. 14–12. We will refer all voltages to the terminal connected to the left-hand *p*-region so it will be, by definition, at zero potential. We will call this terminal the *emitter*. The *n*-type region is called the *base* and it is connected to a slightly negative potential. The right-hand *p*-type region is called the *collector*, and is connected to a somewhat larger negative potential. Under these circumstances the variation of potential across the crystal will be as shown in the graph of Fig. 14–12(b).

Let’s first see what happens to the positive carriers, since it is primarily their behavior which controls the operation of the *p-n-p* transistor. Since the emitter is

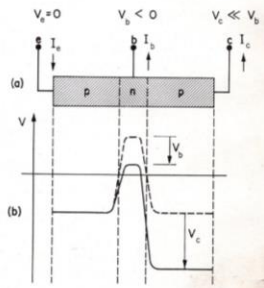


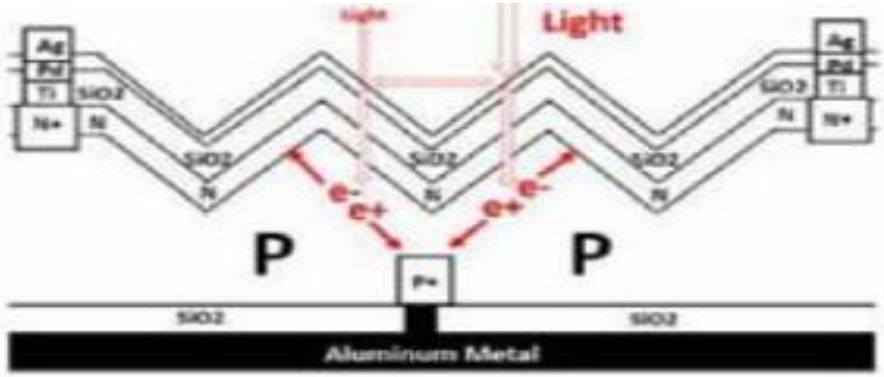
Fig. 14–12. The potential distribution in an operating transistor.

History_of_Invention_and_Development_of_Pinned_Photodiode

Yoshiaki Hagiwara

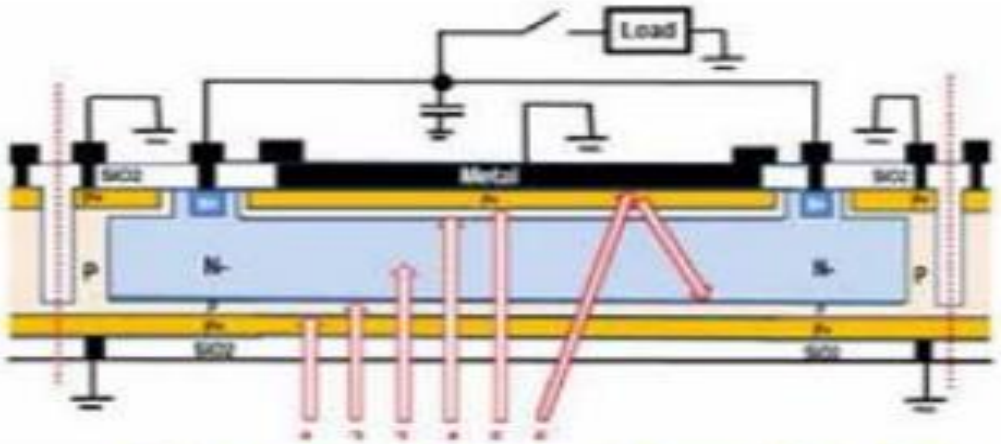
Conventional Single Junction type Solar Cell (A) and (B) Double Junction Type Solar Cell (D) and (D).

(A)



Poor Blue Light Sensitivity Problem

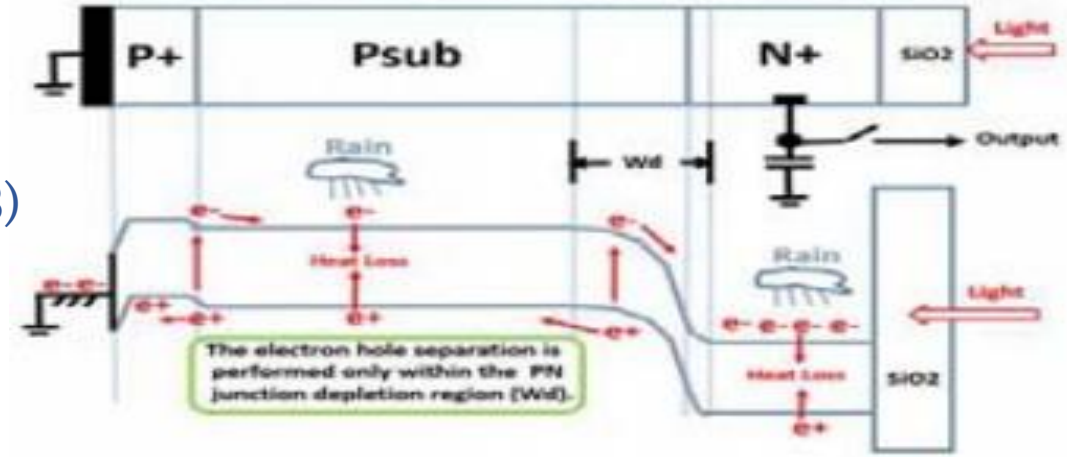
(C)



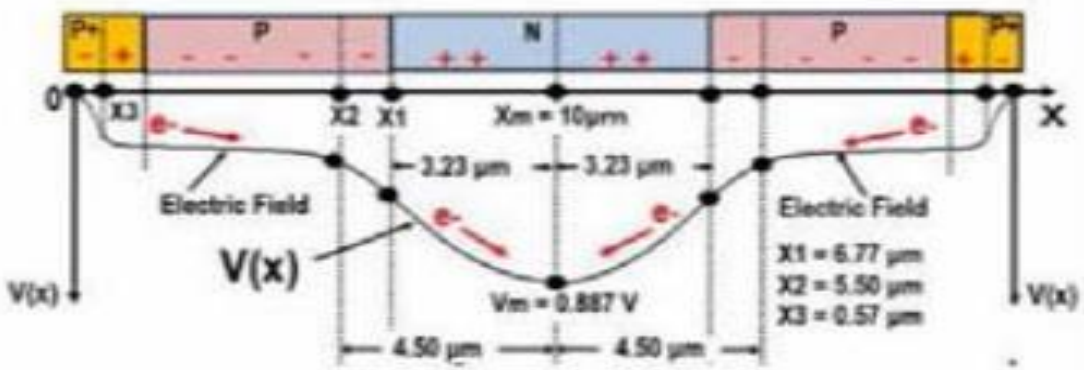
PNP Double Junction Type Solar Cell proposed by Hagiwara in 2020

Classical N+PsubP+ Junction Photodiode

(B)



(D)



Japanese Patent Application JPA2020_131313_on_Doubel_Junction_Pinned_Photodiode_Solar_Cell

History_of_Invention_and_Development_of_Pinned_Photodiode

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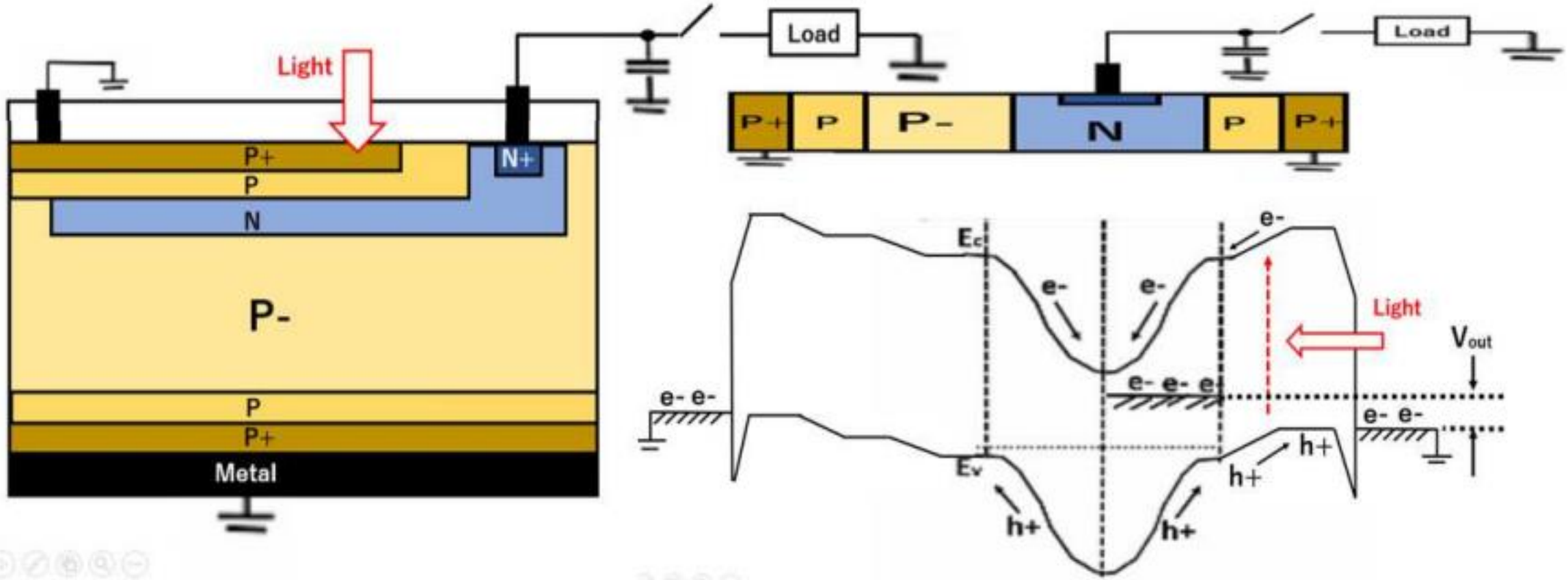
The P+PNP-PP+ Double Junction Type Solar Cell



Japanese Patent Application JPA2020_131313_on_Doubel_Junction_Pinned_Photodiode_Solar_Cell

History_of_Invention_and_Development_of_Pinned_Photodiode

Yoshiaki Hagiwara

Comparison of (1) the P+PNPP+ Double Junction Pinned Photodiode Type Solar Cell proposed by Hagiwara in the Japanese Patent JPA2020-131313 and (2) the conventional floating surface N+P Single Junction Type Solar Cell