Invention and Historical Development Efforts of Pinned Photodiode and Electric Shutter

Hagiwara at Sony Kumamoto Tech Center
in 2017, 2019 and 2022.

2019



2001



1980



1996



Hagiwara also visited Sony Atsugi-Tech Center in July 2020.

Invention and Historical Development Efforts of Pinned Photodiode and Electric Shutter

2019



Hagiwara at Sony Kumamoto Tech Center
in 2017, 2019 and 2022.

2001



1. Introduction
2. Patent Wars on Pinned Photodiode
3. Double Junction type Solar Cell
4. Physics of Image Sensor and Solar Cell
5. Conclusion and Summary

1980



1996



Hagiwara also visited Sony Atsugi-Tech Center in July 2020.

Invention and Historical Development Efforts of Pinned Photodiode and Electric Shutter

2019



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1. Introduction

1980



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1. Introduction



こんにちは、SONYのOBの萩原良昭、旧姓　大門良昭です。
１９７５年２月２０日の途中入社扱いで、２００８年７月に
６０歳定年退職し、その後熊本市池田にある崇城大学の
情報学部の教授として勤務し、今も理事長付き特任教授です。
大学の本館別棟３階に教授室を持ち、毎月１週間ほどいます。

1. Introduction



1. Introduction



1. Introduction

おかげさまで10回目！

Tobioギャラリー写真まつり

2012年にスタートした「地域の魅力」がテーマの写真コンテスト。昨年はコロナで一休みしましたが、おかげさまで今年10回目をむかえます。厚木に限らず、日本各地、世界各国の写真、大歓迎です。受賞作品は、ご来場いただいたみなさまの投票で選出します。会場のTobioギャラリーでお会いしましょう。

締　切　2022年10月14日（金）＊今回からEメールのみの募集となります
展覧会　11月1日（火）～30日（水）10～16時（日・木は休み）
表彰式　12月3日（土）14時～（どなたでもご参加ください）
会　場　Tobioギャラリー（鳶尾団地内、厚木鳶尾郵便局横）

1. Introduction



ソニーのHADセンサー(Pinned Photodiode) という超光感度の受光素子を使う事により、さらなる複雑な駆動制御技術の発明工夫によりアナログＴＶ時代もデジタルＴＶ時代もScan Systemに適した電子シャッターが実現します。

NIKKEI MICRODEVICES 1987年10月号

pp.60～67

ICX022

38万画素に達した固体撮像素子

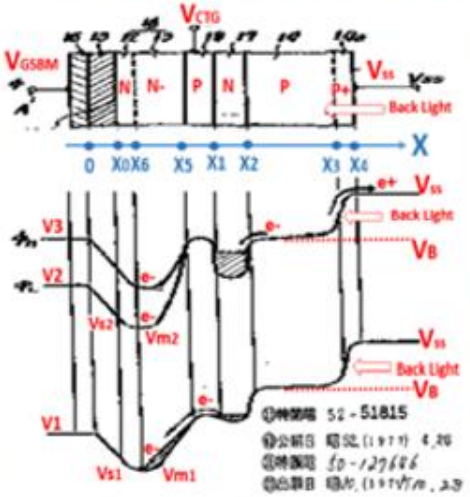
最低照度5 lxの高感度インターライン型CCD

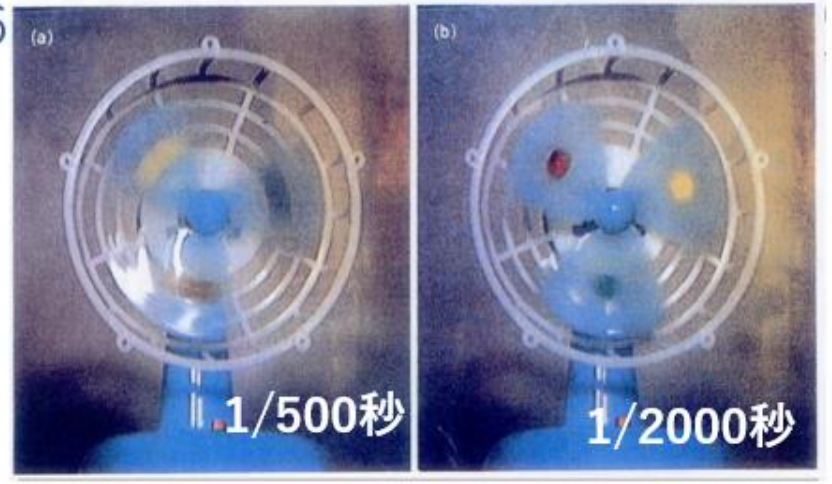
基板に余剰電荷を掃き出し,可変電子シャッタを実現

ソニー 半導体事業本部 CCD 事業部
浜崎 正治
鈴木 智行
賀川 能明
石川 貴久枝
宮田 克郎
ソニー国分セミコンダクタ CCD 製造部
神戸 秀夫

最も一般的な固体撮像素子であるインターライン型 CCD で,
2/3 インチで 38 万と大規模な画素数を持つ素子をソニーが製品化した。
画素面積が小さくなることで減少する信号量を確保するため,
縦型オーバーフロー・ドレインを採用して開口率を上げ,
補色フィルタで光の利用効率を上げた。
さらに界面準位からの暗電流を抑えている。
この結果, 81 dB のダイナミック・レンジが得られた。

JPA1975-127646







JPA1975-127646の図７と同一受光構造である。受光表面はGNDにピン留めされた、P+NPNsub 接合型、 すなわち Triple 接合型の Pinned Photodiode.



ICX022

電子shutterの動作原理の説明図

図 4

SONYの1987年発表の電子シャッター機能付き Hole Accumulation Diode (HAD) 受光素子構造

SonyのCCDの初期の開発チームで中塩みあきさんは活躍されました。

ソニー特許表彰はすばらしい仕事をした証拠です。

pp.166-167

pp. 161~178



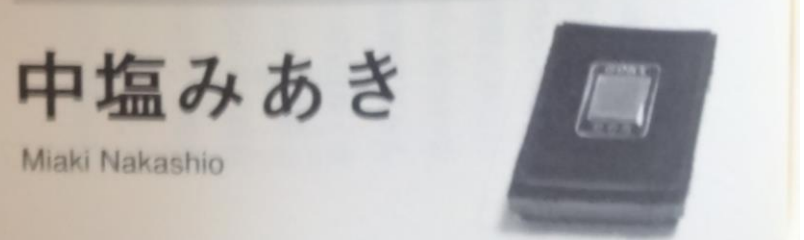
だ。彼は実験に夢中になって、昼食をすっかり忘れていたのである。また、突然、前の席からカップラーメンをすする音がしてきたりする。彼もまた食事時間がわからなくなったクチだろう。かと思うと、急にヘンな音がする。隣の人が仕事に目を置いたまま歯ブラシを握っていた。研究に没頭するあまり時間の感覚を失っていた。しかもそのめちゃくちゃぶりを正そうとはしないで、全員が嬉々として研究に没頭していた。

会議のときも驚いたことがあった。一人の男性が靴をはいたままの足を机の上にドッカとあげている。隣の人と行儀が悪いなあと思っていると、アメリカの有名な大学でドクター（博士）の取った人であった。アメリカ映画などで、大統領が執務室で足を上げているのを見たことがあるから、きっとあちらの国ではいけないこととは思われていないのだろう。「しかしそこの横でアメリカに行っていない上司までも一緒に足を上げているんです（笑）。こっちのほうがラクチンだ。なんて、なんと屈託のない自由な会社かと感心しました」

大学ではかなり進んだ内容まで習ったと思うが



ソニー特許表彰はすばらしい仕事をした証拠です。



SonyのCCDの初期の開発チームで中島みあきさんは活躍されました。

ソニー特許表彰は中島みあきさんがすばらしい仕事をしされた証しです。

p.178

pp. 161~178



ソニーに勤務していたときは、ただただ忙しかった。「ソニーは、大学出たての小娘に、予算をつけて自由にチャレンジさせてくれた。やはりすごい会社だったと思います」。当時の金額で一気に7千万円くらいの投資をしてもらったこともあった。きっとこれは「しっかりやれよ」というメッセージだったのだろう。「感謝していますか」と聞くと、「実際、成功して、それだけ稼いでお返ししていますからね（笑）」と言いきる。「ソニーでは頑張ったけれど、私の名前はどこにも出てこないし残らない。むろん優れた製品という〝モノ〟としては残るのですが、しかし、そのモノといっても、次々に新しい製品が出るので、私の作ったモノはすぐに忘れられるでしょう。でも、だからといってむなしさなどはありません。やりがいのある質の高い仕事に関われ、すばらしい経験をしたことは間違いないのです」。

ソニーではやるべきことをやりとげ、なんの悔いもない。しかしネパールの子どもの輝くひとみと無心な笑顔に出会うと、なぜか涙が止まらない。自分はどうしてこんなに彼らに癒されるのだろうか。彼らのためなら、なんでもやってやりたい。それはむろん彼らのためであるが、同時に自分のためでもあると、感じている。



ソニー特許表彰はすばらしい仕事をした証拠です。

中塩みあき

Miaki Nakashio



SonyのCCDの初期の開発チームで電子シャッターの発明とその実用化開発で活躍されました。

電子シャッターに関するソニー社内特許表彰および発明協会からの発明賞の受賞はすばらしい仕事をした証拠です。

実務経験等を記載した研究業績書

学会及び社会における活動状況（学術論文、研究報告、口頭発表、特許など）

https://humanstory.jp/ishikawa_kikuyo/

［たった一人の本氣が世界を変える！］



株式会社ダヴィンチ・ブレインズ 代表取締役社長　石川耀弓

1987 年 10 月　「38 万画素に達した固体撮像素子ー最低照度５１ｘの高感度インターライン型 CCDー」日経マイクロデバイス 87 年 10 月号、pp60－67

1988 年 2 月　「可変速電子シャッター付 IT-CCD 撮像素子」テレビジョン学会技術報告　ITEJ Technical Report Vol.12,pp31-36

1989 年 3 月　「IT CCD Imaging Sensor with Variable Speed Electronic Shutter」 Kikue Ishikawa et al, Proceeding of SPIE Vol.1107,　pp66－76

’89.3.30 に Orland の技術発表会にて口頭発表。

1992 年 2 月　「2M pixels FIT-CCD with Hyper HAD Sensor and Camera for HDTV」 Kikue Ishikawa et al, Proceeding of SPIE Vol.1656,　pp30－40

’92.2.10 に SanJose の技術発表会にて口頭発表。

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1992 年 10 月	「1 インチ 200 万画素 CCD カラーカメラシステム」石川貴久枝　他　テレビジョン学会技術報告　ITEJ Technical Report Vol.16,No69,pp25-30 '92.10.22.に東京の技術報告会にて口頭発表。
1992 年 11 月	「1 inch 2M pixels CCD with Hyper HAD Sensor and Camera system for HDTV」 Kikue Ishikawa et al, Proceeding of the International Workshop on HDTV'92 pp437－444 '92.11.18 に川崎の技術発表会にて口頭発表。
1993 年 10 月	「HDTV-CCD カメラの現状と今後の課題」テレビジョン学会関西支部　専門講習会講演論文集　カメラとディスプレイの最新技術　pp29-35 '93.10.28.に大阪の専門講習会にて口頭発表。
1999 年 7 月	「産業用カメラに望まれる固体撮像素子の特性」石川貴久枝他　映像情報メディア学会技術報告　ITE Technical Report Vol.1.23,No49,pp37-41 '99.7.30.に東京の技術報告会にて口頭発表。
2002 年 7 月	「PTZ（パン・ティルト・ズーム）機能付きネットワークカメラ」　石川貴久枝　他　映像情報メディア学会技術報告　ITE Technical Report Vol.26,No50,pp1-4

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No	公開・公表・再公表No	公告・登録No	発明の名称
1	特再WO97/048226		撮像装置及びその制御装置
2	特開平10-191179		撮像制御方法、撮像制御装置、撮像システム及び撮像装
3	特開平10-145683		撮像装置
4	特開平08-241978	登録595924	固体撮像装置
5	特開平08- 46875	登録565247	固体撮像装置及びビデオカメラの露光時間制御方法
6	特開平05-308579	登録223570	固体撮像装置
7	特開平05-153502	登録033299	固体撮像装置の駆動回路
8	特開平04- 34977	登録010161	固体撮像素子
9	特開平01- 29067	登録668883	固体撮像装置

No	公開・公表・再公表No	公告・登録No	発明の名称
10	特開昭63-158981	登録517882	固体撮像装置
11	特開昭63-105579	特公平07- 59055	固体撮像装置
12	特開昭63- 36562	登録508507	固体撮像装置
13	特開昭63- 15459	登録586455	固体撮像装置
14	特開昭63- 14467	登録545801	固体撮像素子
15	特開昭62-291967	登録542927	電荷転送装置
16	特開昭62-277863	登録508638	固体撮像装置
17	特開昭62-221147		固体撮像装置
18	特開昭62-219565	特公平07- 63090	固体撮像装置

NIKKEI MICRODEVICES 1987年10月号

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ICX022

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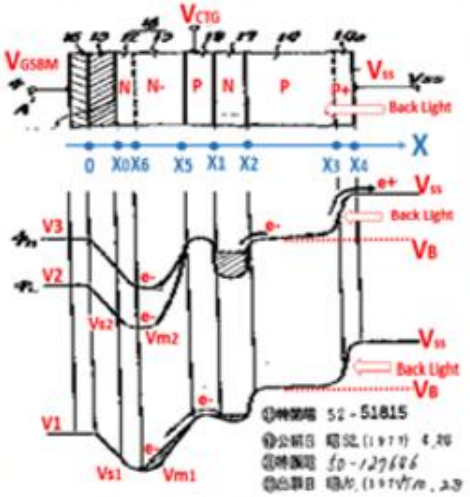
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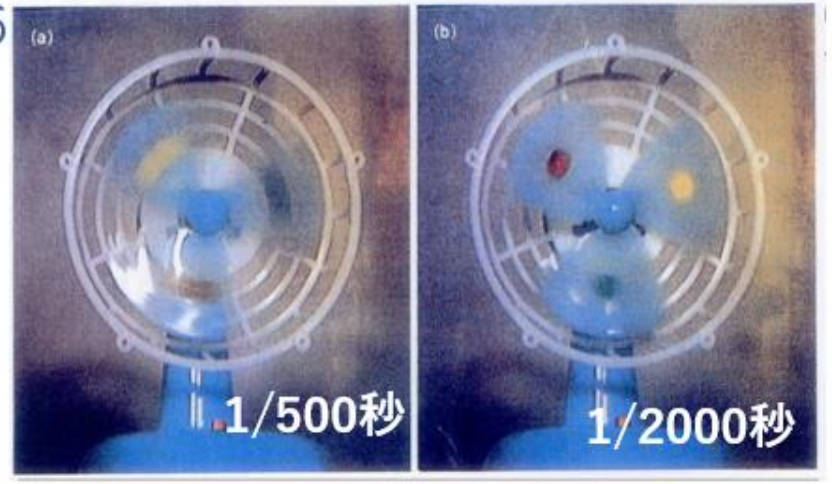
基板に余剰電荷を掃き出し,可変電子シャッタを実現

ソニー 半導体事業本部 CCD 事業部
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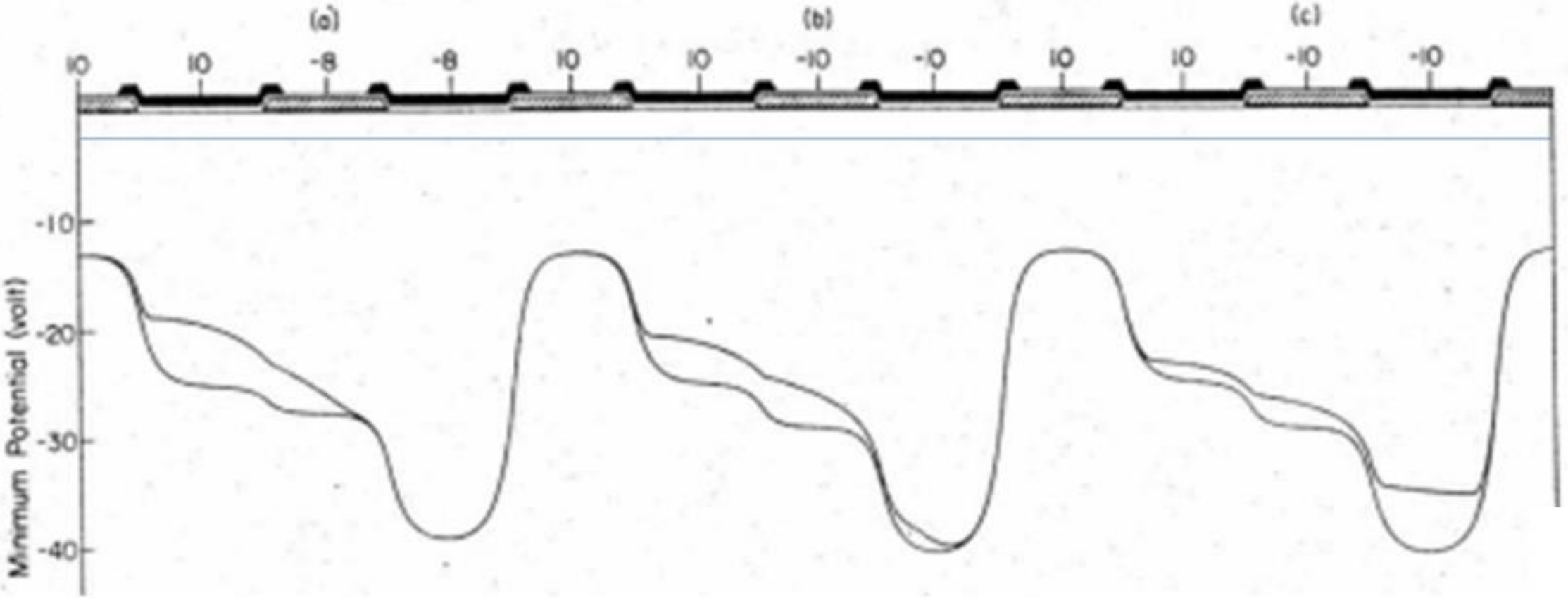
ICX022

電子shutterの動作原理の説明図

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SONYの1987年発表の電子シャッター機能付き Hole Accumulation Diode (HAD) 受光素子構造

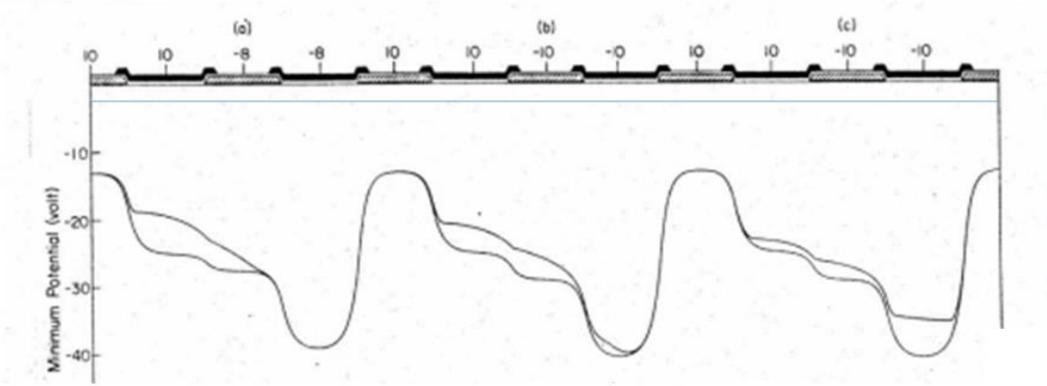
Exact Numerical Computer Simulation of Charge Transfer Action in Buried Channel CCD presented in ISSCC1974 by Yoshiaki Daimon-Hagiwara



for details see the PhD Thesis by Yoshiaki Daimon-Hagiwara on June 1975 from Caltech.

Caltech_1975_PhD_Thesis_Yoshiaki_Daimon_Hagihara.pdf

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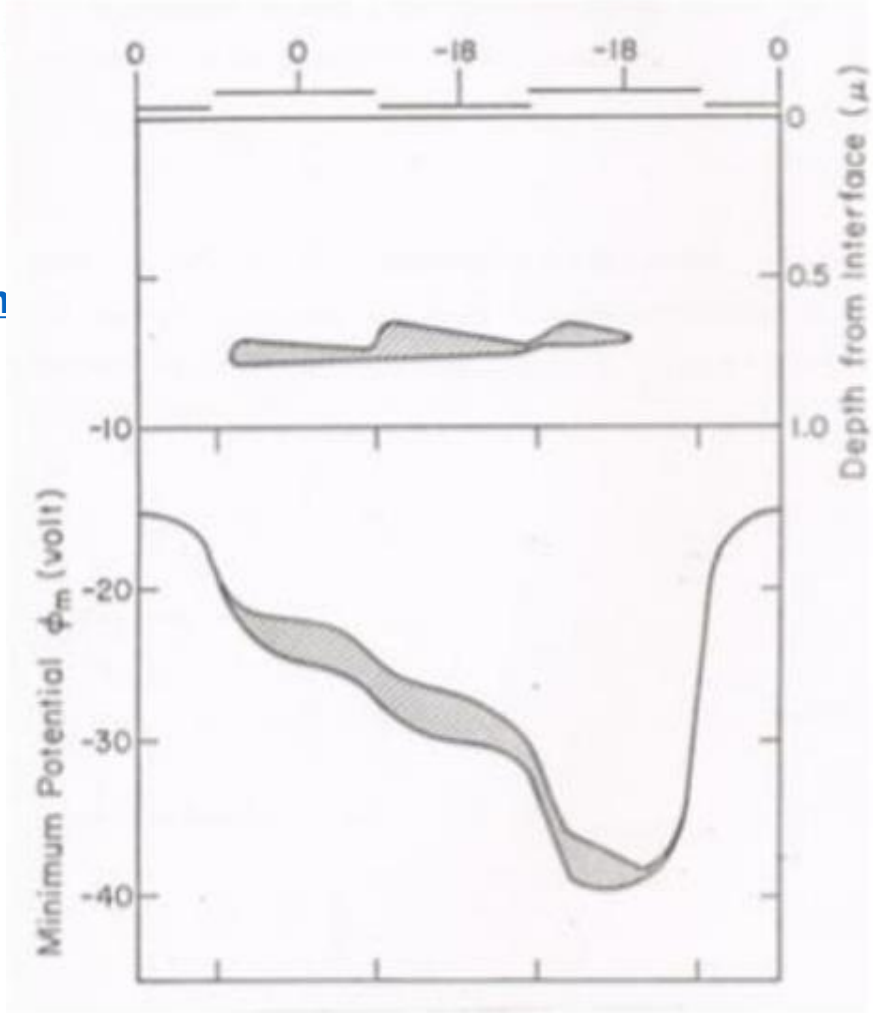
for details see the PhD Thesis by Yoshiaki Daimon-Hagiwara on June 1975 from Caltech.

[Caltech_1975_PhD_Thesis_Yoshiaki_Daimon_Hagih]



Prof. James McCaldin and Hagiwara

My PhD thesis paper
on buried channel CCD
at ISSCC1974, in Philadelphia, USA





Prof. T. C. McGill



Prof. C. A. Mead

True History of Photodiode

(1) Single Junction Type Dynamic Photodiode was used in image sensors before 1970

(2) CCD/MOS type dynamic Photodiode was invented in 1970 with no image lag with the Pinned Gate.

(3) Double Junction type Dynamic Photodiode invented by Philips in June 9, 1975 with RC delay time.

(4) Triple Junction type Dynamic Photodiode with the pinned surface invented by Sony in Oct 23, 1975.



⑪特開昭 51－150288

⑬公開日 昭51.(1976) 12 23

㉑特願昭 51－65705

㉒出願日 昭51.(1976) 6.7

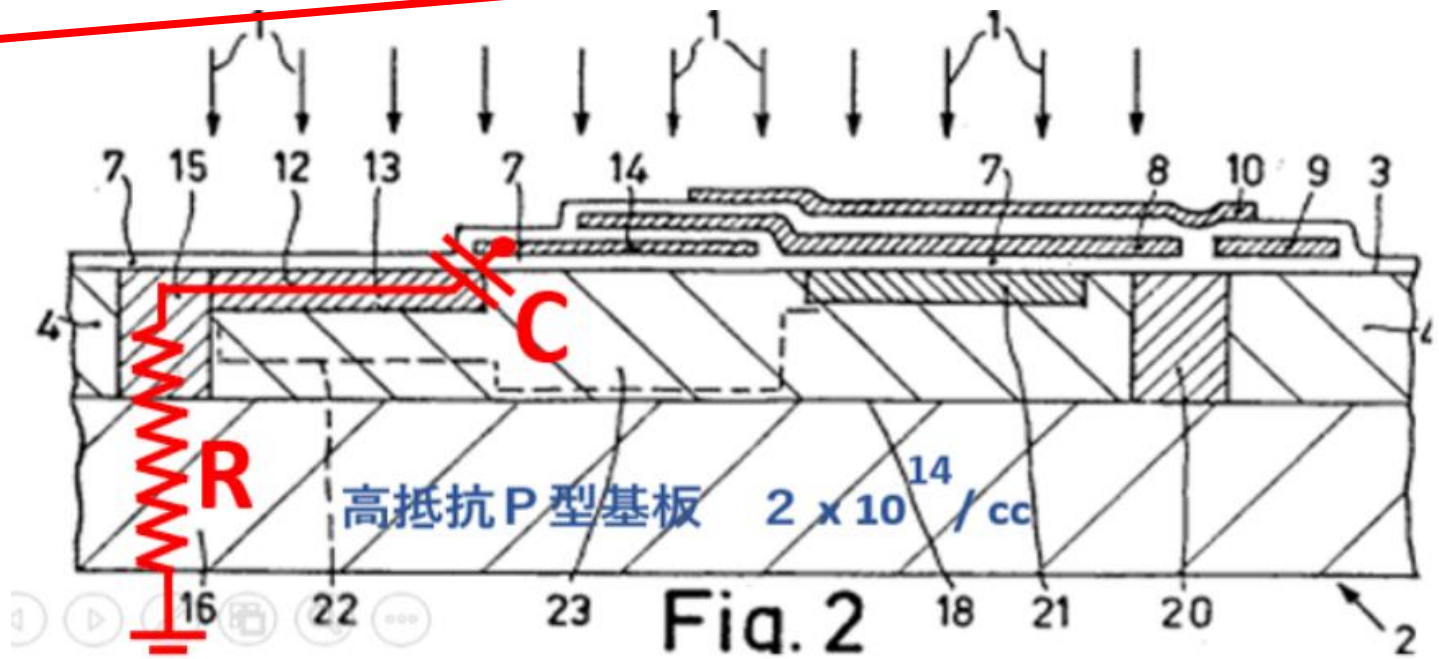


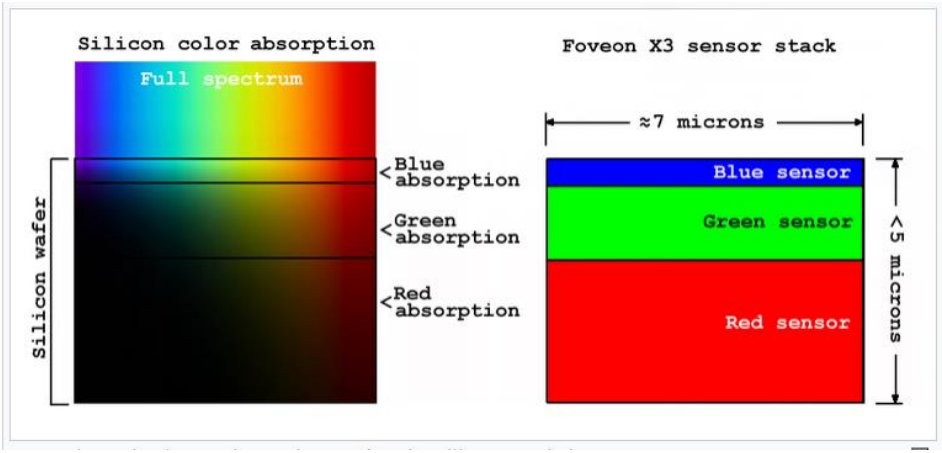
Fig. 2

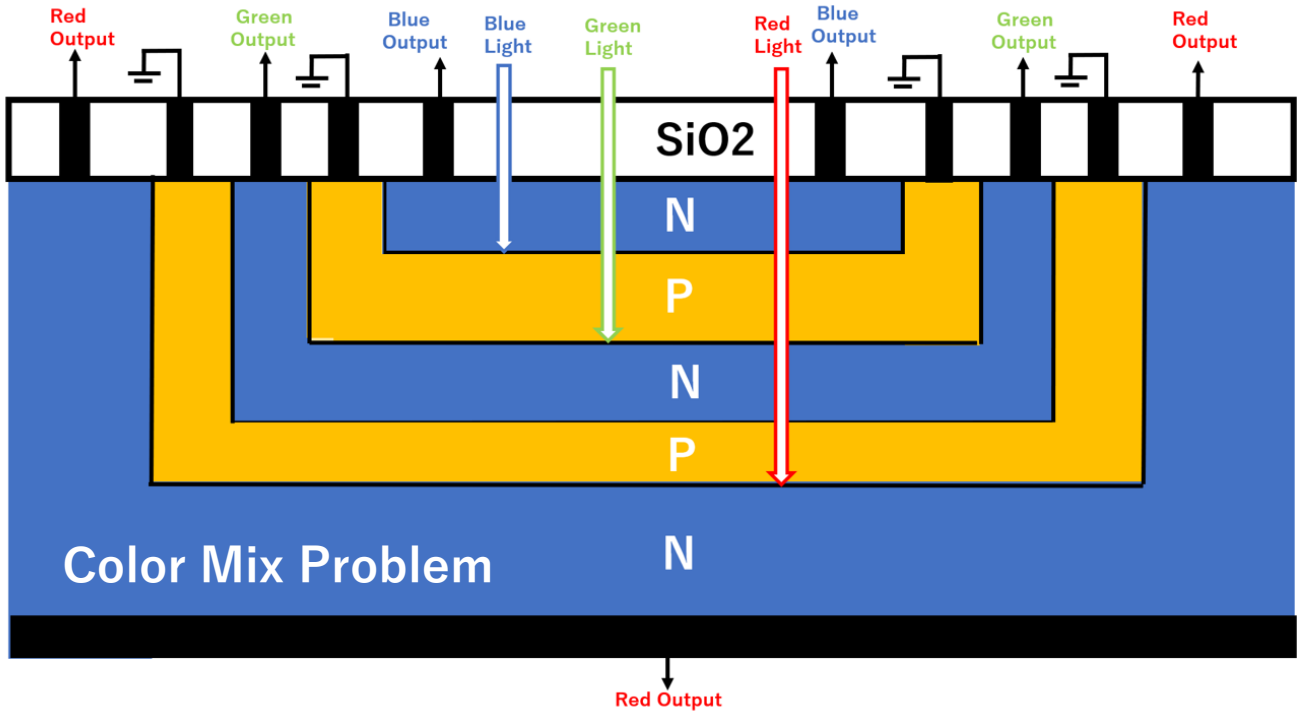
JPA1976-150288(Netherland Patent 7506795, priority June 7, 1975)

https://en.wikipedia.org/wiki/Foveon_X3_sensor

Foveon X3 sensor

From Wikipedia, the free encyclopedia





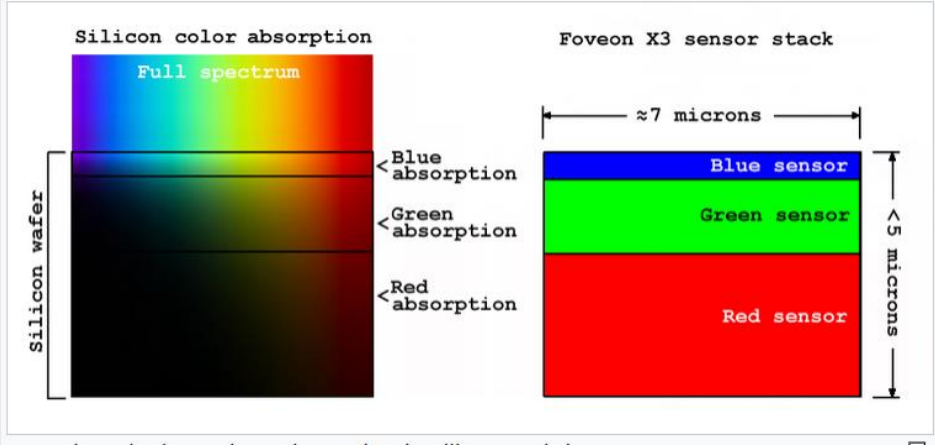
Light gathering and low-light performance

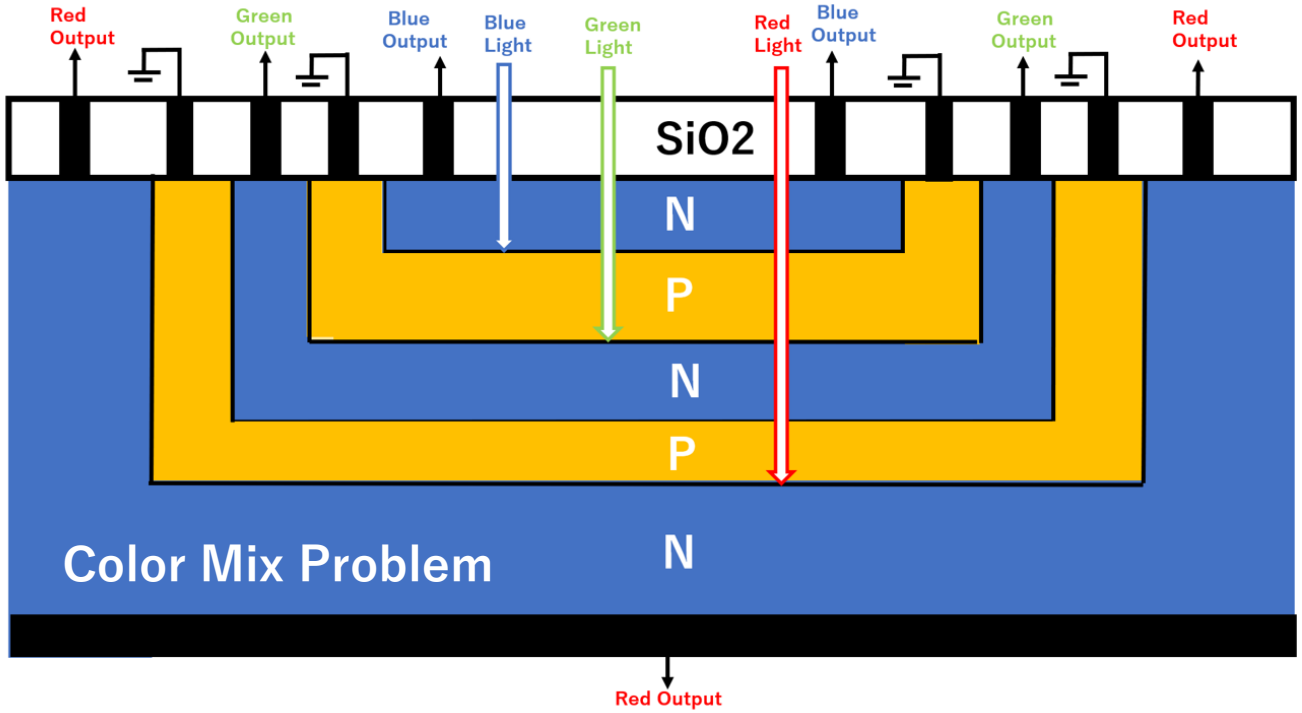
The Foveon X3 photosensor can detect more photons entering the camera than a mosaic sensor, because each of the color filters overlaying each photosite of a mosaic sensor passes only one of the primary colors and absorbs the other two. The absorption of these colors reduces the total amount of light gathered by the sensor and destroys much of the information about the color of the light impinging on each sensor element. Although the Foveon X3 has a greater light-gathering ability, the individual layers do not respond as sharply to the respective colors; thus color-indicating information in the sensor's raw data requires an "aggressive" matrix (i.e., the removal of common-mode signals) to produce color data in a standard color space, which can increase color noise in low-light situations.[15]

https://en.wikipedia.org/wiki/Foveon_X3_sensor

Foveon X3 sensor

From Wikipedia, the free encyclopedia





The **Foveon X3 sensor** is a digital camera image sensor designed by Foveon, Inc., (now part of Sigma Corporation) and manufactured by Dongbu Electronics.[1] It uses an array of photosites that consist of three vertically stacked photodiodes. Each of the three stacked photodiodes has a different spectral sensitivity, allowing it to respond differently to different wavelengths.[2] The signals from the three photodiodes are then processed as additive color data that are transformed to a standard RGB color space.

The X3 sensor technology was first deployed in 2002 in the Sigma SD9 DSLR camera, and subsequently in the SD10, SD14, SD15, SD1 (including SD1 Merrill), the original mirrorless compact Sigma DP1 and Sigma DP2 in 2008 and 2009 respectively, the Sigma dp2 Quattro series from 2014, and the Sigma SD Quattro series from 2016. The development of the Foveon X3 technology is the subject of the 2005 book *The Silicon Eye* by George Gilder.

Japanese Patent JPA 1977-837

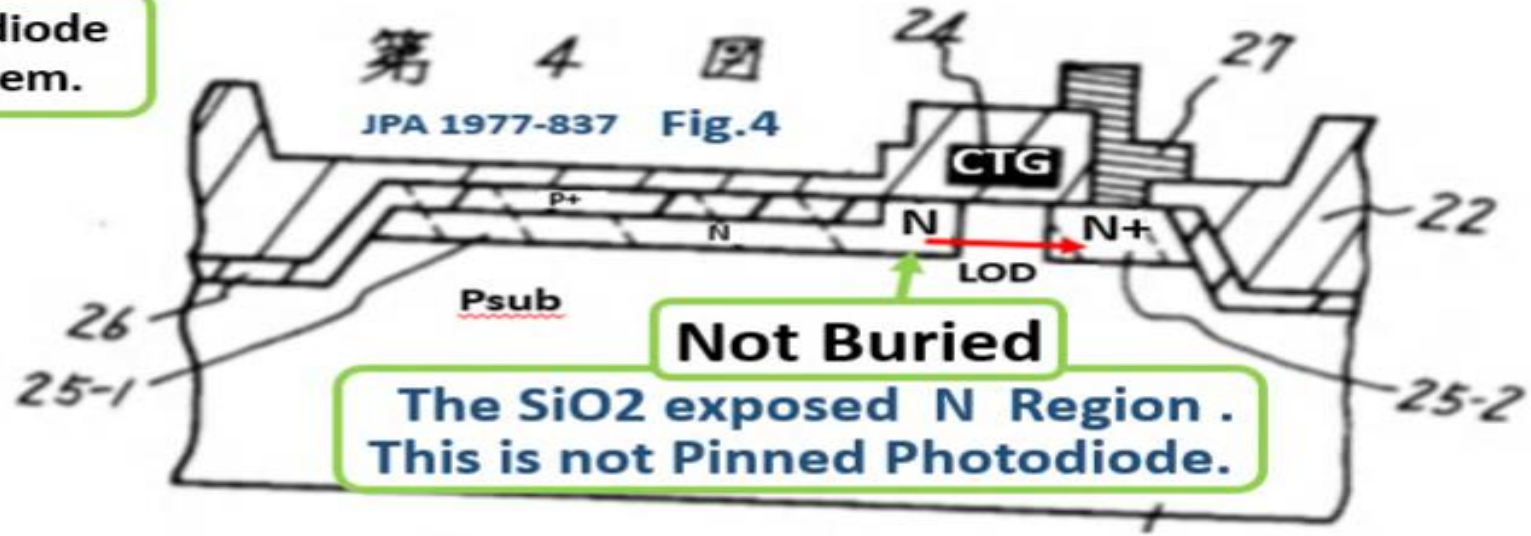
This patent is applied for the lateral overflow drain (LOD) function.
The excess charge is drained to the N+ lateral output drain (LOD).

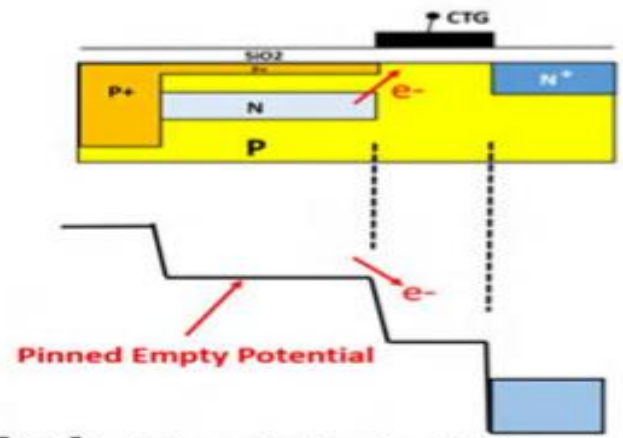
This SiO2 surface exposed photodiode has the serious Image lag problem.

㊵固体撮像装置

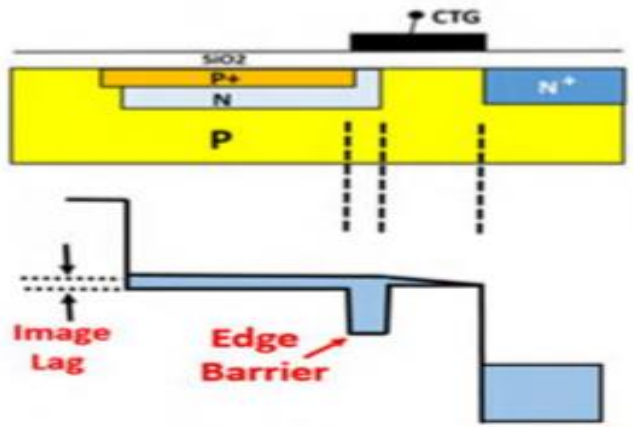
㉑特　　願　昭52—837
㉒出　　願　昭52(1977) 1 月10日
㉗発 明 者　小池紀雄
㊶特許出願公開　昭53—86516

第 4 図
JPA 1977-837 Fig.4

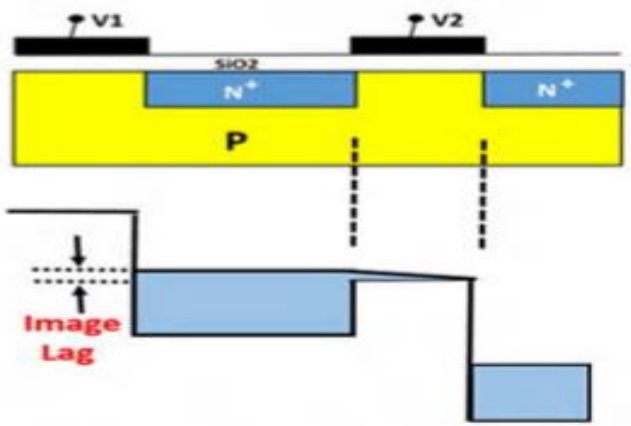




(1) Pinned Photodiode with No Image Lag



(2) Buried Photodiode with BBD Barrier



(3) Bucket Brigade Device (BBD)

JPA1978-1971 by T. Yamada at Toshiba, an invention of the in-pixel anti-blooming using the NPN junction photodiode with the floating N photo charge storage

⑲日本国特許庁(JP)

⑪特許出願公開

⑫公開特許公報(A)

昭54—95116

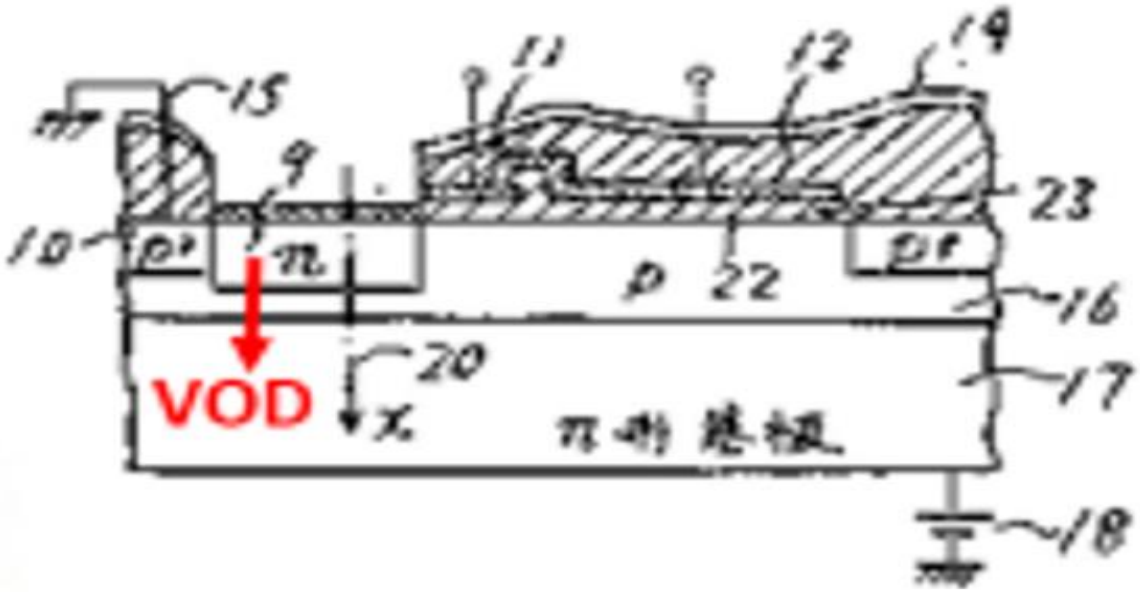
⑤固体撮像装置

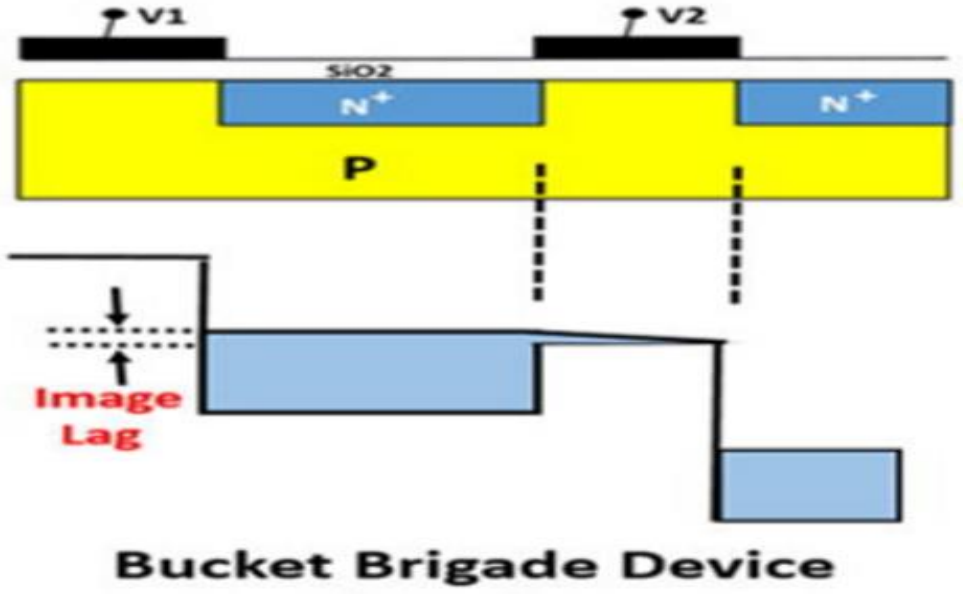
⑳特　　願　昭53—1971

㉒出　　願　昭53(1978)1月13日

㉓発　明　者　山田哲生

⑬公開　昭和54年(1979)7月27日



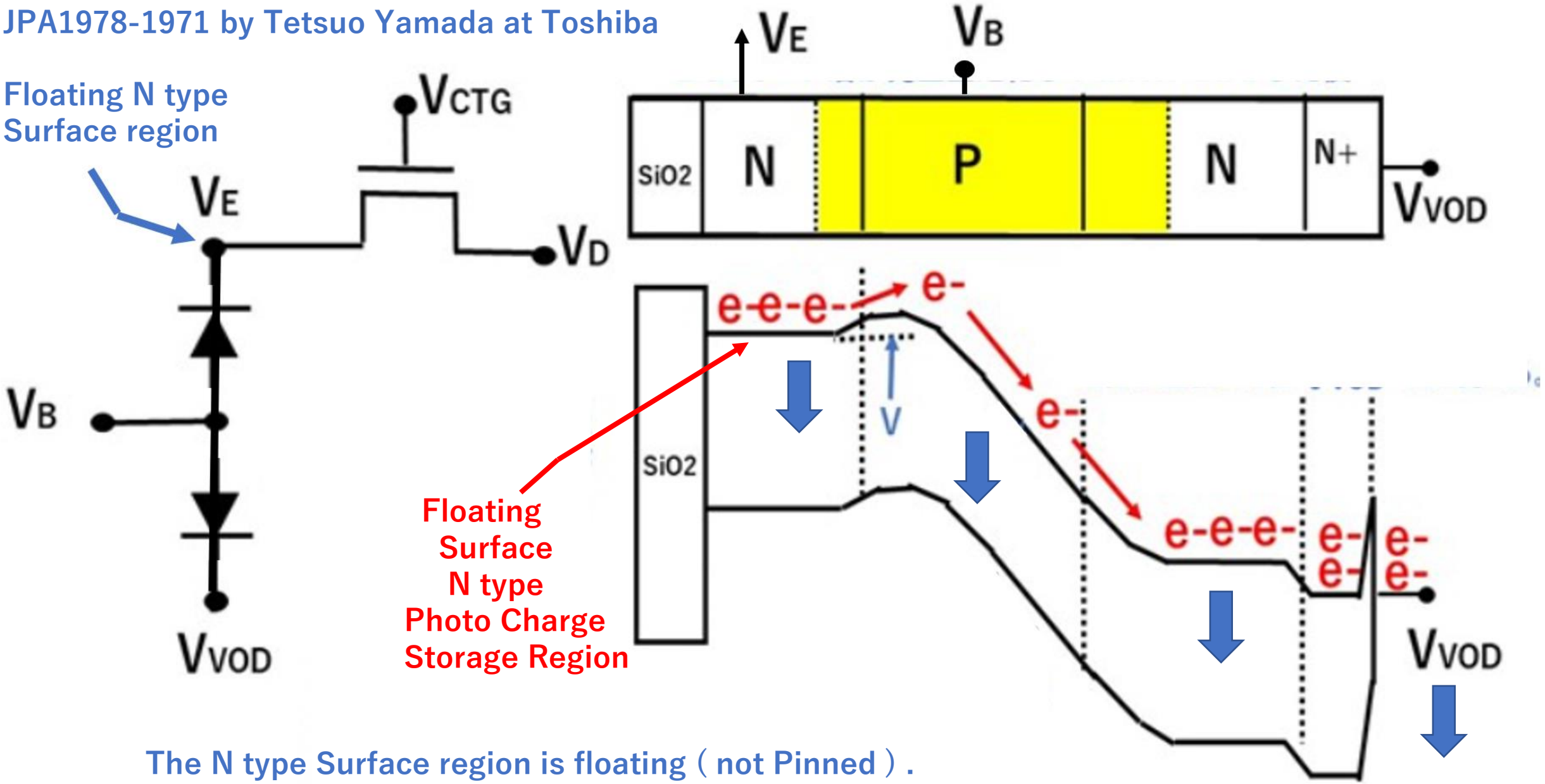


Bucket Brigade Device

This floating surface photodiode operates in the BBD type charge transfer mode with the serious image lag and the truth is that the in-pixel anti-blooming function does not function properly at high frequency.

JPA1978-1971 by Tetsuo Yamada at Toshiba

Floating N type
Surface region



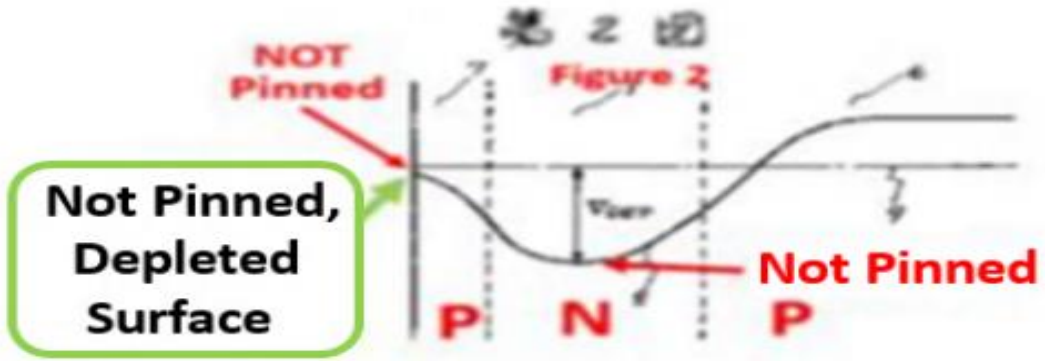
The N type Surface region is floating (not Pinned) .
The anti-blooming VOD does not function well because the N-type surface will also be pulled down as the VOD voltage is pulled down deeper.

JPA1980-138026 by N. Teranishi et al at NEC

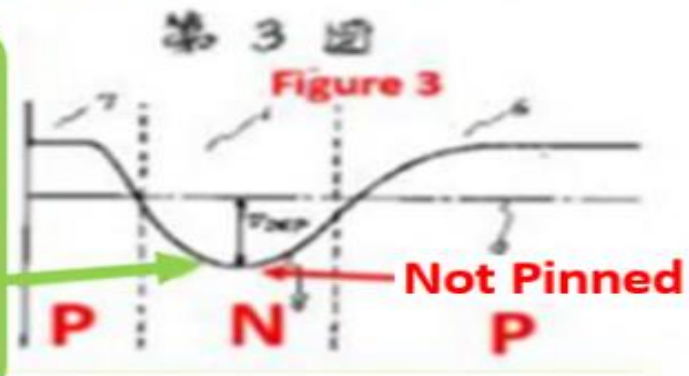
JPA 1980-138026

1980年10月2日出願

⑫特　　願　昭55—138026
⑫出　　願　昭55(1980)10月2日
⑫発　明　者　寺西信一
⑫発　明　者　石原保雄
⑫発　明　者　白木廣光



Not Pinned, Depleted Surface

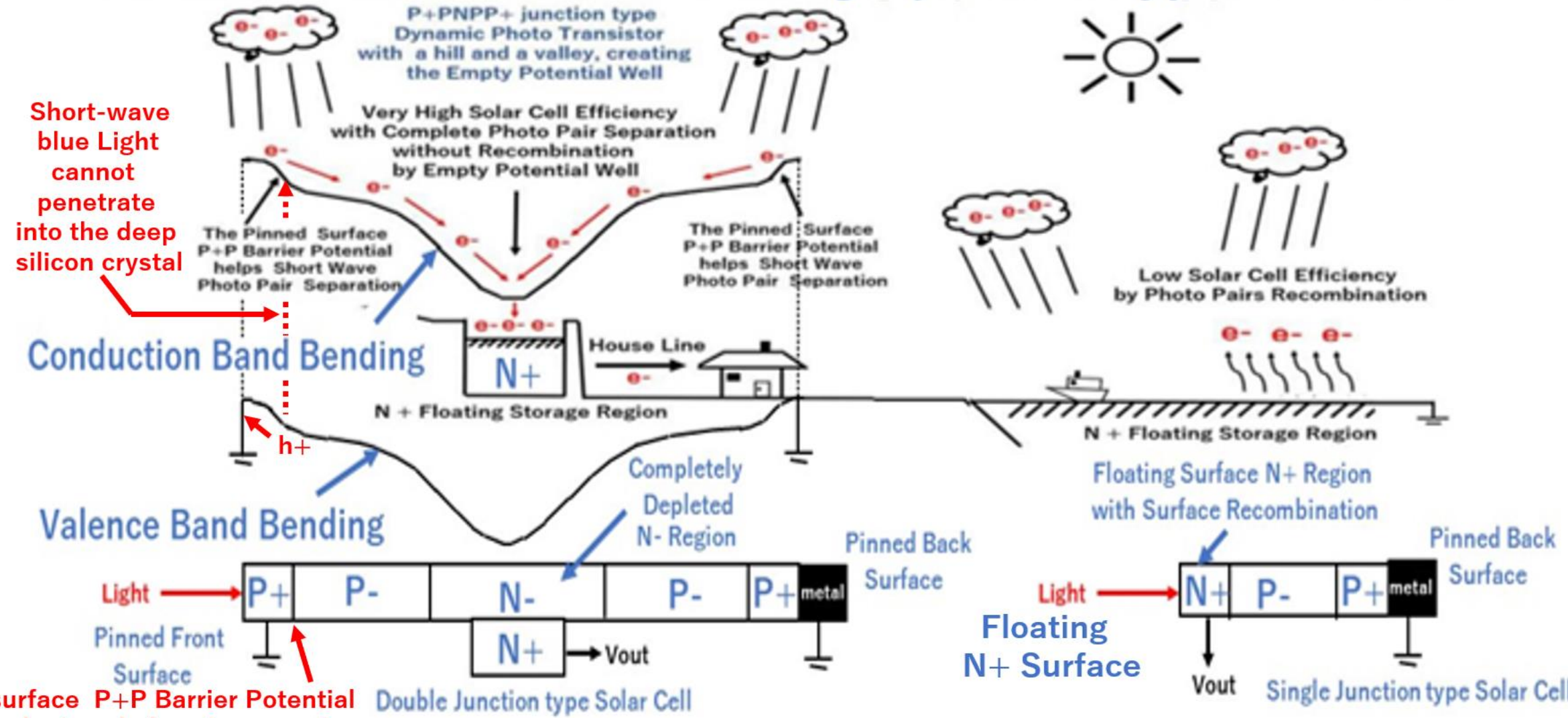


The surface P region is not Pinned. The Buried N region is still floating.

This patent is on the PNP junction type Buried Photodiode but NOT Pinned Photodiode. The surface P region is not pinned and grounded. The surface potential can be of any value depending on the floating buried N region potential, which is actually controlled by the substrate Psub potential which is grounded in this case, but in case of a built-in VOD function P+NPNsub junction photodiode, the P region potential is controlled by the Nsub VOD voltage and can be any value. The surface P region must be pinned by the adjacent P+ channel Stops region or the adjacent metal contact wiring.

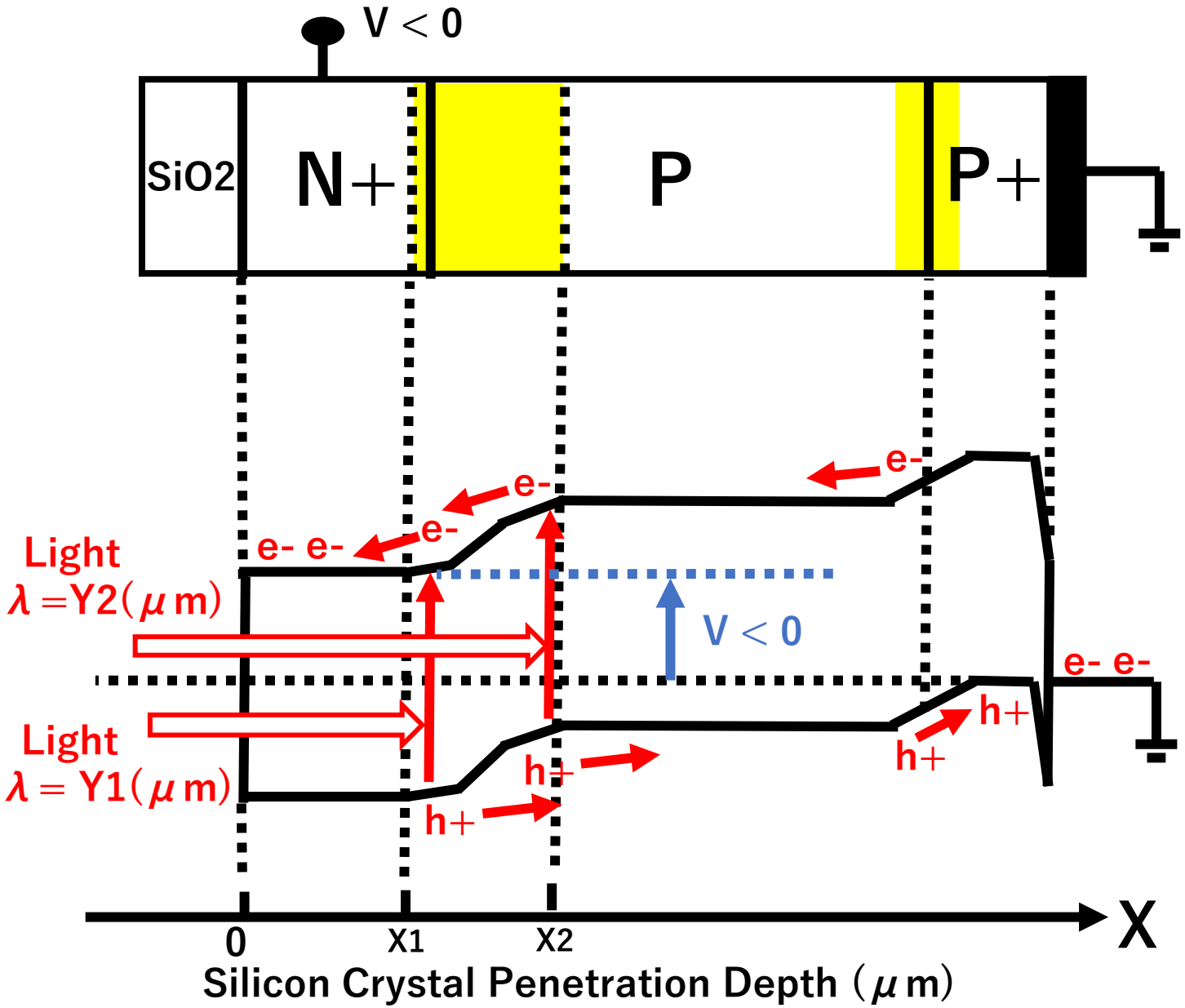
True History of Photodiode

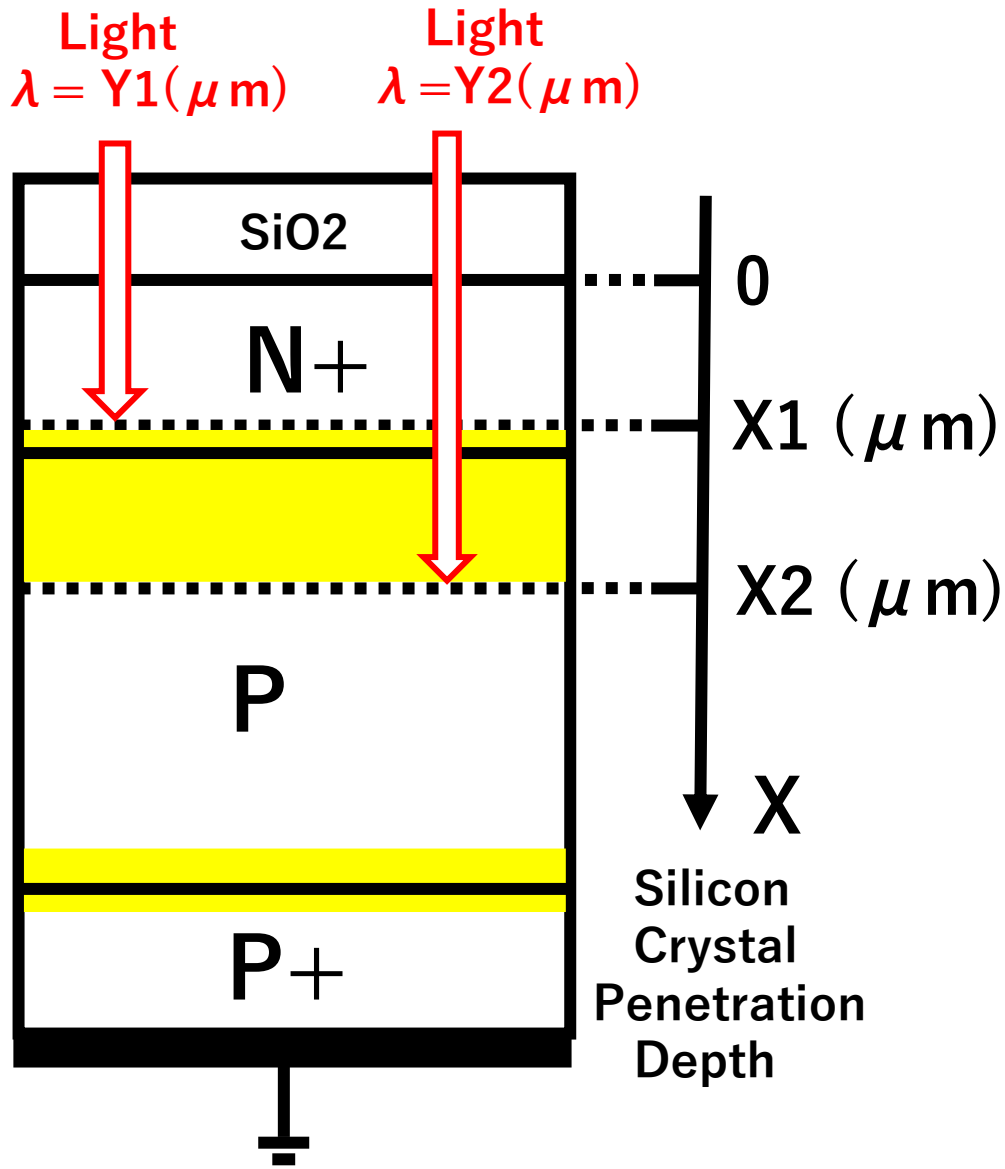
The difference of Double and Single junction type Solar Cells



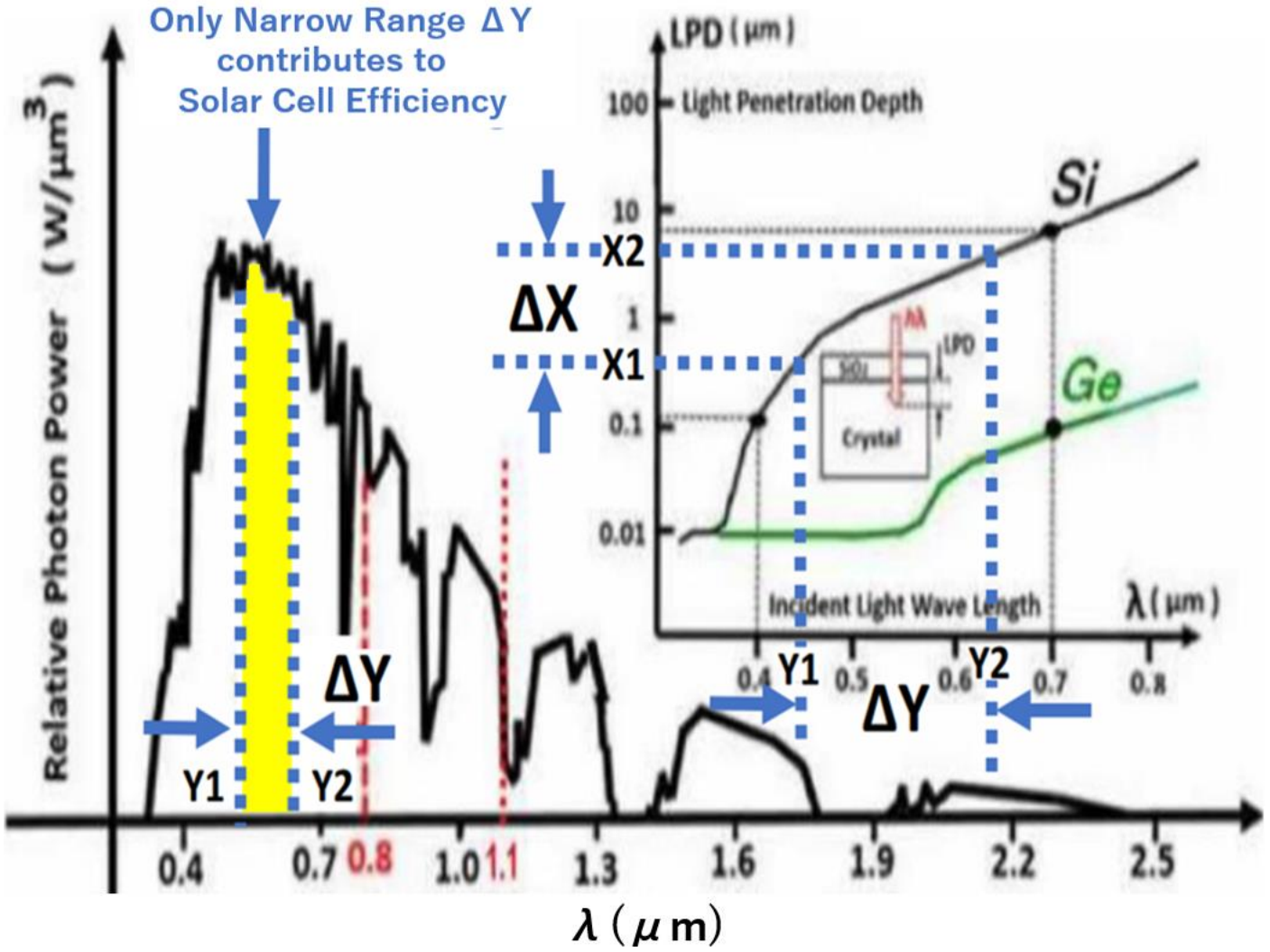
The surface P+P Barrier Potential helps electron-hole pair separations.

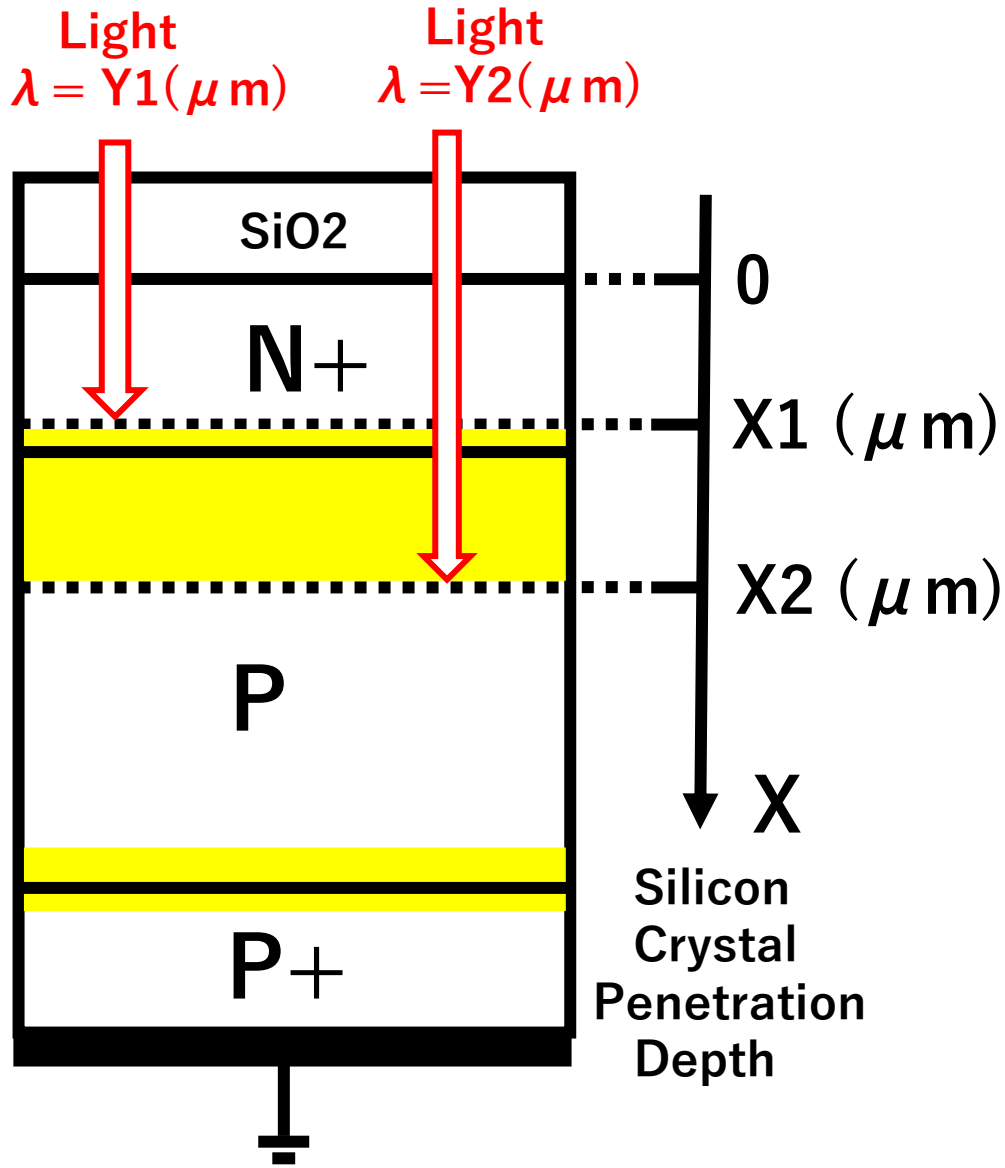
For Single Junction type Solar Cell with the floating N+ surface photo charge storage region, only the wave length between Y1(μm) and Y2(μm) can contribute to the Efficiency.





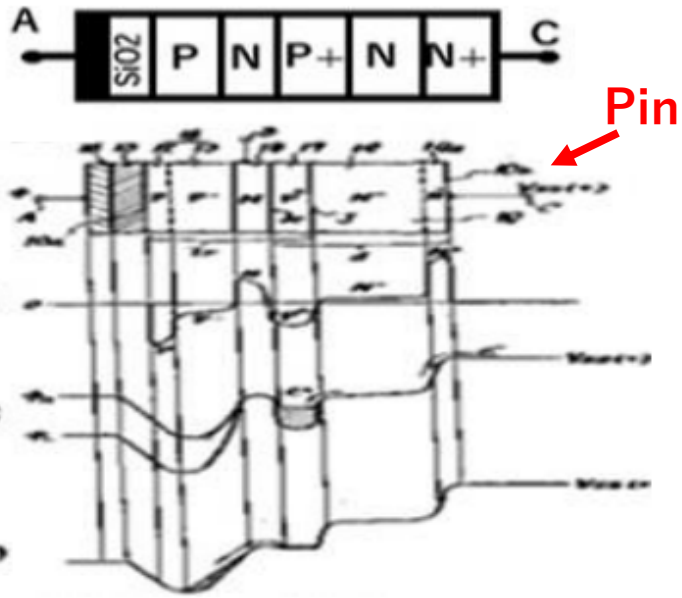
For Single Junction type Solar Cell with the floating N+ surface photo charge storage region, only the wave length between Y1(μm) and Y2(μm) can contribute to the Efficiency.



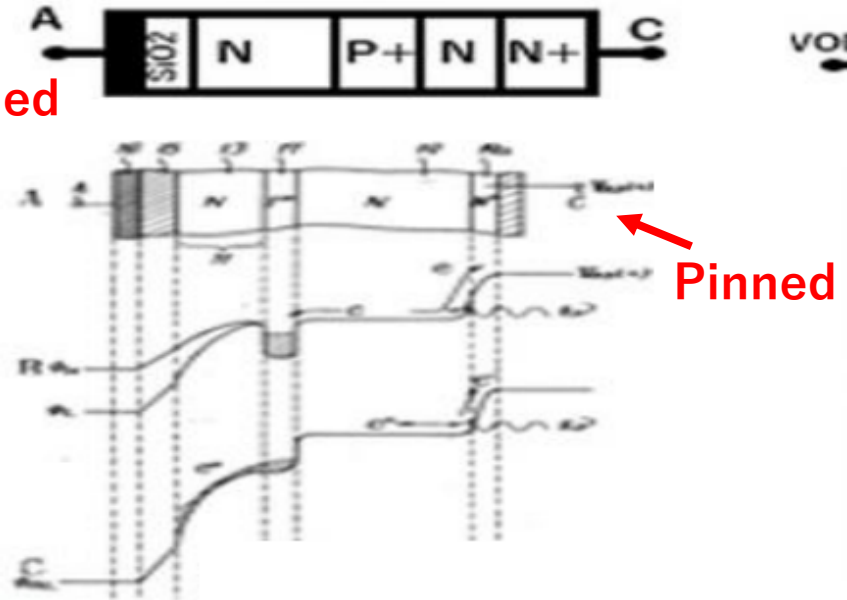


Who invented Pinned Photodiode ?

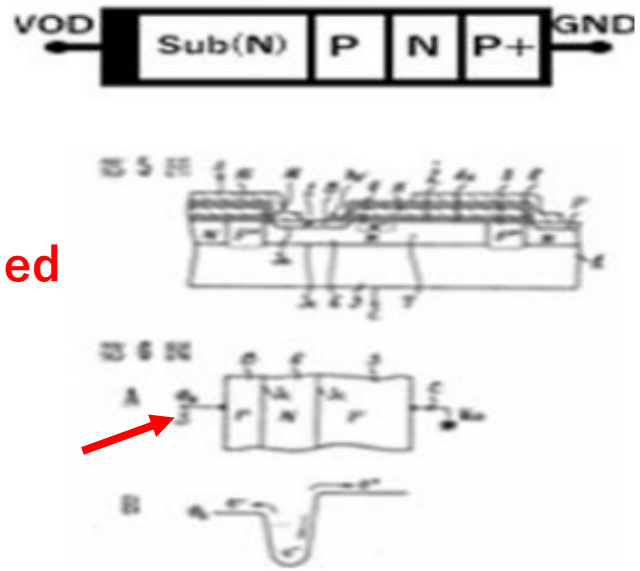
Hagiwara at Sony invented Pinned Photodiode in 1975. The evidence is give by the three Japanese patent applications, JPA1975-127646, JPA1975-127647 and JPA1975-134985. The first Pinned Photodiode was defined in October 23, 1975 as the N+NPNP triple junction(in Fig. 7 of JAP1975-127646) type and the N+NPN double junction type (in Fig. 7 of JAP1975-127647) type photodiodes with the N+ type pinned surface and the P type buried photo charge storage region with the complete charge transfer capability and the no-image-lag feature. The photo charge is transferred and drained to the CCD/MOS type charge storage buffer memory quicky by the strong punch-thru action. The second Pinned Photodiode was defined in November 10, 1975 as the PNP double junction (in Fig. 6 of JAP1975-134985) type photodiode with the vertical overflow drain action also with the complete charge transfer capability and the no-image-lag feature as evidence the empty potential well of the buried photo charge storage, completely depleted of the charge.



JPA1975-127646 Fig. 7



JPA1975-127647 Fig. 7



JPA1975-134985 Fig. 6

Proceedings of the 9th Conference on Solid State Devices, Tokyo, 1977;
Japanese Journal of Applied Physics, Volume 17 (1978) Supplement 17–1, pp. 255–261

Two Phase CCD with Narrow-Channel Transfer Regions

Yoshiaki DAIMON-HAGIWARA

Sony Corporation Research Center Yokohama 240

with no image lag

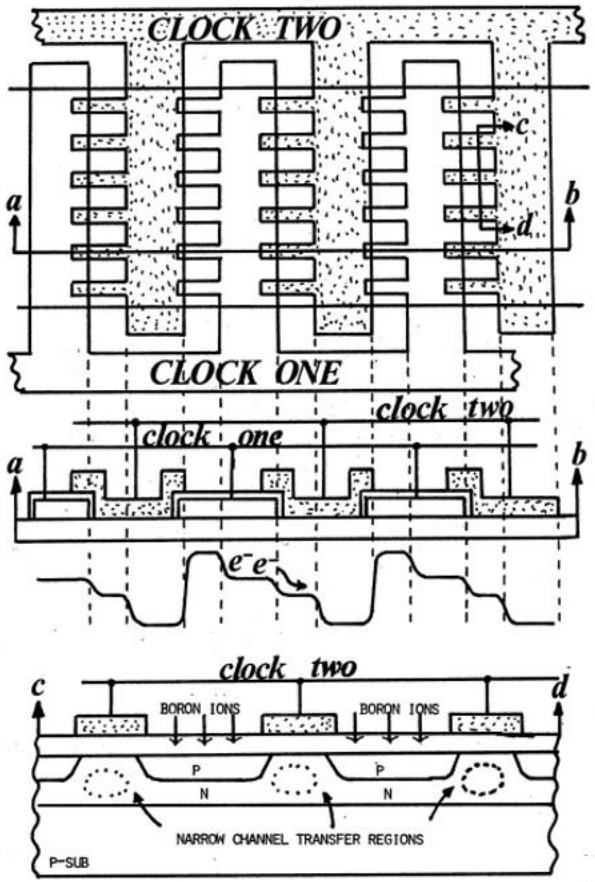


Fig. 1. Top and crosssectional views of the electrode structure for two phase CCD with narrow-channel transfer regions.

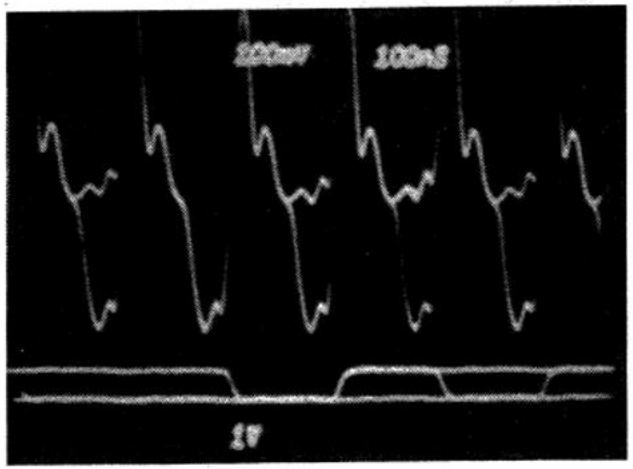


Fig. 4. Input and output wave forms for 242 analo delay line in buried channel version.

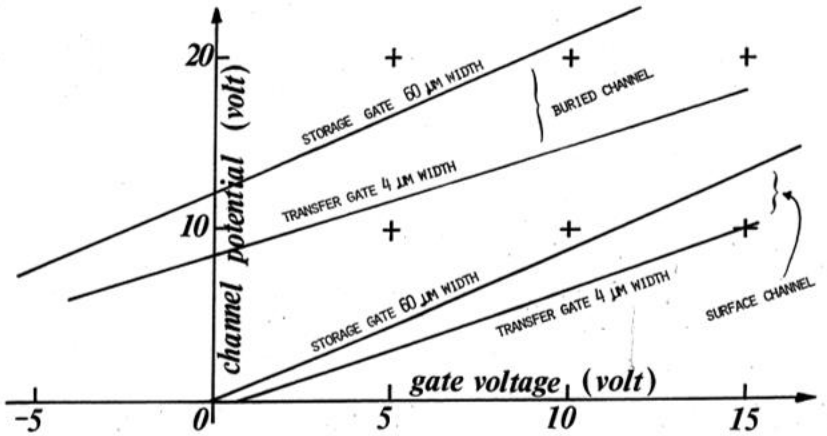


Fig. 2. The actual measured channel potentials plotted against the gate voltage for both surface and buried channel versions.

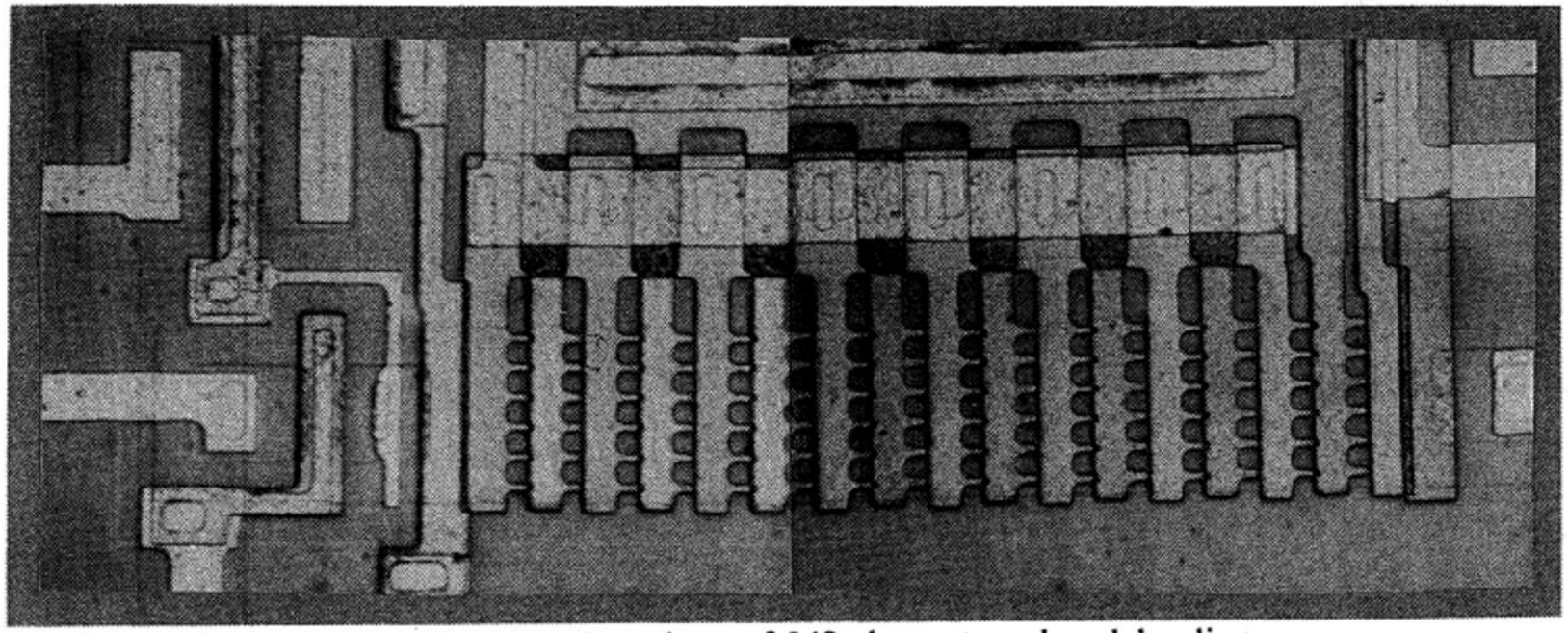
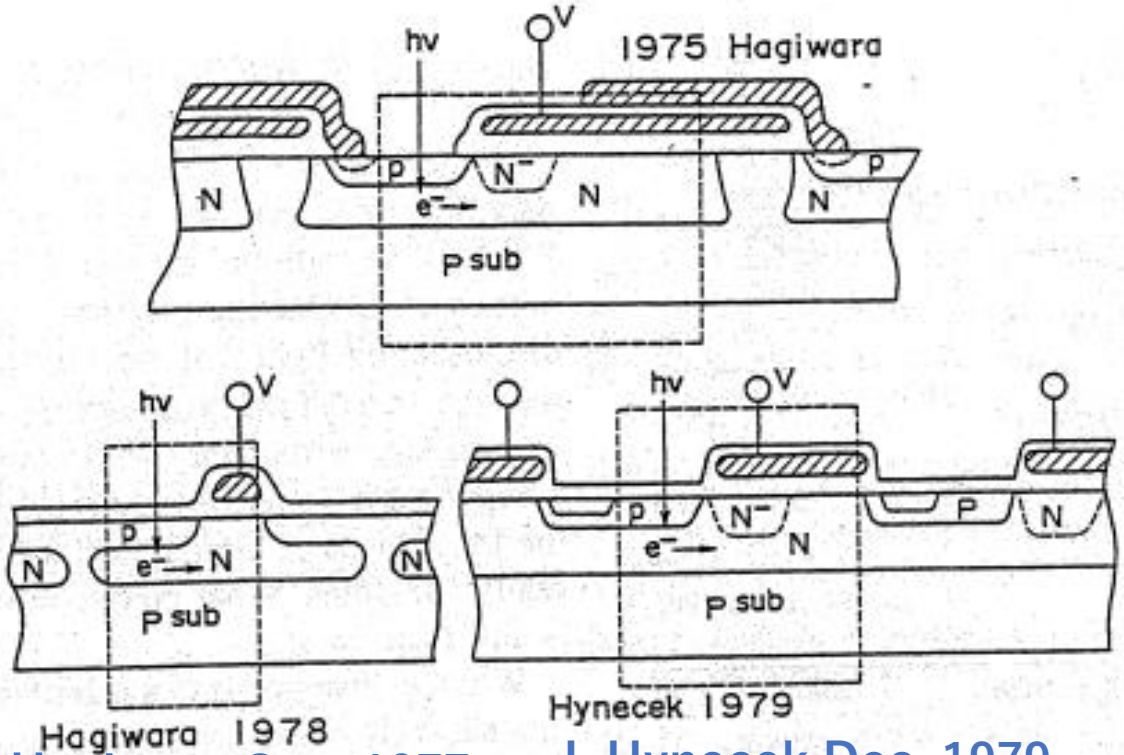


Fig. 3. The end sections of 242 element analog delay line.

High-Density and High-Quality Frame Transfer CCD Imager with Very Low Smear, Low Dark Current, and Very High Blue Sensitivity

Yoshiaki Hagiwara, *Member, IEEE*

Y.D. Hagiwara Nov 10, 1975

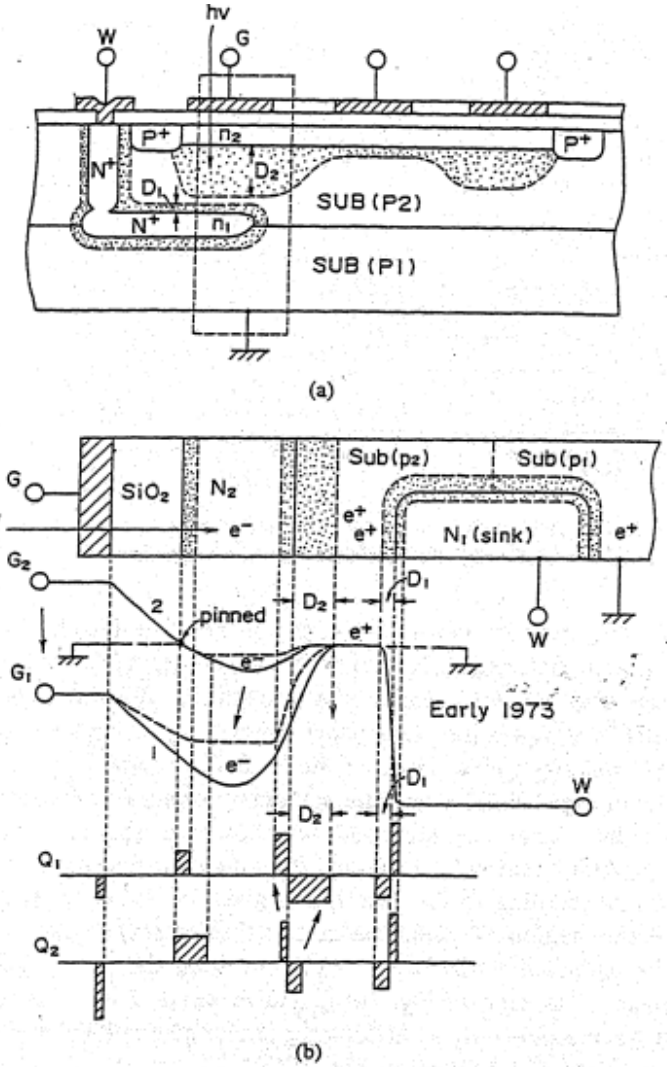


Y.D. Hagiwara Sep, 1977

J. Hynecek Dec, 1979

[16] J. Hynecek, "Virtual phase CCD technology," in *IEEE Proc. IEDM*, Dec. 1979, pp. 611–614.

J.M. Early Dec 3, 1973



[17] J. M. Early, U.S. Patent 3896485, Dec. 3, 1973.

Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978;
Japanese Journal of Applied Physics, Volume 18 (1979) Supplement 18-1, pp. 335-340

A 380H × 488V CCD Imager with Narrow Channel Transfer Gates

Yoshiaki Daimon-HAGIWARA, Motoaki ABE† and Chikao OKADA†

Sony Corporation Research Center, Yokohama 240
†Semiconductor Development Division, Yokohama 240

with no image lag

When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of threshold voltage is observed. This narrow-channel effect has been applied successfully in creating an asymmetric potential well under an electrode for two phase CCD operations. The feasibility of this new structure has been confirmed in a 242 element analog delay line and the application is now extended to a 380H × 488V CCD Imager. In the constructed B/W CCD camera,

Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978;
Japanese Journal of Applied Physics, Volume 18 (1979) Supplement 18-1, pp. 335-340

A 380H × 488V CCD Imager with Narrow Channel Transfer Gates

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Sony Corporation Research Center, Yokohama 240
†Semiconductor Development Division, Yokohama 240

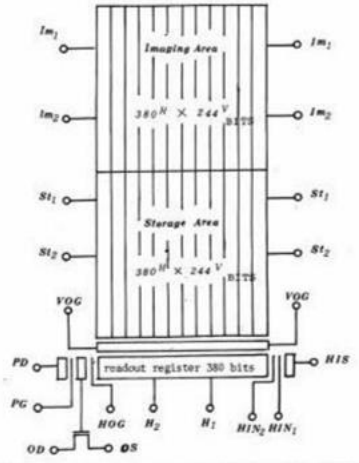


Fig. 1. The block diagram of a 380 H×488 V CCD imager in frame transfer organization.

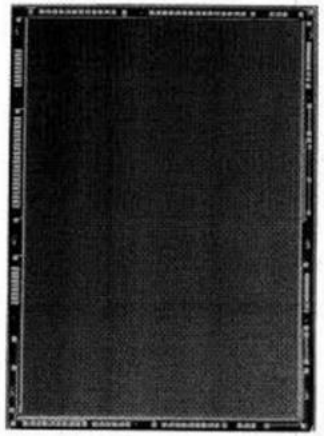


Fig. 3. Photomicrograph of the 380 H×488 V CCD imager. The chip size is 14.6 mm by 10.1 mm.

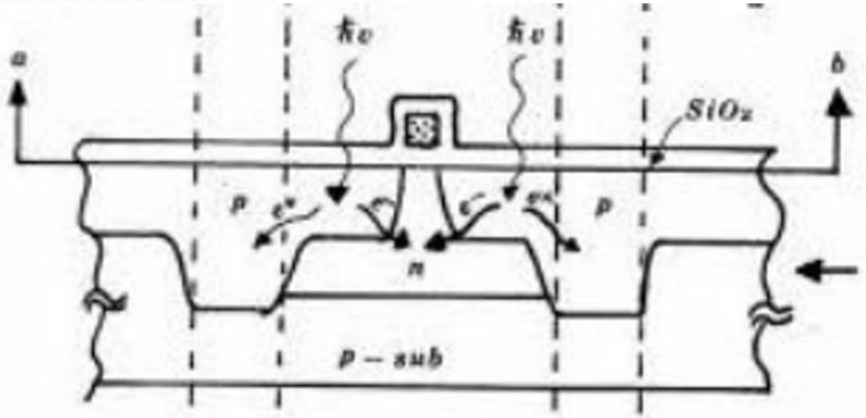


Fig. 2. Top and cross sectional views of the electrode for two phase CCD structure.

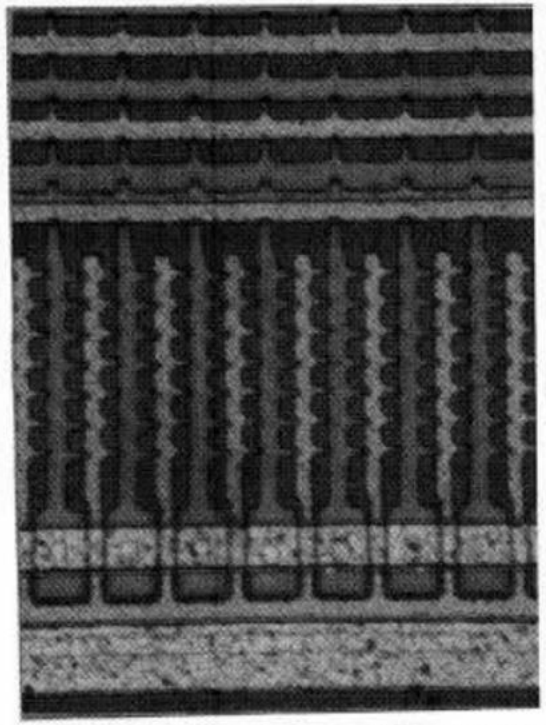


Fig. 5. The horizontal readout register with 14 μm-pitch-per bit electrode structure.

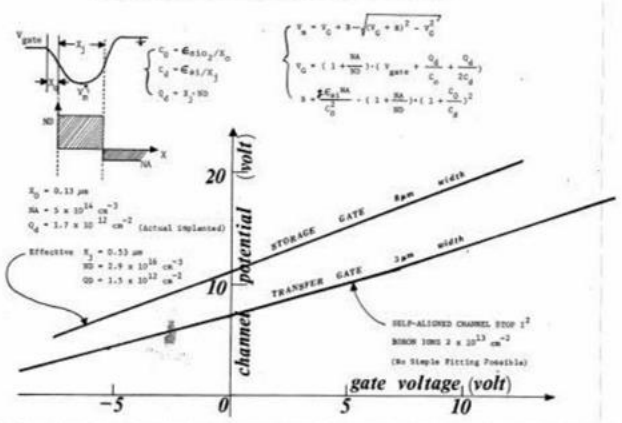


Fig. 9. The actual measured channel potentials plotted against the gate voltage for the buried channel version. The curve fitting with the simple relations by depletion approximation gives the effective values of X_j, ND and QD as seen in the figure.

with no image lag

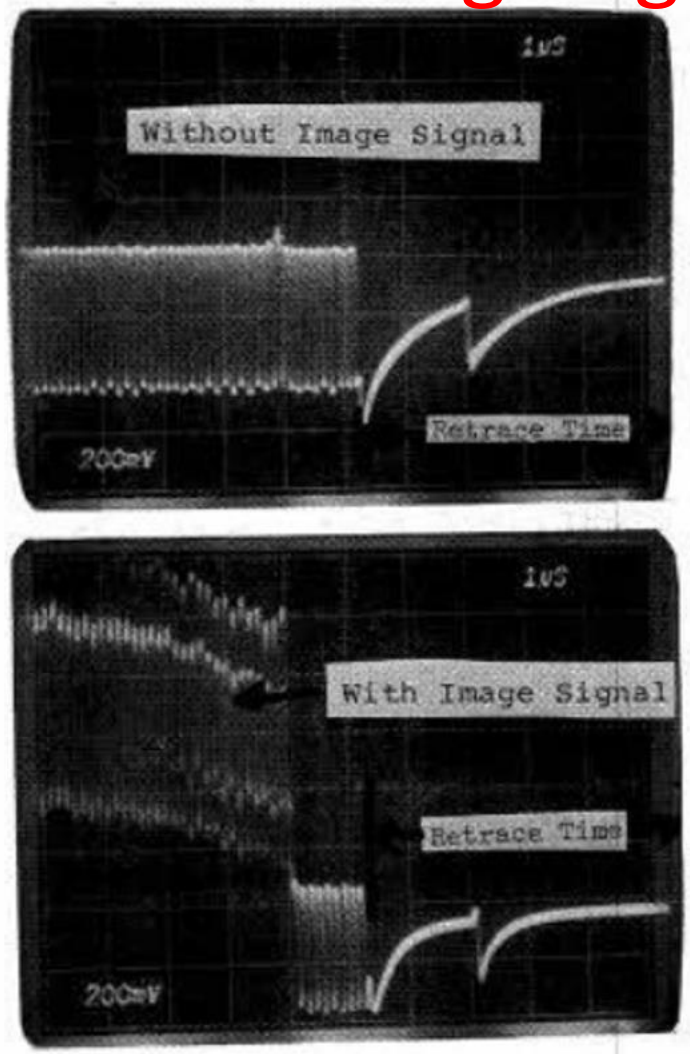
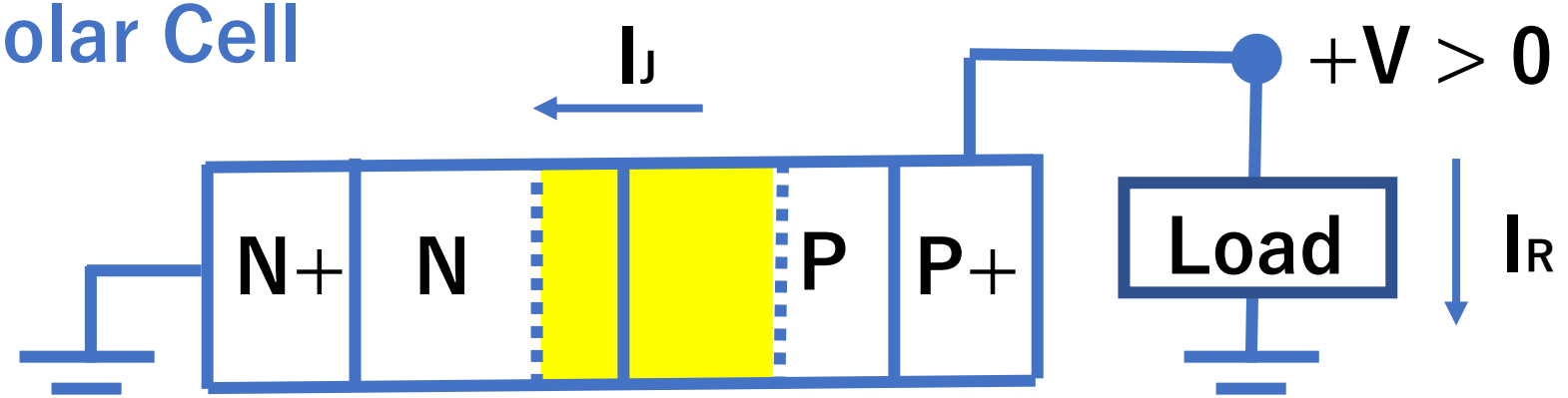


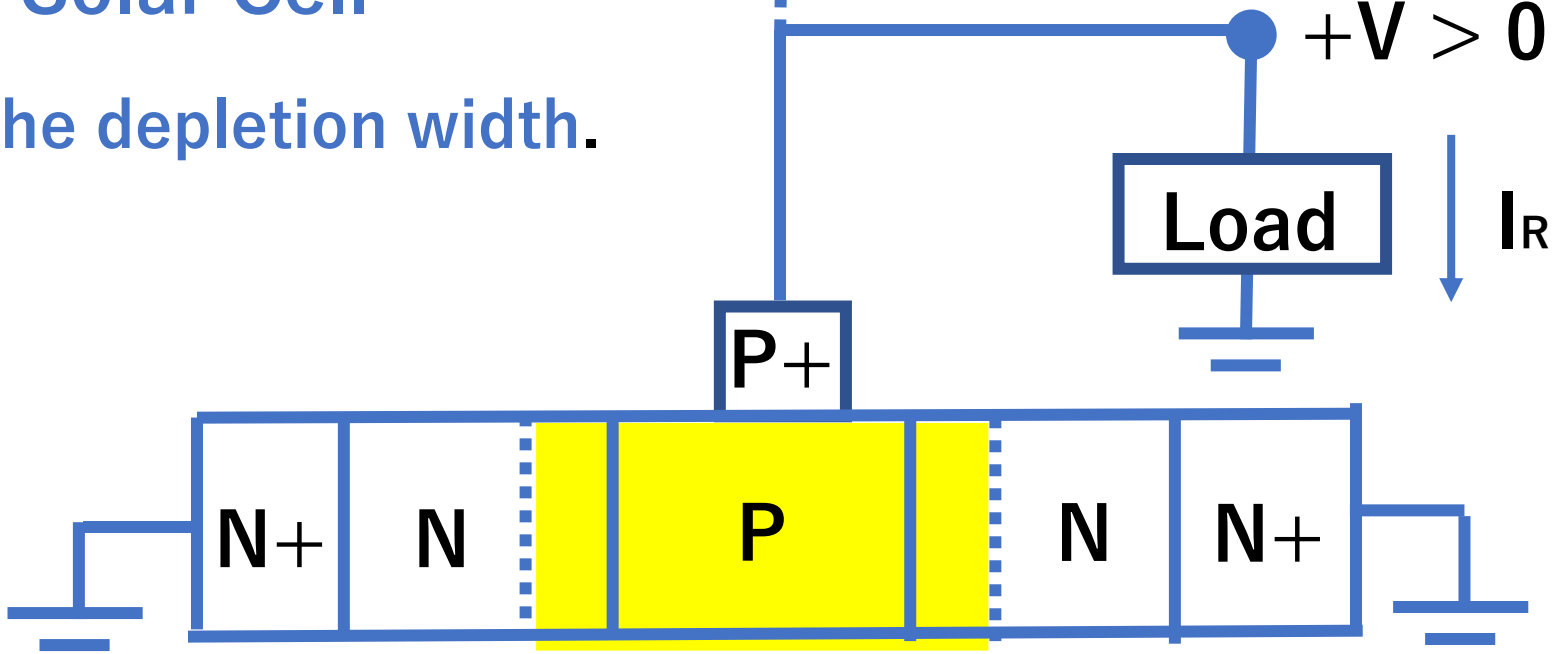
Fig. 12. The output wave forms of the horizontal readout register at the tailing end of a TV picture line, that is, right before the horizontal retrace time. The comparison of the output levels with and without image signal gives the dark current level of the imager.

Single Junction Solar Cell

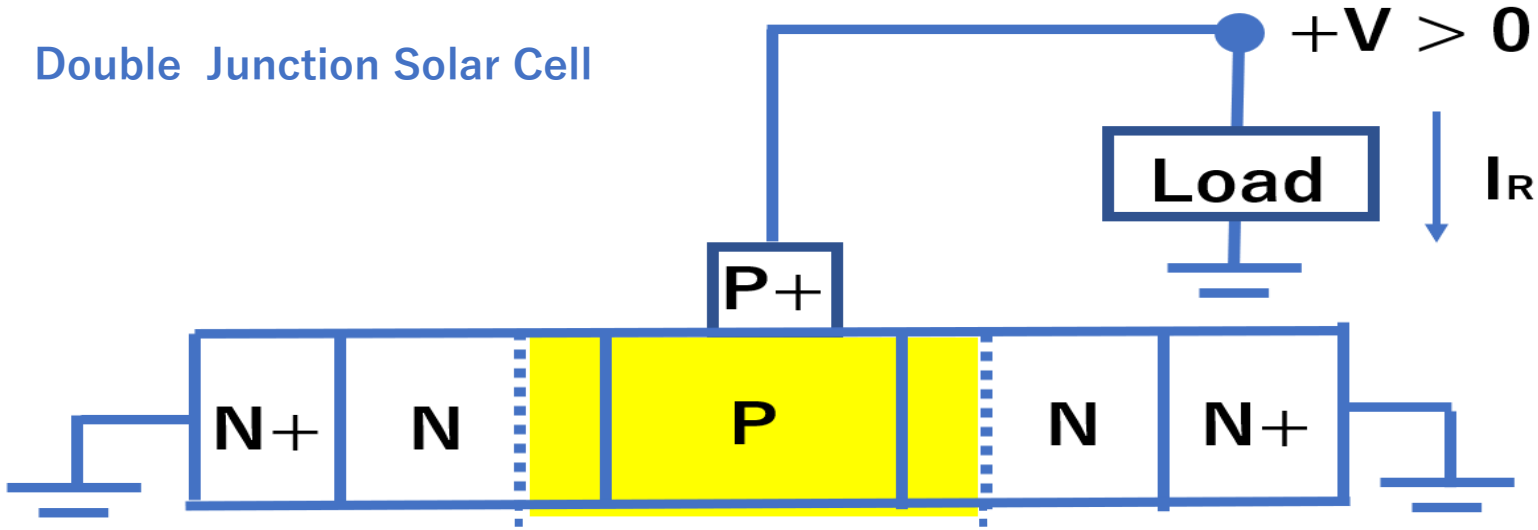


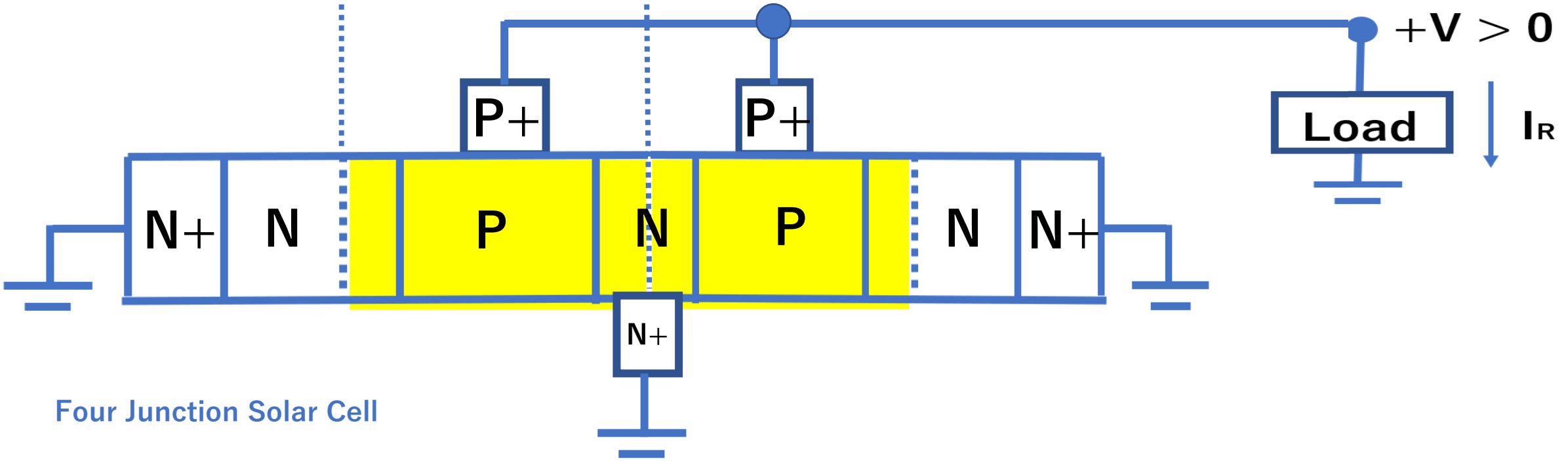
Double Junction Solar Cell

We can double the depletion width.



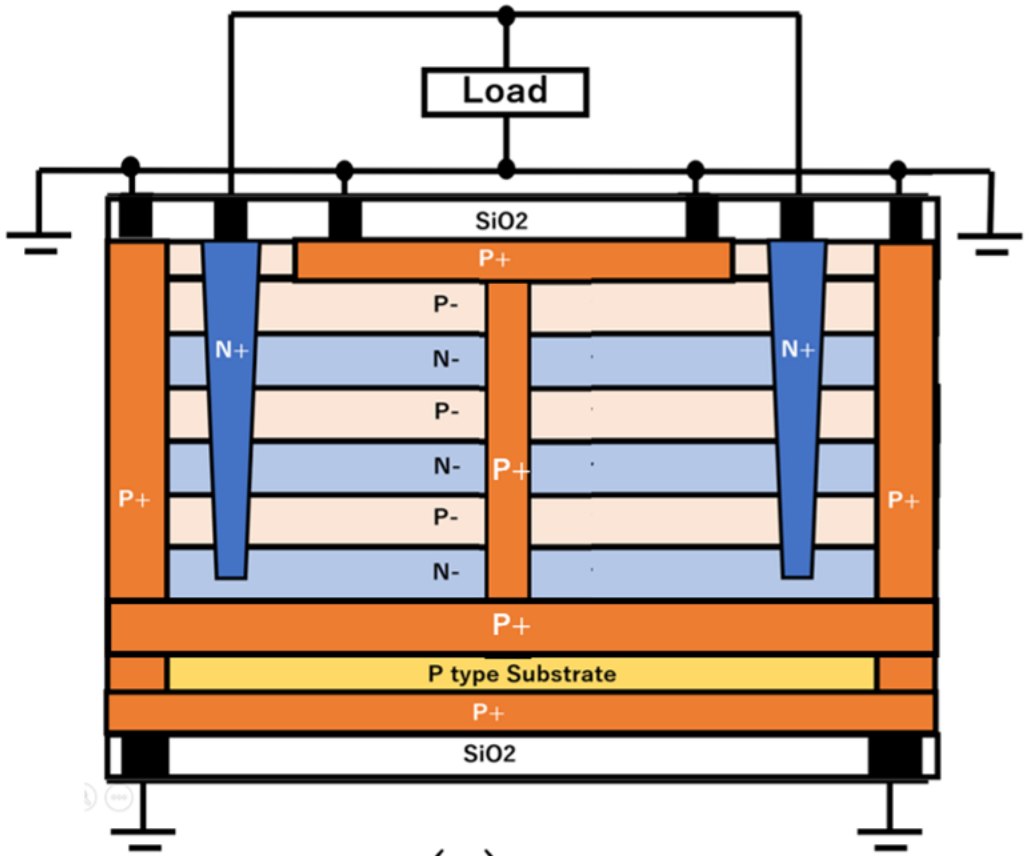
Double Junction Solar Cell





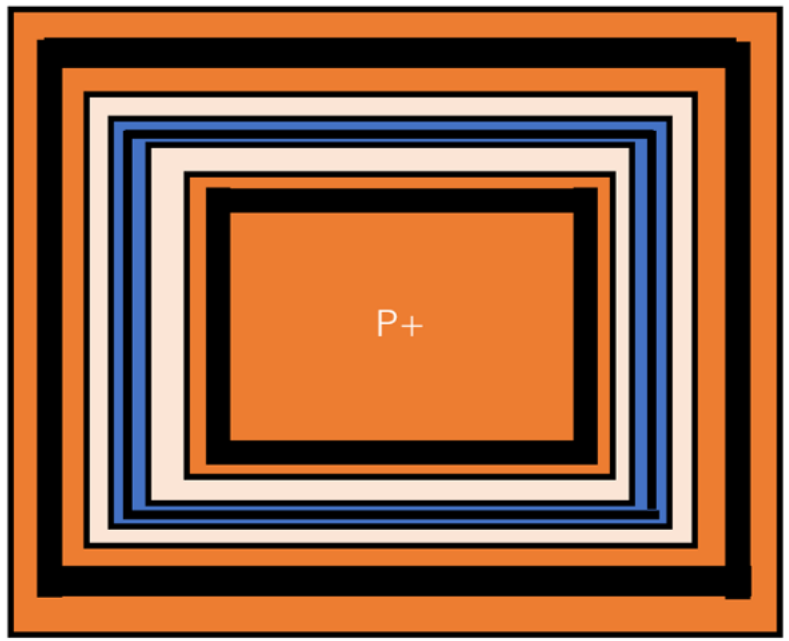
Four Junction Solar Cell

Multi-junction Solar Cell, based on JPA2020-131313 by Yoshiaki Hagiwara, applied on Aug. 1, 2020.



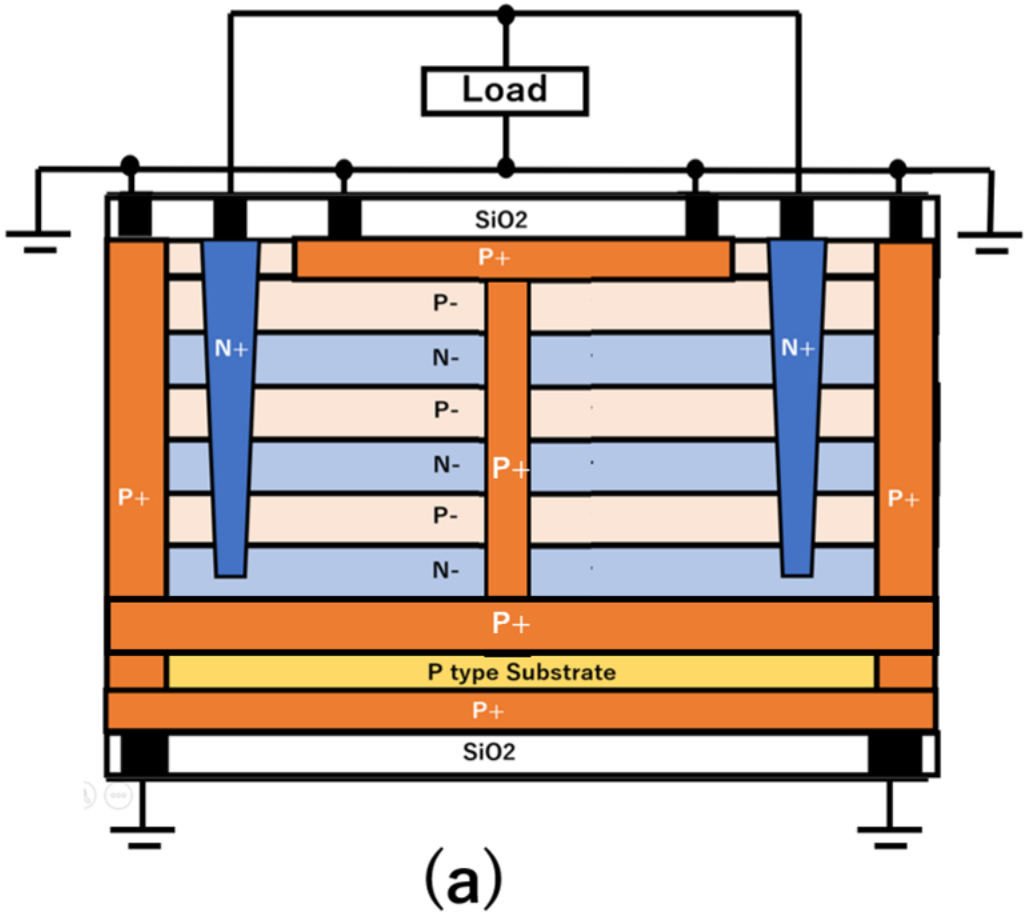
(a)

Top View

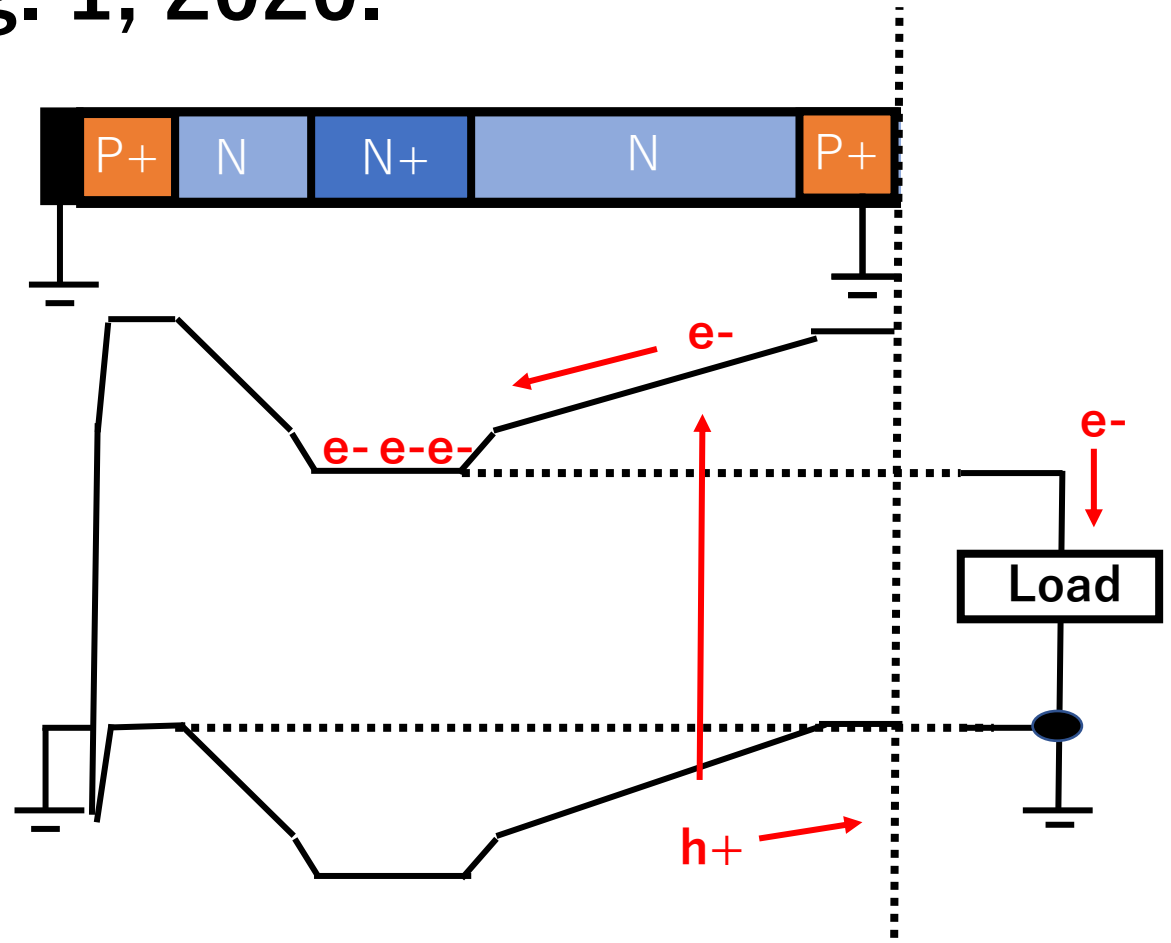


(b)

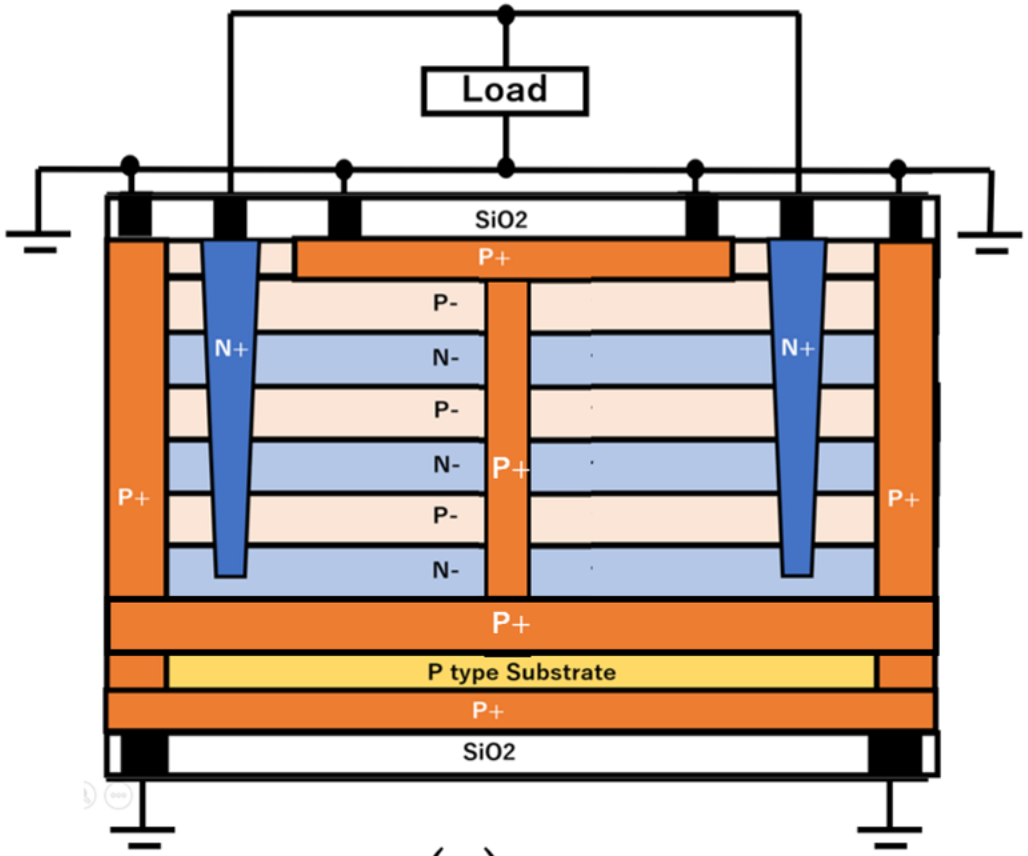
Multi-junction Solar Cell, based on JPA2020-131313 by Yoshiaki Hagiwara, applied on Aug. 1, 2020.



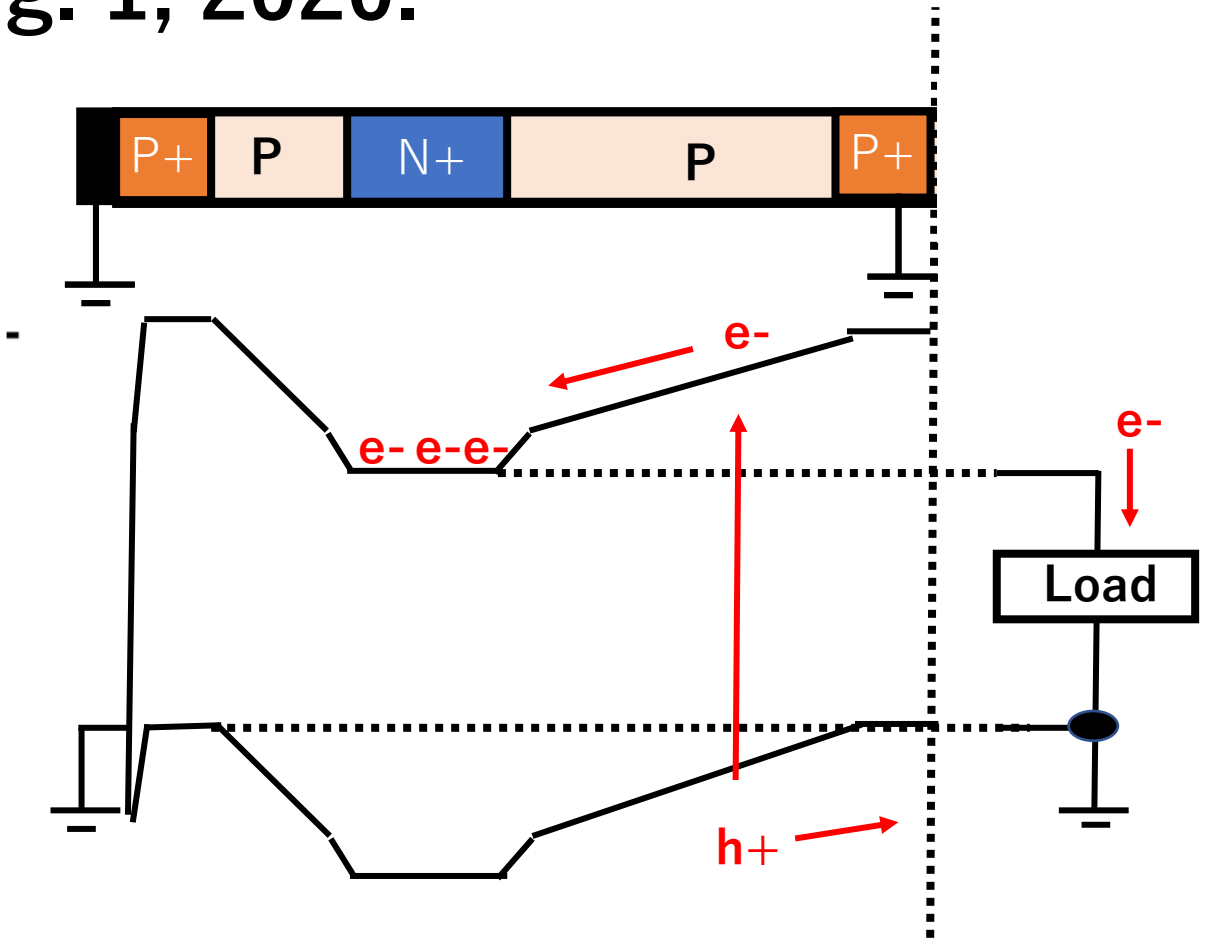
(a)



Multi-junction Solar Cell, based on JPA2020-131313 by Yoshiaki Hagiwara, applied on Aug. 1, 2020.

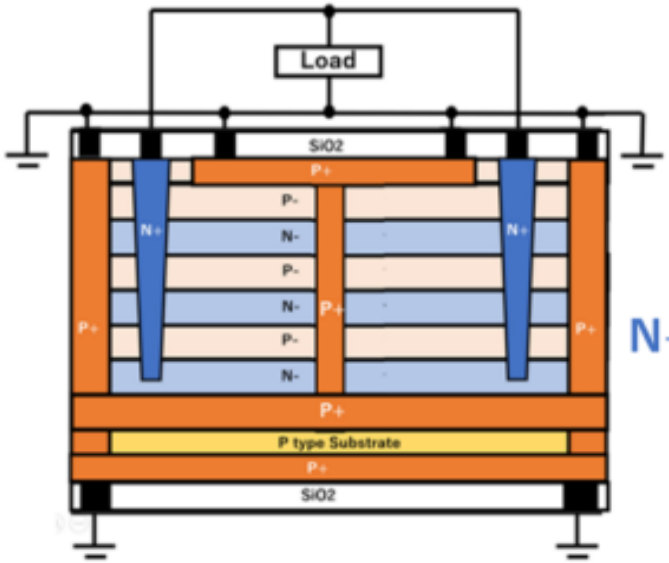


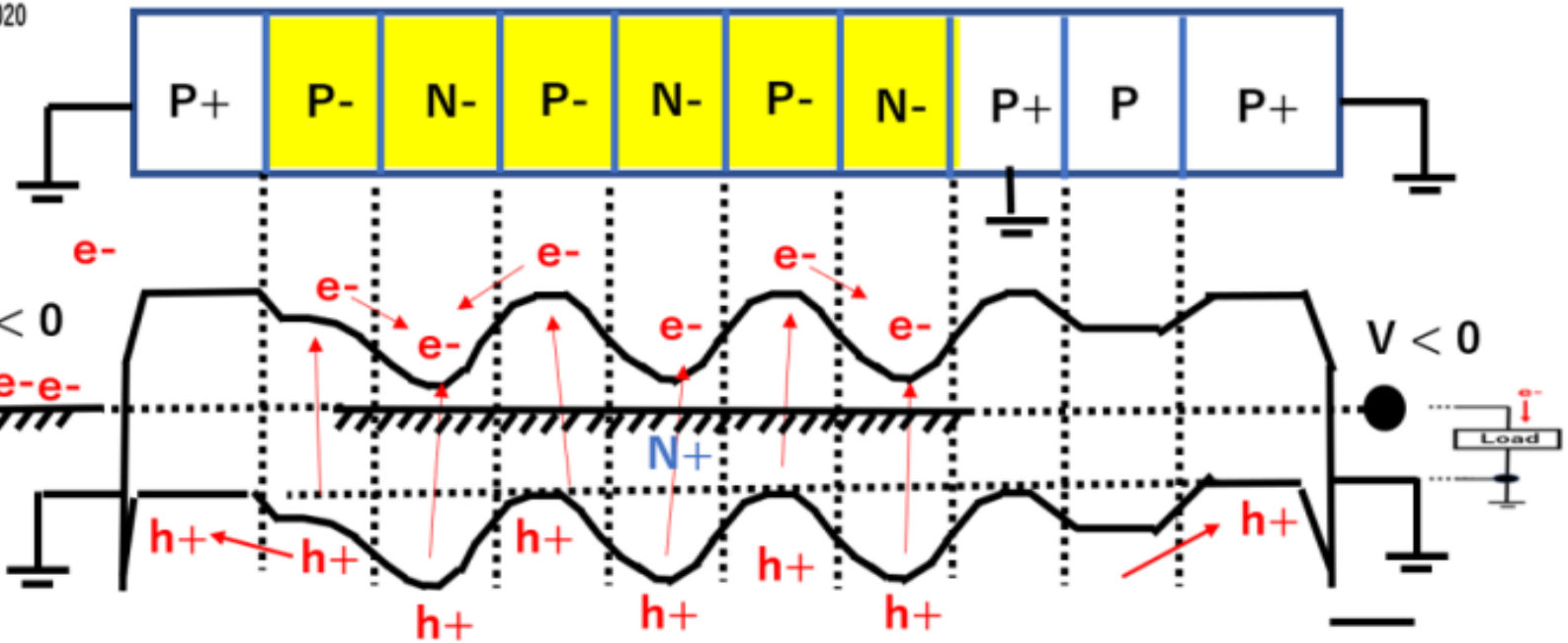
(a)

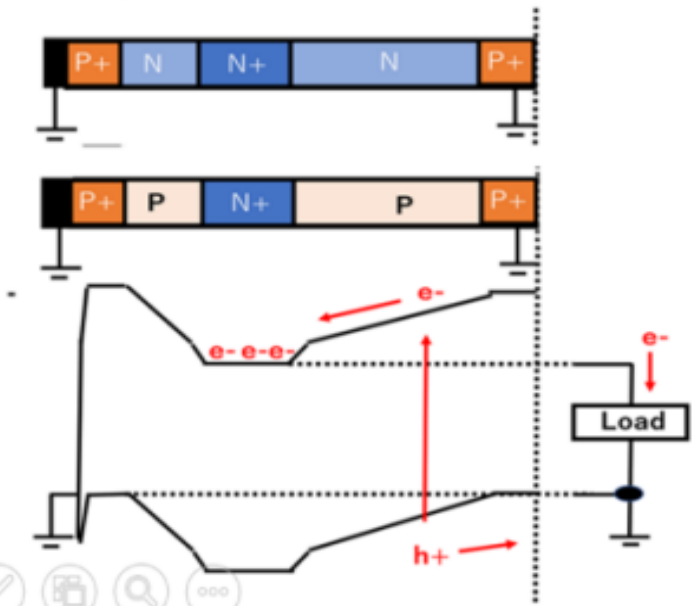


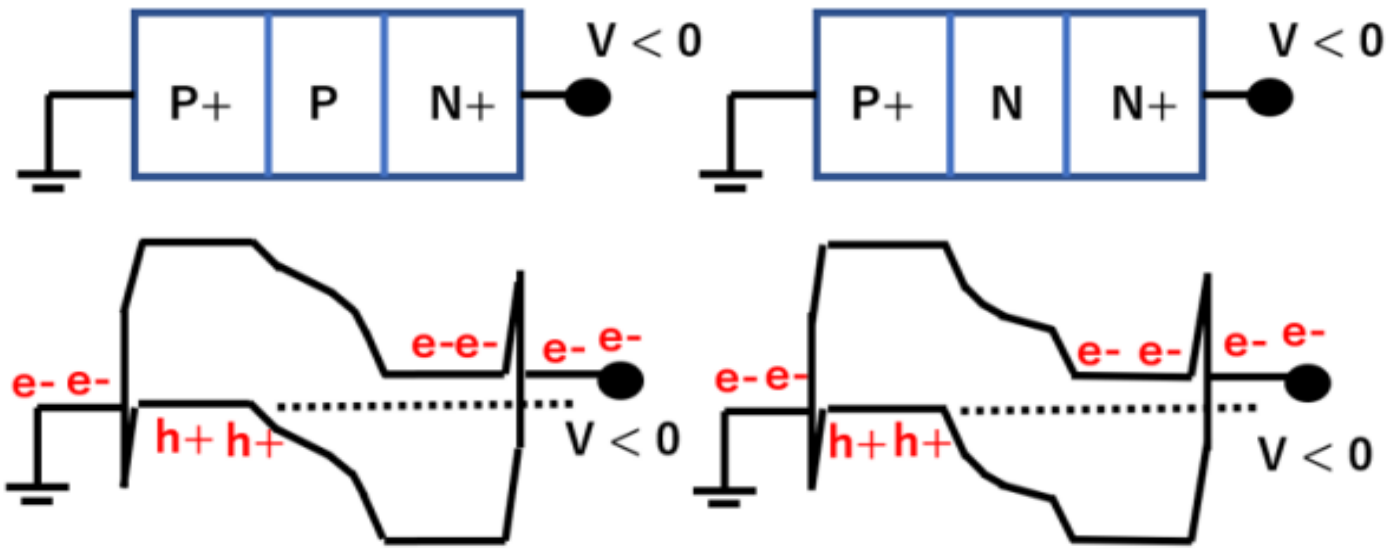
Multi-junction Pinned Photodiode with Completely Depleted of Photo Electron and Hole

Multi-junction Pinned Photodiode type Solar Cell Structure,
based on Double Junction Solar Cell , defined in JPA2020-131313, applied Aug. 1, 2020
by Yoshiaki Hagiwara, Sept 12, 2022



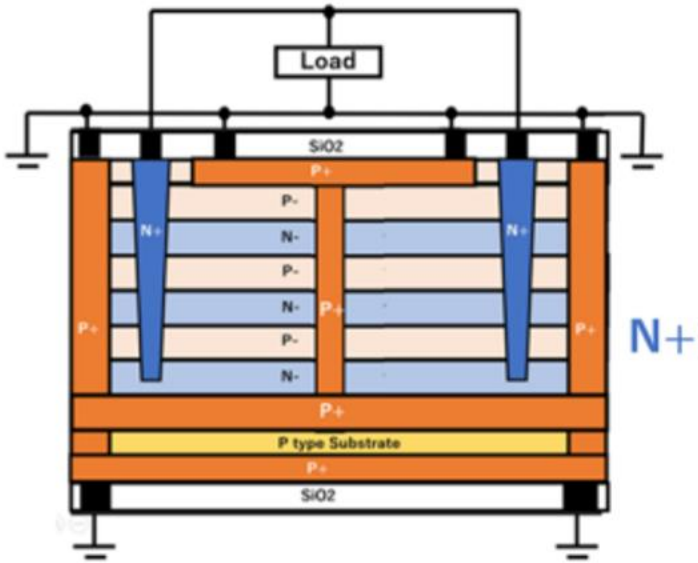


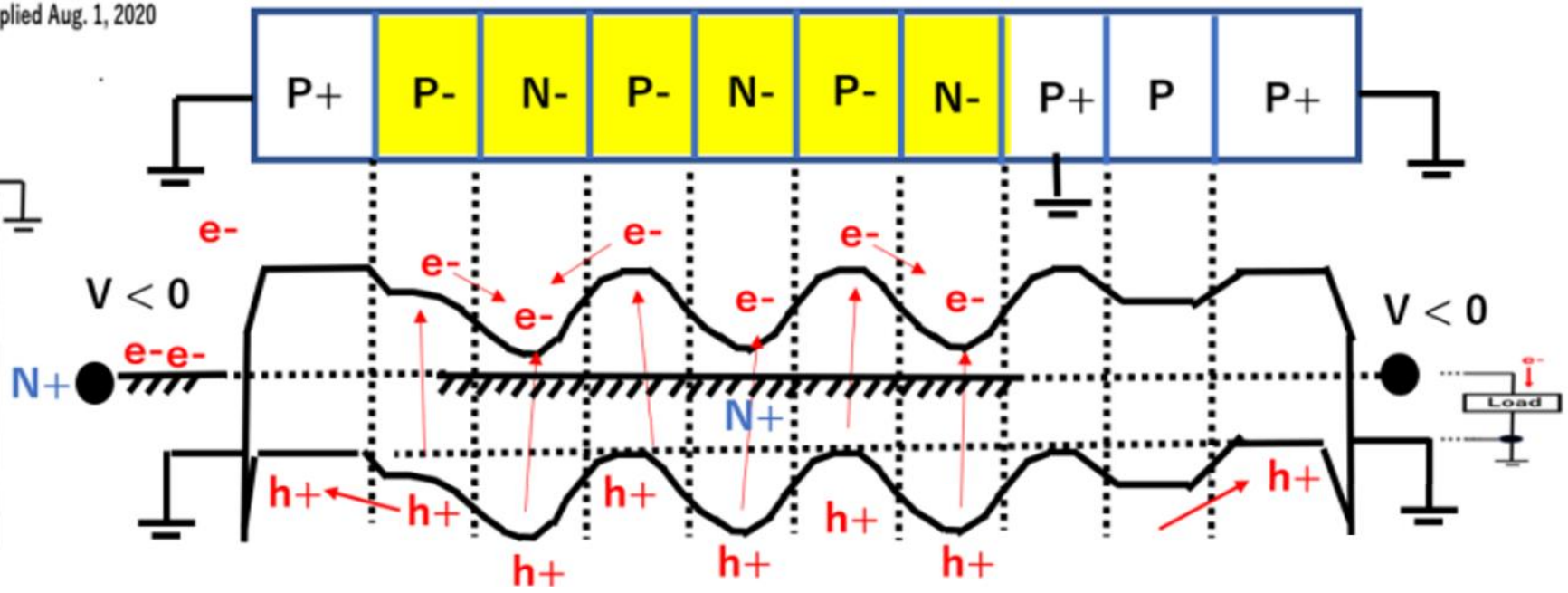


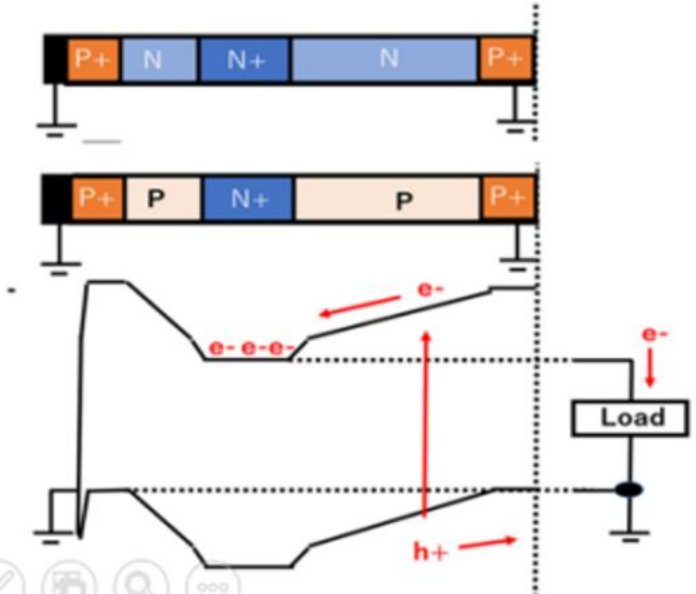


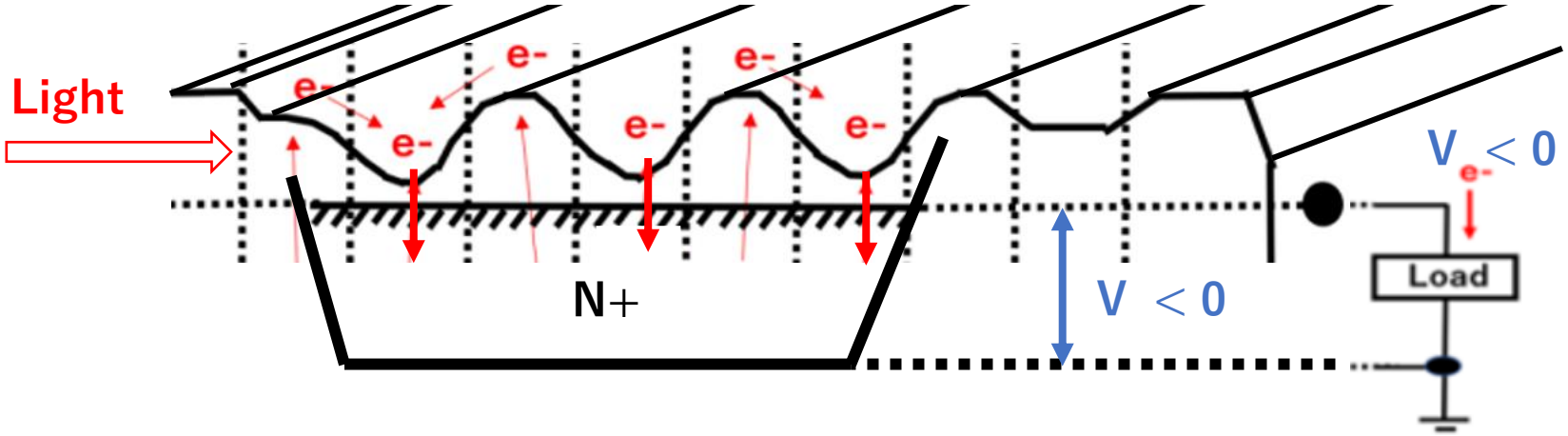
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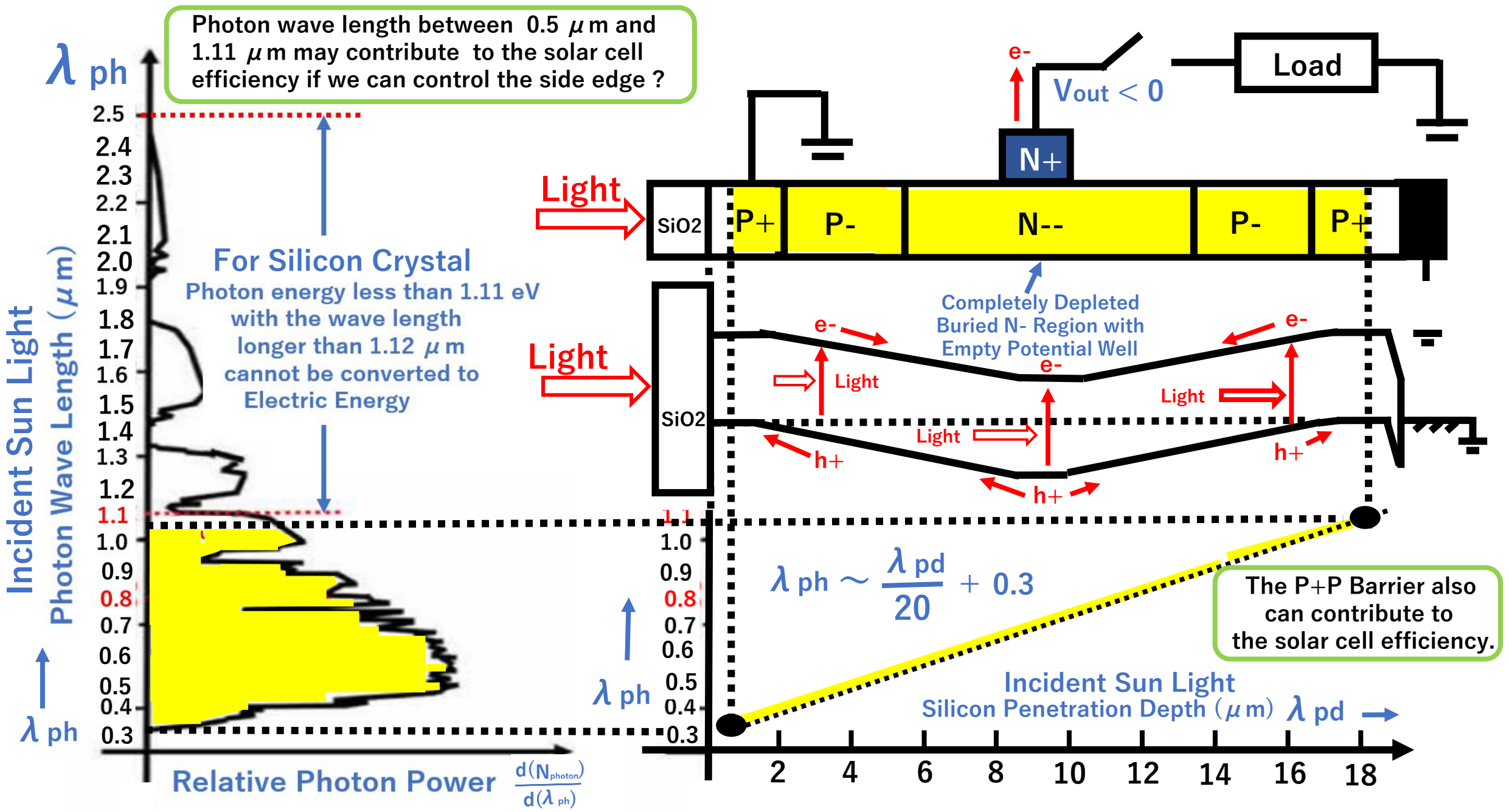






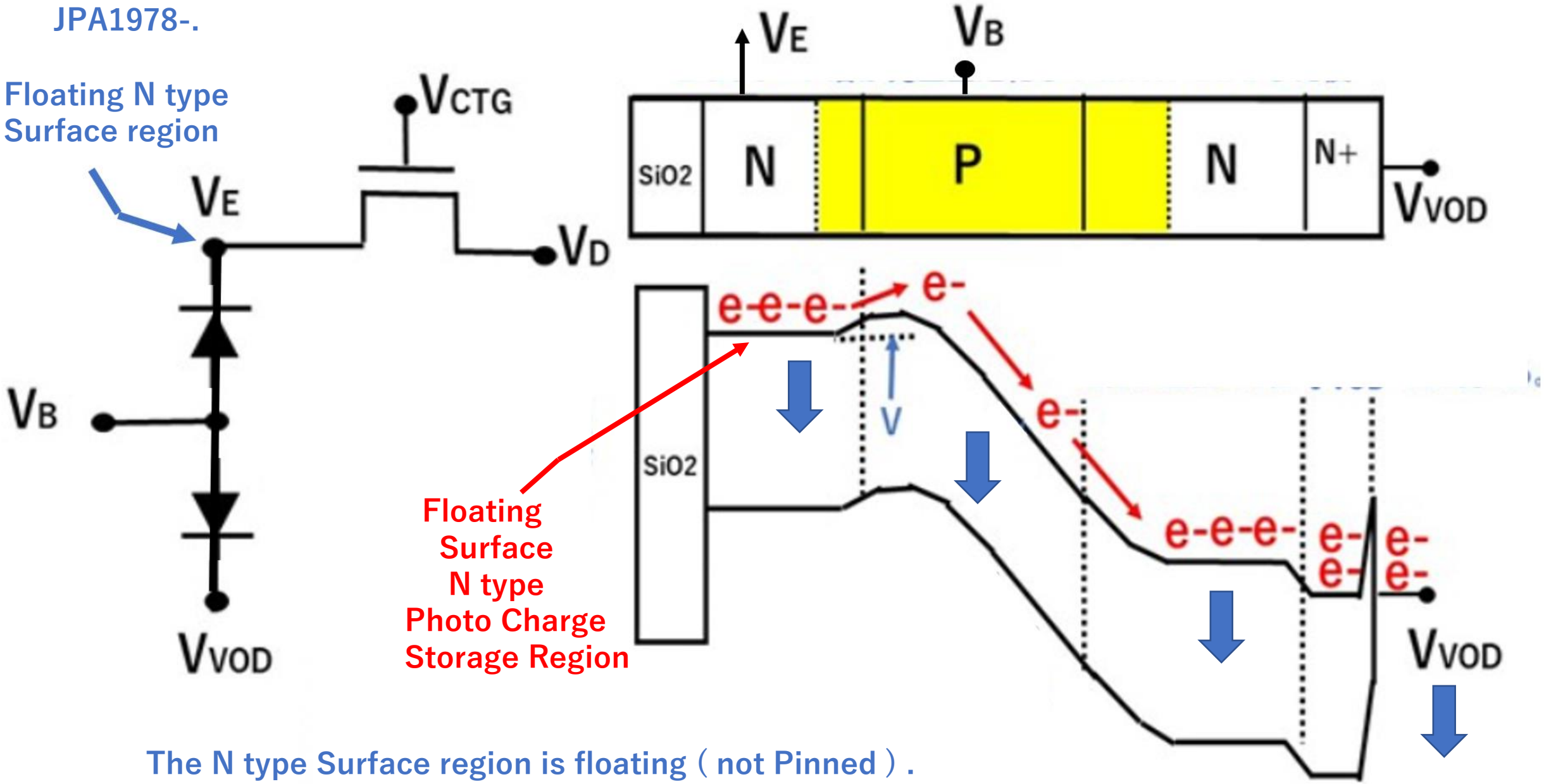


The P+P-N-P-P+ double junction type Solar Cell may have much higher efficiency



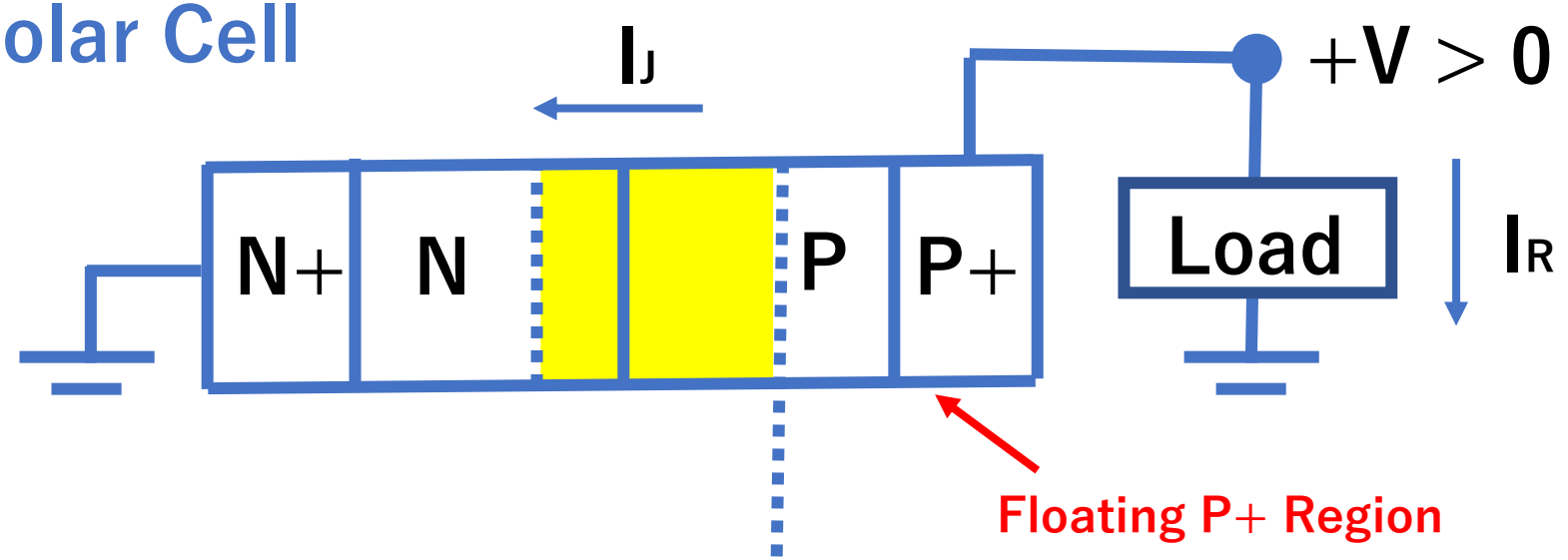
JPA1978-.

Floating N type
Surface region



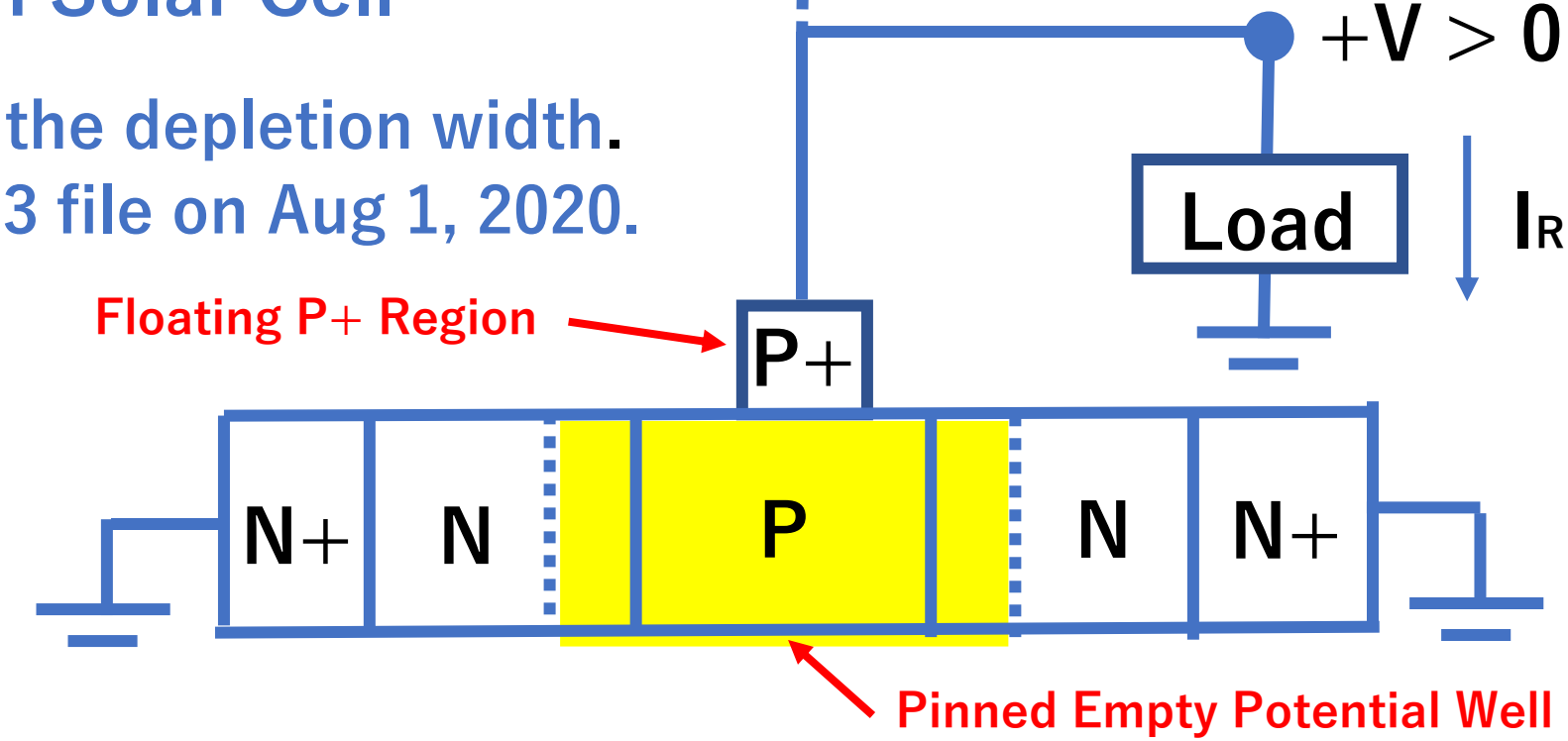
The N type Surface region is floating (not Pinned) .
The anti-blooming VOD does not function well because the N-type surface will also be pulled down as the VOD voltage is pulled down deeper.

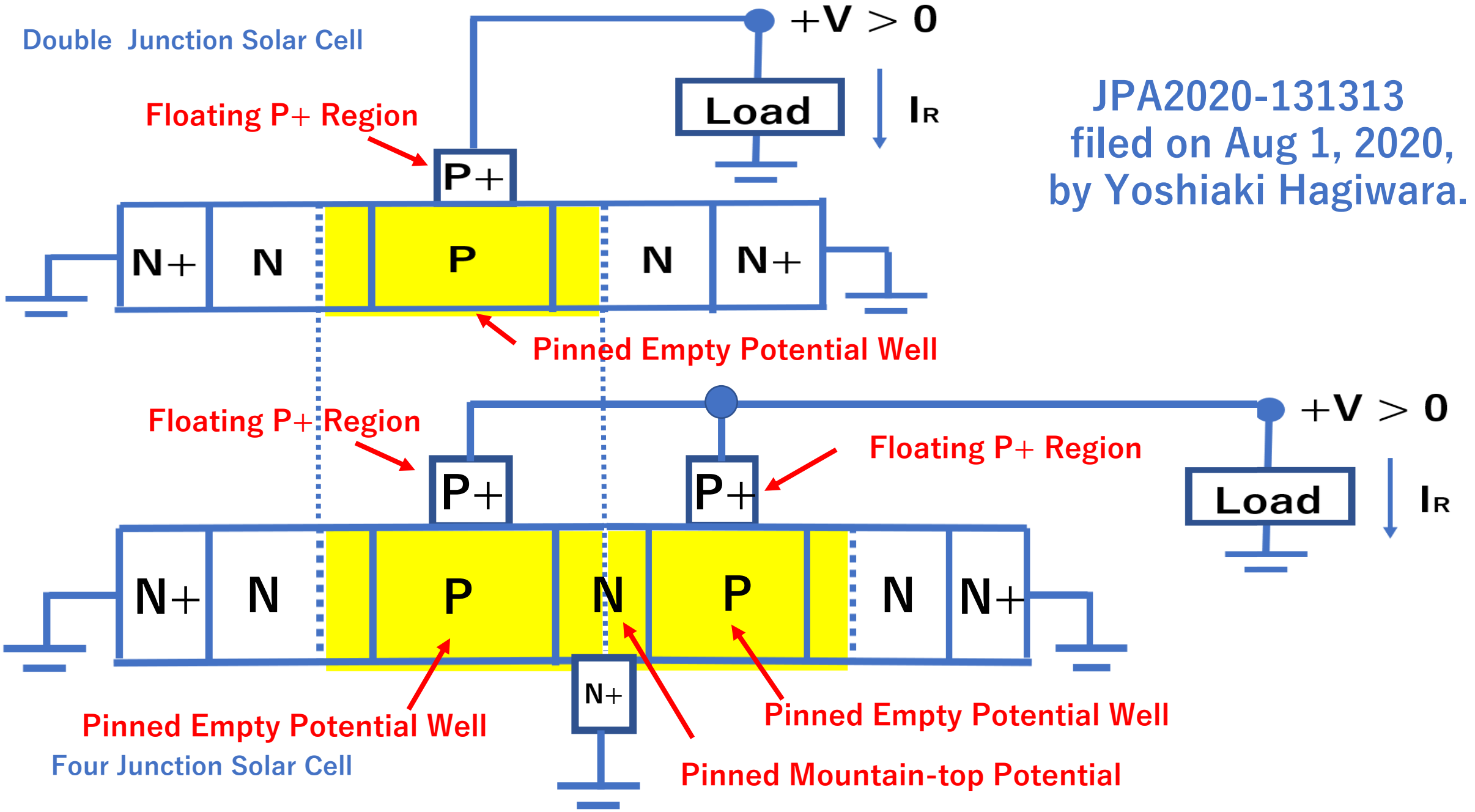
Single Junction Solar Cell



Double Junction Solar Cell

We can double the depletion width.
JPA2020-131313 file on Aug 1, 2020.

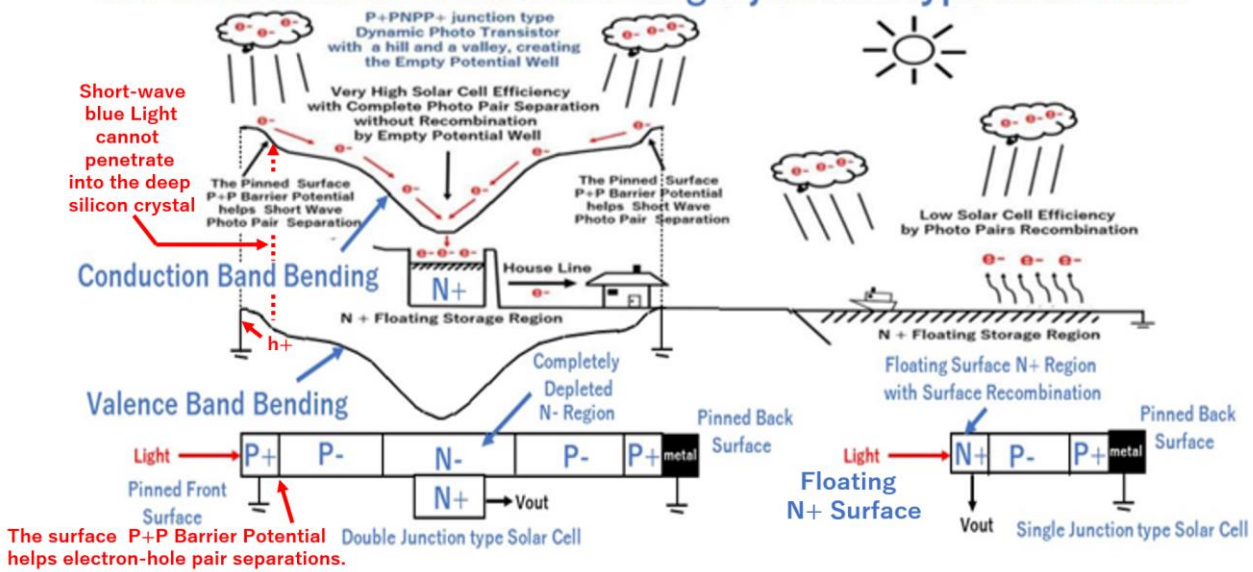




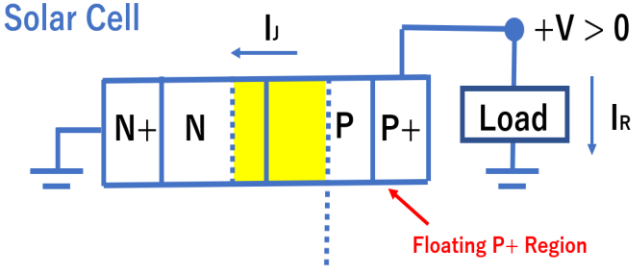
JPA2020-131313
filed on Aug 1, 2020,
by Yoshiaki Hagiwara.

True History of Photodiode

The difference of Double and Single junction type Solar Cells

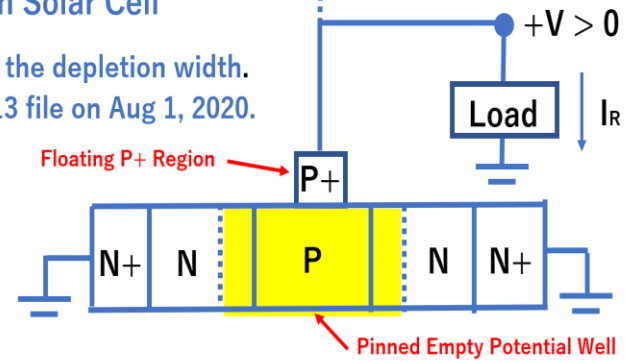


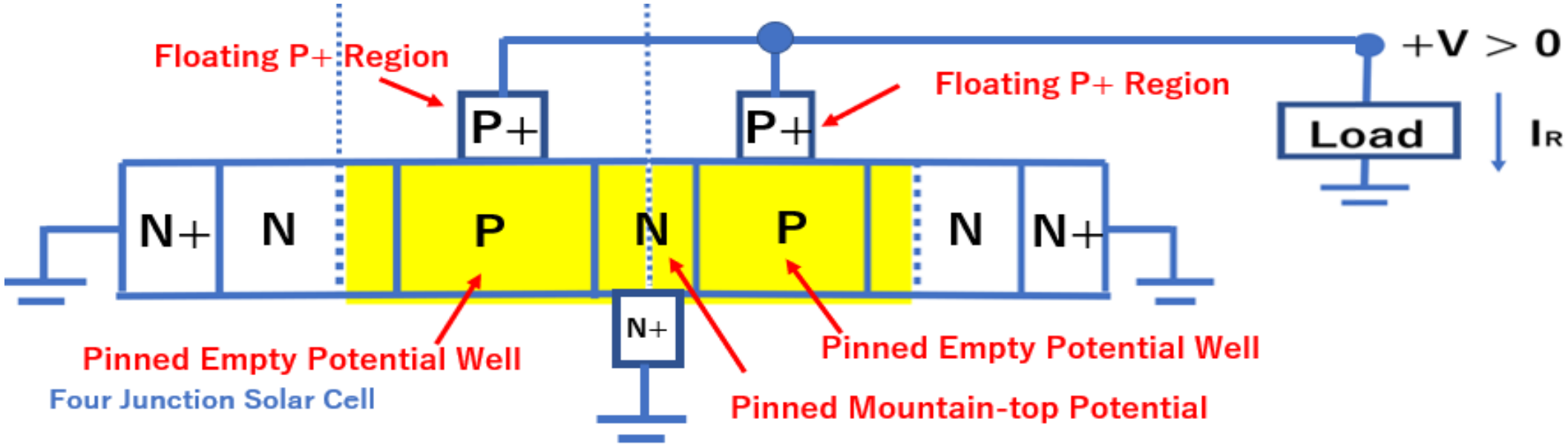
Single Junction Solar Cell



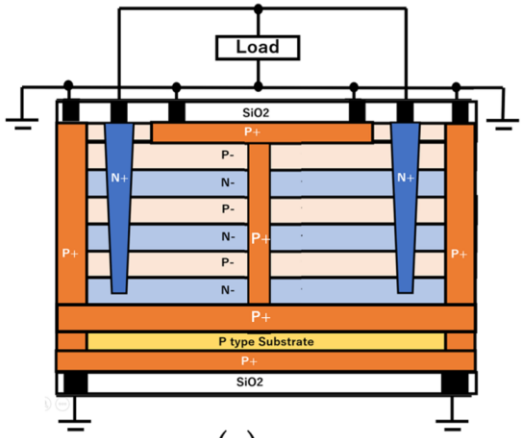
Double Junction Solar Cell

We can double the depletion width.
JPA2020-131313 file on Aug 1, 2020.



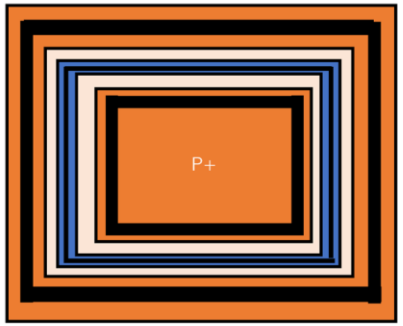


Multi-junction Solar Cell, based on JPA2020-131313 by Yoshiaki Hagiwara, applied on Aug. 1, 2020.



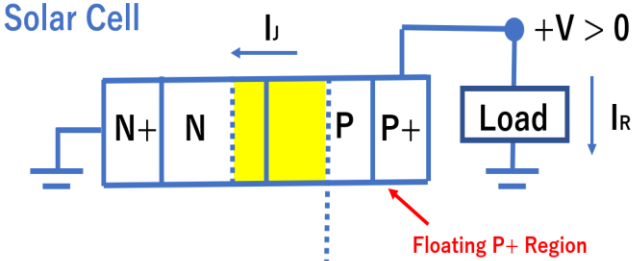
(a)

Top View



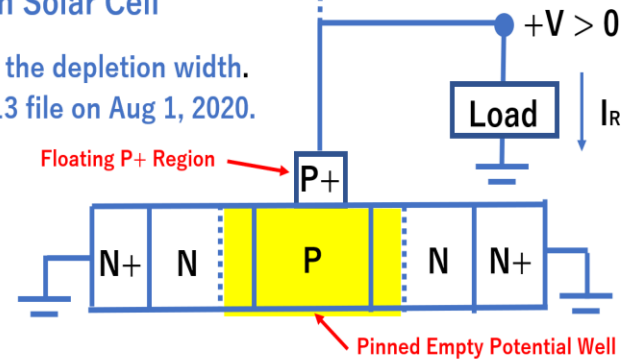
(b)

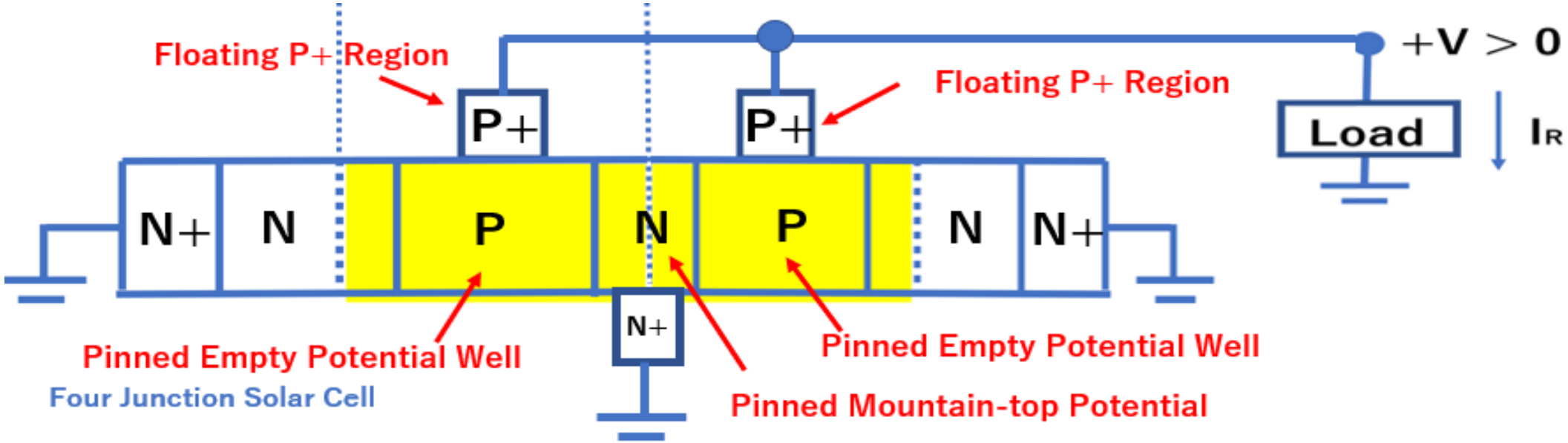
Single Junction Solar Cell



Double Junction Solar Cell

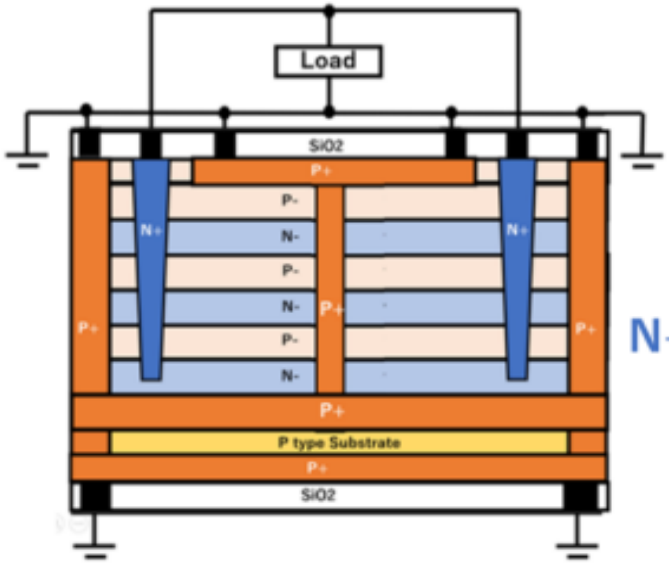
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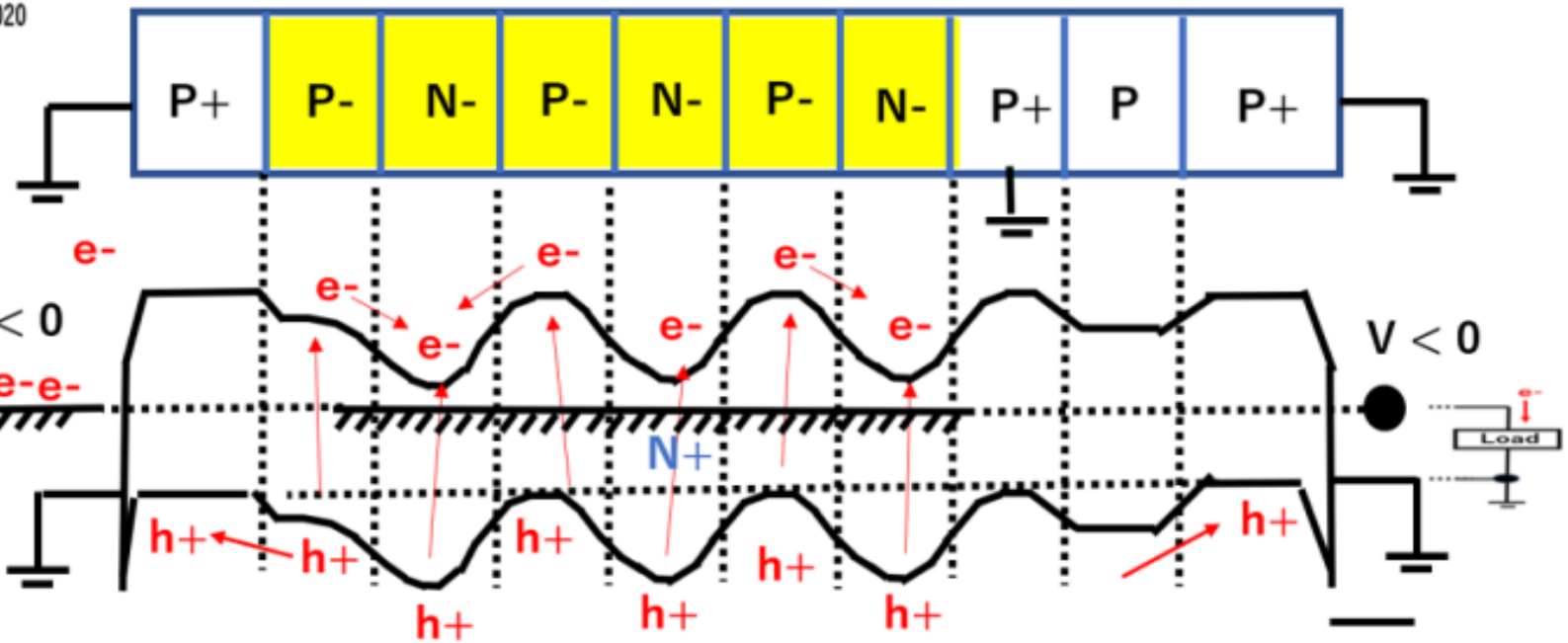


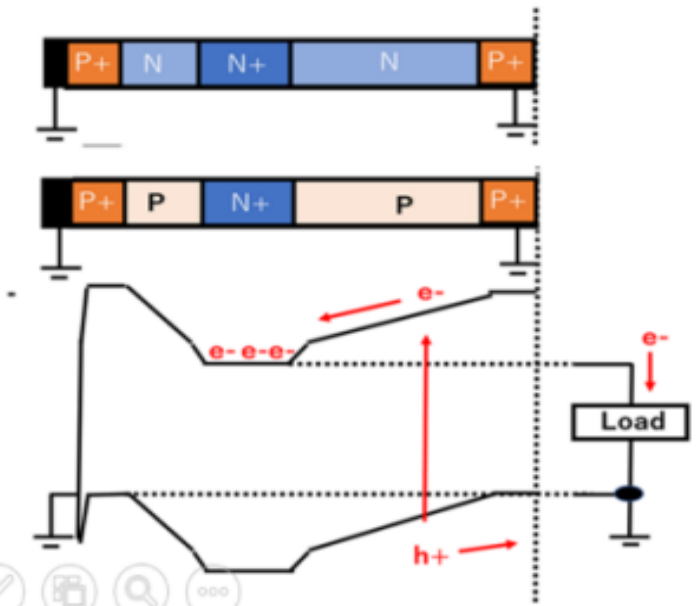


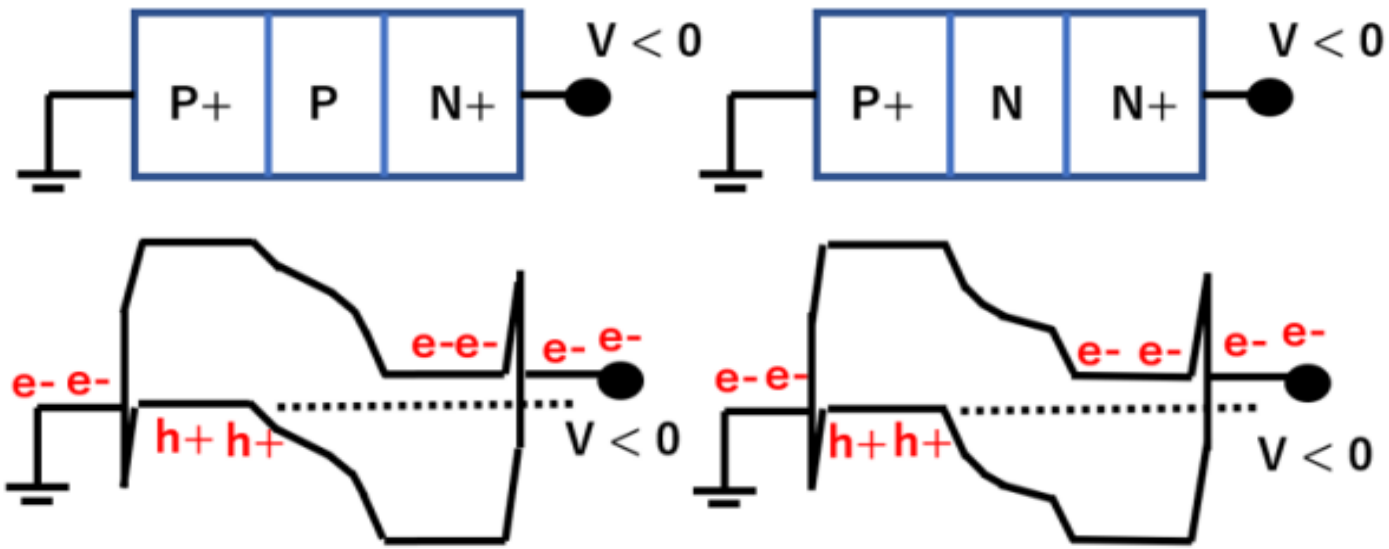
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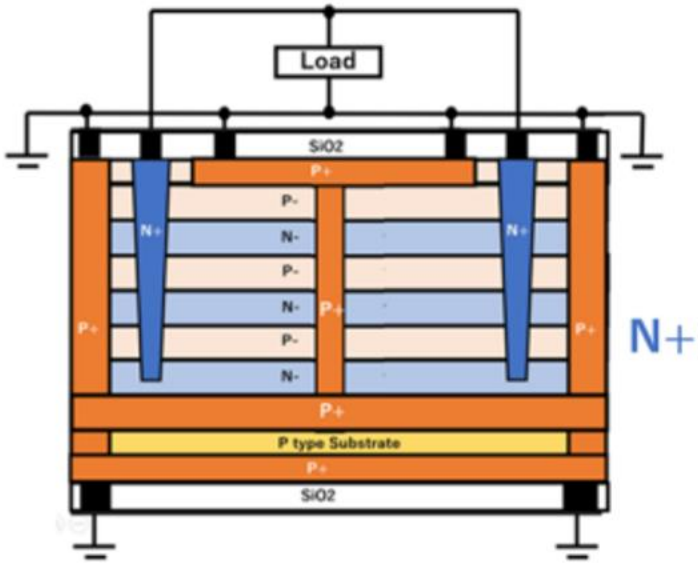


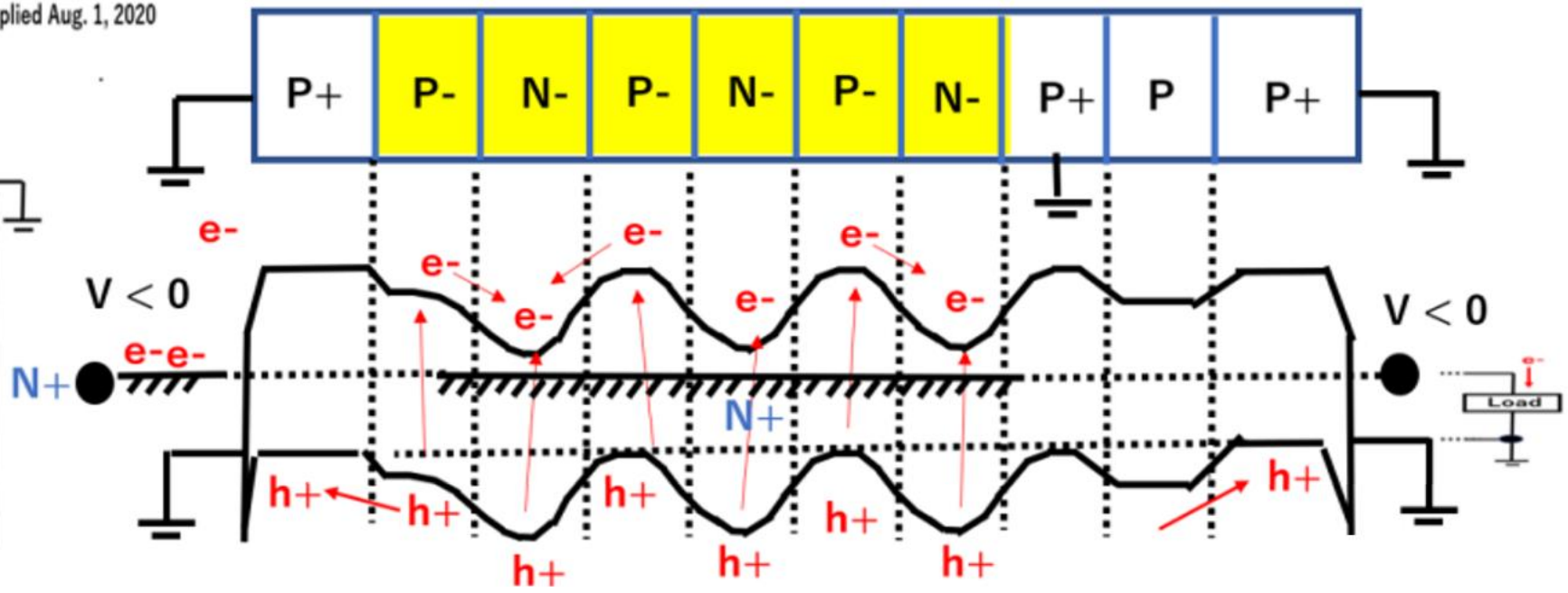


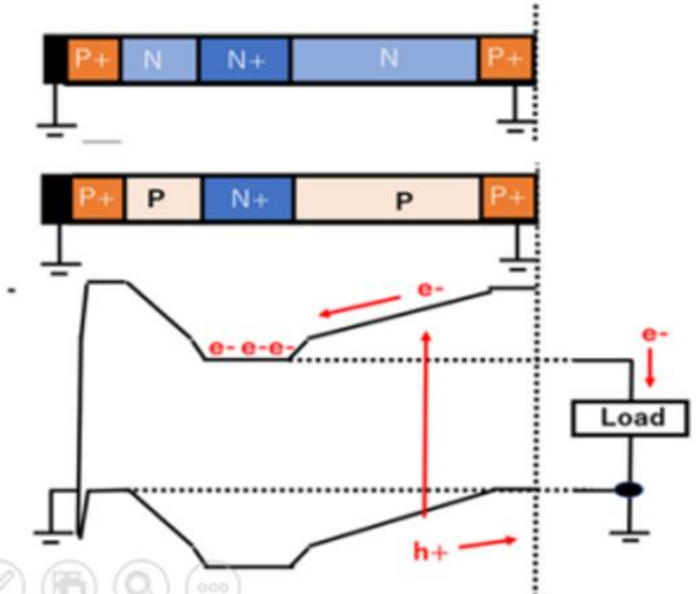


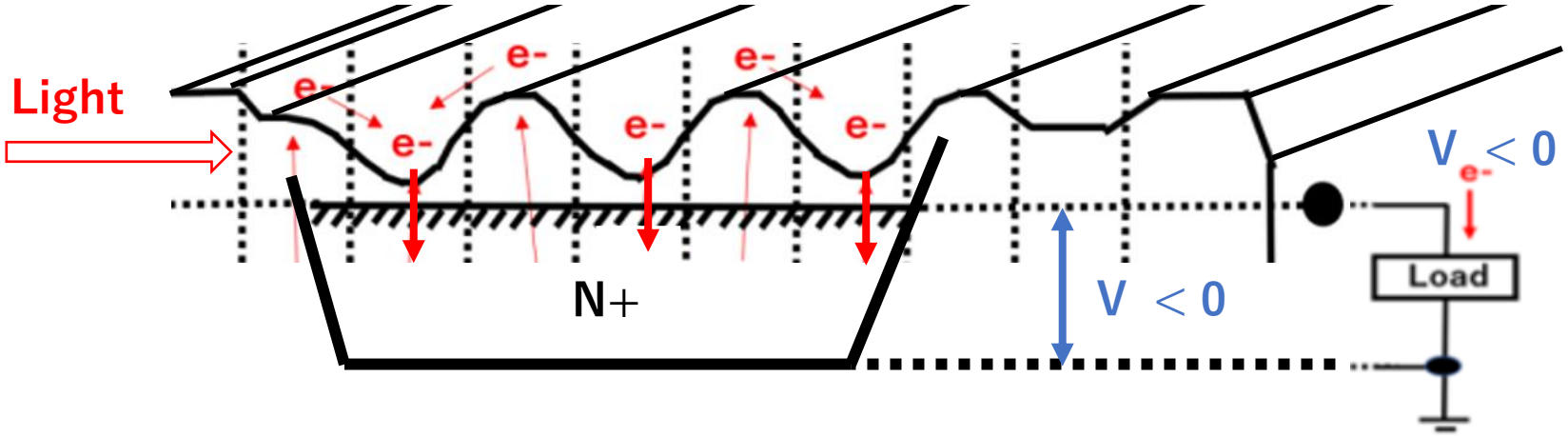
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いつもは神奈川県厚木市の郊外はるか北部のゴルフ場のそばの森林地帯に囲まれた自宅で、野山を散歩して老後をのんびり暮らしています。しかし、コロナ禍で孫にも会わず、妻と12歳のメス猫と一緒に静かに生活し、毎日が日曜日で過ごしています。



自分の1975年の発明が盗まれていることも知らず、実は2017年にNECの寺西さんが英国女王賞を受賞したいたことも知らず、毎日、鉄腕アトムをどうしたら造れるかと考え、没頭していました。今もその夢を追っています。鉄腕アトムに車をつければ自動走行車です。



SONYには「鉄腕アトムを造りたい」と思い最初に入社しました。
その夢を今もSONYの後輩たちが継承してくれて夢を追っている
元気な姿を見てたいへん喜んでいます。萩原が現役時代にイメージ
センサーを担当したのは１９７５年から１９８１年の間だけでした。

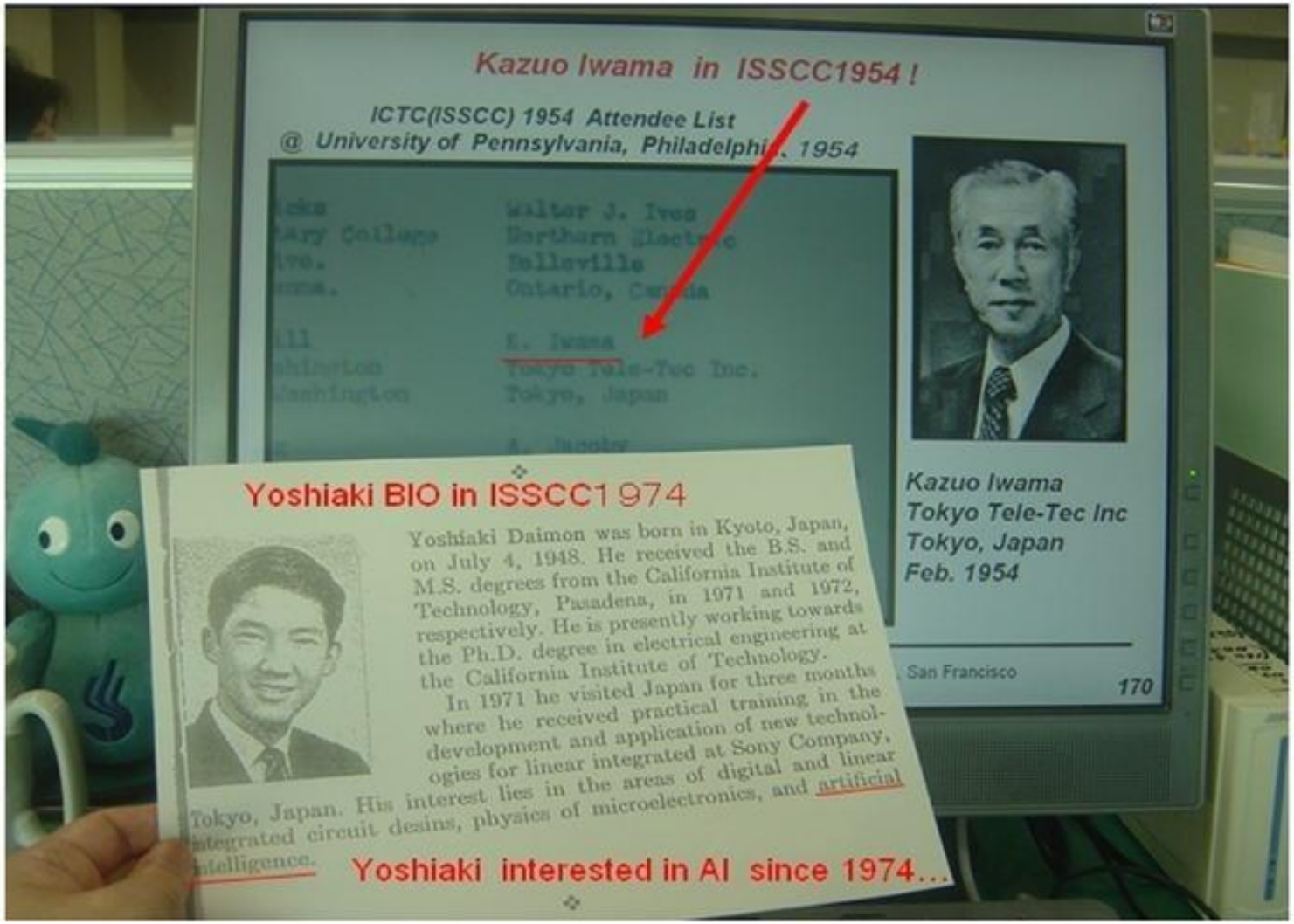
岩間 和夫（1919年2月7日 - 1982年8月24日）
日本の技術者、経営者、実業家である。
第4代ソニー社長。トランジスタに着目し、
日本における半導体産業の基盤を創った。





ISSCC1954 の国際会議に初めて岩間さんは東洋人として出席した技術者です。その20年後の 1974年2月には萩原良昭は 国際学会の SSCC1974にて PhD 学生論文を発表。



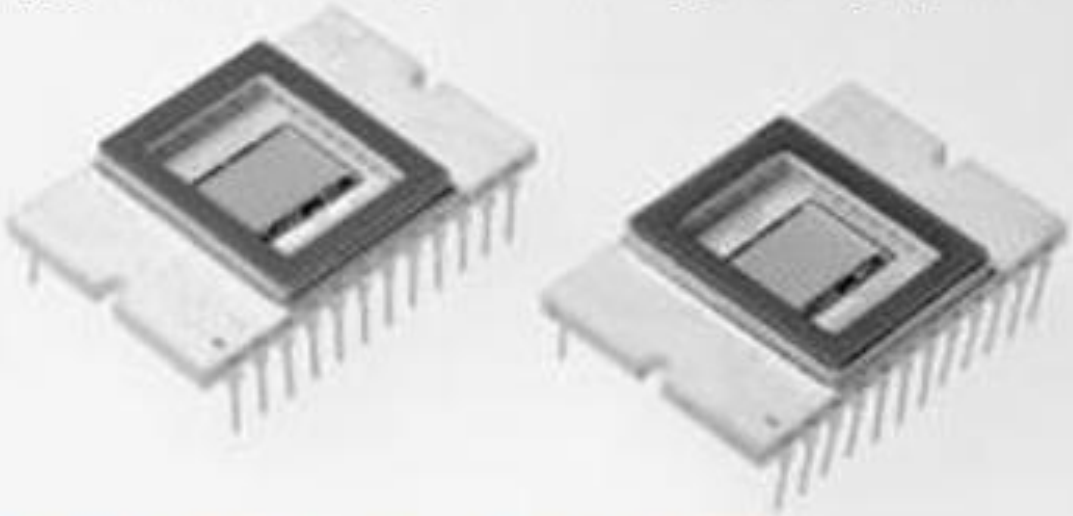


Computer数値計算を駆使し、埋め込み型CCDのデイバス回路モデル解析結果を報告しました。
埋め込み型CCDの将来展望を説明し、高感度ビデオカメラへの応用があることに注目しました。
電子の目として期待が大きかった夢ある時代でした。その論文に注目してくれた人々の中には、
SONYの岩間和夫氏もいました。1974年当時SONY本社の副社長で SONY USAの会長でした。

ＣＣＤ撮像素子（ICX008）

SONYが初めて1980 年商品化した国産の CCD Image Sensorです。
日本発明協会公式WEBでも掲載していただいております(笑顔)。

http://koueki.jiii.or.jp/innovation100/innovation_detail.php?eid=00059&test=open&age



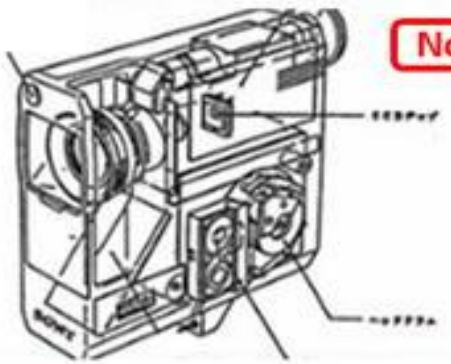
「高密度インターライン転送方式CCD撮像素子」
岡田静夫、島田孝、松本博行、
安藤哲雄、狩野靖夫、桑沢哲郎、萩原良昭
Japan SSD Conferenc , DDD78-5, May , 1978.

（画像提供：ソニー）

SONY HAD (Pinned Photodiode) Publications at the International Solid State Device Conference in 1978 and the Tokyo & New York SONY Press Conference in 1980

The original Pinned Photodiode (PPD) structure was invented by Hagiwara at Sony in 1975. The first one-chip color video camera with a FT CCD image sensor with P+NP junction type Pinned Photodiode (PPD) was reported by Sony in 1980 at Tokyo Press Conference by Iwama Kazuo of Sony president, and at New York Press conference by Morita Akio of Sony chairman.

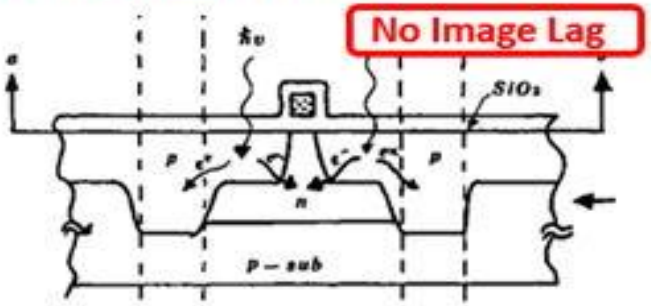
Sony original 570H x 498 V one-chip FT CCD Image Sensor with Pinned Photodiode, July 1980



No Image Lag



P+NP Junction Pinned Photodiode



On July 1980, Iwama Kazuo at Sony Tokyo Press Conference and Morita Akio at New York Press Conference announced the one chip CCD video camera with the 8 mm VTR in one box.

See the Original 1978 Publication of the Pinned Photodiode Sensor

Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488V CCD imager with narrow channel transfer gates," Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Appllied Physics , vol. 18, supplement 18–1, pp. 335–340, 1979

High quality picture of SONY CMOS Imager is also based on SONY HAD (Pinned Photodiode).

1975-1982 Engineer in CCD Imagers and Camera System
1983-1989 Engineering Manager in SRAM/DRAM/ADC
1990-1998 General manager in Sony /NVM/MCU/PS1
1998-2008 Executive Staff Sony Semiconductor
Strategic Planning PS2/PS3



IEEE Computer Elemets Workshop
@ Vail, Colorado, 1995

Mitsuo Saito（Toshiba)

Bob Guensey（IBM)

Ken Kutaragi

Yoshiiaki Hagihara

特別セッション(6):未来の生活を変えるAIPSロボティクス[Artificial Intelligent Partner System]～未来の生活を変えるメカエレキソフトの融合技術～

パネル討論　「未来の生活を変えるAIPSロボティクス」

基調講演　　「コンピュータ・エンタテインメント＋AIPSの可能性」



PlayStation　久夛良木 健

パネル討論「未来の生活を変えるAIPSロボティクス」
3月12日(木)15:20-16:20[第1イベント会場(プリズムハウス　1F　プリズムホール)]

[討論概要]
近年では，二足歩行ロボットによるサッカー大会が開催され，またITによる自動車の運転補助が実用化するなど，ロボティクス技術，及びイメージング[illegible]は各家庭にもゲームに代表されるコンピュ[illegible]分野とロボット技術が融合し，Real Timeで[illegible]話もするパートナー・システム(PS)としての[illegible]本パネル討論では我々の未来の[illegible]ともに，その実現の為の要素技術とは何か[illegible]割りつつ，具体的にはREAL TIMEでの音声[illegible]の紹介や将来へ向けての研究課題について[illegible]

電子情報通信学会全国大会
@立命会館草津キャンパス
2009年3月



司会:萩原　良昭(AIPSコンソーシアム)
1971年米国カリフォルニア工科大学卒業．1975年6月同大学博士課程卒業(主:電子工学，副:物理学)．
1975年2月ソニー入社．固体撮像素子とそのカメラシステム，ADC，メモリチップ，MCUマイコン，システムLSIの開発事業化担当．主幹技師，半導体技術企画室長などを歴任．2008年7月，60歳定年退職．
2008年8月神奈川県庁認定(NPO法人)AIPSコンソーシアム設立．その理事長に就任，現在に至る．

Prof. Yoshiaki Hagiwara talks on Fuji TV, March 24, 2013

崇城大学　萩原良昭教授　「自動走行車は可能！」



https://www.sojo-u.ac.jp/　　hagiwara@ofc.sojo-u.ac.jp

"I wish to have Artificial Intelligent Self-Driving Car in 2033 at age 85.."

旧半導体産業新聞

電子デバイス産業新聞 | 商業施設新聞 | 工場計画情報 | 医療産業情報

電子デバイス産業新聞 電子版 21年10月1日 サービス開始
Electronic Device Industry News

ボロボロになった取材ノートは語る
～半導体業界最古参記者　泉谷渉の独り言～

Oct 13, 2020

第408回

「鉄腕アトムを創りたい」という男が画像の新世界を切り開く

元ソニーの萩原良昭氏が開発したPPDは超優れものデバイス

2020/11/13

「鉄腕アトムを創りたいというのが、ソニーに入社した動機であった。そしてまた、みんなが夢を共有していくというソニーの基本哲学は、自分にマッチングしていると考えた。IEEE主催の国際固体集積回路会議（ISSCC）の委員長をやらせていただくなど活躍の場を与えられ、今でもソニーには感謝している」（萩原氏）



ソニーの半導体で活躍した萩原良昭氏

Sangyo-Times.jp/article_ID=5331_(html)

https://www.seizansha.co.jp/



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デジタル回路の世界

IEEE Life Fellow, Ph.D.

萩原 良昭 著

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未来の人間社会には人工知能パートナーシステム(AIPS)とも言える人間にやさしい支援システムが出現すると期待している。AIPS搭載の自動走行車や老人介護システム、人間型歩行ロボットやロボット・ハウスなどである。そこで本書では、そのAIPSを支える「デジタル回路の世界」と題し、ハードとソフトの両面で、人とコンピュータをつなぐデジタル技術について紹介している。図や絵をたくさん用意して、基礎からやさしく解説している。

Invention and Historical Development Efforts of Pinned Photodiode and Electric Shutter

2019



Hagiwara at Sony Kumamoto Tech Center
in 2017, 2019 and 2022.

2001



1. Introduction
2. Patent Wars on Pinned Photodiode

1980



1996



Hagiwara also visited Sony Atsugi-Tech Center in July 2020.

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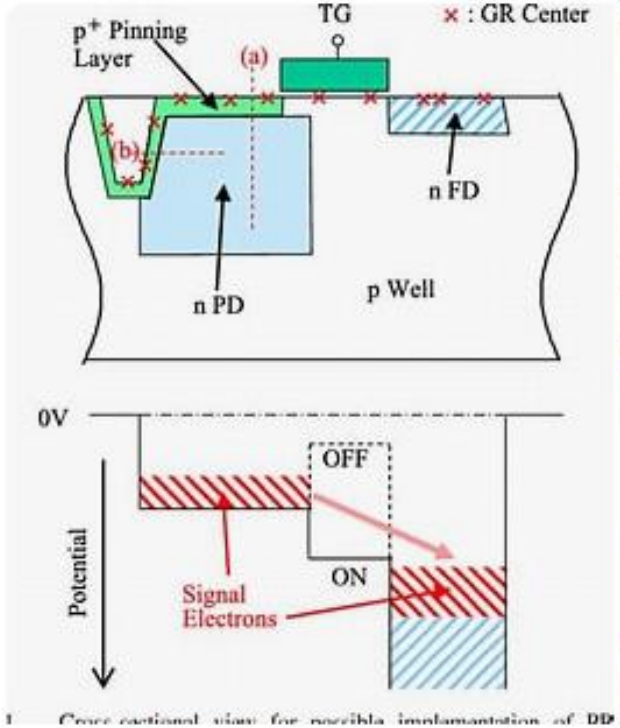


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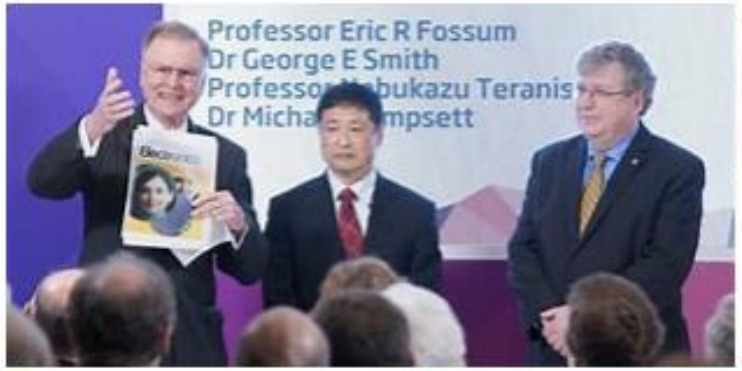
Queen Elizabeth Pinned Photodiode Invention



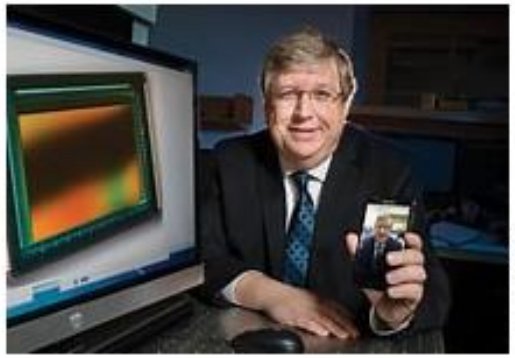


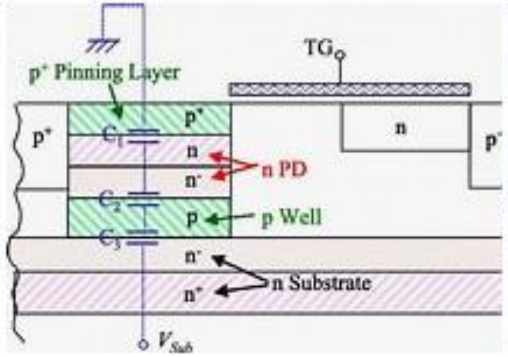
















http://koueki.jiii.or.jp/innovation100/innovation_detail.php?eid=00059&test=open&age=stable-growth

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（画像提供：ソニー）

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2017年にNECの寺西さんが英国女王賞を受賞したいたことも知らず、
鉄腕アトムをどうしたら造れるかと没頭していました。いまも
その夢を追っています。

国家戦略として、半導体電子産業の重要性を政府が見直しをかけており、
その波に萩原も乗ることができて、再び熊本にある崇城大学でこの４月
からは偉くなり理事長付きの特任教授として熊本県や日本政府の産業
開発推進組織と渡り合う立場になりました。１ヶ月に１週間ぐらい熊本
に滞在します。今回は、９月１９日～１０月１日の間熊本に滞在します。

清水さん、山口さん、慶児さんのご好意で今回は３回目の熊本テックの
訪問になります。若手社員への話す内容は、大学の授業と同じいもので
毎年同じものを授業で教えているのと同じで毎回同じお話ですが新しく
入学した若い学生や企業の新人社員には、はじめて聞く話でいつも新鮮
に受け留めてくれます。

半導体産業人協協会では、2017年４月から教育委員会のメンバーとして講師として奉仕していましたが、今年で引退して、後は奈良部さんに引き継いでもらう予定です。鈴木利治さんはずっと　CMOSプロセスの講師をしています。

2017年にNECの寺西さんが英国女王賞を受賞したことをずっと知らずに、自慢話を教材に入れて半導体っ産業人協会のセミナーの講師をしてのんびりと楽しんでいました。

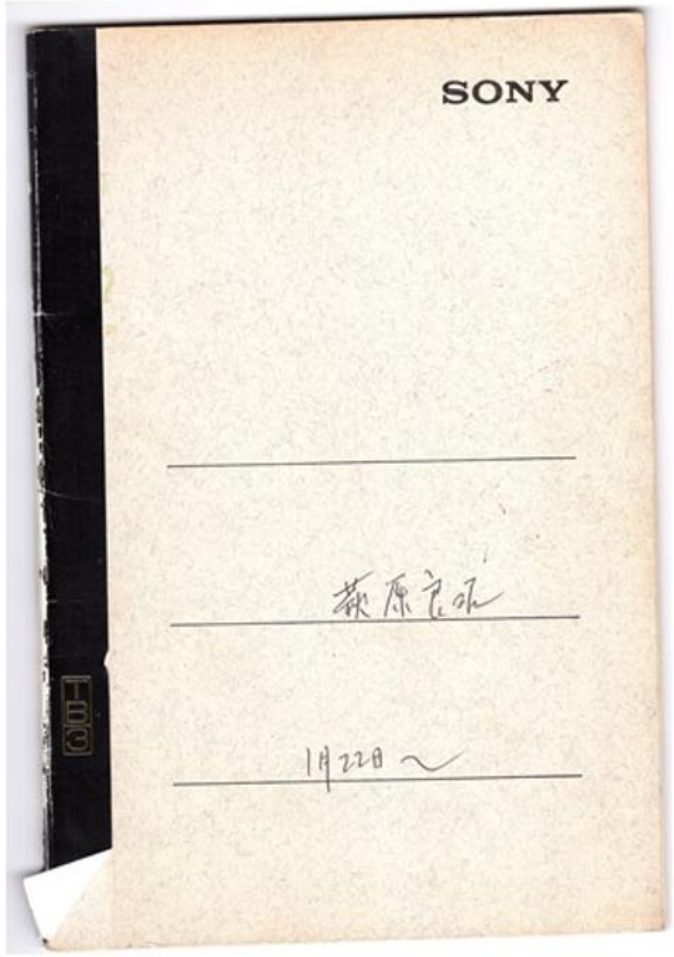
同じ講師の仲間で、SONY中研時代の先輩でもある、鈴木利治さんが、「あれはヒゲちゃんの発明だったのでは？」と教えてくれたのはそれから２年近くたってからでした。自分の発明が盗まれていることにびっくりでしたが。しかし、あとの祭りでした。

国内で特許を出願しても国際的には、発明者としてその証拠になります。
しかし、日本語で記載され、外国人には読めません。

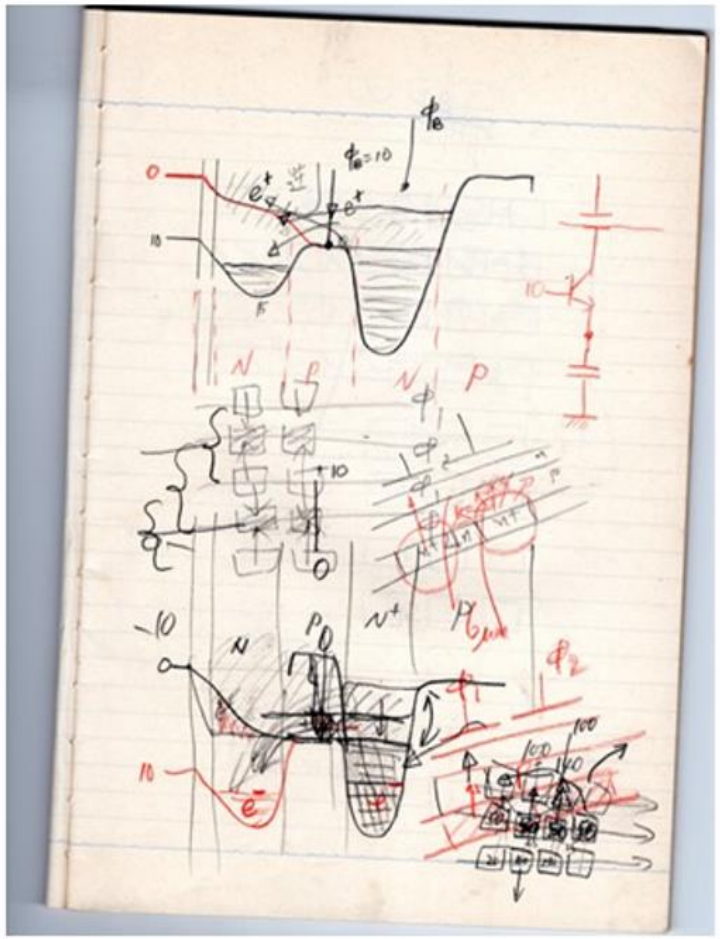
2018年の６月でした。その後奈良部さんたち厚木の後輩に萩原の発明が盗まれている事を説明し、厚木工場を訪問して理解をもとめました。
奈良部さんたちも知りびっくりです。特許というものは、上司と発明者以外は極秘扱いで他の技術者は通常誰がどんな特許を出願したか知りません。
奈良部さんたちが詳細を知らなくても当然でした。遠い昔の特許の詳細を萩原自身も忘れていました。国際会議でも発表などはした事はなく、その発明特許出願の存在が国際社会で知られていなくても当然でした。

SONYのHAD（Hole Accumulation Diode）の基本構造を定義した３件の出願特許（JPA1975-127646, JPA1975-127647, JPA1975-134985)とそれに使う電子シャッターのClock駆動方式の発明特許(JPA1977-126885)が重要な特許だったと判明し、その事実をSONYのTOPも知ったのはつい最近で、2020年６月26日にSONYは初めて萩原の発明だと公言しました。

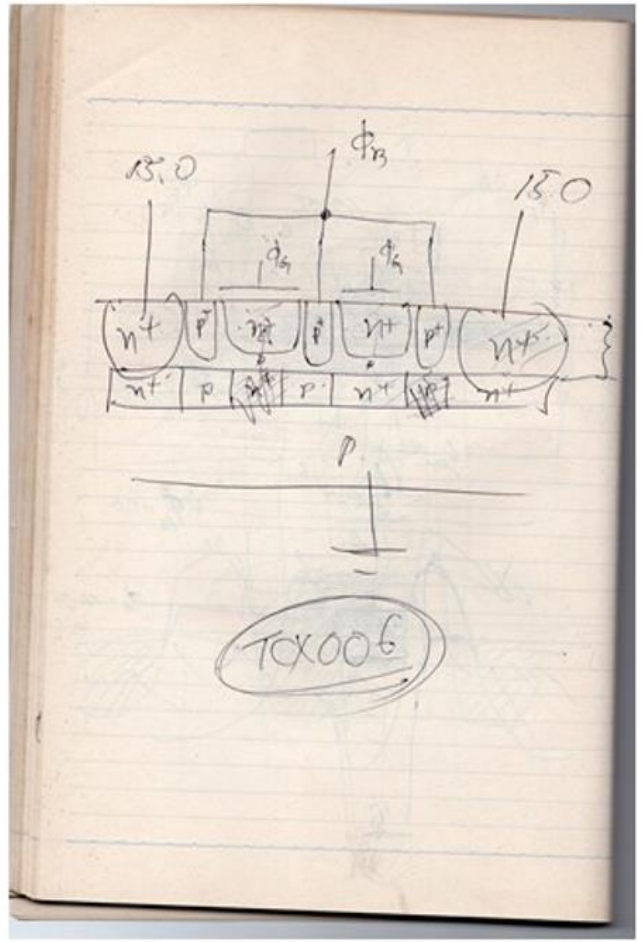
Hagiwara Lab Note Jan 22, 1976 at Sony Yokohama Central Research Lab.



Hagiwara Lab Note Jan 22, 1976



The first Sketch of
Pinned Buried Photodiode



Sony TCX006 Test Chip for
Back-Light Pinned Buried Photodiode

Basic Idea of JPA1975-127646 (Sony Top Secrets in late 1970s)

http://koueki.jiii.or.jp/innovation100/innovation_detail.php?eid=00059&test=open&age=stable-growth

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June 26, 2020

Sony's Representative Inventions Supporting Stacked Multi-Functional CMOS Image Sensors

Sony Corporation

Sony Semiconductor Solutions Corporation

Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

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ELECTRICAL ENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

Asked 8 years, 10 months ago Modified 2 years, 8 months ago Viewed 6k times

6

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

Share Cite Follow

edited Aug 16, 2018 at 19:17

answered Sep 21, 2013 at 14:34



placeholder

29.6k ● 10 ● 60 ● 110

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

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Pinned_Photodiode_Adopted_for_Back_Illuminated_CMOS_Image_Sensors

announce_in_public_by_Sony_on_2020_06_26

https://www.sony.com/en/SonyInfo/News/notice/20200626/

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Japanese Patent No. 1215101（Japanese Patent Application 1975-134985） by Yoshiaki Hagiwara

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https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

Semiconductor History Museum of Japan

1975-85

Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

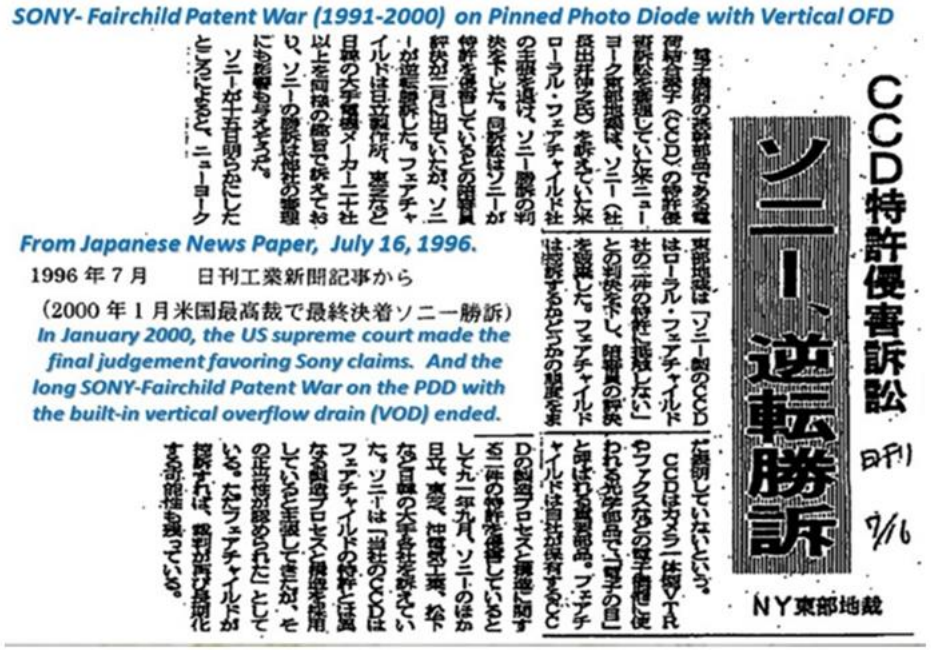
~ Discrete Semiconductor/Others ~

Semiconductor History Museum of Japan says that Hagiwara invented Pinned Photodiode.

In 1975, Sony proposed using a PNP transistor as the photodetector [3]. By providing a P^+ layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated to improve the light sensitivity greatly. It was a basic proposal for a pinned photodiode with a P^+ layer on the surface of the light receiving part.

【3】Y. Hagiwara, Japanese Patent JP1975—134985

SONY- Fairchild Patent War (1991-2000) on Pinned Photo Diode with Vertical OFD



CCD特許侵害訴訟

ソニー、逆転勝訴

NY東部地裁

From Japanese News Paper, July 16, 1996.

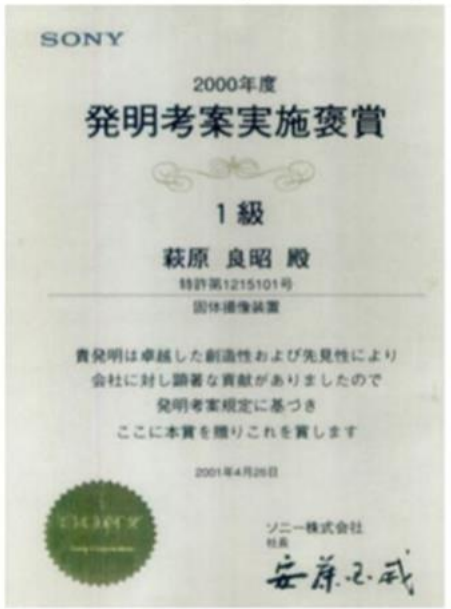
1996 年 7 月　日刊工業新聞記事から

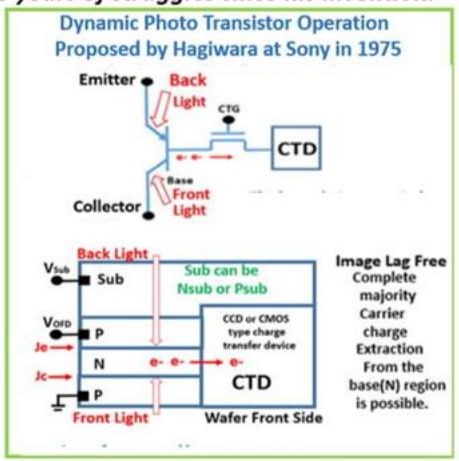
（2000 年 1 月米国最高裁で最終決着ソニー勝訴）

In January 2000, the US supreme court made the final judgement favoring Sony claims. And the long SONY-Fairchild Patent War on the PDD with the built-in vertical overflow drain (VOD) ended.

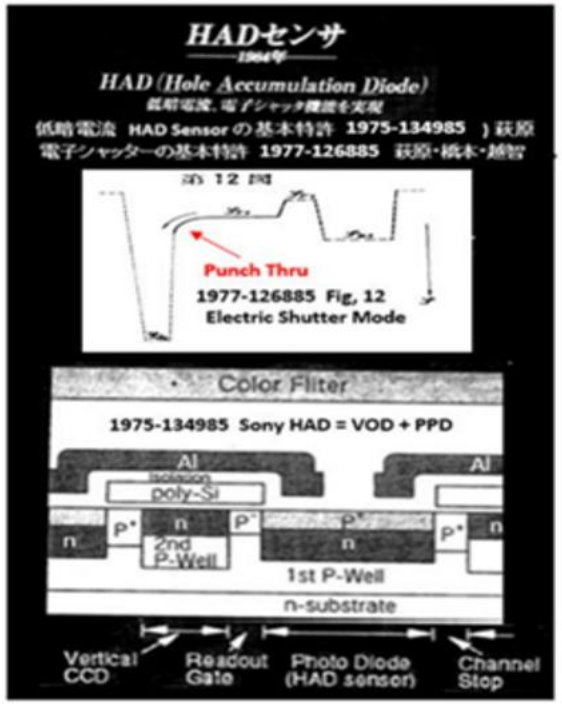
Finally the Sony-Fairchild Patent Wat(1991-2000) ended over the Sony HAD Sensor which is identical to the P+NPNsub junction type Pinned Photodiode with Vertical Overflow Drain, originally invented by Hagiwara at Sony in 1975.

And finally Hagiwara received for his 1975-134985 Japanese Patent officially , the First Patent Award from Mr. Ando, Sony president in April, 2001 after more 26 years of struggles since his invention.





Hagiwara also proposed the thyristor type punch-thru clocking scheme, synchronized with the TV scanning system to achieve the electric shutter.



Electric Shutter Basic Patent Award from Sony President Idei to Yoshiaki Hagiwara for Japanese Patent 1977-126885 by Hagiwara



Four Japanese Patent Applications on Pinned Photodiode with Electric Shutter Function and the in-Pixel Global Shutter MOS/CCD Buffer Memory Function for Modern CMOS Image Sensors.

Japanese Patent Application JPA1975-127646

Japanese Patent Application JPA1975-127647

Japanese Patent Application JPA1975-134985

Japanese Patent Application JPA1977-126885

The first Pinned Photodiode papers in 1977 and 1978 by Hagiwara at Sony

P1977_Narrow_Cahnnel_Transfer_Gate_CCD_SSDM1977_Paper_by_Hagiwara.pdf"

Hagiwara_SSDM1978_Paper_on_Pinned_Buried_Photodiode.pdf

Five Recently Published Papers by Hagiwara(AIPS)

P2019_3DIC2019_Paper_on_3D_Pinned_Photodiode_6_pages.pdf

EDTM2020 Conference Paper_ID_3C4_by_Hagiwara(PDF)

IJSSM2021 e-Journal Paper on Pinned Photodiode.html

ICECET2021_Paper61.pdf

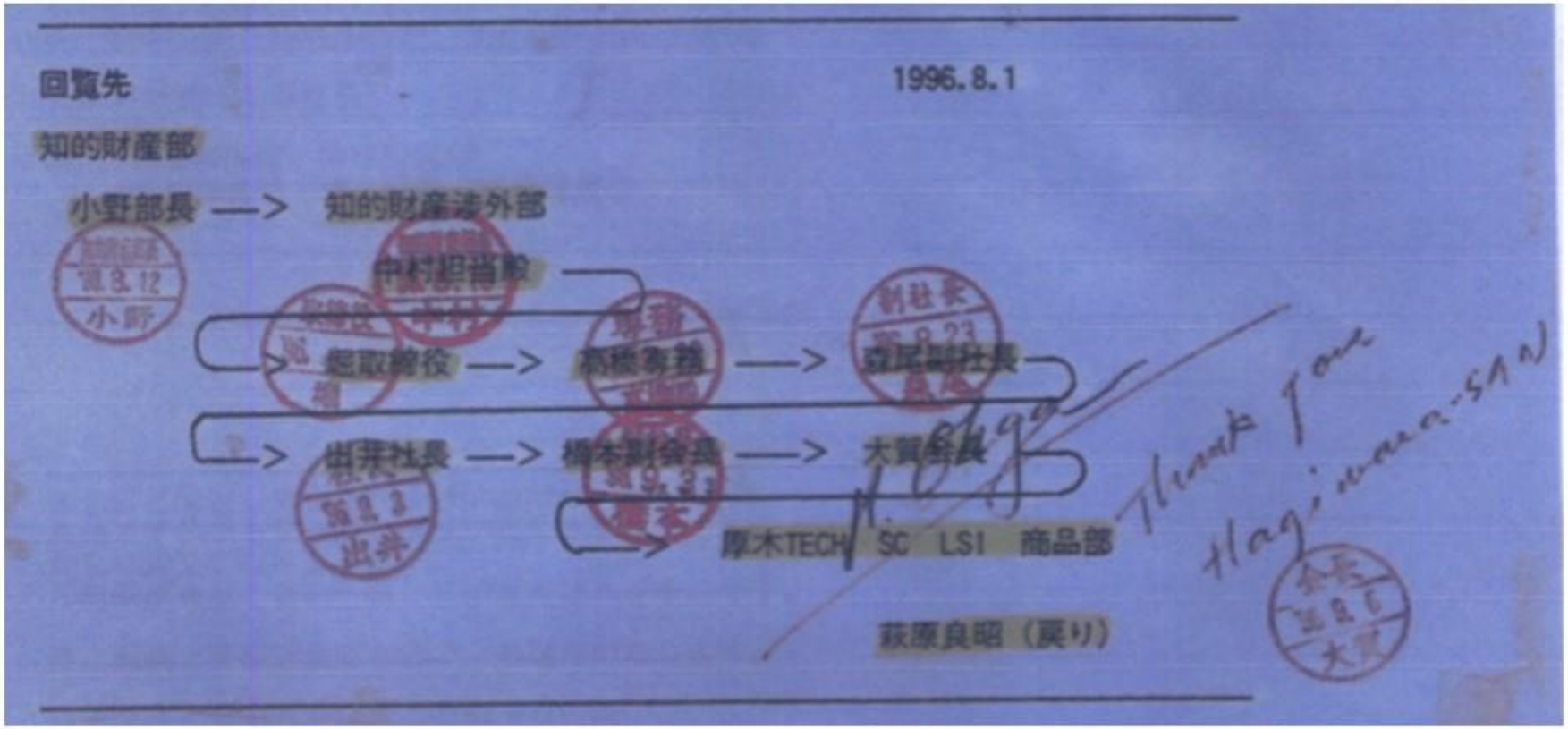
ICECET2021_Paper75.pdf

SONY―Fairchild 社の特許戦争の終結は、SONYの勝利に終わった。

萩原は　別にSONYからお金をもらってやったわけでない。

世界の半導体大手のFairchild 社から萩原の1975 年特許が攻撃され、それを発明者である萩原が、自分の名誉を守るために、世界に訴え、萩原が自発的に行動に出た結果である。

当時のSONYの大賀会長、橋本副会長、出井社長からねぎらいの言葉を萩原はもらった。





１９８２年からはデジカメ用に不可欠な高速４ＭビットのCache SRAMの商品開発を担当しました。１９８９年のＩＳＳＣＣで世界最高速　25nsecの４ＭＳＲＡＭの開発に成功し学会に発表。ＳＲＡＭ事業部の大きな宣伝にもなり大賀社長からＣＥＯを受賞。



1975年に萩原が発明したPNPN接合型のHADセンサーは電子シャッターを可能にする受光素子でしたが、その実用化には石川さんたち後輩のさらなる発明と開発努力が必要でした。その後１２年もの年月の努力の結果、石川さんたちは１９８７年、電子シャッターの実用化商品化に成功し、SONYの市場制覇が始まり、その遺産が今も後輩に継承されています。



萩原が担当したのは、あくまで半導体電子デバイス部品の技術開発です。実際のAIBOロボットは土井さんが、Play Stationは久夛良木さんが陣頭指揮をとり開発部隊を指導していました。土井さんと久夛良木さんたちはあくまで私たちの製品のユーザー側です。われわれのお客さまでした。

https://en.wikipedia.org/wiki/Photodiode

Pinned photodiode [edit]

Not to be confused with PIN photodiode.

The pinned photodiode (PPD) has a shallow implant (P+ or N+) in N-type or P-type diffusion layer, respectively, over a P-type or N-type (respectively) substrate layer, such that the intermediate diffusion layer can be fully depleted of majority carries, like the base region of a bipolar junction transistor. The PPD (usually PNP) is used in CMOS active-pixel sensors; a precursor NPN variant with a clocked top N layer was invented at Sony in 1975 for use in CCD image sensors.

Early charge-coupled device image sensors suffered from shutter lag. This was largely resolved with the invention of the pinned photodiode.[21] It was invented by Nobukazu Teranishi, Hiromitsu Shiraki and Yasuo Ishihara at NEC in 1980.[21][22] They recognized that lag can be eliminated if the signal carriers could be transferred from the photodiode to the CCD. This led to their invention of the pinned photodiode, a photodetector structure with low lag, low noise, high quantum efficiency and low dark current.[21] It was first publicly reported by Teranishi and Ishihara with A. Kohono, E. Oda and K. Arai in 1982, with the addition of an anti-blooming structure.[21][23] The new photodetector structure invented at NEC was given the name "pinned photodiode" (PPD) by B.C. Burkey at Kodak in 1984. In 1987, the PPD began to be incorporated into most CCD sensors, becoming a fixture in consumer electronic video cameras and then digital still cameras.[21]

In 1994, Eric Fossum, while working at NASA's Jet Propulsion Laboratory (JPL), proposed an improvement to the CMOS sensor: the integration of the pinned photodiode. A CMOS sensor with PPD technology was first fabricated in 1995 by a joint JPL and Kodak team that included Fossum along with P.P.K. Lee, R.C. Gee, R.M. Guidash and T.H. Lee. Since then, the PPD has been used in nearly all CMOS sensors. The CMOS sensor with PPD technology was further advanced and refined by R.M. Guidash in 1997, K. Yonemoto and H. Sumi in 2000, and I. Inoue in 2003. This led to CMOS sensors achieve imaging performance on par with CCD sensors, and later exceeding CCD sensors.[21]

On June 9, 1975 Philips invented Buried Photodiode with RC delay time (Netherland Patent 7506975)
On Oct 23, 1975Hagiwara at Sony invented Pinned Photodiode with the pinned surface and the complete charge transfer capability of no-image-lag feature, realize the Electric Shutter and Global Shutter.
In SSDM1978, Hagiwara team at Sony reported PNP junction type Pinned Photodiode with the complete charge transfer capability and the no-image-lag with the very low dark current and the defect-free feature
In IEDM1982, Teranishi team in NEC reported Buried Photodiode with Image Lag data.

True History of Photodiode

(1) Single Junction Type Dynamic Photodiode before 1970

(2) CCD/Mos type dynamic Photodiode invented in 1970

(3) Double Junction type Dynamic Photodiode invented by Philips in June 9, 1975

(4) Triple Junction type Dynamic Photodiode with the pinned surface invented by Sony in Oct 23, 1975.



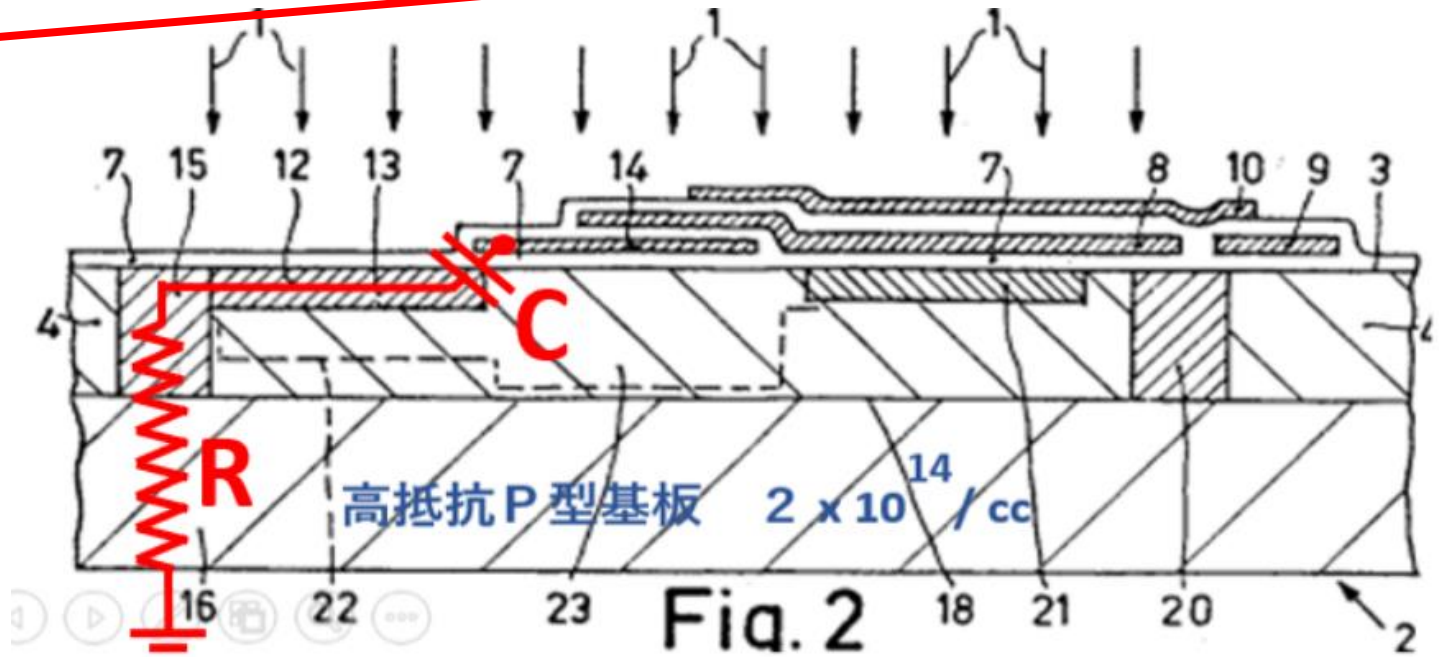


Fig. 2

JPA1976-150288(Netherland Patent 7506795, priority June 7, 1975)

https://ja.wikipedia.org/wiki/埋込フォトダイオード

埋込フォトダイオード – Wikipedia

埋込フォトダイオードとは、電荷蓄積部が半導体表面に露出し浮遊状態にある表面型受光素子に対して、電荷蓄積部が半導体表面には 露出されていない構造を持つ埋め込み型受光素子であり、NPN接合または PNP接合のトランジスタ構造を持つフォトダイオードのことである。 受光面に直接露出していないベース領域が埋め込み層として光電荷蓄積部となる構造を持つ。

埋込フォトダイオード（または埋め込みフォトダイオード）の構造や動作原理については多くの解説があるが、一例として「電子情報通信学会「知識ベース」8 群－4 編－1 章」のP46[1]などがある。

埋め込み型フォトダイオード [編集]

最初のNPNP接合型の埋め込みフォトダイオードは、1975年10月23日にソニーから特許出願が行われている。[2]

その構造は、コレクタ端子を受光面とし、エミッタ端子を過剰電荷の掃き出し端子とし、ベース領域を電荷蓄積部とするPNP接合のトランジスタ構造を示していた。 ベース領域に蓄積された信号電荷はリセット時に、隣接する電荷転送電極を通して受け皿となる電荷転送装置に信号電荷を転送するPNP接合、またはNPN接合のダイナミック・フォトトランジスタ構造をしていた。

1975年6月7日にはオランダのフィリップスが PNP接合型の埋め込みフォトダイオード受光素子構造をInterline Transfer (ILT)CCDイメージセンサ として考案しているが、これは表面がピン留めされていない埋め込みフォトダイオードであった。[3]

また、1980年10月2日にNECから出願された特許[4]でも同様の内容が提案されている。

https://ja.wikipedia.org/wiki/埋込フォトダイオード

埋込フォトダイオード – Wikipedia

Pinned Photodiode [編集]

Pinned Photodiode(PPD)はピン留めフォトダイオード[5] とも呼ばれる、埋め込み型フォトダイオードの一種で、受光面が外部電圧によりピン留め固定さ れた受光素子である。ピン留めされる事が残像のない受光素子として機能するために必要条件となる。

往々にして"PINダイオード (p-intrinsic-n Diode)"と混同されることがあるので注意が必要である。

Pinned Photodiodeは必ず埋め込み型フォトダイオードであるが、埋め込み型フォトダイオードは必ずしも Pinned Photodiode ではない。Pinned Photodiodeは必ず受光面の電圧が固定される必要があり、それが残像のない特性を実現する為の必要条件となる。

ソニーから1975年10月23日にソニーの萩原良昭により出願されたもう1件のNPN接合の発明特許 [6] と、その発展形として1975年11月10日に出願されたPNP接合の発明特許[7]の受光素子構造は、受光面の電圧がピン留め固定された Pinned Photodiode の発明であった。

ソニーのホームページにも「裏面照射型CMOSイメージセンサーに採用されたPinned Photodiode」[8] と題してCMOSイメージセンサーの発明の歴史がより詳細に解説されている。

また、「戦後日本のイノベーション100選」には「1979年には寺西信一（当時 ＮＥＣ）が、白傷や暗電流を大幅に低減し、残像や転送ノイズを解消する埋込フォトダイオード（Pinned Photodiode）を発明した」[9] と改良が進められてきた経緯が示されている。

Sonyの生産技術は世界一でNECよりはるかに先を行ったいたが、他社の追従を恐れ、学会発表の許可が出なかった。

IEDM1984 KODAK Paper

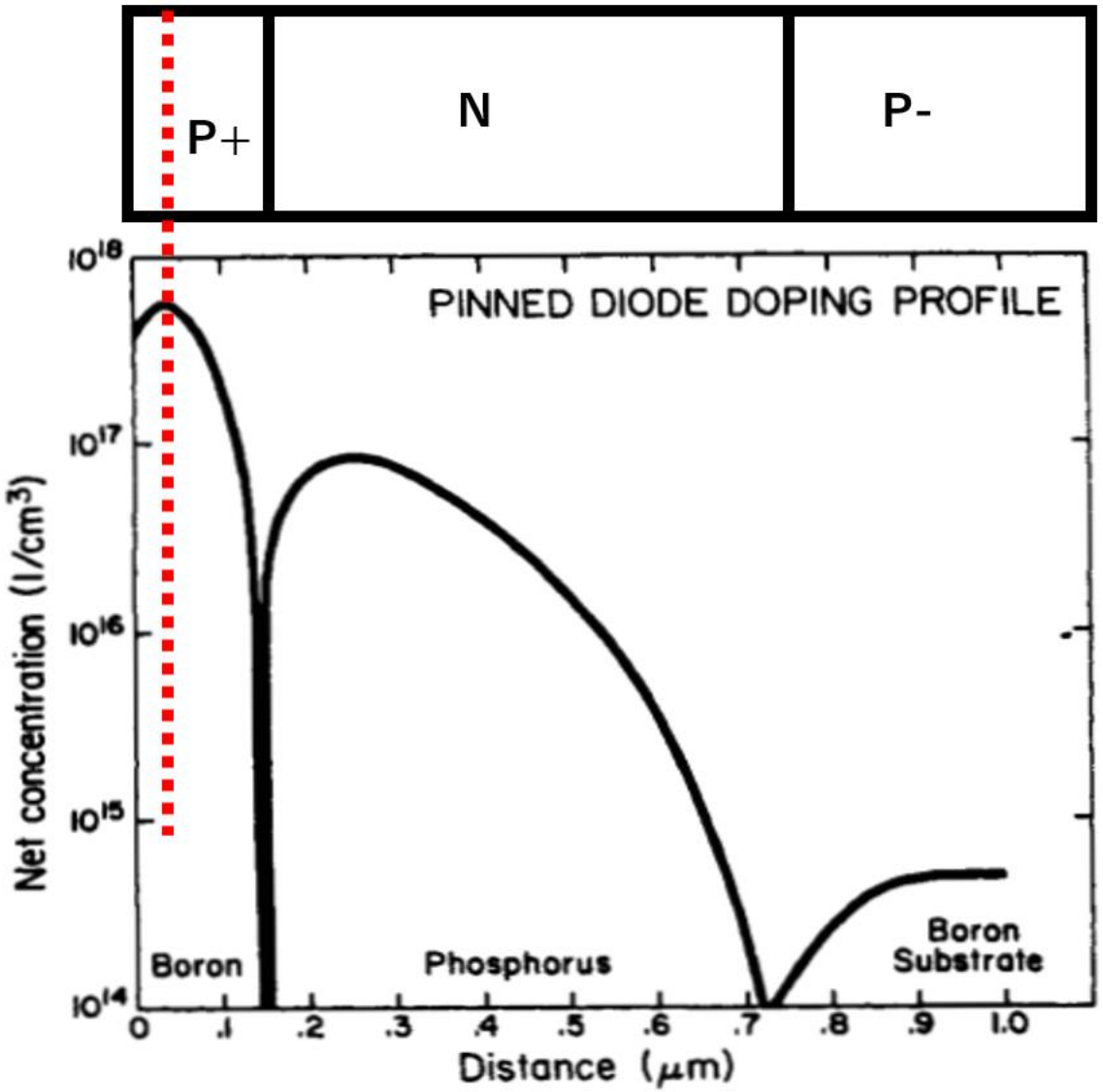


Fig. 2. Pinned diode doping profile.

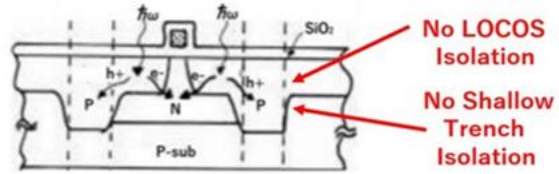
True Historv of Photodiode

First Pinned Photodiode was invented by Hagiwara in 1975 and reported at SSDM1978 by Sony.

Sony never used LOCOS isolation nor Shallow Trench Isolation. Both suffer the yield problem of Dark Current and White Defects. Instead, Sony used high energy ion implantation to form the adjacent heavily doped P+ channel stops region with the Lamp Anneal Technology invented by Kazuo Nishiyama at Sony.

(1) The first Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation invented and reported at SSDM1978 by Hagiwara.

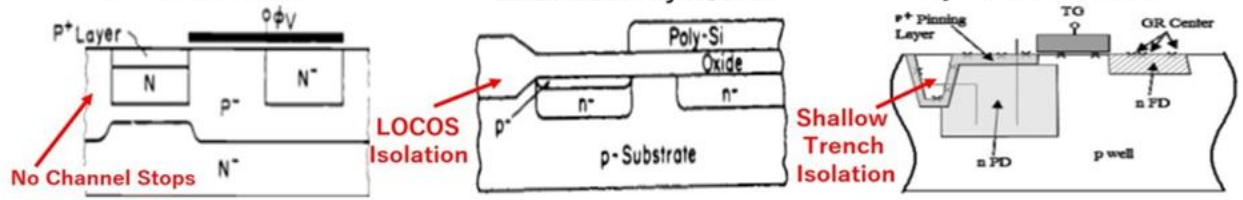
(2) Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation as explained by ssis.or.jp in the official Semiconductor History Museum WEB site.



(3) Buried Photodiode reported at IEDM1982 by NEC

(4) Pinned Photodiode reported at IEDM1984 by KODAK

(5) Pinned Photodiode reported by Teranishi in 2014



Sony Pinned Photodiode has the adjacent P+ heavily doped channel stops always directly grounded to the metal wire at the surface since 1978. Sony never used LOCOS isolation nor Shallow Trench Isolation.

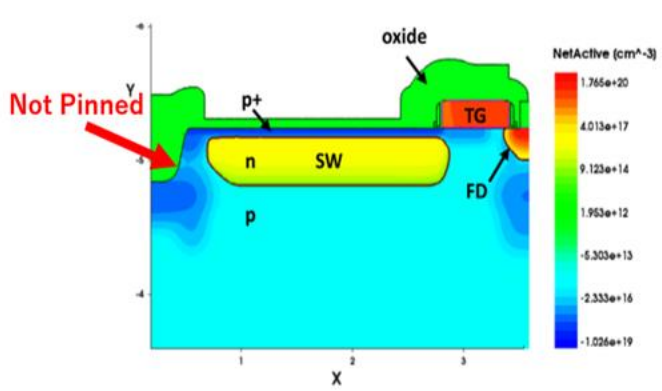


Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

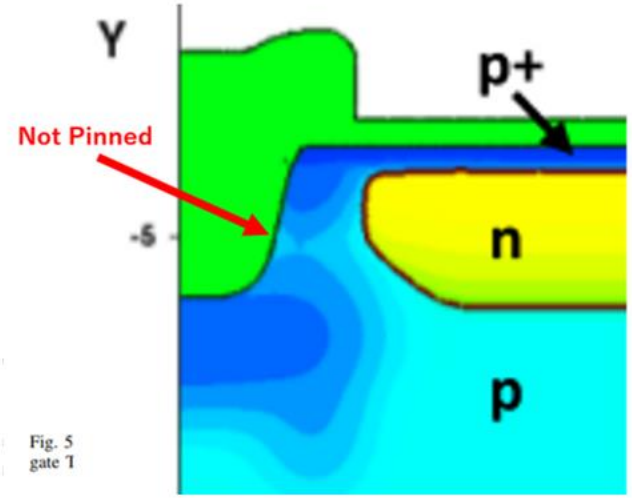


Fig. 5 gate T

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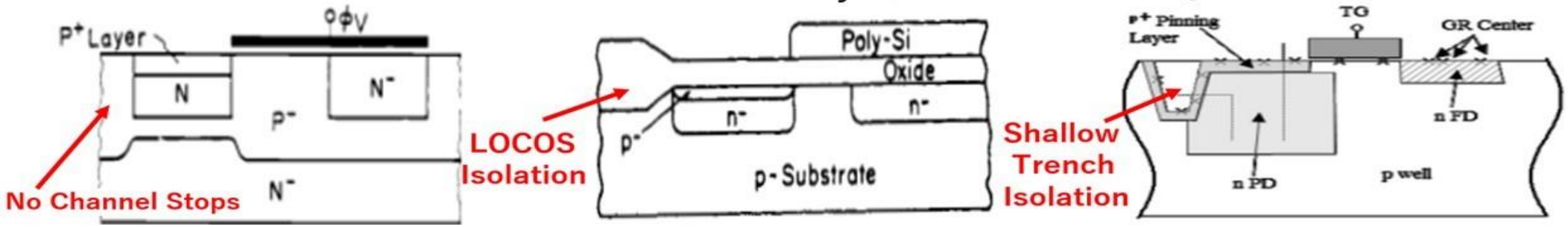
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ELECTRICAL ENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

Asked 8 years, 10 months ago Modified 2 years, 8 months ago Viewed 6k times

6

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

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edited Aug 16, 2018 at 19:17

answered Sep 21, 2013 at 14:34



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29.6k ● 10 ● 60 ● 110

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

Semiconductor History Museum of Japan

1975-85

Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

~ Discrete Semiconductor/Others ~

Semiconductor History Museum of Japan also says that Hagiwara invented PNP Pinned Photodiode in 1975.

In 1975, Sony proposed using a PNP transistor as the photodetector [3]. By providing a P^+ layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated to improve the light sensitivity greatly. It was a basic proposal for a pinned photodiode with a P^+ layer on the surface of the light receiving part.

【3】Y. Hagiwara, Japanese Patent JP1975—134985

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

Semiconductor History Museum of Japan

1975-85

Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

~ Discrete Semiconductor/Others ~

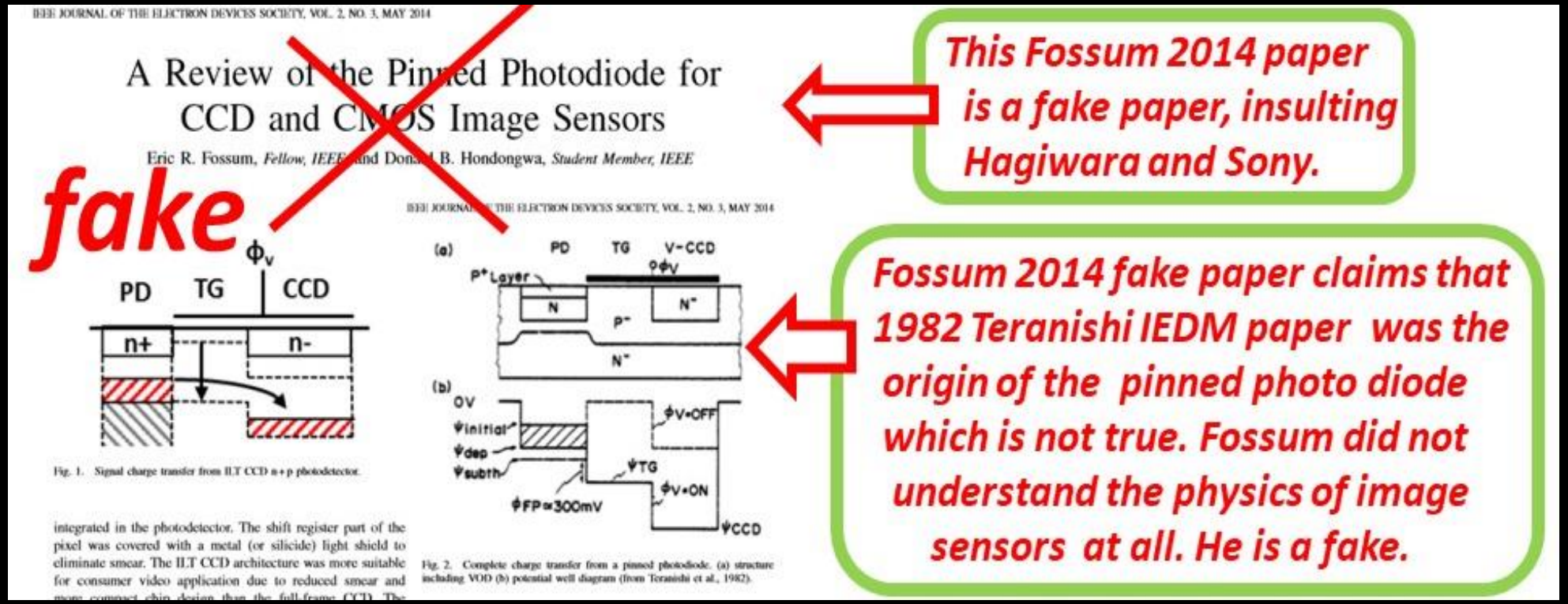
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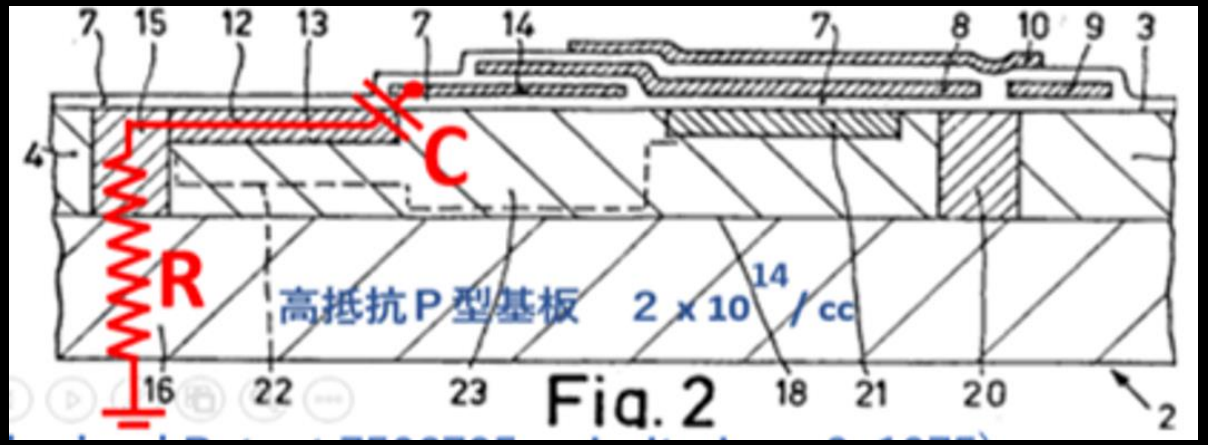
In 1978, Sony announced an FT (Frame Transfer) -CCD image sensor, using the photodiode with the same structure [5]. Sony succeeded for the first time in the world in prototyping a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor that developed this technology, in 1981 [6].

【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

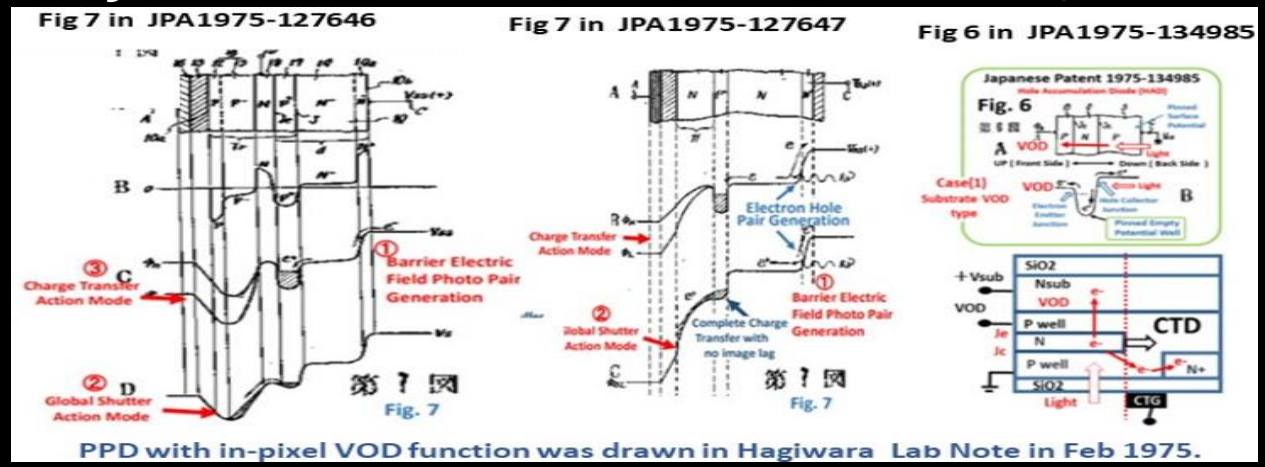
【6】I. Kajino, M. Shimada, Y. Nakada, Y. Hirata and Y. Hagiwara, "Single Chip Color Camera Using Narrow channel CCD Imager with Over Flow Drain"、Technical Report of The Institute of Image Information and Television Engineers、vol. 5, no. 29, pp. 32-3S, (1981)



Philips Buried Photodiode June 9, 1975



Sony Pinned Photodiode Oct 23～Nov 10, 1975



A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, *Fellow, IEEE,* and Donald B. Hondongwa, *Student Member, IEEE*

***Abstract*—The pinned photodiode is the primary photodetector structure used in most CCD and CMOS image sensors. This paper reviews the development, physics, and technology of the pinned photodiode.**

***Index Terms*—Charge-coupled device (CCD), CMOS active pixel image sensor (CIS), photodetector, pinned photodiode (PPD), pixel.**

I. Introduction

THE "pinned photodiode" is a photodetector structure used in almost all charge-coupled device (CCD) and CMOS image sensors (CIS) due to its low noise, high quantum efficiency and low dark current. We found that a comprehensive review paper on this device structure was needed in the literature. In this paper we will review the history of the pinned photodiode development, discuss the physics of its operation, briefly discuss its fabrication, and review its application.

The photocurrent depends on the wavelength-dependent photon flux $\phi(\lambda)$ incident on the semiconductor and the wavelength-dependent quantum efficiency $\eta(\lambda)$ which accounts for optical reflection, absorption and carrier collection:

$$I_{ph} = q \int_{\lambda} \phi(\lambda) . \eta(\lambda) \, d\lambda \tag{2}$$

The integrating photodiode was the basis for the earliest MOS passive pixel sensors (PPS) [5].

In 1968, Nobel at Plessey proposed a buried photodiode-structure for MOS PPS to reduce dark current (the collected signal in the dark due to thermal generation and diffusion) and to improve the packing density of pixels [6]. (A more modern-looking buried photodiode was proposed by Koike at Hitachi in 1977 to increase photodiode capacitance in MOS PPS [7].)

The CCD was invented in 1969 at Bell Labs by Boyle and Smith [8] and its application to image sensors was

Conventional N+P Single Junction type Photodiode with Serios Image Lag

NEC Double Junction type Buried Photodiode reported also Serios Image Lag in IEDM1982 Paper

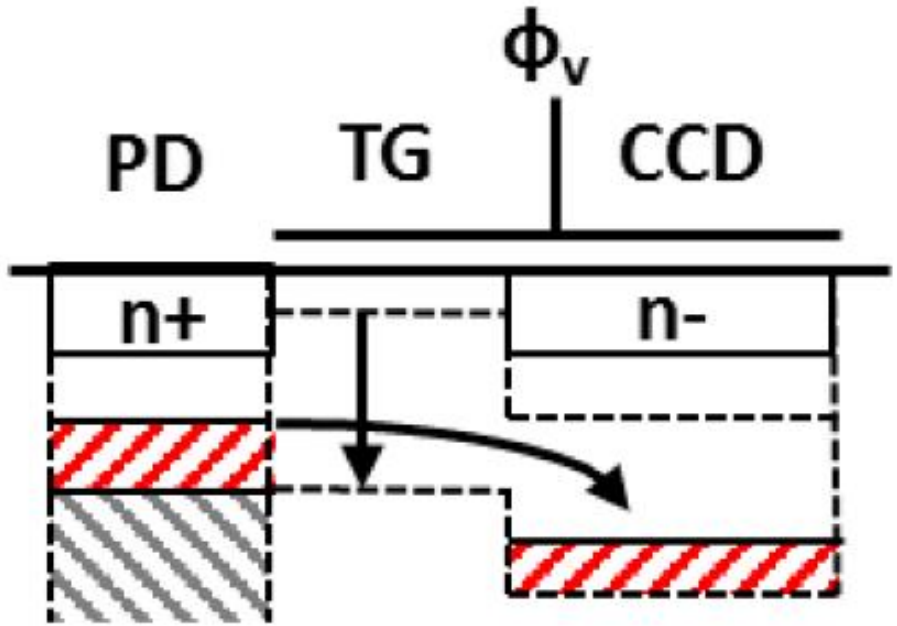


Fig. 1. Signal charge transfer from ILT CCD n + p photodetector.

B. Complete Charge Transfer to Eliminate Lag

To solve the ILT lag (and kTC noise) problem, a low-lag structure was invented by Teranishi, et al. at NEC in 1980 [19] and reported in 1982 [20] as shown in Fig. 2.

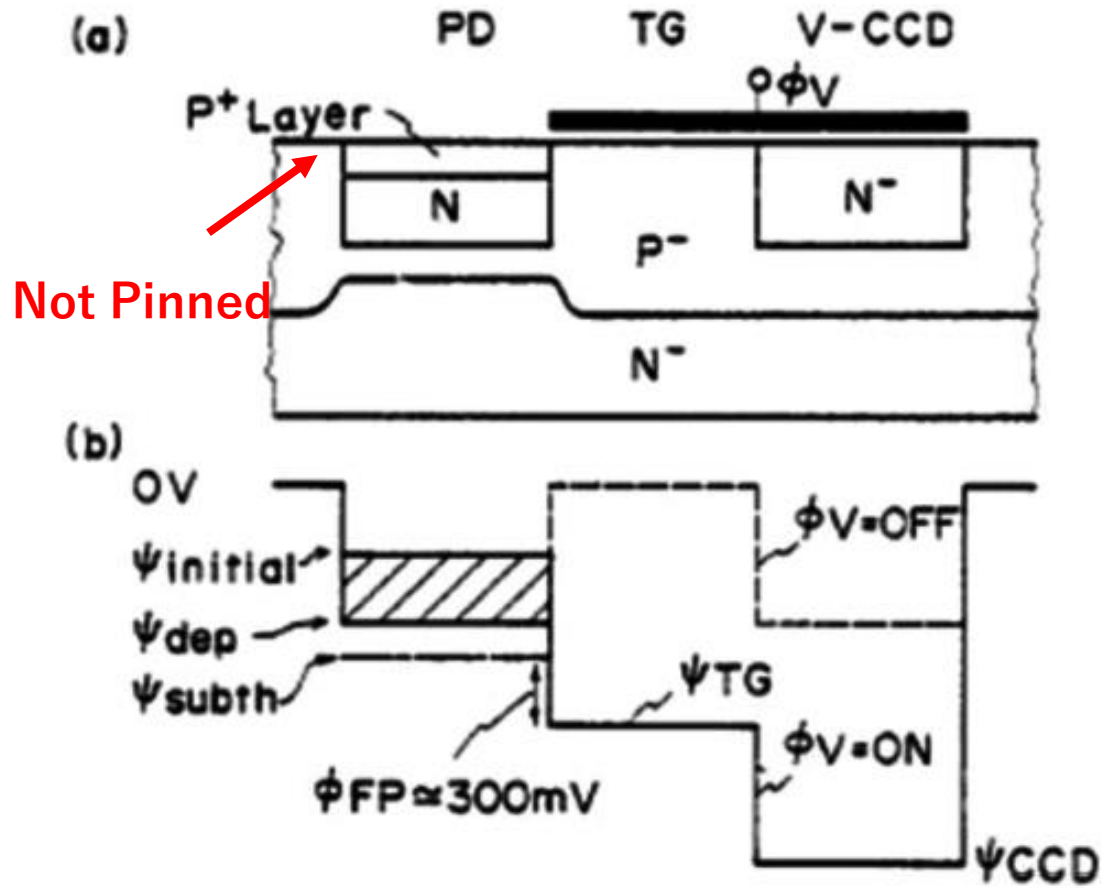


Fig. 2. Complete charge transfer from a pinned photodiode. (a) structure including VOD (b) potential well diagram (from Teranishi et al., 1982).

IEDM1984 KODAK Paper

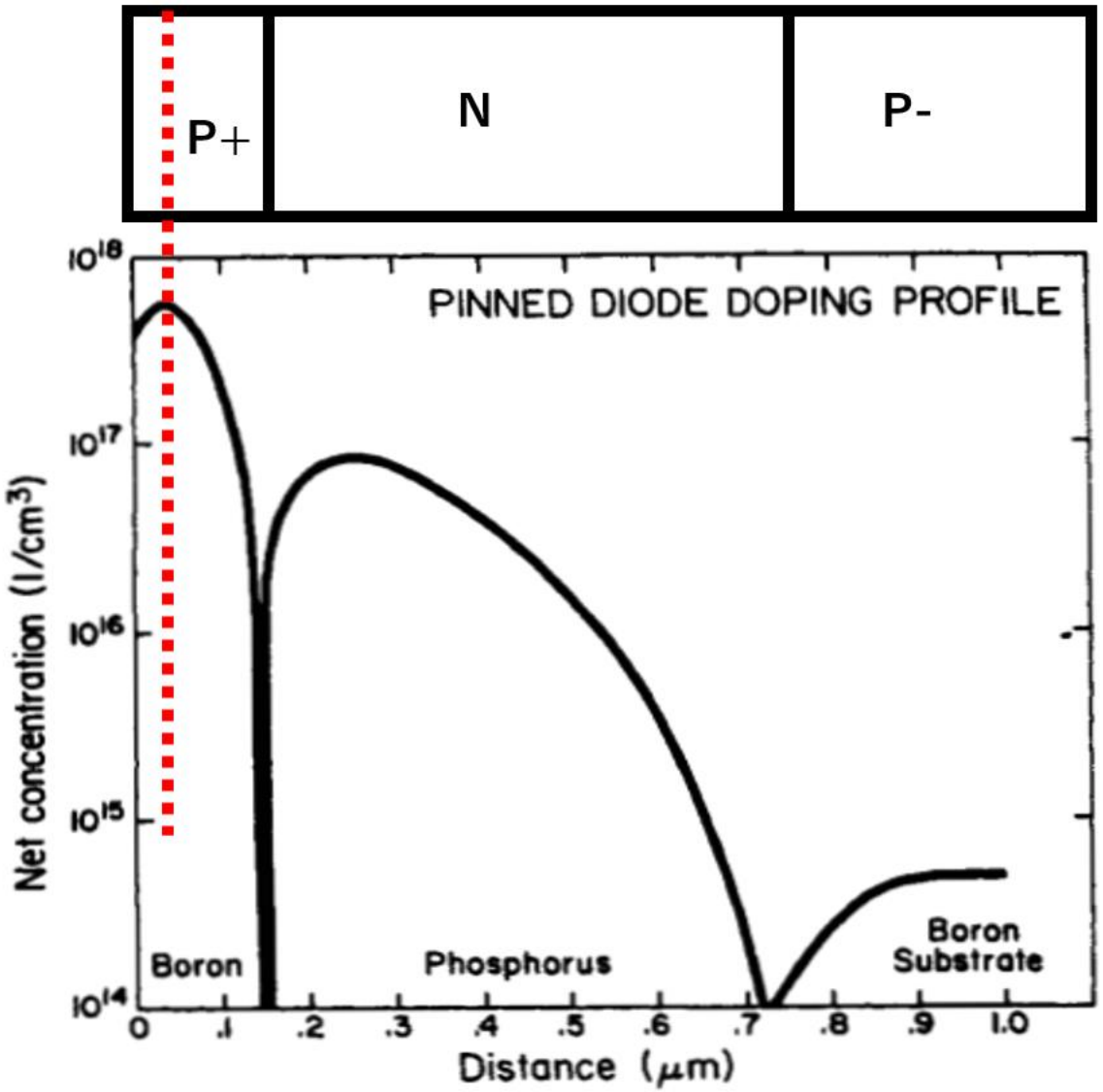


Fig. 2. Pinned diode doping profile.

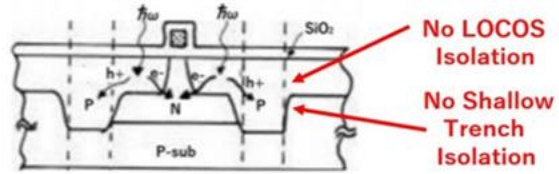
True Historv of Photodiode

First Pinned Photodiode was invented by Hagiwara in 1975 and reported at SSDM1978 by Sony.

Sony never used LOCOS isolation nor Shallow Trench Isolation. Both suffer the yield problem of Dark Current and White Defects. Instead, Sony used high energy ion implantation to form the adjacent heavily doped P+ channel stops region with the Lamp Anneal Technology invented by Kazuo Nishiyama at Sony.

(1) The first Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation invented and reported at SSDM1978 by Hagiwara.

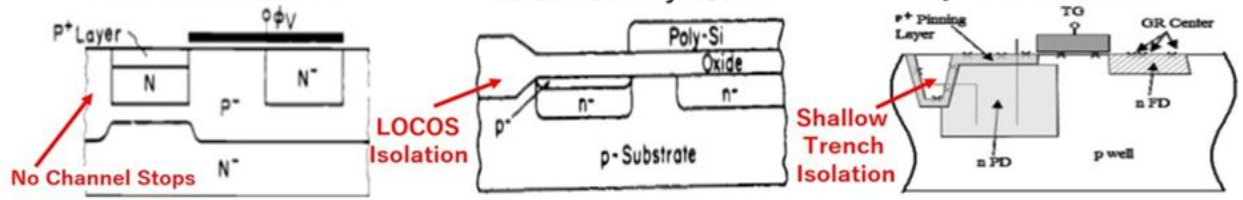
(2) Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation as explained by ssis.or.jp in the official Semiconductor History Museum WEB site.



(3) Buried Photodiode reported at IEDM1982 by NEC

(4) Pinned Photodiode reported at IEDM1984 by KODAK

(5) Pinned Photodiode reported by Teranishi in 2014



Sony Pinned Photodiode has the adjacent P+ heavily doped channel stops always directly grounded to the metal wire at the surface since 1978. Sony never used LOCOS isolation nor Shallow Trench Isolation.

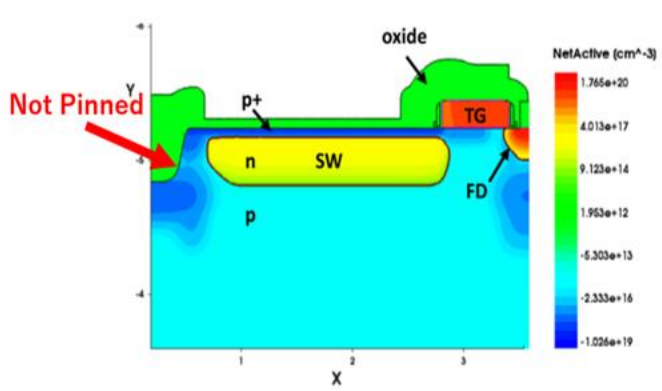


Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

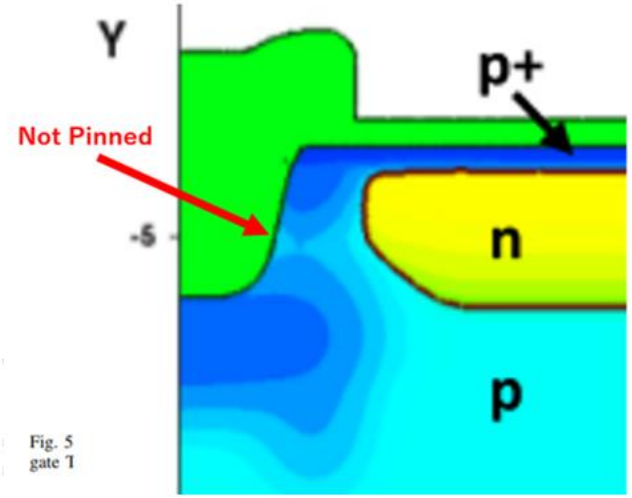


Fig. 5 gate T

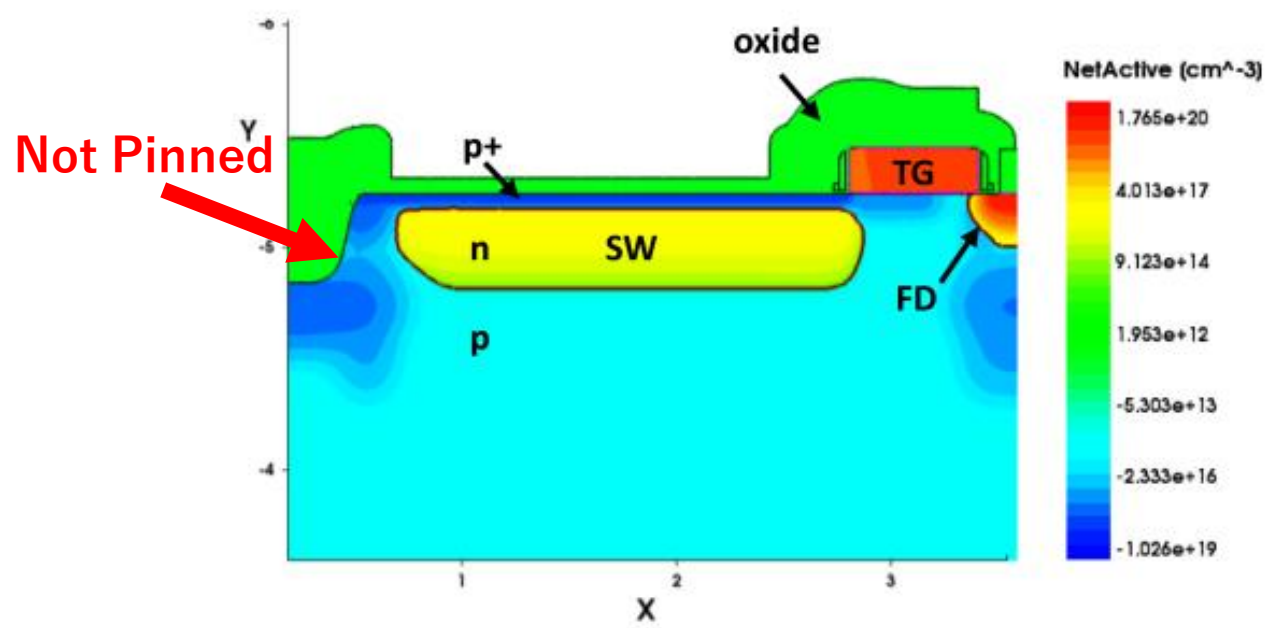


Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

CMOS manufacturing method was filed in 1999 [45]. Since then, many other methods for BSI manufacturing have been

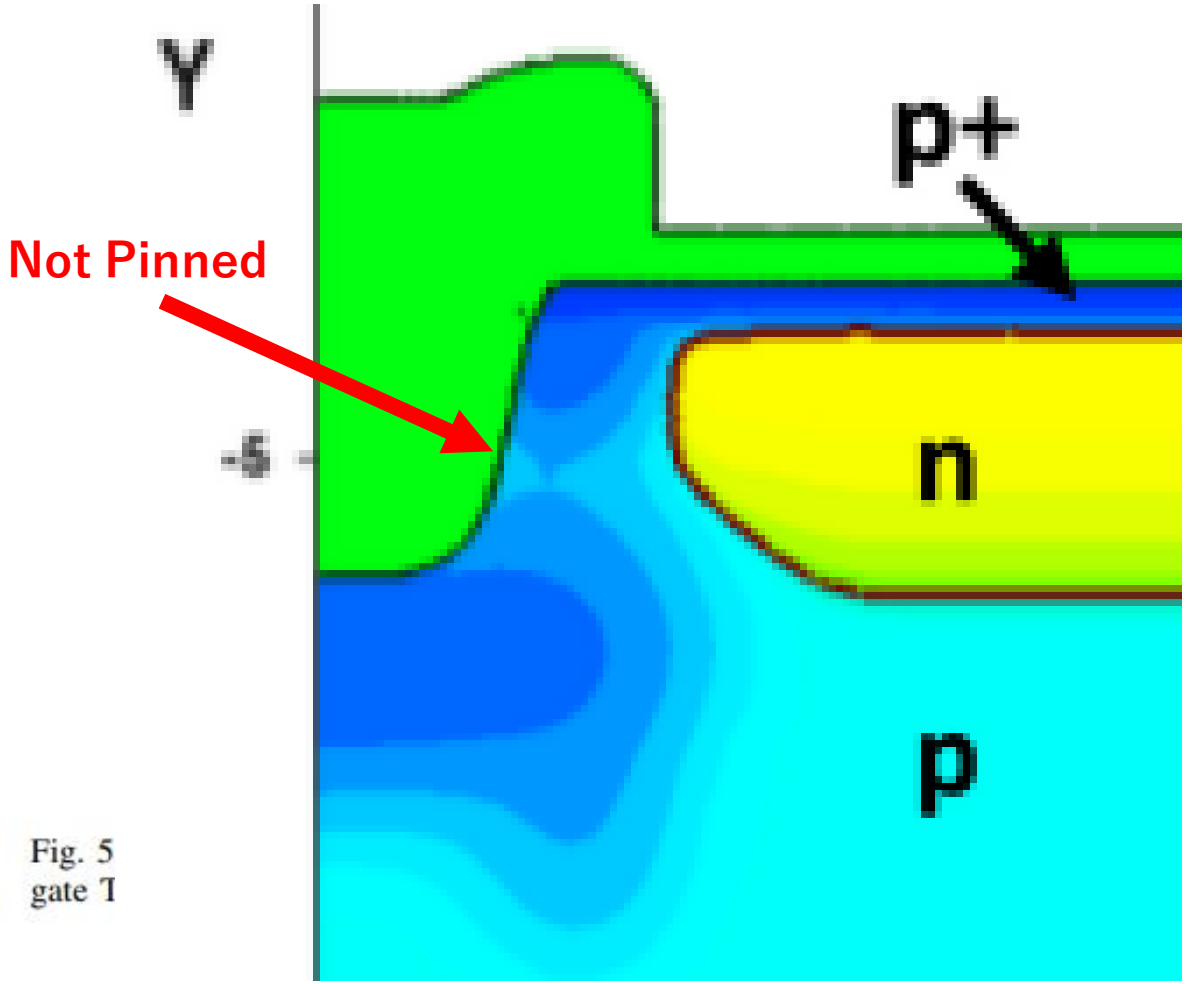
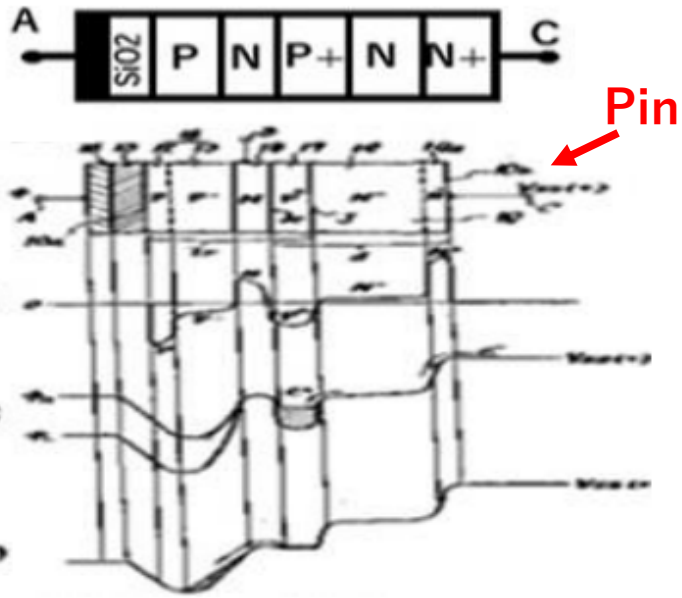


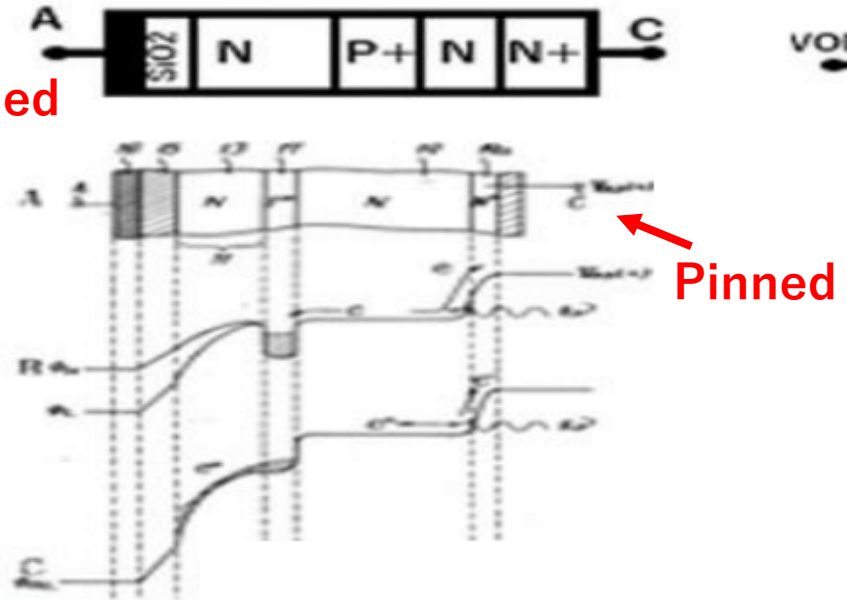
Fig. 5
gate T

Who invented Pinned Photodiode ?

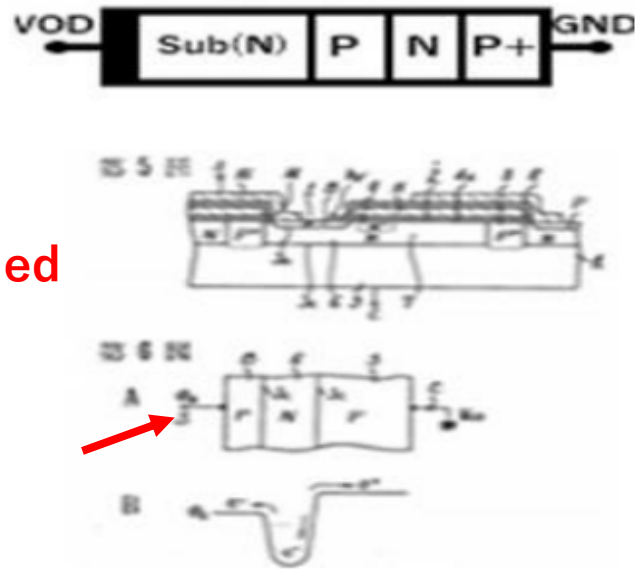
Hagiwara at Sony invented Pinned Photodiode in 1975. The evidence is give by the three Japanese patent applications, JPA1975-127646, JPA1975-127647 and JPA1975-134985. The first Pinned Photodiode was defined in October 23, 1975 as the N+NPNP triple junction(in Fig. 7 of JAP1975-127646) type and the N+NPN double junction type (in Fig. 7 of JAP1975-127647) type photodiodes with the N+ type pinned surface and the P type buried photo charge storage region with the complete charge transfer capability and the no-image-lag feature. The photo charge is transferred and drained to the CCD/MOS type charge storage buffer memory quicky by the strong punch-thru action. The second Pinned Photodiode was defined in November 10, 1975 as the PNP double junction (in Fig. 6 of JAP1975-134985) type photodiode with the vertical overflow drain action also with the complete charge transfer capability and the no-image-lag feature as evidence the empty potential well of the buried photo charge storage, completely depleted of the charge.



JPA1975-127646 Fig. 7



JPA1975-127647 Fig. 7



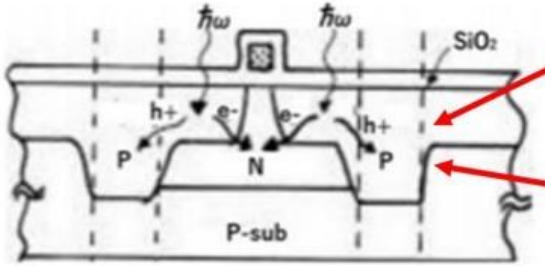
JPA1975-134985 Fig. 6

True Historv of Photodiode

First Pinned Photodiode was invented by Hagiwara in 1975 and reported at SSDM1978 by Sony.

Sony never used LOCOS isolation nor Shallow Trench Isolation. Both suffer the yield problem of Dark Current and White Defects. Instead, Sony used high energy ion implantation to form the adjacent heavily doped P+ channel stops region with the Lamp Anneal Technology invented by Kazuo Nishiyama at Sony.

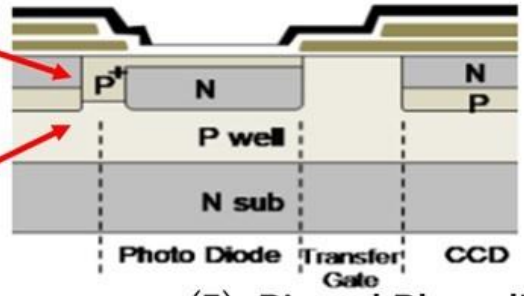
(1) The first Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation invented and reported at SSDM1978 by Hagiwara.



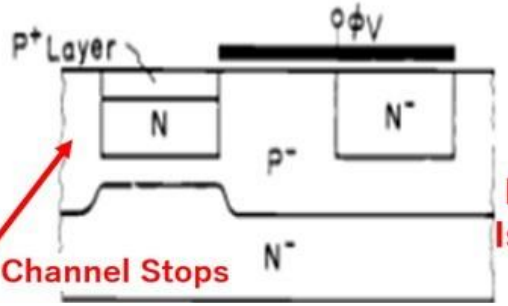
No LOCOS Isolation

No Shallow Trench Isolation

(2) Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation as explained by ssis.or.jp in the official Semiconductor History Museum WEB site.

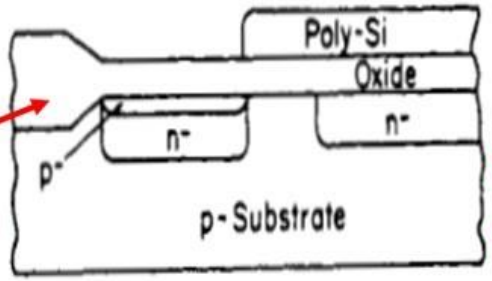


(3) Buried Photodiode reported at IEDM1982 by NEC



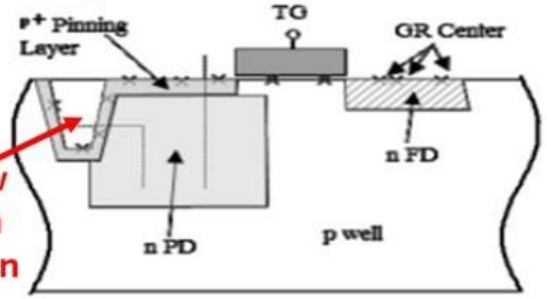
No Channel Stops

(4) Pinned Photodiode reported at IEDM1984 by KODAK



LOCOS Isolation

(5) Pinned Photodiode reported by Teranishi in 2014



Shallow Trench Isolation

Sony Pinned Photodiode has the adjacent P+ heavily doped channel stops always directly grounded to the metal wire at the surface since 1978. Sony never used LOCOS isolation nor Shallow Trench Isolation.

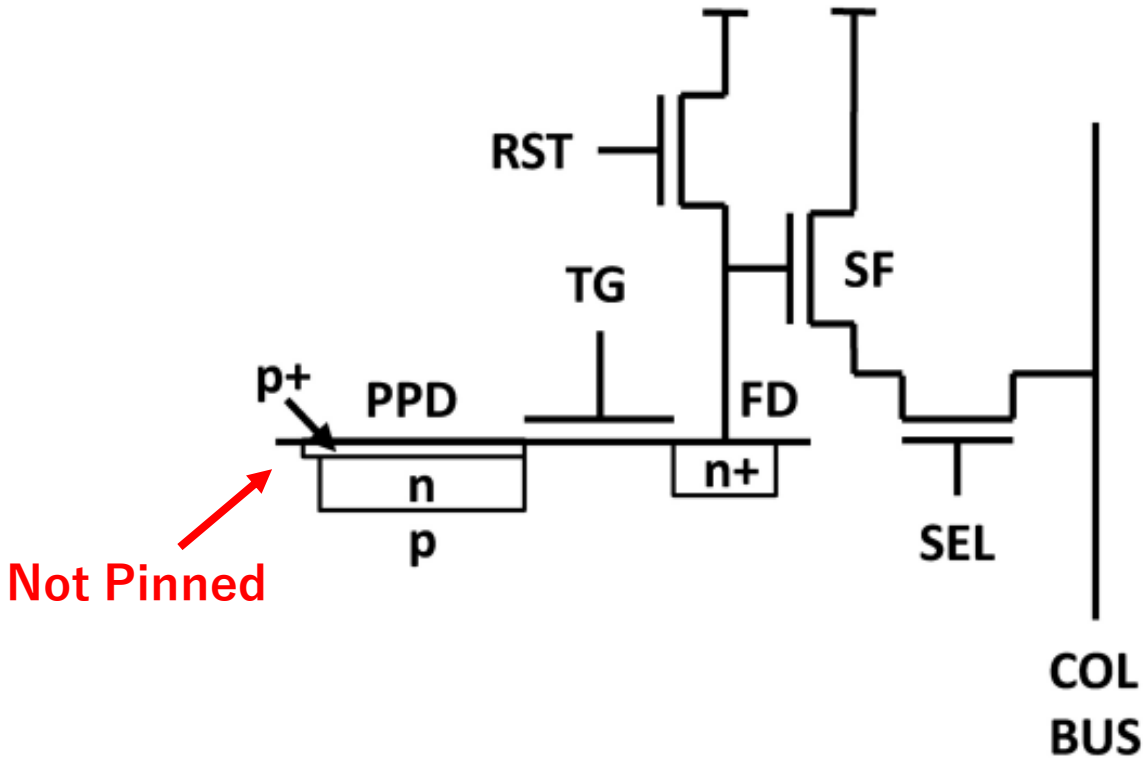


Fig. 3. Schematic of CMOS APS pixel with PPD.

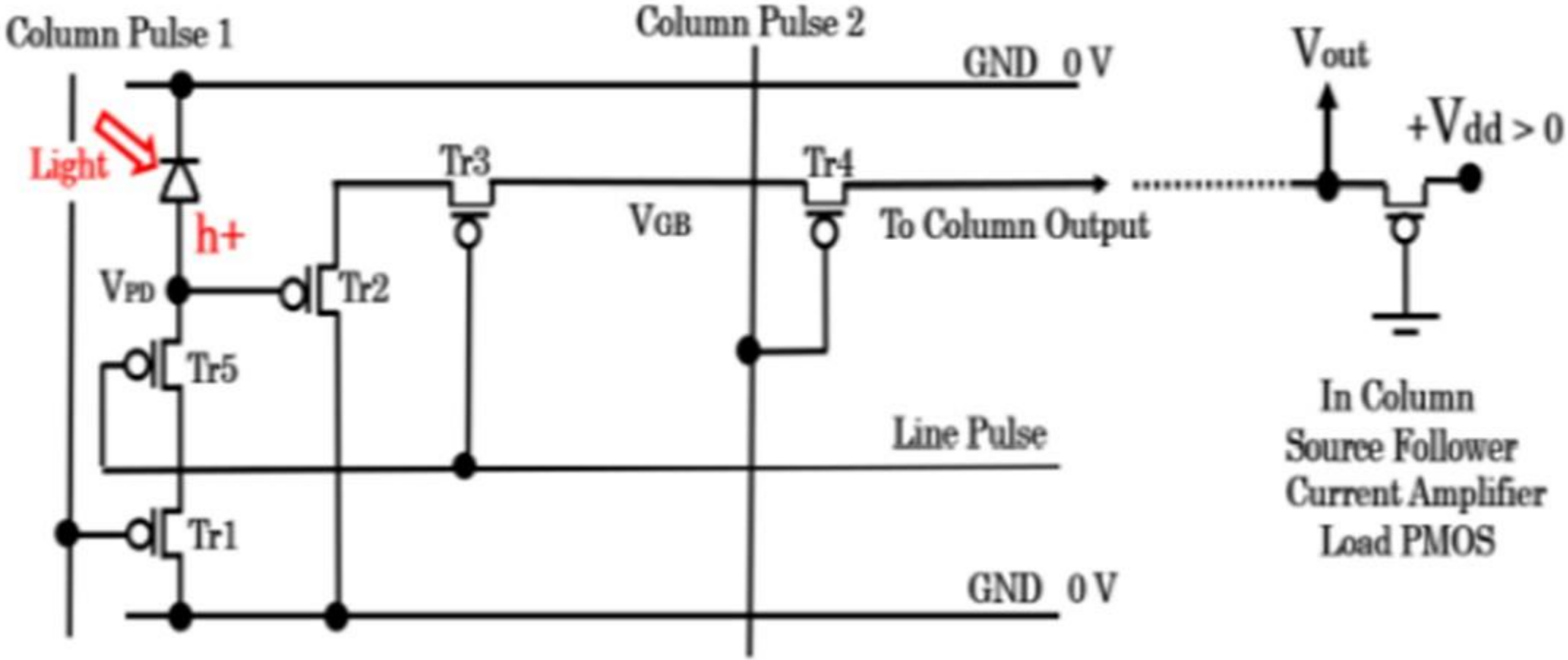
NEC paper was published. However, the "narrow-gate" CCD with an open *p*-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

The PPD, as it is most commonly used today, bears the strongest resemblance to the Teranishi et al. ILT CCD device. Thus, these days Teranishi is considered as the primary inventor of the modern PPD [29].

D. Application to CMOS Active Pixel Image Sensors

In 1993, a CMOS active pixel image sensor (APS) with intra-pixel charge transfer was proposed by Fossum et al. at JPL [30], [31]. Performance improvement using backside illumination (BSI) and a pinned photodiode was suggested in 1994 [32]. A CMOS APS pixel with a PPD is shown schematically in Fig. 3. Signal charge collected by the pixel

Active in-pixel AMP circuit invented by Peter Noble in 1968



Peter Nobel, IEEE Tran. of Electron Devices 15-4 (1968) pp. 202-209

True History of Photodiode

(1) Single Junction Type Dynamic Photodiode before 1970

(2) CCD/Mos type dynamic Photodiode invented in 1970

(3) Double Junction type Dynamic Photodiode invented by Philips in June 9, 1975

(4) Triple Junction type Dynamic Photodiode with the pinned surface invented by Sony in Oct 23, 1975.



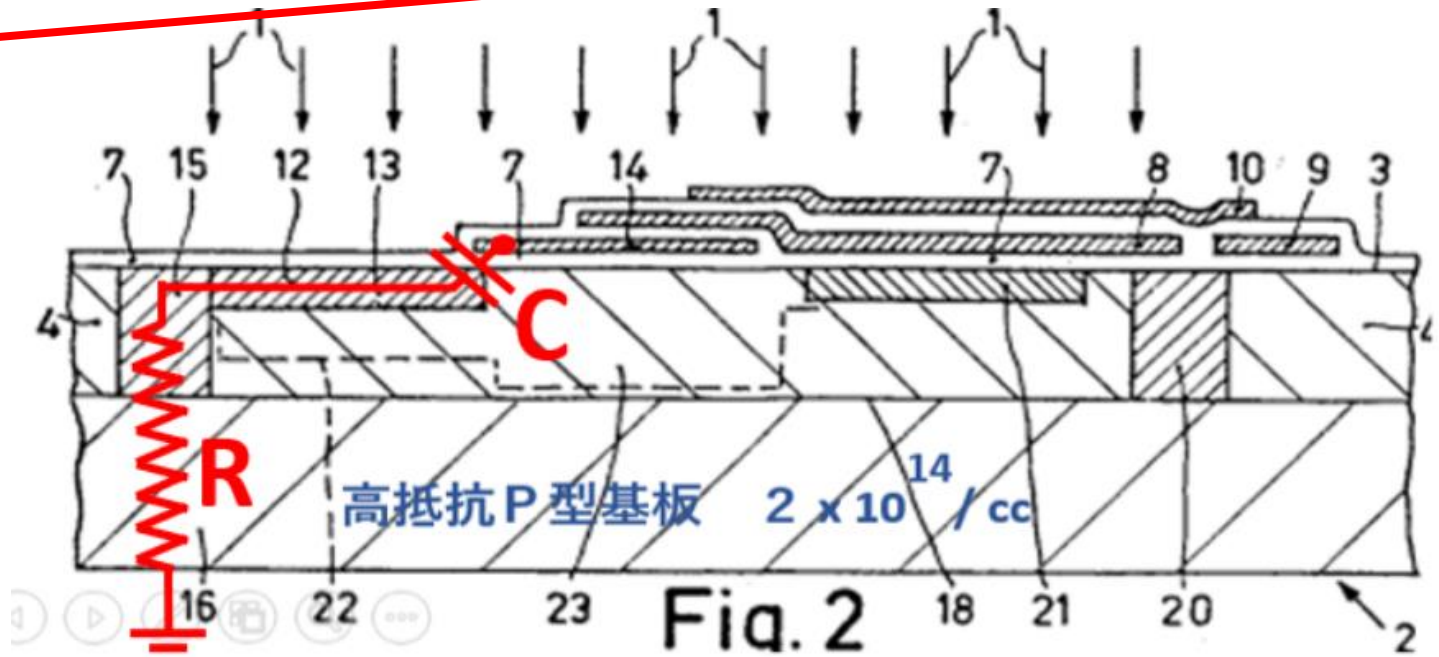
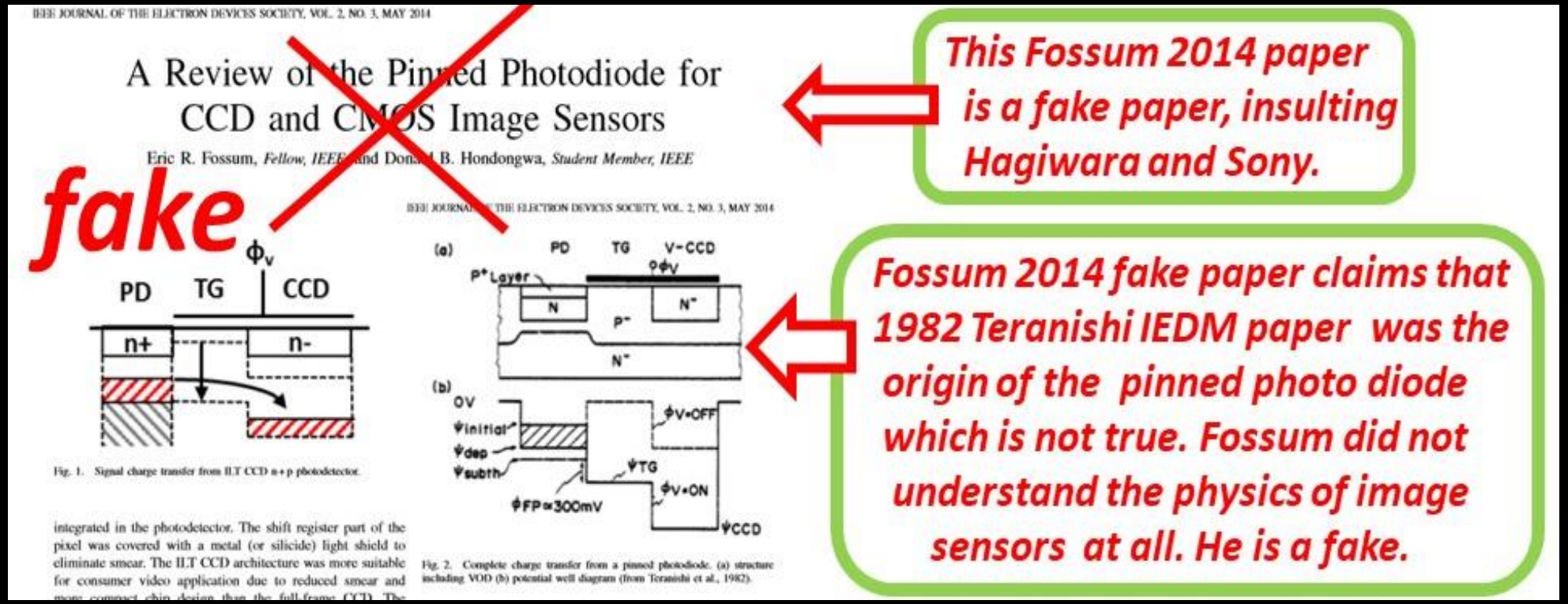
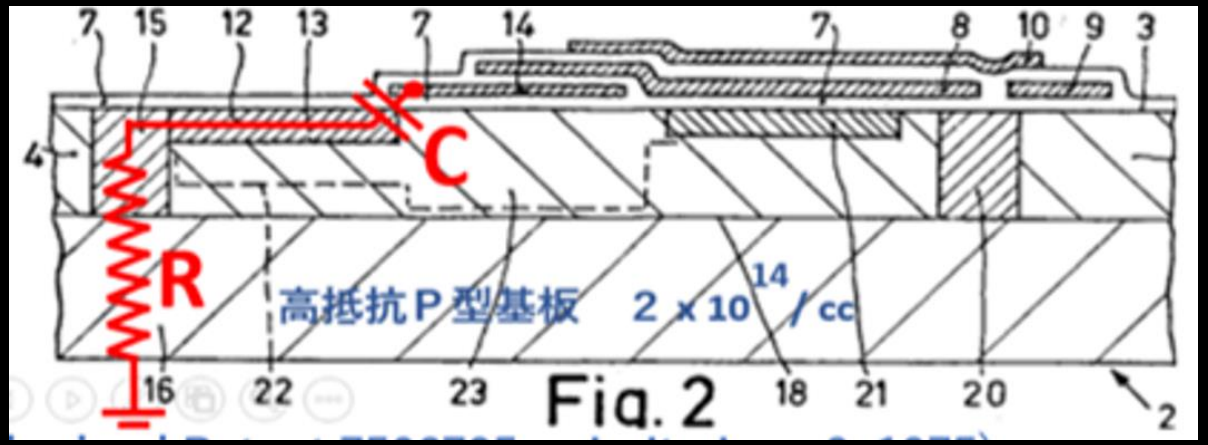


Fig. 2

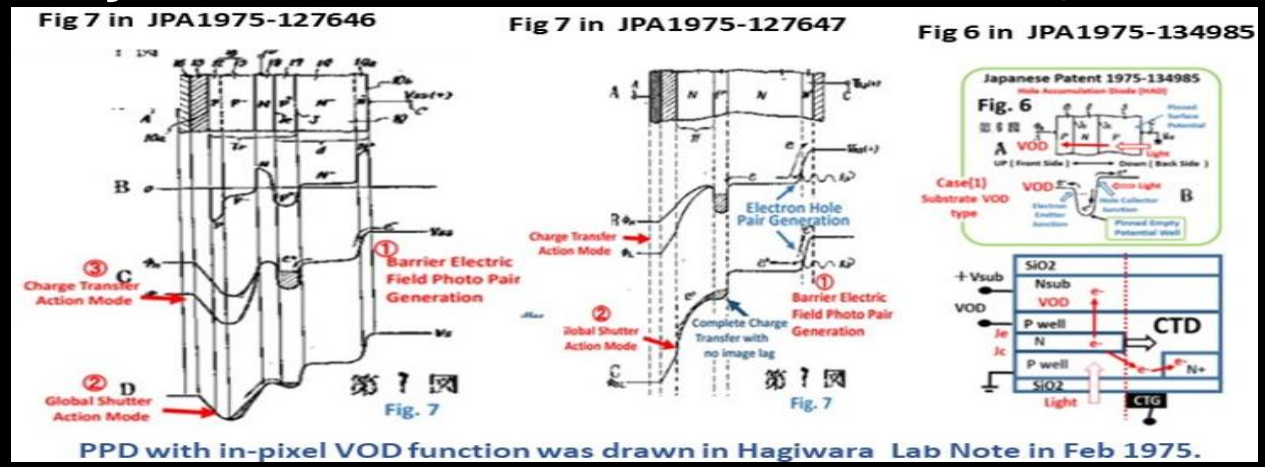
JPA1976-150288(Netherland Patent 7506795, priority June 7, 1975)



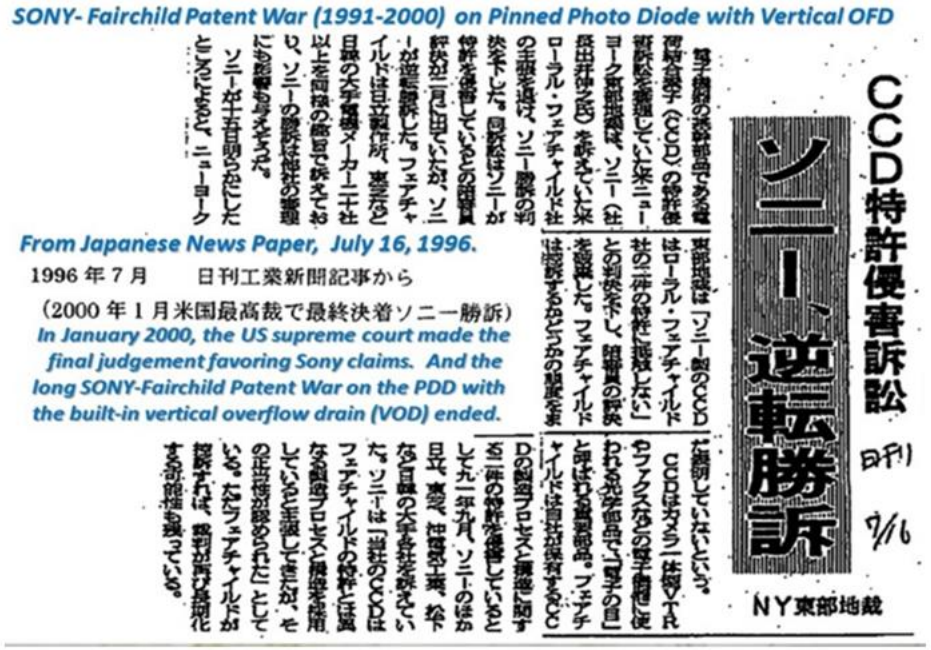
Philips Buried Photodiode June 9, 1975



Sony Pinned Photodiode Oct 23～Nov 10, 1975



SONY- Fairchild Patent War (1991-2000) on Pinned Photo Diode with Vertical OFD



CCD特許侵害訴訟

ソニー、逆転勝訴

NY東部地裁

From Japanese News Paper, July 16, 1996.

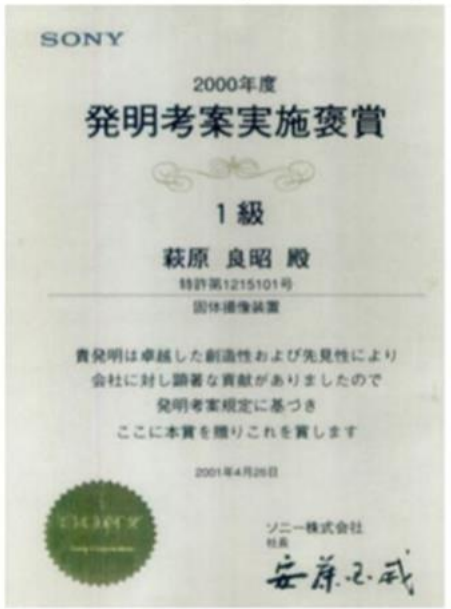
1996 年 7 月　日刊工業新聞記事から

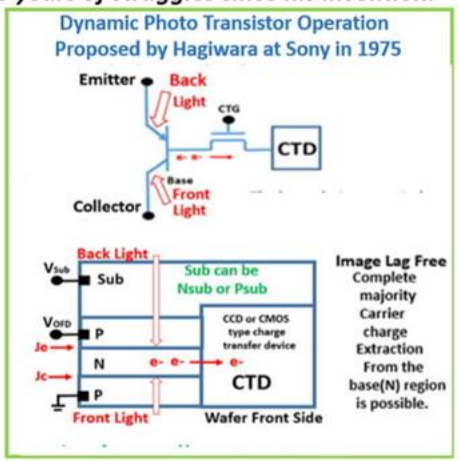
（2000 年 1 月米国最高裁で最終決着ソニー勝訴）

In January 2000, the US supreme court made the final judgement favoring Sony claims. And the long SONY-Fairchild Patent War on the PDD with the built-in vertical overflow drain (VOD) ended.

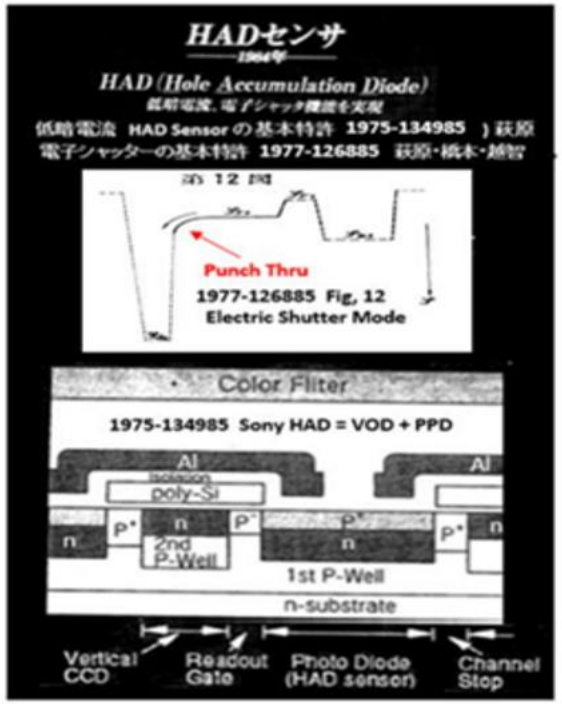
Finally the Sony-Fairchild Patent Wat(1991-2000) ended over the Sony HAD Sensor which is identical to the P+NPNsub junction type Pinned Photodiode with Vertical Overflow Drain, originally invented by Hagiwara at Sony in 1975.

And finally Hagiwara received for his 1975-134985 Japanese Patent officially , the First Patent Award from Mr. Ando, Sony president in April, 2001 after more 26 years of struggles since his invention.





Hagiwara also proposed the thyristor type punch-thru clocking scheme, synchronized with the TV scanning system to achieve the electric shutter.



Electric Shutter Basic Patent Award from Sony President Idei to Yoshiaki Hagiwara for Japanese Patent 1977-126885 by Hagiwara



Four Japanese Patent Applications on Pinned Photodiode with Electric Shutter Function and the in-Pixel Global Shutter MOS/CCD Buffer Memory Function for Modern CMOS Image Sensors.

Japanese Patent Application JPA1975-127646

Japanese Patent Application JPA1975-127647

Japanese Patent Application JPA1975-134985

Japanese Patent Application JPA1977-126885

The first Pinned Photodiode papers in 1977 and 1978 by Hagiwara at Sony

P1977_Narrow_Cahnnel_Transfer_Gate_CCD_SSDM1977_Paper_by_Hagiwara.pdf"

Hagiwara_SSDM1978_Paper_on_Pinned_Buried_Photodiode.pdf

Five Recently Published Papers by Hagiwara(AIPS)

P2019_3DIC2019_Paper_on_3D_Pinned_Photodiode_6_pages.pdf

EDTM2020 Conference Paper_ID_3C4_by_Hagiwara(PDF)

IJSSM2021 e-Journal Paper on Pinned Photodiode.html

ICECET2021_Paper61.pdf

ICECET2021_Paper75.pdf

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- Y. Daimon-Hagiwara, M. Abe, and C. Okada, “A 380Hx488V CCD imager with narrow channel transfer gates,” Japanese J. Appl. Phys., vol. 18, supplement 18–1, pp. 335–340, 1979.
- N. Teranishi, A. Kohono, Y. Ishihara, E. Oda, and K. Arai, “No image lag photodiode structure in the interline CCD image sensor,” in Proc. IEDM, Dec. 1982, pp. 324–327.
- B. C. Burkey et al., “The pinned photodiode for an interline-transfer CCD image sensor,” in Proc. IEDM, Dec. 1984, pp. 28–31.
- N. Teranishi, Y. Ishihara, and H. Shiraki, Japanese Patent JP 1,728,783, 1990.
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- Y. Hagiwara, “High-density and high-quality frame transfer CCDimager with very low smear, low dark current and very high blue sensitivity,” IEEE Trans. Electron Devices, vol. 43, no. 12, pp. 2122–2130, Dec. 1996.
- K. Yonemoto, H. Sumi, R. Suzuki, and T. Ueno. “A CMOS image sensor with a simple FPN-reduction technology and a hole accumulated diode,” in Proc. ISSCC, Feb. 2000, pp. 102–103.
- Y. Hagiwara, “Microelectronics for home entertainment,” in Proc. ESSCIRC, Sep. 2001, pp. 153–161.
- E.R. Fossum, D.B. Hondongwa, "A Review of the Pinned Photodiode for CCD and CMOS Image Sensors," IEEE J. Electron Device Soc. 2014, 2, 33–43.

Who invented Pinned Photodiode ? Who invented Electric Shutter function with no image lag feature ?

Sony invented in 1975 and developed in 1987 the Anti-Blooming Electric Shutter in Pinned Photodiode.
Hagiwara invented Pinned Photodiode in 1975. Sony developed Pinned Photodiode in 1978 for the first time.
Sony also developed in 1987 the PNPN junction type Pinned Photodiode with Electric Shutter Function.

Priority	R/D Efforts	by	Pinned Surface	Low Surface Dark Current	Blue Light Sensitivity	Photo Sensor Structure	Buried PN junction Memory Capacitor	Pinned Photo Sensor No Image Lag	Anti-blooming Electric Shutter
(1)1970~1974	Buried Channel CCD	Bell Lab	yes	NO	NO	MOS＋NP	YES	YES	NO
(2) June 9, 1975	JPA 1976-65707	Philips	NO	YES	YES	PNP	NO	NO	NO
(3) Oct 23, 1975	JPA 1975-127646	Sony	yes	YES	YES	N+NP+NP	YES	YES	YES
(4) Oct 23, 1975	JPA 1975-127647	Sony	yes	YES	YES	N+NP+N	YES	YES	YES
(5) Nov 10, 1975	JPA 1975-134985	Sony	yes	YES	YES	PNP	YES	YES	YES
(6) Sept, 1978	SSDM1978	Sony	yes	YES	YES	PNP	NO	YES	NO
(7) Oct 2, 1980	JPA 1980-138026	NEC	NO	YES	YES	PNP	YES	NO	NO
(8) Dec, 1982	IEDM1982	NEC	NO	YES	YES	PNP	YES	NO	NO
(9) Dec, 1984	IEDM1984	KODAK	yes	YES	YES	PNP	YES	YES	NO

Only Pinned Photodiode with the pinned surface can have the Electric Function with no image lag feature.

E-MAIL communications on Sony-Fairchild Patent War

February 6, 1996

Evidence of Hagiwara contribution in the Patent War on the PPD VOD patent (Hagiwara JPA 1975-134985)

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****

(1)　当時の SONY 中央研究所所長の山田敏之さんからのメッセージ

****

Subject: CCD Patent Report

X-Mailer: Eurora-J(1.3.8.5-J13)

中研の山田です。

ずいぶん前になりますが、分厚いレポートを
送って頂きありがとうございました。

CCD 裁判は越智さんはじめ関係者の大きな努力に
もかかわらず（一審での判決では）不本意な結果
となりましたが（その後逆転勝利となり）アメリ
カの裁判制度の問題点を如実に表しているような
気がします。

それはそれとして、この過程で萩原さんのこの
資料が越智さんにとっても大いに参考になった
ようです。

ご協力ありがとうございました。

CCD 開発史の一ページというか、読み物としても
面白く読ませて頂きました。

裁判の方はまだこれから延々と（最高裁まで）続く
でしょうが、引き続きご支援をお願いします。

萩原さんのことですから自分のやりたいことを
やりたいようにやっておられることと推察します。

私も少しその爪の垢を煎じて飲みたいものです。
すっかり遅くなりましたがひとこと御礼まで。

以上

****

(2)　当時の SONY 中央研究所副所長の越智成之さんからのメッセージ

****

Date: Tue. 6 Feb　9608:51:07 JST

To: hagiwara@mica.semicon.sony.co.jp(NanaeSato)

From:nanae@avzna.av.crl.sony.co.jp

Subject:testimony3

Cc: msato@saccd.semicon.sony.co.jp,ochi@av.crl.sony.co.jp

X-Mailer: Eurora-J(1.3.8-J13)

おはようございます。

中央越智副所長からの e-mail を forward します。

お忙しいのにもかかわらず、
多大なご協力を下さいまして
ありがとうございました。

****

(3)　SONY の森尾副社長、高橋専務、山田所長に対して
　米国滞在の越智さんから発信された裁判に関する報告

****

>X-POP3-Rcpt: nanae@avzna

>Date: Tue. 6, Feb 96 06:48:53 JST

>To: m-morio@cv.sony.co.jp, takahasi@rd.sony.co.jp,

>hashi@re.sony.co.jp,tyamada@dpo.crl.sony.co.jp

>Cc: ochi@av.crl.sony.jp,

>msato@saccd.semiocn.sony.co.jp,nanae@av.crl.sony.co.jp

>Subject: testimony3

>From: 越智　成之　<ochi@av.crl.sony.co.jp>

>X-Mailer: Winbiff[version 1.50 beta1]

>私に対する証人尋問が終わりました。

>direct exam は主に

>74 年の Amelio（Apple Computer の社長になってしまいましたが）

>特許や粂沢、松本レポートより前に、

> 既に　two phase overlapping gate

>buried channel self-aligned implanted barrier

>が考えられていたことを、

>Caltech（Bower, McGill, Daimon-Hagiwara ほか）

>と Hughes(Erb, Su ほか）と Sony（三船,二神ほか）

>等の資料を使い、実証致しました。

>cross exam は米国政府の御用達と独禁法と粂沢レポートに

>対する先方からの攻撃が中心でしたがどれも不発に終わりました。

>特に、Caltech の　Dr. Daimon(Hagiwara）が

>75 年 2 月 20 日にソニーに入社している事実が

>ショックを与えたようで、質問が止まって

>しまいました。

>Prof. Bower からも、Dr. Daimon（Hagiwara)が Caltech から

>Sony に(埋め込み型)CCD の Ion Implantation 構造

>（ISSCC1974 で学会発表ずみでその後中研時代には

>P+NPNsub 接合の　Pinned Photo Diode 構造の特許を出願し

>その Ion Implantation 構造解析に活用した）解析技術を

>持ち込んだ事実の Story の流れがすばらしいとのことでした。

>佐藤真木さん佐藤七重さん恐れ入りますが、

>感謝の気持ちを込めて、この e-mail を

>萩原良昭さんに forward してください。

>萩原さんはこの 2 晩で 100 ページ以上にも

>及ぶ個人資料を fax で送ってくれました。

>馬橋さんの証言も成功裏に終わり、

>今後弁護士と今後の相談を致します。

>越智

＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊

E-MAIL communications on Sony-Fairchild Patent War
February 6, 1996

Evidence of Hagiwara contribution in the Patent War
on the PPD VOD patent (Hagiwara JPA 1975-134985)

＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊

****

(1) 当時のSONY中央研究所所長の山田敏之さんからのメッセージ

****

Subject: CCD Patent Report
X-Mailer: Eurora-J(1.3.8.5-J13)

中研の山田です。

ずいぶん前になりますが、分厚いレポートを送って頂きありがとうございました。

CCD裁判は越智さんはじめ関係者の大きな努力にもかかわらず（一審での判決では）不本意な結果となりましたが（その後逆転勝利となり）アメリカの裁判制度の問題点を如実に表しているような気がします。

E-MAIL communications on Sony-Fairchild Patent War
February 6, 1996

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****

(1) 当時のSONY中央研究所所長の山田敏之さんからのメッセージ

****

それはそれとして、この過程で萩原さんのこの資料が越智さんにとっても大いに参考になったようです。ご協力ありがとうございました。

CCD開発史の一ページというか、読み物としても面白く読ませて頂きました。

裁判の方はまだこれから延々と（最高裁まで）続くでしょうが、引き続きご支援をお願いします。

萩原さんのことですから自分のやりたいことをやりたいようにやっておられることと推察します。

私も少しその爪の垢を煎じて飲みたいものです。すっかり遅くなりましたがひとこと御礼まで。

以上

E-MAIL communications on Sony-Fairchild Patent War
February 6, 1996

Evidence of Hagiwara contribution in the Patent War
on the PPD VOD patent (Hagiwara JPA 1975-134985)

＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊

****

(2) 当時のSONY中央研究所副所長の越智成之さんからのメッセージ

****

Date: Tue. 6 Feb 9608:51:07 JST
To: hagiwara@mica.semicon.sony.co.jp(NanaeSato)
From:nanae@avzna.av.crl.sony.co.jp
Subject:testimony3
Cc: msato@saccd.semicon.sony.co.jp,ochi@av.crl.sony.co.jp
X-Mailer: Eurora-J(1.3.8-J13)

おはようございます。中央越智副所長からのe-mailをforwardします。

お忙しいのにもかかわらず、多大なご協力を下さいまして
ありがとうございました。

E-MAIL communications on Sony-Fairchild Patent War
February 6, 1996

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(3) SONYの森尾副社長、高橋専務、山田所長に対して
　米国滞在の越智さんから発信された裁判に関する報告

****

>Date: Tue. 6, Feb 96 06:48:53 JST
>To: m-morio@cv.sony.co.jp,takahasi@rd.sony.co.jp,
>hashi@re.sony.co.jp,tyamada@dpo.crl.sony.co.jp
>Cc: ochi@av.crl.sony.jp,
>msato@saccd.semiocn.sony.co.jp,nanae@av.crl.sony.co.jp
>Subject: testimony3
>From: 越智　成之　<ochi@av.crl.sony.co.jp>
>X-Mailer: Winbiff[version 1.50 beta1]
>私に対する証人尋問が終わりました。
>direct exam は主に

E-MAIL communications on Sony-Fairchild Patent War
February 6, 1996

Evidence of Hagiwara contribution in the Patent War
on the PPD VOD patent (Hagiwara JPA 1975-134985)

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　米国滞在の越智さんから発信された裁判に関する報告

****

>74年のAmelio（Apple Computerの社長になってしまいましたが）
>特許や粂沢、松本レポートより前に、
> 既に　two phase overlapping gate
>buried channel self-aligned implanted barrier
>が考えられていたことを、
>Caltech（Bower, McGill, Daimon-Hagiwaraほか）
>と Hughes(Erb, Suほか）と Sony（三船,二神ほか）
>等の資料を使い、実証致しました

E-MAIL communications on Sony-Fairchild Patent War
February 6, 1996

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>及ぶ個人資料をfaxで送ってくれました。

>馬橋さんの証言も成功裏に終わり、
>今後弁護士と今後の相談を致します。

>越智



1975年に萩原が発明したPNPN接合型のHADセンサーは電子シャッターを可能にする受光素子でしたが、その実用化には石川さんたち後輩のさらなる発明と開発努力が必要でした。その後１２年もの年月の努力の結果、石川さんたちは１９８７年、電子シャッターの実用化商品化に成功し、SONYの市場制覇が始まり、その遺産が今も後輩に継承されています。



萩原が担当したのは、あくまで半導体電子デバイス部品の技術開発です。実際のAIBOロボットは土井さんが、Play Stationは久夛良木さんが陣頭指揮をとり開発部隊を指導していました。土井さんと久夛良木さんたちはあくまで私たちの製品のユーザー側です。われわれのお客さまでした。

June 26, 2020

Sony's Representative Inventions Supporting Stacked Multi-Functional CMOS Image Sensors

Sony Corporation

Sony Semiconductor Solutions Corporation

Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

ELECTRICAL ENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

Asked 8 years, 10 months ago Modified 2 years, 8 months ago Viewed 6k times

6

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

Share Cite Follow

edited Aug 16, 2018 at 19:17

answered Sep 21, 2013 at 14:34



placeholder

29.6k ● 10 ● 60 ● 110

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

Proceedings of the 9th Conference on Solid State Devices, Tokyo, 1977;
Japanese Journal of Applied Physics, Volume 17 (1978) Supplement 17–1, pp. 255–261

Two Phase CCD with Narrow-Channel Transfer Regions

Yoshiaki DAIMON-HAGIWARA

Sony Corporation Research Center Yokohama 240

with no image lag

When the channel width of a FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of threshold voltage is observed. This narrow-channel effect has been applied successfully in creating an asymmetrical potential well under an electrode for two phase CCD operations. The basic performance of this new structure has been evaluated in a 242 element analog delay line with 60 μm channel width and 36 μm element length. Observed inefficiencies per transfer are in the low 10^{-4} for surface channel versions and in the low 10^{-5} for buried channel versions.

Proceedings of the 9th Conference on Solid State Devices, Tokyo, 1977;
Japanese Journal of Applied Physics, Volume 17 (1978) Supplement 17–1, pp. 255–261

Two Phase CCD with Narrow-Channel Transfer Regions

Yoshiaki DAIMON-HAGIWARA

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with no image lag

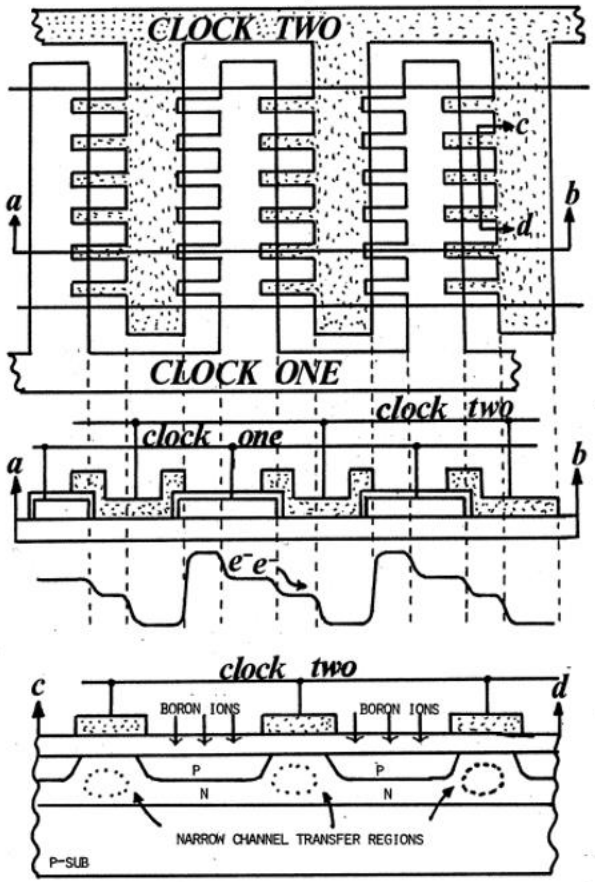


Fig. 1. Top and crosssectional views of the electrode structure for two phase CCD with narrow-channel transfer regions.

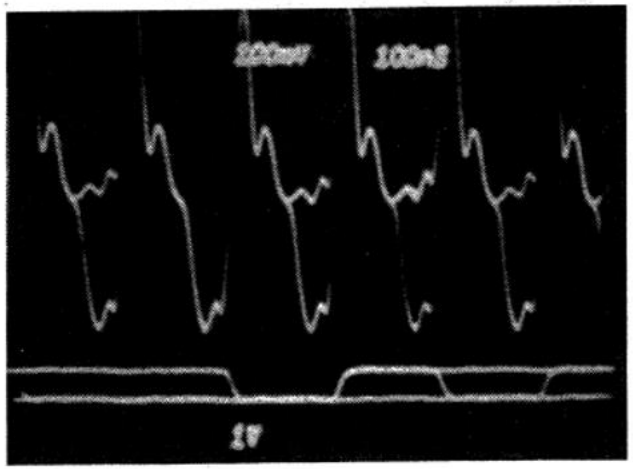


Fig. 4. Input and output wave forms for 242 analo delay line in buried channel version.

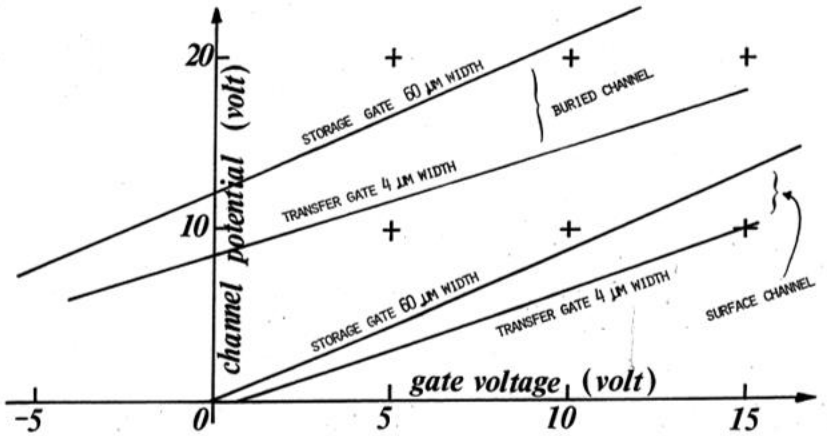


Fig. 2. The actual measured channel potentials plotted against the gate voltage for both surface and buried channel versions.

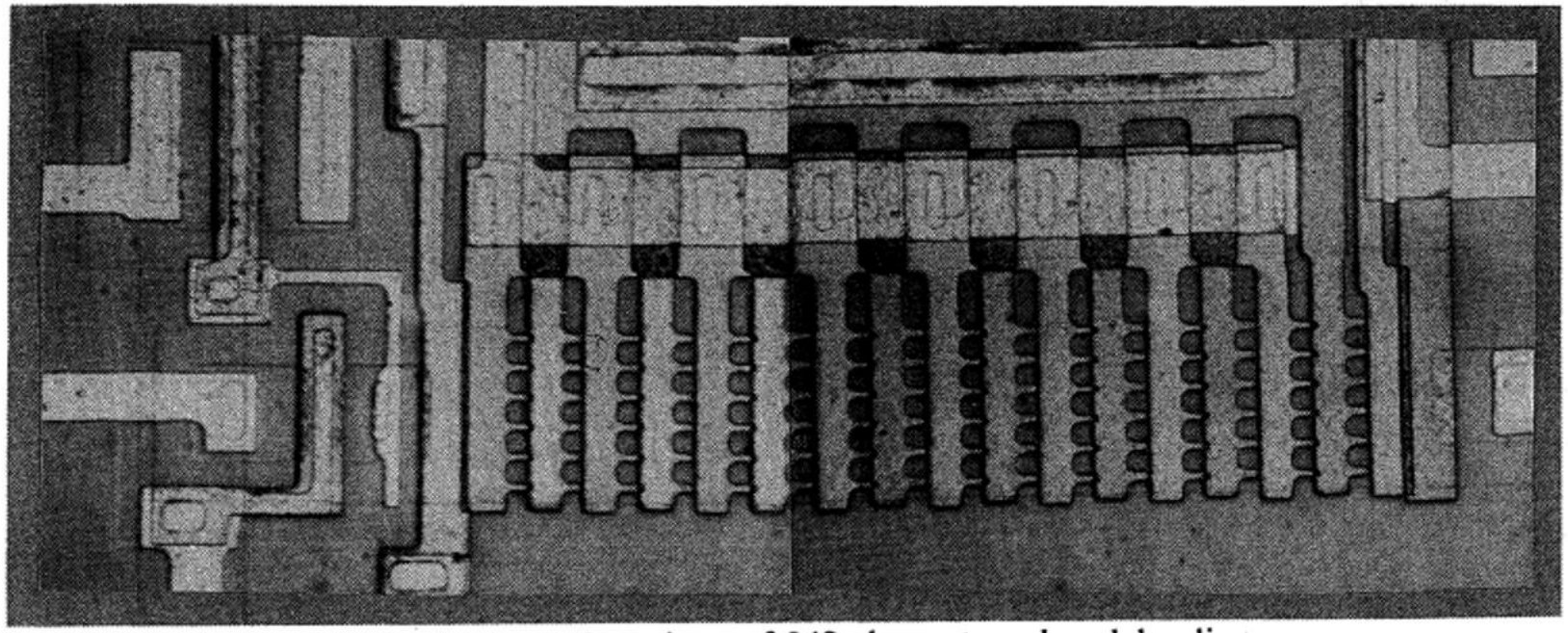


Fig. 3. The end sections of 242 element analog delay line.

Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978;
Japanese Journal of Applied Physics, Volume 18 (1979) Supplement 18-1, pp. 335-340

A 380H × 488V CCD Imager with Narrow Channel Transfer Gates

Yoshiaki Daimon-HAGIWARA, Motoaki ABE† and Chikao OKADA†

Sony Corporation Research Center, Yokohama 240
†Semiconductor Development Division, Yokohama 240

with no image lag

When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of threshold voltage is observed. This narrow-channel effect has been applied successfully in creating an asymmetric potential well under an electrode for two phase CCD operations. The feasibility of this new structure has been confirmed in a 242 element analog delay line and the application is now extended to a 380H × 488V CCD Imager. In the constructed B/W CCD camera,

Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978;
Japanese Journal of Applied Physics, Volume 18 (1979) Supplement 18-1, pp. 335-340

A 380H × 488V CCD Imager with Narrow Channel Transfer Gates

Yoshiaki Daimon-HAGIWARA, Motoaki ABE† and Chikao OKADA

Sony Corporation Research Center, Yokohama 240
†Semiconductor Development Division, Yokohama 240

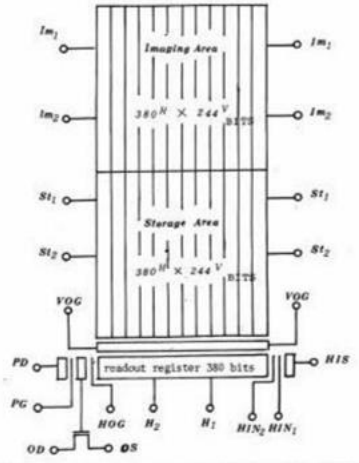


Fig. 1. The block diagram of a 380 H×488 V CCD imager in frame transfer organization.

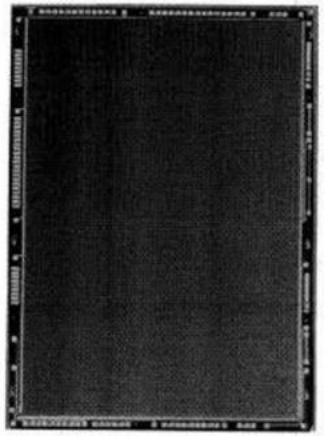


Fig. 3. Photomicrograph of the 380 H×488 V CCD imager. The chip size is 14.6 mm by 10.1 mm.

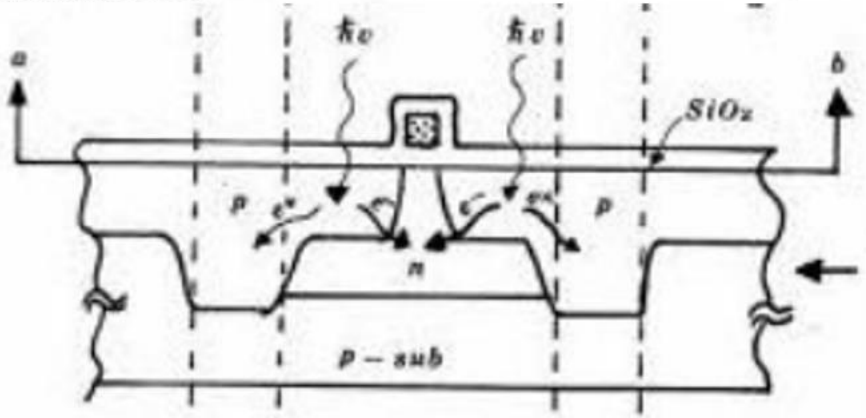


Fig. 2. Top and cross sectional views of the electrode for two phase CCD structure.

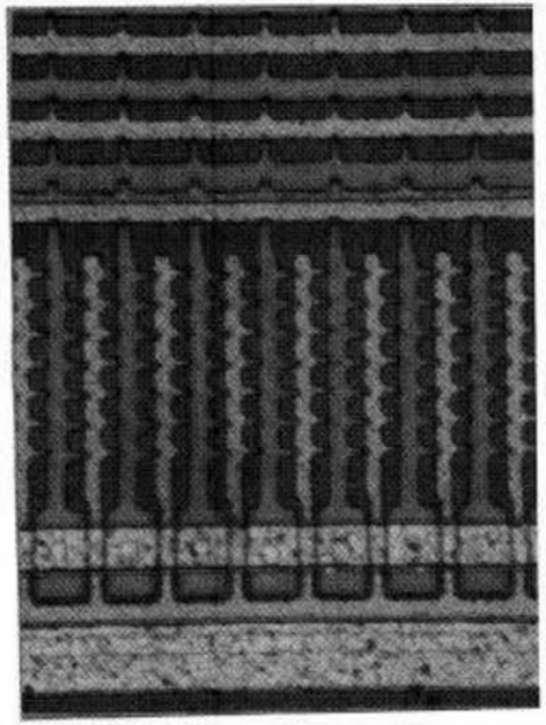


Fig. 5. The horizontal readout register with 14 μm-pitch-per bit electrode structure.

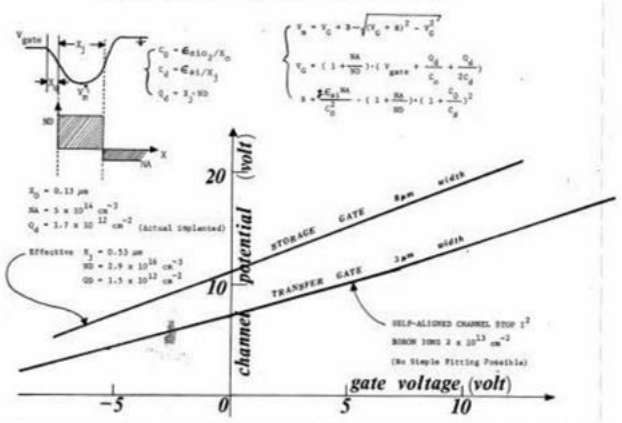


Fig. 9. The actual measured channel potentials plotted against the gate voltage for the buried channel version. The curve fitting with the simple relations by depletion approximation gives the effective values of X_j, ND and QD as seen in the figure.

with no image lag

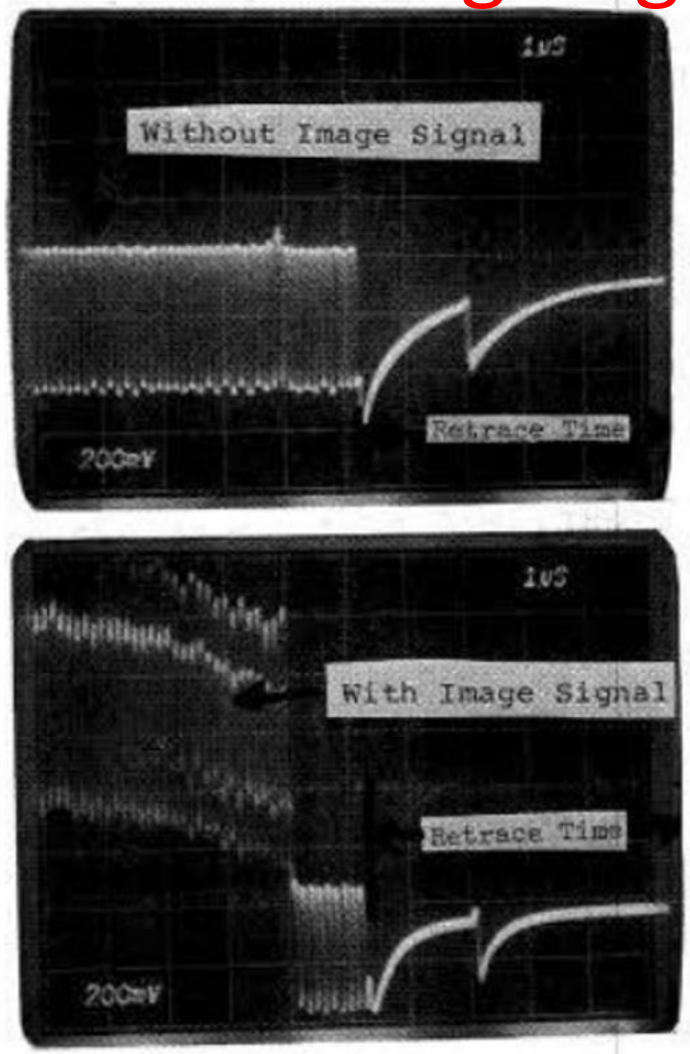


Fig. 12. The output wave forms of the horizontal readout register at the tailing end of a TV picture line, that is, right before the horizontal retrace time. The comparison of the output levels with and without image signal gives the dark current level of the imager.

High-Density and High-Quality Frame Transfer CCD Imager with Very Low Smear, Low Dark Current, and Very High Blue Sensitivity

Yoshiaki Hagiwara, *Member, IEEE*

with no image lag

Abstract—**When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of the threshold voltage is observed. This narrow channel effect has been applied successfully in creating an asymmetric potential well under an electrode for two-phase CCD operation. The feasibility of this structure has been confirmed in a 242-element analog delay line. The application is now extended to a 800 H × 492 V frame transfer-type buried channel CCD imager with 14.31818 MHz frame shift, which results in a very low smear level of 0.01%, which is good enough for low-cost multimedia video camera applications.**

I. Introduction

Since their introduction in the 1970's, CCD sensors have improved dramatically. CCD's, however, have a number of disadvantages in multimedia applications. Ackland emphato the interline-type CCD imager, yet holds a large signal charge packet. The on-chip frame memory can also be used as a buffer memory for various multimedia applications.

On these points, some brief discussions regarding a new frame-transfer CCD structure and their results are reported. The new structure is bipolar-type image sensing element with a p-n-p SUB structure. The structure was originally proposed by the author in 1975 [8]. Some related ideas, hidden in the form of difficult legal wording, and other efforts, disclosed in the form of published papers, will be reviewed and discussed in details to explain the background and originality of the author's proposed structure.

II. Bipolar Image Sensing Element

High-Density and High-Quality Frame Transfer CCD Imager with Very Low Smear, Low Dark Current, and Very High Blue Sensitivity

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with no image lag

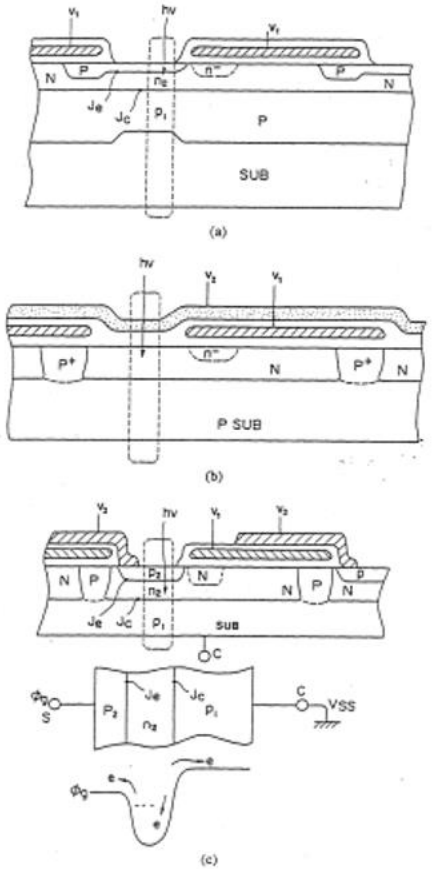


Fig. 1. (a) Basic structure of bipolar junction-type image sensing element now widely adapted in interline transfer CCD imagers. The hatched regions (V_1) covering the top are the polysilicon electrodes for the vertical CCD shift registers. The sensor regions are not covered by the polysilicon electrodes. (b) MOS capacitance-type imaging sensing element quoted in the author's invention of November 10, 1975, and known then as a conventional structure. The top layer (V_2) can be either a thin polysilicon or a transparent sensor electrode. (c) Bipolar junction-type image sensing element with a top wiring lead (V_3). In this case, as a simple example, the first p-region (P_1) is set equal to the silicon substrate.

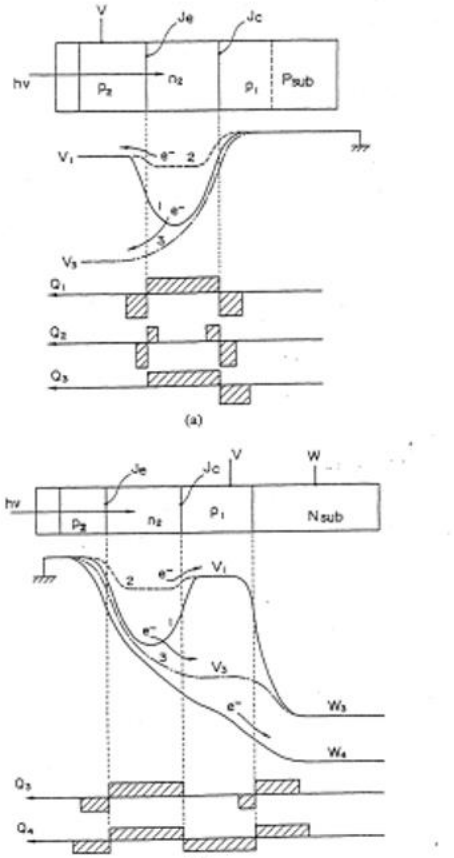


Fig. 2. (a) Operations of bipolar junction-type image sensing element when the substrate is chosen to be the same as the P1 region. Q1, Q2, and Q3 are fixed charges in the depletion regions. (b) Operations of a bipolar junction-type image sensing element when the substrate is different from the P1 region. Q3 and Q4 are fixed charges in the depletion regions, where no mobile carriers are present.

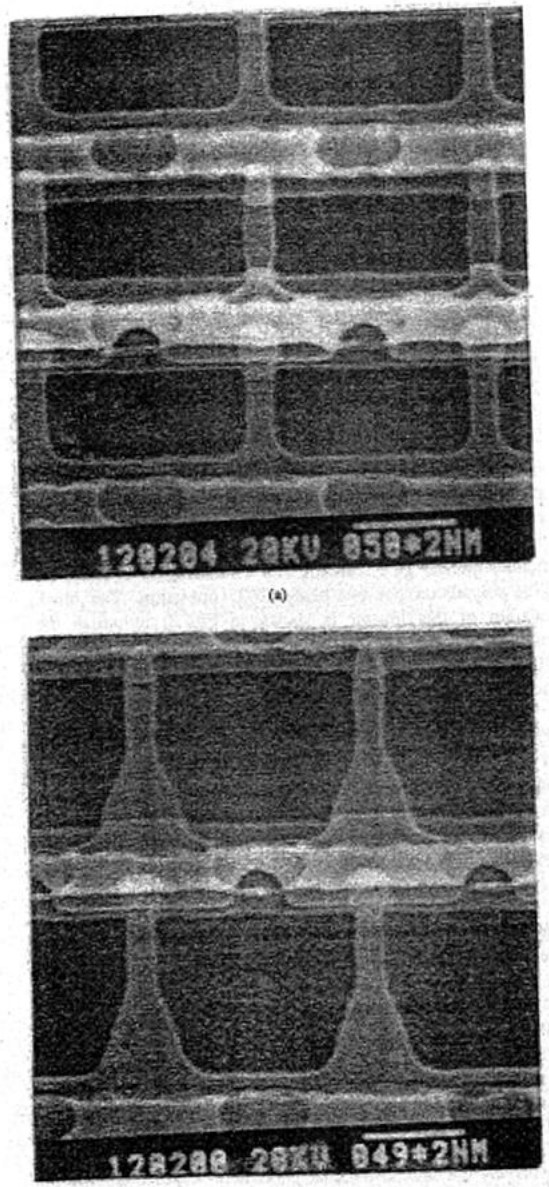


Fig. 4. (a) SEM picture of storage area. Cell size is 11 μm H × 9 μmV. (b) SEM picture of imaging area. Cell size is 11 μm H × 13 μmV.

TABLE II
DEVICE CHARACTERISTICS

Optical Format	2/3 inch
Transfer System	Frame Transfer
Total Number of Pixels	800 H x 492 V
Chip Size	10.0 mm H x 12.5 mm V
Cell Size Imaging Area	11 μm H x 13 μm V
Cell Size Storage Area	11 μm H x 9 μm V
Silicon Substrate	p-type (100) 10-15 ohm-cm
Horizontal Resolution	560 TV lines
Vertical Resolution	350 TV lines
Smear	0.01 %
Noise	10 electrons/pixel
Output Gain	4 μV/e
Lag	Undetectable
Dynamic Range	83 dB
Charge Capacity	200,000 electrons/pixcel
Minimum Illumination (F1.4)	1.6 lux

with no image lag

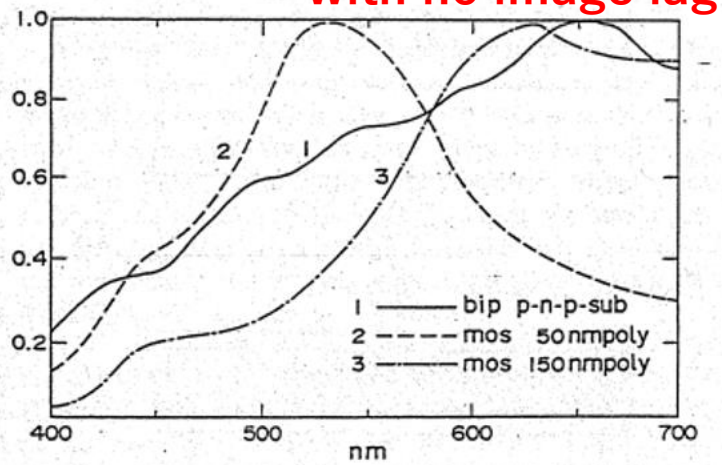
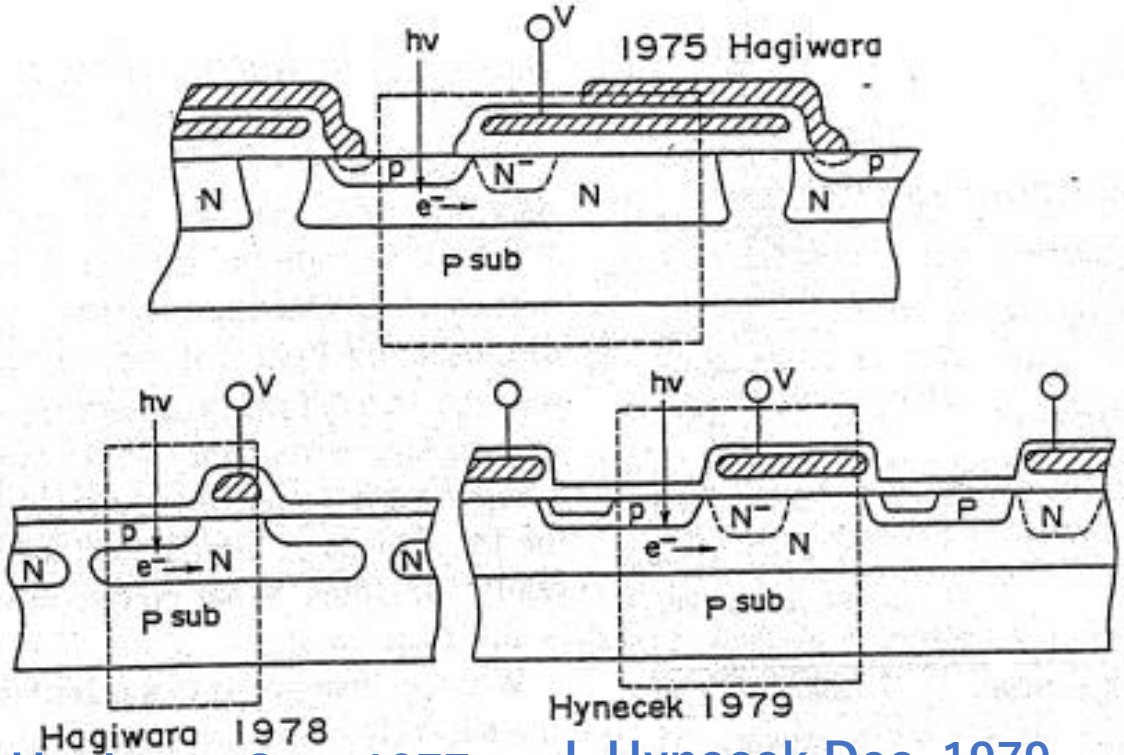


Fig. 7. Relative spectrum response. The relative response of the bipolar-type SiO_2–P2–N1–P1–SUB structure is compared with poly–SiO_2–N2–P(SUB) structures of the polysilicon thickness of 50 and 150 nm.

High-Density and High-Quality Frame Transfer CCD Imager with Very Low Smear, Low Dark Current, and Very High Blue Sensitivity

Yoshiaki Hagiwara, *Member, IEEE*

Y.D. Hagiwara Nov 10, 1975

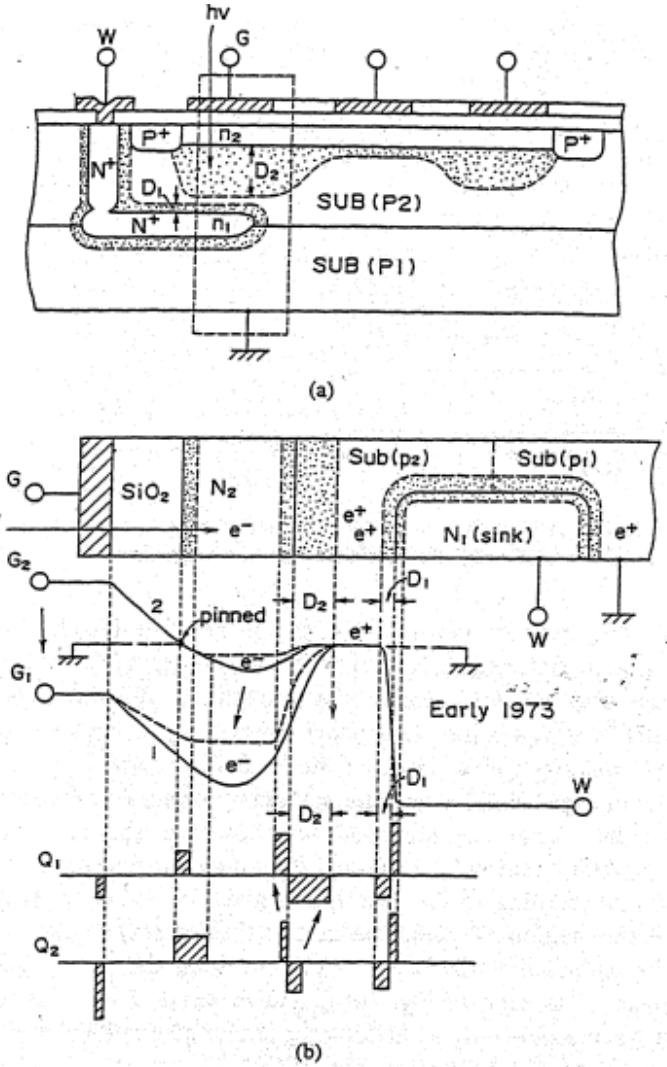


Y.D. Hagiwara Sep, 1977

J. Hynecek Dec, 1979

[16] J. Hynecek, "Virtual phase CCD technology," in *IEEE Proc. IEDM*, Dec. 1979, pp. 611–614.

J.M. Early Dec 3, 1973



[17] J. M. Early, U.S. Patent 3896485, Dec. 3, 1973.

The First Pinned Photodiode was invented by Hagiwara at Sony in 1975 in order to realize the in-pixel electric shutter function. The evidence is given in the Japanese patent application JPA1975-127646, which defined the pinned-surface triple-junction dynamic-thyristor type Pinned Photodiode.

The evidence are given in the Japanese Patent Applications, JPA1975-127646, JPA1975-127646 and JPA1975-134985.

Fig 7 in JPA1975-127646

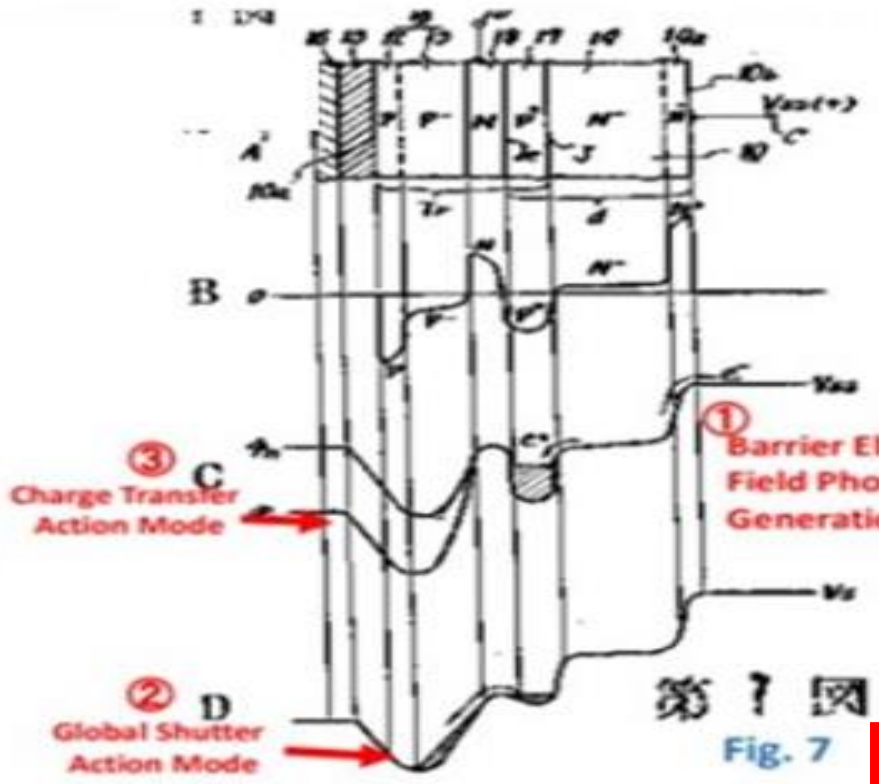


Fig 7 in JPA1975-127647

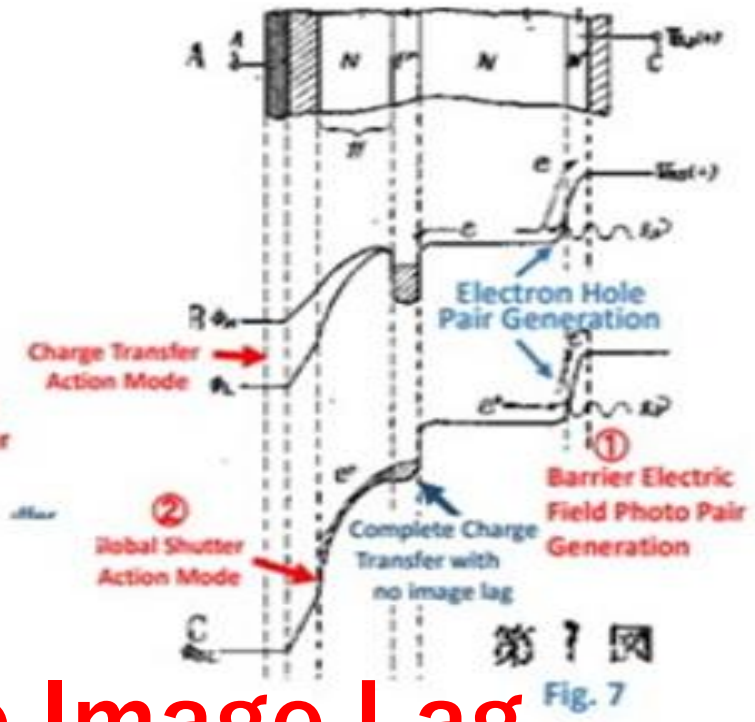
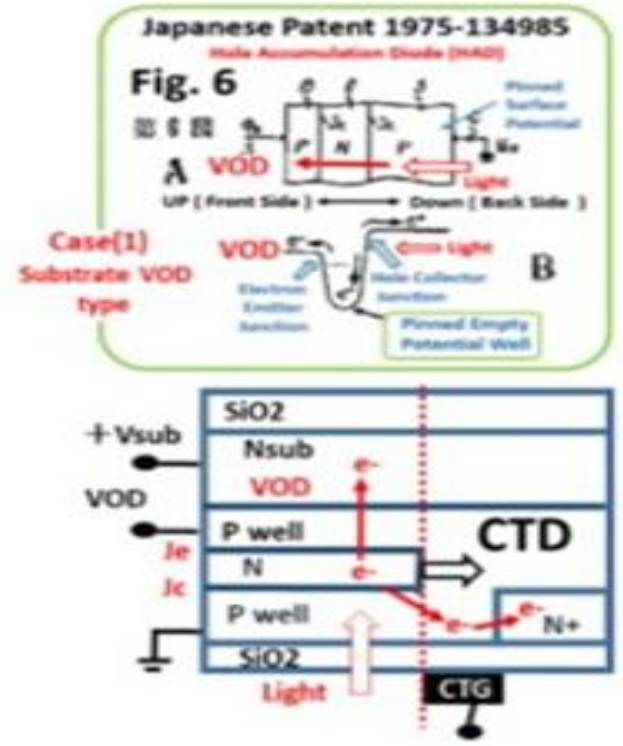


Fig 6 in JPA1975-134985



No Image Lag

PPD with in-pixel VOD function was drawn in Hagiwara Lab Note in Feb 1975.

SONY- Fairchild Patent War (1991-2000) on Pinned Photo Diode with Vertical OFD

CCD特許侵害訴訟

ソニー、逆転勝訴

NY東部地裁

日刊 7/16

電子機器の基幹部品である電荷結合素子（CCD）の特許侵害訴訟を審理していた米ニューヨーク東部地裁は、ソニー（社長出井伸之氏）を訴えていた米ローラル・フェアチャイルド社の主張を退け、ソニー勝訴の判決を下した。同訴訟はソニーが特許を侵害しているとの陪審員評決が二月に出ていたが、ソニーが逆転勝訴した。フェアチャイルドは日立製作所、東芝など日欧の大手電機メーカー二十社以上を同様の訴訟で訴えており、ソニーの勝訴は他社の審理にも影響も与えそうだ。

ソニーが十五日明らかにしたところによると、ニューヨーク東部地裁は「ソニー製のCCDはローラル・フェアチャイルド社の二件の特許に抵触しない」との判決を下し、陪審員の評決を破棄した。フェアチャイルドは控訴するかどうかの態度をまだ表明していないという。

CCDはカメラ一体型VTRやファクスなどの電子機器に使われる光学部品で「電子の目」と呼ばれる基幹部品。フェアチャイルドは自社が保有するCCDの製造プロセスと構造に関する二件の特許を侵害しているとして九一年九月、ソニーのほか日立、東芝、仲電気工業、松下など日欧の大手各社を訴えていた。ソニーは「当社のCCDはフェアチャイルドの特許とは異なる製造プロセスと構造を採用していると主張してきたが、その正当性が認められた」としている。ただフェアチャイルドが控訴すれば、裁判が再び長期化する可能性も残っている。

From Japanese News Paper, July 16, 1996.

1996 年 7 月　　日刊工業新聞記事から

（2000 年 1 月米国最高裁で最終決着ソニー勝訴）

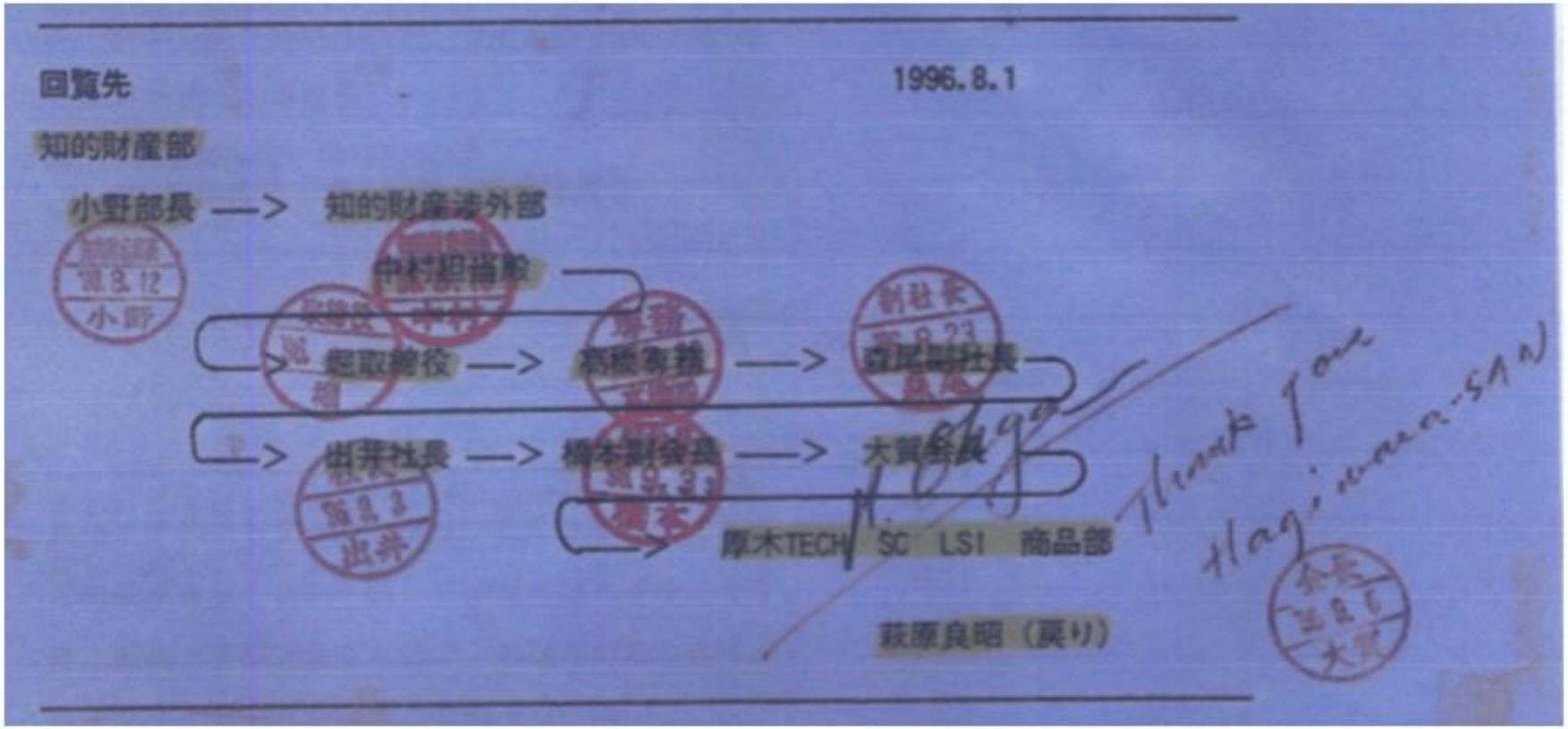
In January 2000, the US supreme court made the final judgement favoring Sony claims. And the long SONY-Fairchild Patent War on the PDD with the built-in vertical overflow drain (VOD) ended.

SONY―Fairchild 社の特許戦争の終結は、SONYの勝利に終わった。

萩原は　別にSONYからお金をもらってやったわけでない。

世界の半導体大手のFairchild 社から萩原の1975 年特許が攻撃され、それを発明者である萩原が、自分の名誉を守るために、世界に訴え、萩原が自発的に行動に出た結果である。

当時のSONYの大賀会長、橋本副会長、出井社長からねぎらいの言葉を萩原はもらった。





1975年に萩原が発明したPNPN接合型のHADセンサーは電子シャッターを可能にする受光素子でしたが、その実用化には石川さんたち後輩のさらなる発明と開発努力が必要でした。その後１２年もの年月の努力の結果、石川さんたちは１９８７年、電子シャッターの実用化商品化に成功し、SONYの市場制覇が始まり、その遺産が今も後輩に継承されています。



萩原が担当したのは、あくまで半導体電子デバイス部品の技術開発です。実際のAIBOロボットは土井さんが、Play Stationは久夛良木さんが陣頭指揮をとり開発部隊を指導していました。土井さんと久夛良木さんたちはあくまで私たちの製品のユーザー側です。われわれのお客さまでした。

Finally the Sony-Fairchild Patent Wat(1991-2000) ended over the Sony HAD Sensor which is identical to the P+NPNsub junction type Pinned Photodiode with Vertical Overflow Drain, originally invented by Hagiwara at Sony in 1975.

And finally Hagiwara received for his 1975-134985 Japanese Patent officially , the First Patent Award from Mr. Ando, Sony president in April, 2001 after more 26 years of struggles since his invention.


SONY

2000年度

発明考案実施褒賞

1級

萩原 良昭 殿

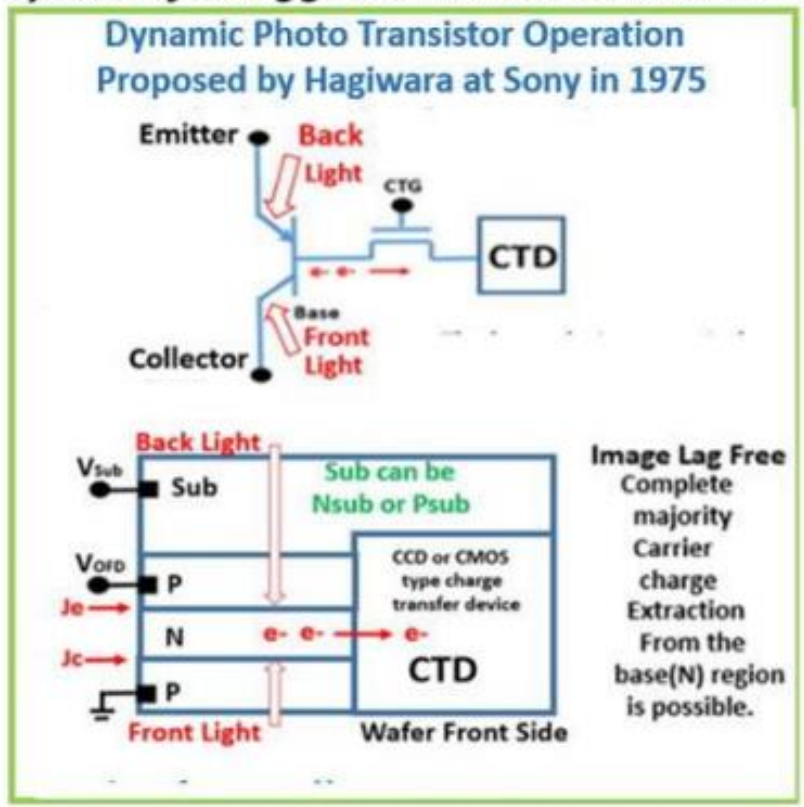
特許第1215101号

固体撮像装置

貴発明は卓越した創造性および先見性により
会社に対し顕著な貢献がありましたので
発明考案規定に基づき
ここに本賞を贈りこれを賞します

2001年4月26日

ソニー株式会社
社長



Pinned_Photodiode_Adopted_for_Back_Illuminated_CMOS_Image_Sensors

announce_in_public_by_Sony_on_2020_06_26

https://www.sony.com/en/SonyInfo/News/notice/20200626/

Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara).

Japanese Patent No. 1215101（Japanese Patent Application 1975-134985） by Yoshiaki Hagiwara

Pinned_Photodiode_Adopted_for_Back_Illuminated_CMOS_Image_Sensors

announce_in_public_by_Sony_on_2020_06_26

https://www.sony.com/en/SonyInfo/News/notice/20200626/

After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)).

Pinned_Photodiode_Adopted_for_Back_Illuminated_CMOS_Image_Sensors announce_in_public_by_Sony_on_2020_06_26

https://www.sony.com/en/SonyInfo/News/notice/20200626/

In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world.

In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

Semiconductor History Museum of Japan

1975-85

Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

~ Discrete Semiconductor/Others ~

Semiconductor History Museum of Japan says that Hagiwara invented Pinned Photodiode.

In 1975, Sony proposed using a PNP transistor as the photodetector [3]. By providing a P^+ layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated to improve the light sensitivity greatly. It was a basic proposal for a pinned photodiode with a P^+ layer on the surface of the light receiving part.

【3】Y. Hagiwara, Japanese Patent JP1975—134985

ELECTRICAL ENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

Asked 8 years, 10 months ago Modified 2 years, 8 months ago Viewed 6k times

6

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

Share Cite Follow

edited Aug 16, 2018 at 19:17

answered Sep 21, 2013 at 14:34



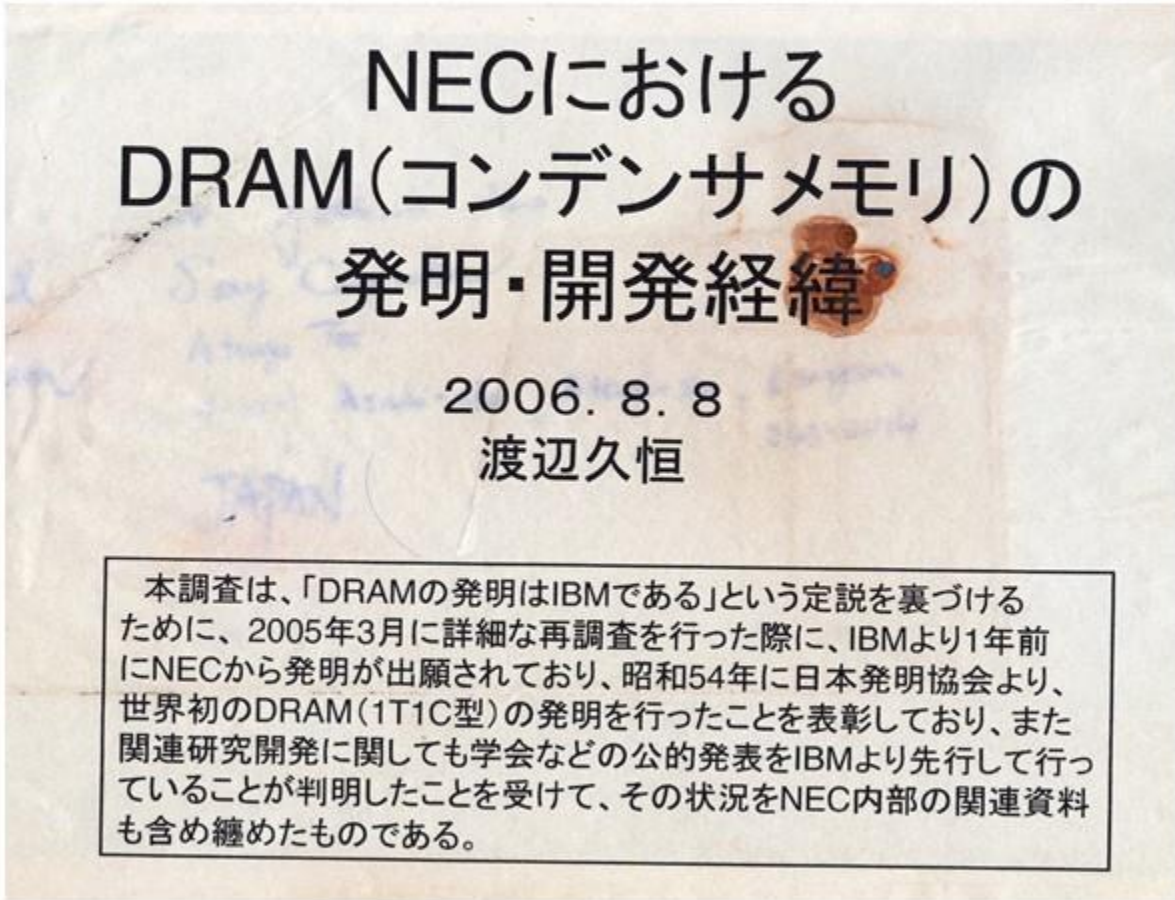
placeholder

29.6k ● 10 ● 60 ● 110

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

日本がどうしてDRAMビジネスで世界を制覇できたか？

その産業の起爆剤は 1T1CのDynamic 容量型のDRAMの発明にあります。しかし国際学会でその発明をPRしなかった事でNECの真の1T1C型DRAMの発明者の名前は世界的には広く認知されないままになっています。



NECにおける
DRAM（コンデンサメモリ）の
発明・開発経緯

2006. 8. 8
渡辺久恒

本調査は、「DRAMの発明はIBMである」という定説を裏づけるために、2005年3月に詳細な再調査を行った際に、IBMより1年前にNECから発明が出願されており、昭和54年に日本発明協会より、世界初のDRAM（1T1C型）の発明を行ったことを表彰しており、また関連研究開発に関しても学会などの公的発表をIBMより先行して行っていることが判明したことを受けて、その状況をNEC内部の関連資料も含め纏めたものである。

https://www.shmj.or.jp/museum2010/exhibi718.html

https://www.nanonet.go.jp/ntjb_pdf/v4n6-1.pdf



株式会社 EUVL 基盤開発センター 渡辺久恒社長

1943 年札幌生まれ．早稲田大学電気通信学科，同修士，名古屋大学応用物理学博士課程修了．日本電気（株）で半導体デバイス，量子構造基礎などの研究開発に従事．同社中央研究所長，執行役員，（株）日本電気特許技術情報センター代表取締役社長，（株）半導体先端テクノロジーズ（Selete）代表取締役社長　兼　半導体 MIRAI プロジェクトのプロジェクト第 3 期リーダを経て現職．JST・CREST プロジェクト研究総括．

The First Pinned Photodiode was invented by Hagiwara at Sony in 1975 in order to realize the in-pixel electric shutter function. The evidence is given in the Japanese patent application JPA1975-127646, which defined the pinned-surface triple-junction dynamic-thyristor type Pinned Photodiode.

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Fig 7 in JPA1975-127646

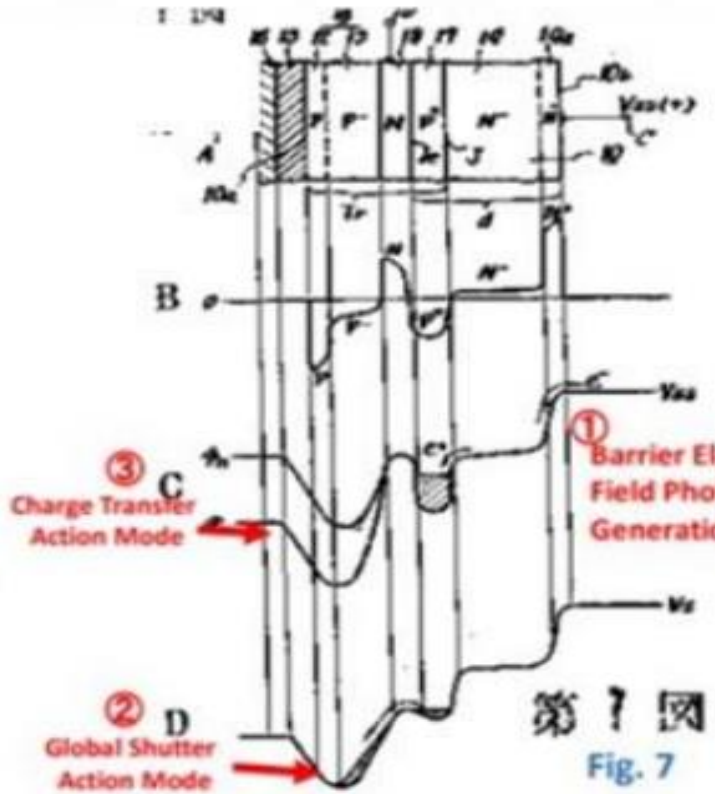


Fig 7 in JPA1975-127647

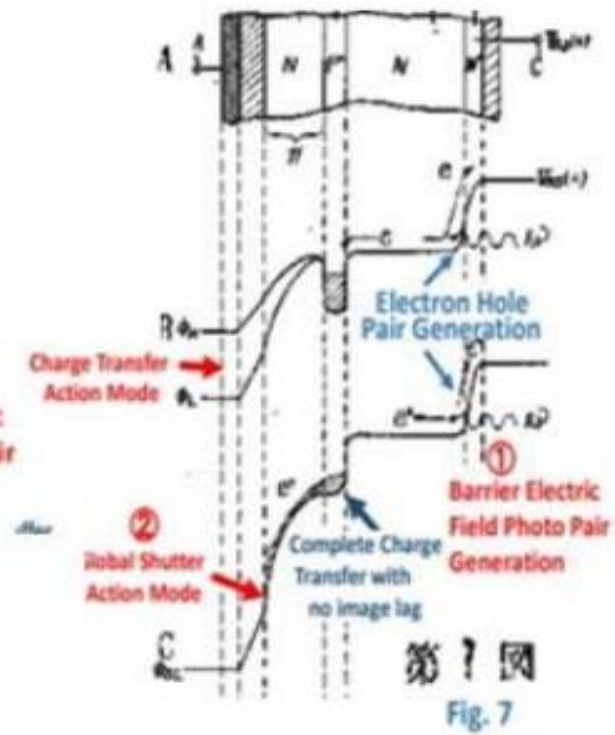
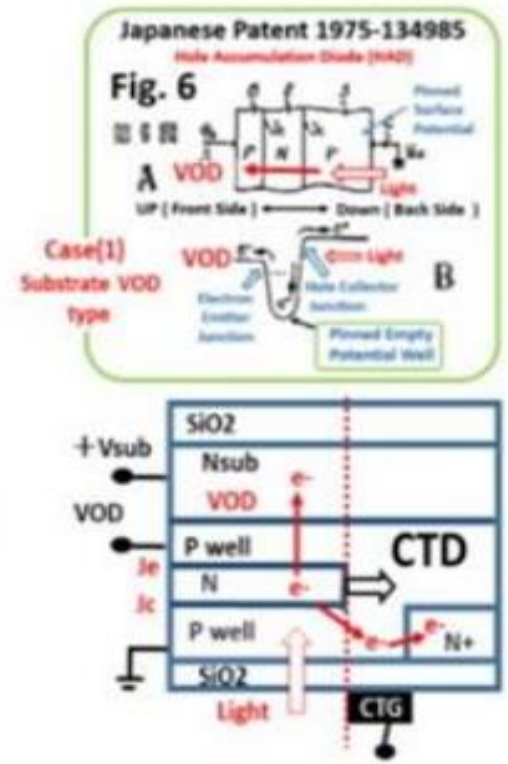
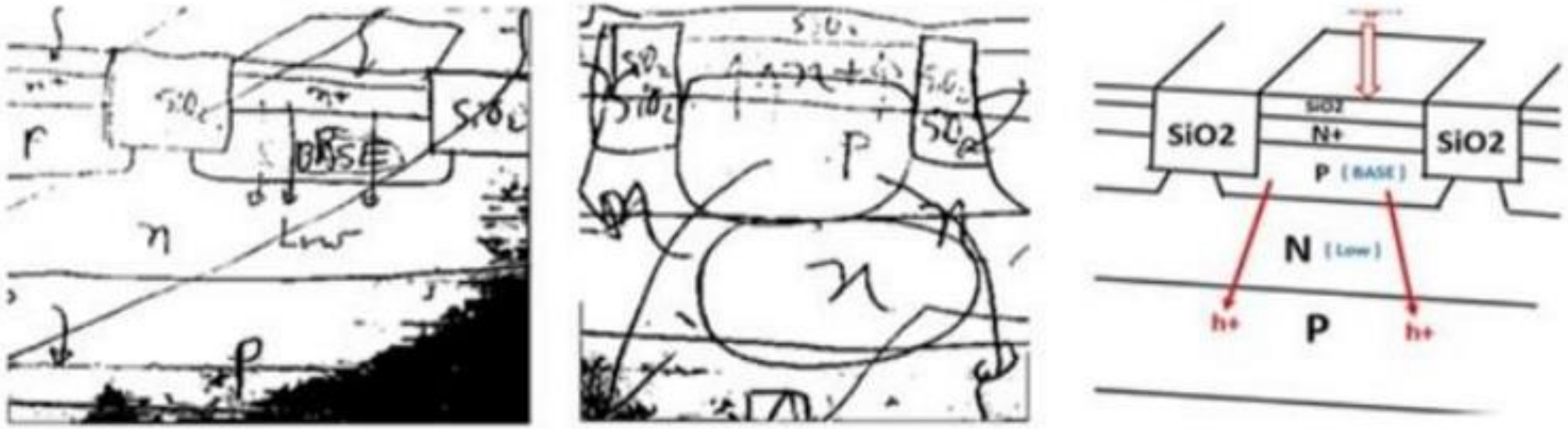


Fig 6 in JPA1975-134985



PPD with in-pixel VOD function was drawn in Hagiwara Lab Note in Feb 1975.

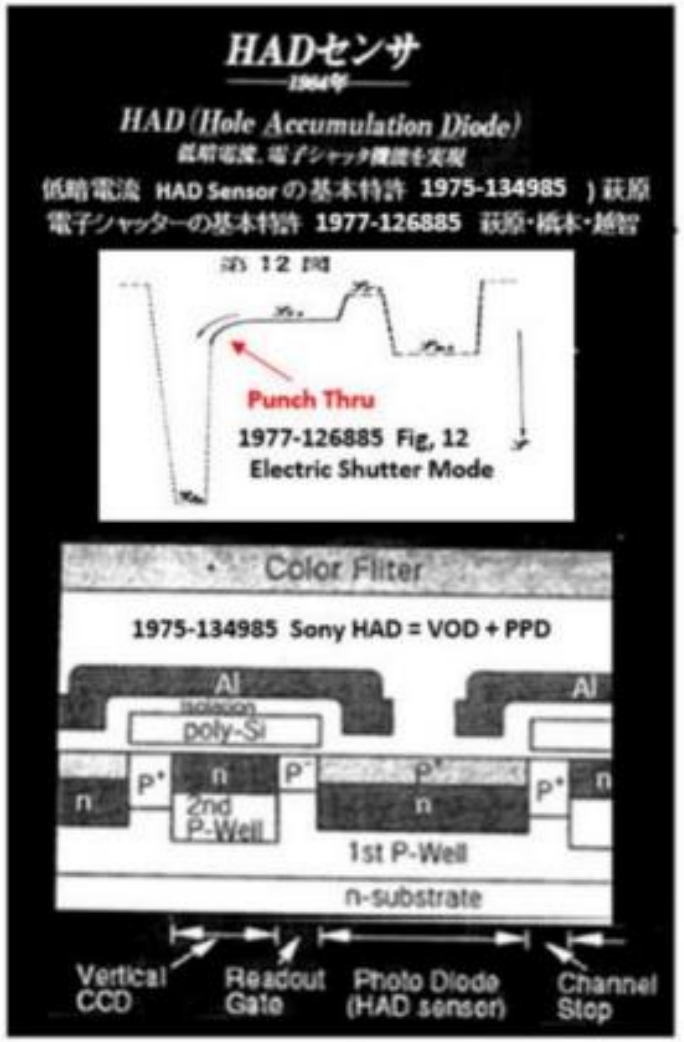


Hagiwara wrote the PPD patent form applied to Sony IP Office on March 5, 1975.

The surface needs be pinned and fixed to achieve the complete charge transfer mode with no image lag feature, which is a necessary condition to realize the Electric function. Any photodiode with the floating surface with some RC delay time constant cannot be used for electric shutter. See JPA1975-127646 and JPA1975-134985 (Japanese patent 1215101).

Hagiwara also proposed the thyristor type punch-thru clocking scheme, synchronized with the TV scanning system to achieve the electric shutter.

The Pinned Photodiode（Sony Original HAD sensor）Structure



(from SONY Product Catalog)

Electric Shutter Basic Patent Award
from Sony President Idei to Yoshiaki Hagiwara
for Japanese Patent 1977-126885 by Hagiwara



SONY- Fairchild Patent War (1991-2000) on Pinned Photo Diode with Vertical OFD

CCD特許侵害訴訟

ソニー、逆転勝訴

NY東部地裁

日刊 7/16

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From Japanese News Paper, July 16, 1996.

1996 年 7 月　　日刊工業新聞記事から

（2000 年 1 月米国最高裁で最終決着ソニー勝訴）

In January 2000, the US supreme court made the final judgement favoring Sony claims. And the long SONY-Fairchild Patent War on the PDD with the built-in vertical overflow drain (VOD) ended.

E-MAIL communications on Sony-Fairchild Patent War

February 6, 1996

Evidence of Hagiwara contribution in the Patent War on the PPD VOD patent (Hagiwara JPA 1975-134985)

＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊

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(1)　当時の SONY 中央研究所所長の山田敏之さんからのメッセージ

****

Subject: CCD Patent Report

X-Mailer: Eurora-J(1.3.8.5-J13)

中研の山田です。

ずいぶん前になりますが、分厚いレポートを
送って頂きありがとうございました。

CCD 裁判は越智さんはじめ関係者の大きな努力に
もかかわらず（一審での判決では）不本意な結果
となりましたが（その後逆転勝利となり）アメリ
カの裁判制度の問題点を如実に表しているような
気がします。

それはそれとして、この過程で萩原さんのこの
資料が越智さんにとっても大いに参考になった
ようです。

ご協力ありがとうございました。

CCD 開発史の一ページというか、読み物としても
面白く読ませて頂きました。

裁判の方はまだこれから延々と（最高裁まで）続く
でしょうが、引き続きご支援をお願いします。

萩原さんのことですから自分のやりたいことを
やりたいようにやっておられることと推察します。

私も少しその爪の垢を煎じて飲みたいものです。
すっかり遅くなりましたがひとこと御礼まで。

以上

****

(2)　当時の SONY 中央研究所副所長の越智成之さんからのメッセージ

****

Date: Tue. 6 Feb　9608:51:07 JST

To: hagiwara@mica.semicon.sony.co.jp(NanaeSato)

From:nanae@avzna.av.crl.sony.co.jp

Subject:testimony3

Cc: msato@saccd.semicon.sony.co.jp,ochi@av.crl.sony.co.jp

X-Mailer: Eurora-J(1.3.8-J13)

おはようございます。

中央越智副所長からの e-mail を forward します。

お忙しいのにもかかわらず、
多大なご協力を下さいまして
ありがとうございました。

****

(3)　SONY の森尾副社長、高橋専務、山田所長に対して
　米国滞在の越智さんから発信された裁判に関する報告

****

>X-POP3-Rcpt: nanae@avzna

>Date: Tue. 6, Feb 96 06:48:53 JST

>To: m-morio@cv.sony.co.jp, takahasi@rd.sony.co.jp,

>hashi@re.sony.co.jp,tyamada@dpo.crl.sony.co.jp

>Cc: ochi@av.crl.sony.jp,

>msato@saccd.semiocn.sony.co.jp,nanae@av.crl.sony.co.jp

>Subject: testimony3

>From: 越智　成之　<ochi@av.crl.sony.co.jp>

>X-Mailer: Winbiff[version 1.50 beta1]

>私に対する証人尋問が終わりました。

>direct exam は主に

>74 年の Amelio（Apple Computer の社長になってしまいましたが）

>特許や粂沢、松本レポートより前に、

> 既に　two phase overlapping gate

>buried channel self-aligned implanted barrier

>が考えられていたことを、

>Caltech（Bower, McGill, Daimon-Hagiwara ほか）

>と Hughes(Erb, Su ほか）と Sony（三船,二神ほか）

>等の資料を使い、実証致しました。

>cross exam は米国政府の御用達と独禁法と粂沢レポートに

>対する先方からの攻撃が中心でしたがどれも不発に終わりました。

>特に、Caltech の　Dr. Daimon(Hagiwara）が

>75 年 2 月 20 日にソニーに入社している事実が

>ショックを与えたようで、質問が止まって

>しまいました。

>Prof. Bower からも、Dr. Daimon（Hagiwara)が Caltech から

>Sony に(埋め込み型)CCD の Ion Implantation 構造

>（ISSCC1974 で学会発表ずみでその後中研時代には

>P+NPNsub 接合の　Pinned Photo Diode 構造の特許を出願し

>その Ion Implantation 構造解析に活用した）解析技術を

>持ち込んだ事実の Story の流れがすばらしいとのことでした。

>佐藤真木さん佐藤七重さん恐れ入りますが、

>感謝の気持ちを込めて、この e-mail を

>萩原良昭さんに forward してください。

>萩原さんはこの 2 晩で 100 ページ以上にも

>及ぶ個人資料を fax で送ってくれました。

>馬橋さんの証言も成功裏に終わり、

>今後弁護士と今後の相談を致します。

>越智

＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊

Finally the Sony-Fairchild Patent Wat(1991-2000) ended over the Sony HAD Sensor which is identical to the P+NPNsub junction type Pinned Photodiode with Vertical Overflow Drain, originally invented by Hagiwara at Sony in 1975.

And finally Hagiwara received for his 1975-134985 Japanese Patent officially , the First Patent Award from Mr. Ando, Sony president in April, 2001 after more 26 years of struggles since his invention.


SONY

2000年度

発明考案実施褒賞

1級

萩原 良昭 殿

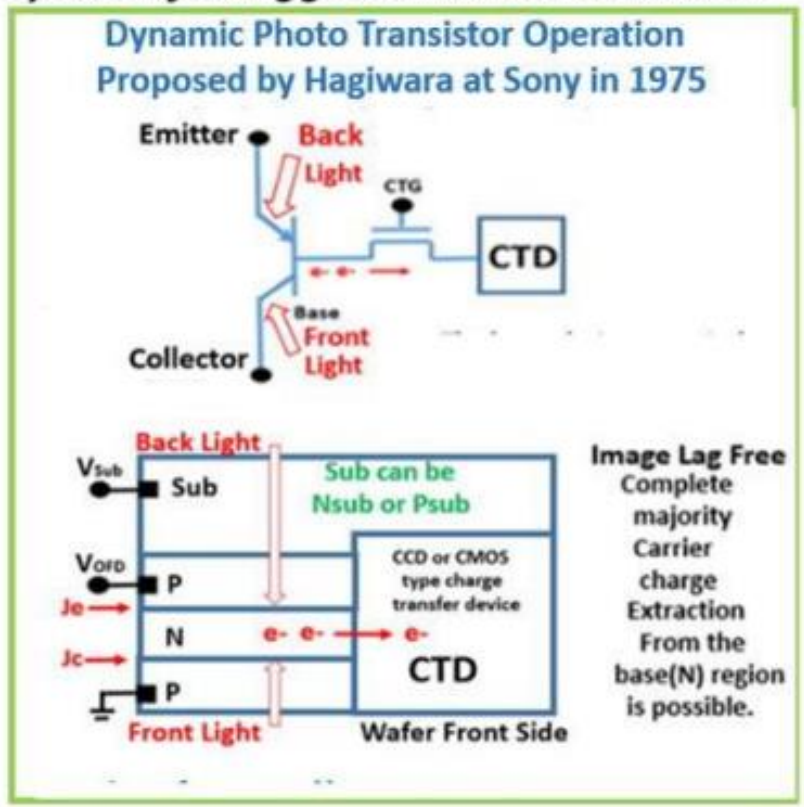
特許第1215101号

固体撮像装置

貴発明は卓越した創造性および先見性により
会社に対し顕著な貢献がありましたので
発明考案規定に基づき
ここに本賞を贈りこれを賞します

2001年4月26日

ソニー株式会社
社長



Invention and Historical Development Efforts of Pinned Photodiode and Electric Shutter

2019



Hagiwara at Sony Kumamoto Tech Center
in 2017, 2019 and 2022.

2001



1. Introduction
2. Patent Wars on Pinned Photodiode
3. Double Junction type Solar Cell

1980



1996



Hagiwara also visited Sony Atsugi-Tech Center in July 2020.

Invention and Historical Development Efforts of Pinned Photodiode and Electric Shutter

2019



Hagiwara at Sony Kumamoto Tech Center
in 2017, 2019 and 2022.

2001



3. Double Junction type Solar Cell

1980



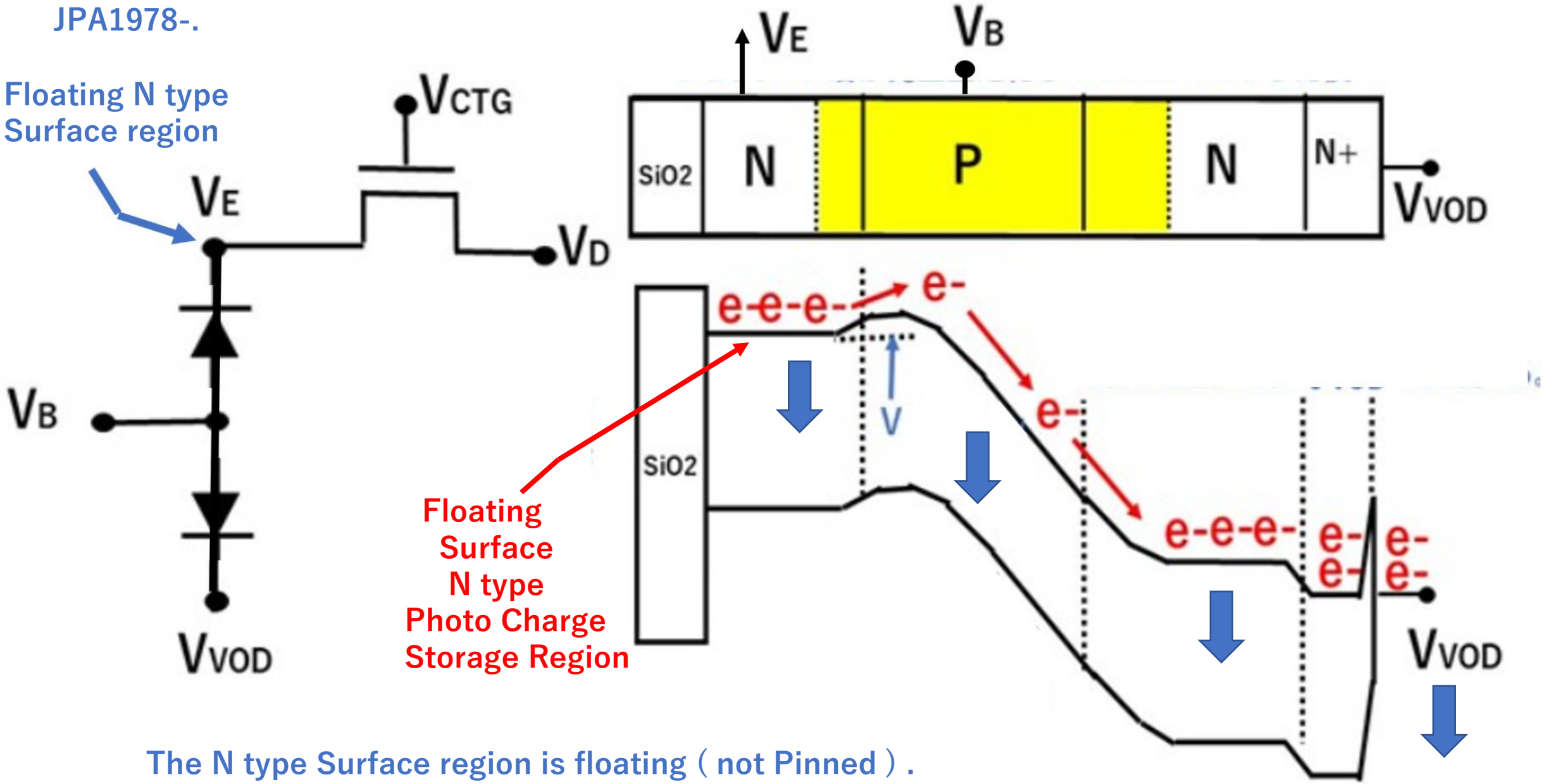
Hagiwara also visited Sony Atsugi-Tech Center in July 2020.

1996



JPA1978-.

Floating N type
Surface region



The N type Surface region is floating (not Pinned) .
The anti-blooming VOD does not function well because the N-type surface will also be pulled down as the VOD voltage is pulled down deeper.

NIKKEI MICRODEVICES 1987年10月号

pp.60～67

ICX022

38万画素に達した固体撮像素子

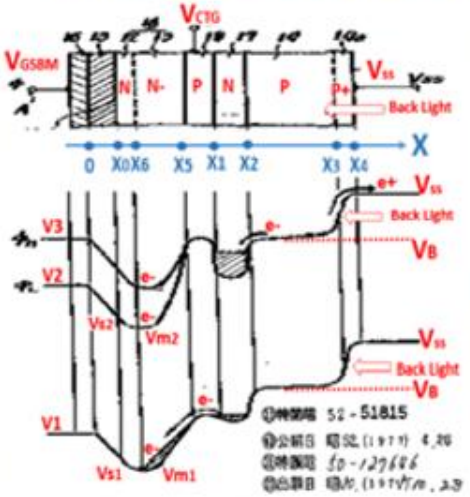
最低照度5 lxの高感度インターライン型CCD

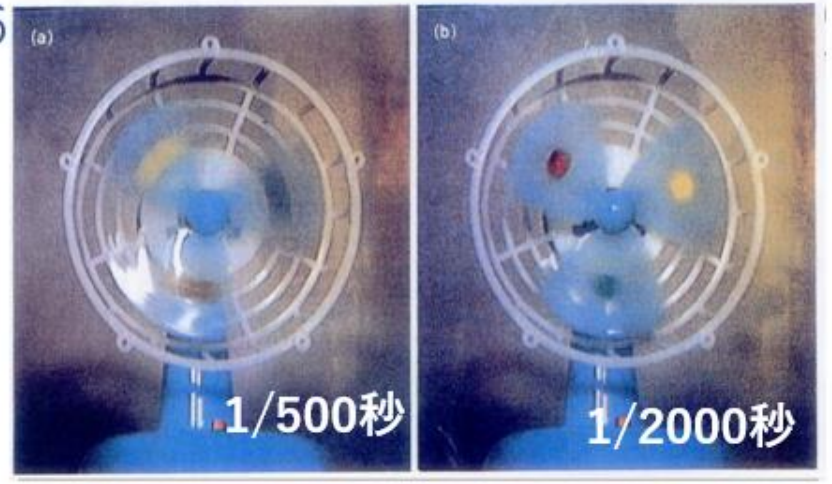
基板に余剰電荷を掃き出し,可変電子シャッタを実現

ソニー 半導体事業本部 CCD 事業部
浜崎 正治
鈴木 智行
賀川 能明
石川 貴久枝
宮田 克郎
ソニー国分セミコンダクタ CCD 製造部
神戸 秀夫

最も一般的な固体撮像素子であるインターライン型 CCD で,
2/3 インチで 38 万と大規模な画素数を持つ素子をソニーが製品化した。
画素面積が小さくなることで減少する信号量を確保するため,
縦型オーバーフロー・ドレインを採用して開口率を上げ,
補色フィルタで光の利用効率を上げた。
さらに界面準位からの暗電流を抑えている。
この結果, 81 dB のダイナミック・レンジが得られた。

JPA1975-127646







JPA1975-127646の図７と同一受光構造である。受光表面はGNDにピン留めされた、P+NPNsub 接合型、 すなわち Triple 接合型の Pinned Photodiode.



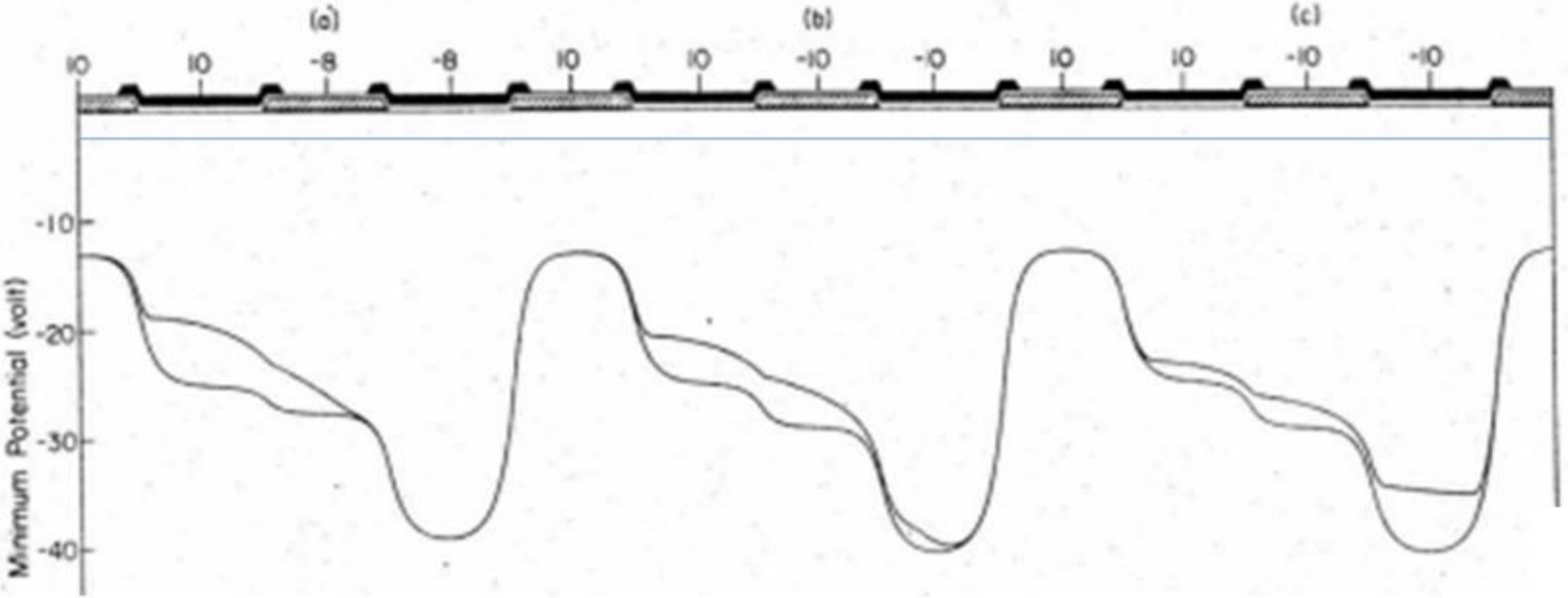
ICX022

電子shutterの動作原理の説明図

図 4

SONYの1987年発表の電子シャッター機能付き Hole Accumulation Diode (HAD) 受光素子構造

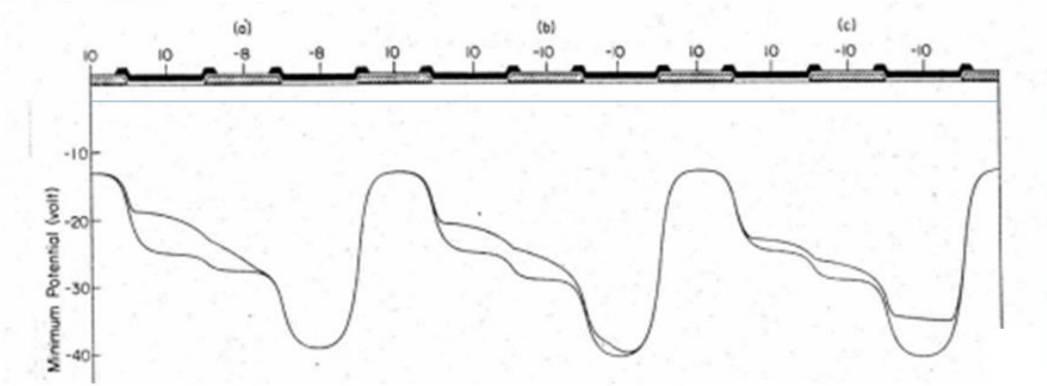
Exact Numerical Computer Simulation of Charge Transfer Action in Buried Channel CCD presented in ISSCC1974 by Yoshiaki Daimon-Hagiwara



for details see the PhD Thesis by Yoshiaki Daimon-Hagiwara on June 1975 from Caltech.

Caltech_1975_PhD_Thesis_Yoshiaki_Daimon_Hagihara.pdf

Exact Numerical Computer Simulation of Charge Transfer Action
in Buried Channel CCD presented in ISSCC1974 by Yoshiaki Daimon-Hagiwara



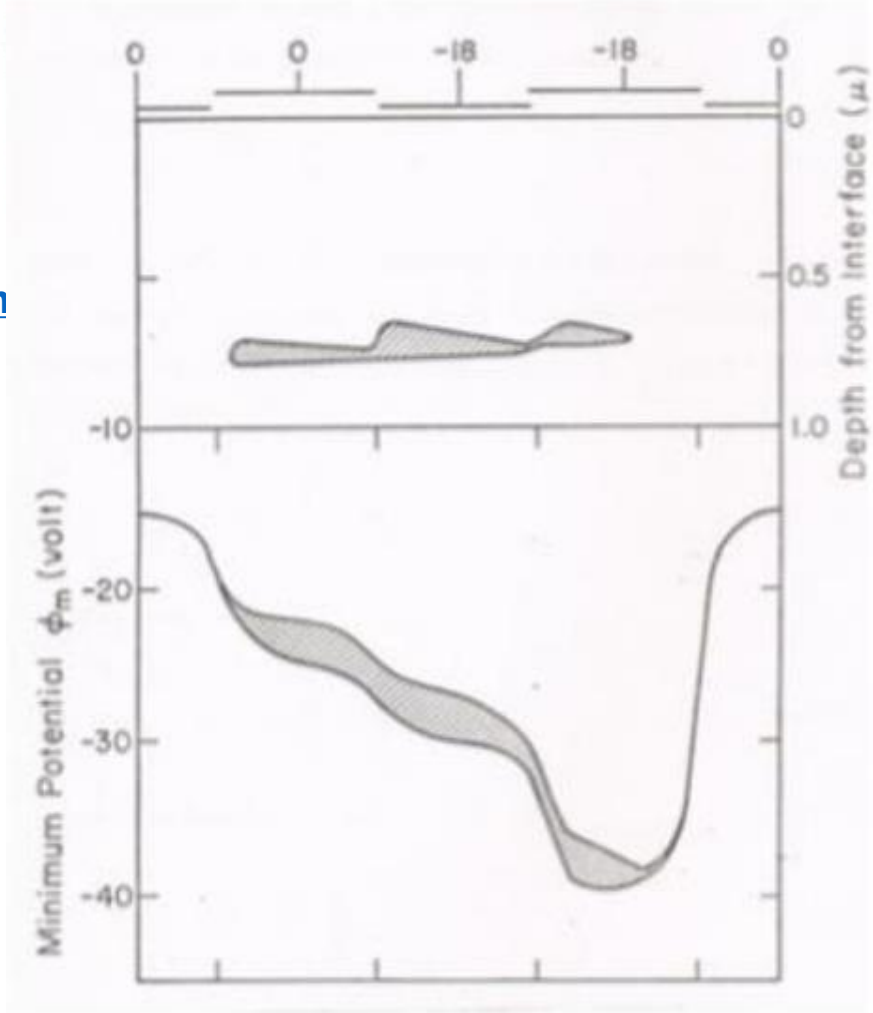
for details see the PhD Thesis by Yoshiaki Daimon-Hagiwara on June 1975 from Caltech.

[Caltech_1975_PhD_Thesis_Yoshiaki_Daimon_Hagih]



Prof. James McCaldin and Hagiwara

My PhD thesis paper
on buried channel CCD
at ISSCC1974, in Philadelphia, USA





Prof. T. C. McGill



Prof. C. A. Mead

True History of Photodiode

(1) Single Junction Type Dynamic Photodiode was used in image sensors before 1970

(2) CCD/MOS type dynamic Photodiode was invented in 1970 with no image lag with the Pinned Gate.

(3) Double Junction type Dynamic Photodiode invented by Philips in June 9, 1975 with RC delay time.

(4) Triple Junction type Dynamic Photodiode with the pinned surface invented by Sony in Oct 23, 1975.



⑪特開昭 51－150288

⑬公開日 昭51.(1976) 12 23

㉑特願昭 51－65705

㉒出願日 昭51.(1976) 6.7

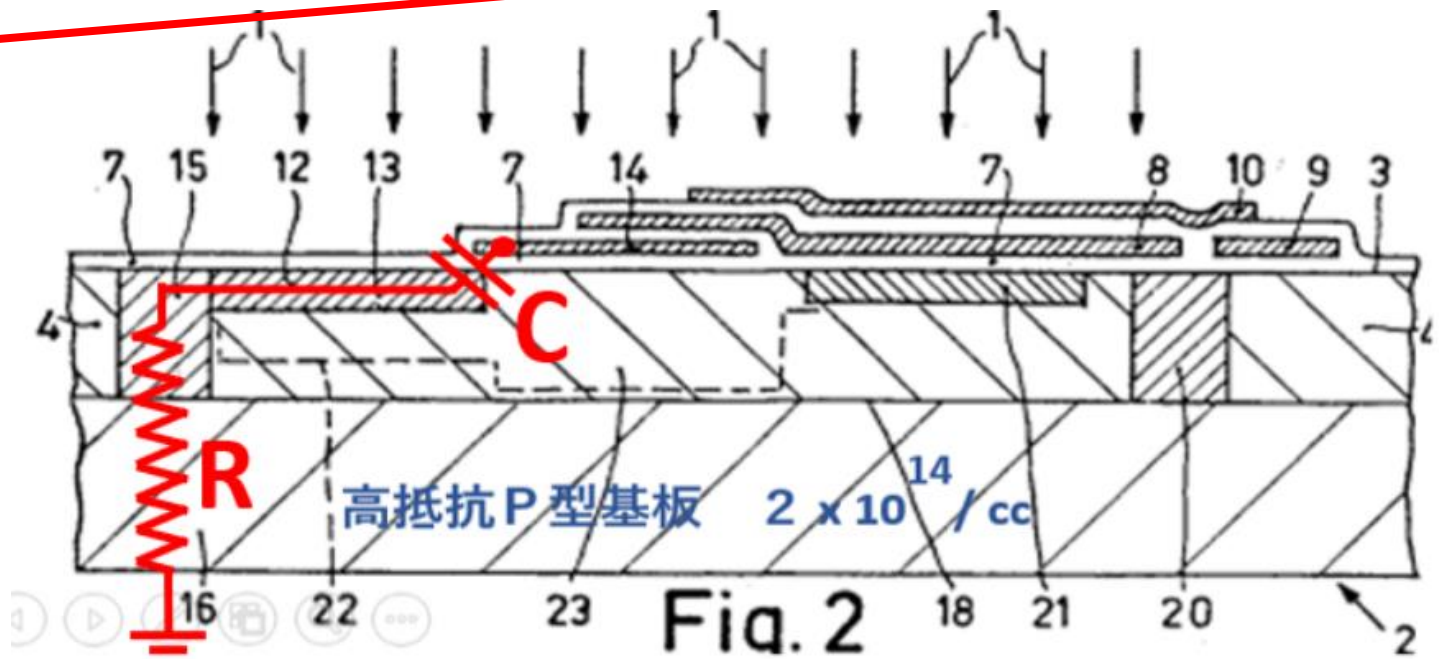


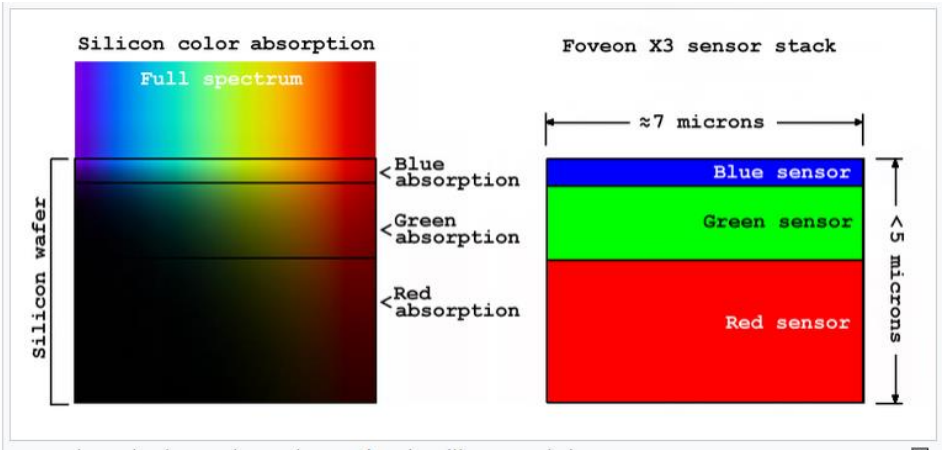
Fig. 2

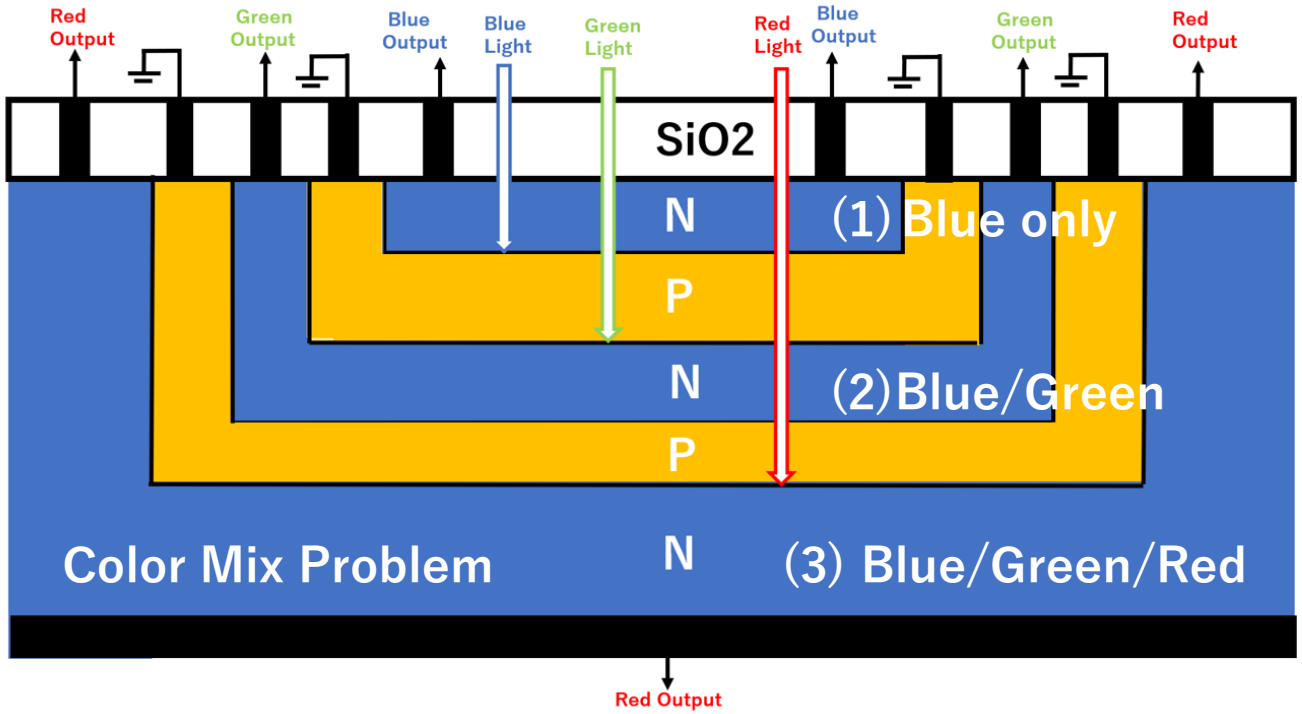
JPA1976-150288(Netherland Patent 7506795, priority June 7, 1975)

https://en.wikipedia.org/wiki/Foveon_X3_sensor

Foveon X3 sensor

From Wikipedia, the free encyclopedia





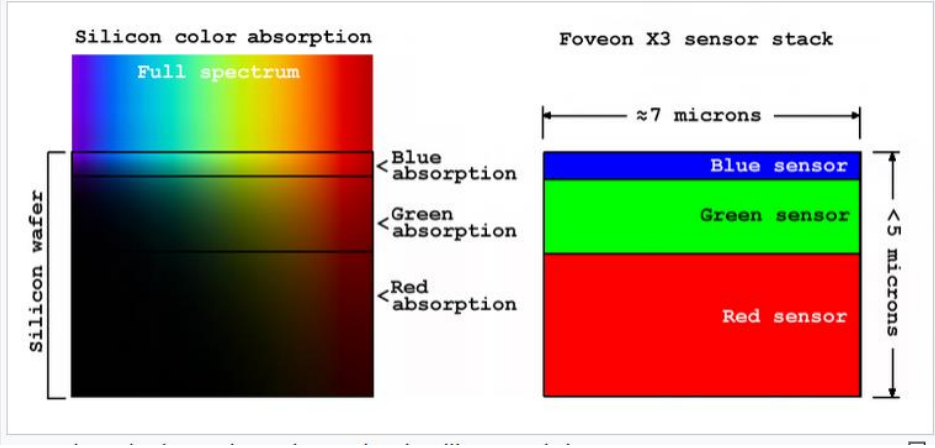
Light gathering and low-light performance

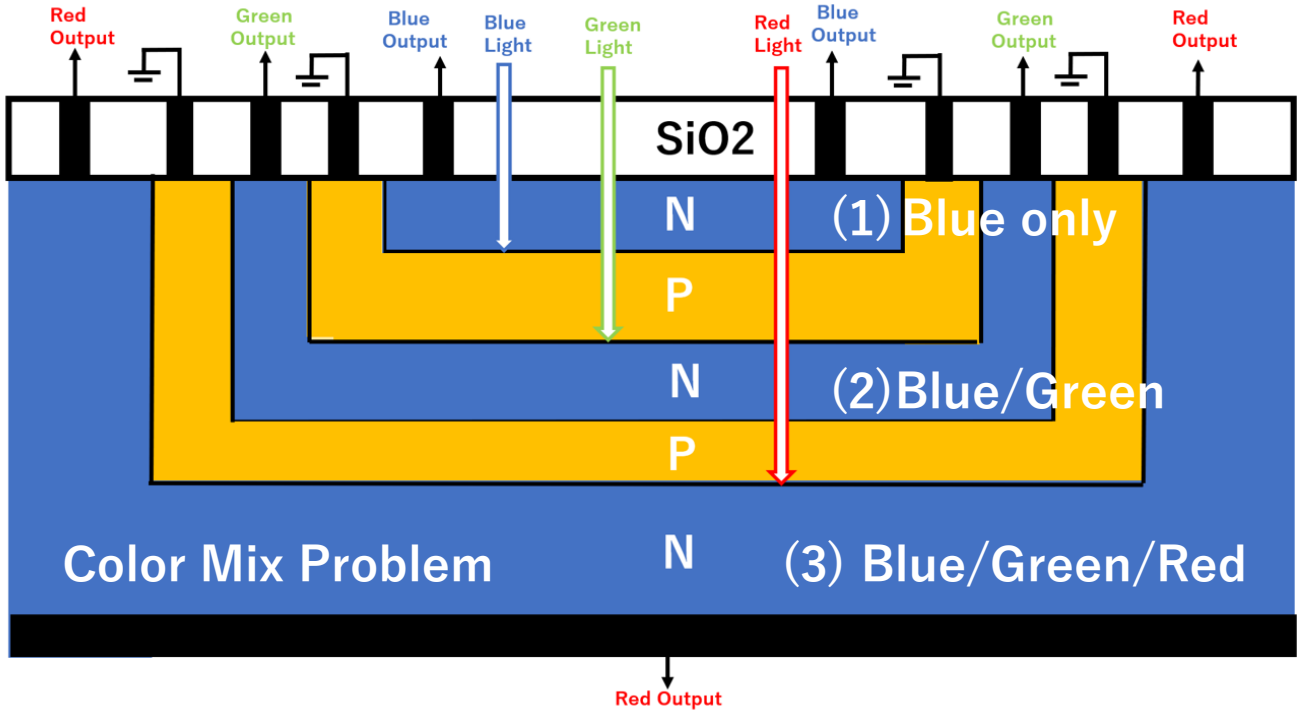
The Foveon X3 photosensor can detect more photons entering the camera than a mosaic sensor, because each of the color filters overlaying each photosite of a mosaic sensor passes only one of the primary colors and absorbs the other two. The absorption of these colors reduces the total amount of light gathered by the sensor and destroys much of the information about the color of the light impinging on each sensor element. Although the Foveon X3 has a greater light-gathering ability, the individual layers do not respond as sharply to the respective colors; thus color-indicating information in the sensor's raw data requires an "aggressive" matrix (i.e., the removal of common-mode signals) to produce color data in a standard color space, which can increase color noise in low-light situations.[15]

https://en.wikipedia.org/wiki/Foveon_X3_sensor

Foveon X3 sensor

From Wikipedia, the free encyclopedia





The **Foveon X3 sensor** is a digital camera image sensor designed by Foveon, Inc., (now part of Sigma Corporation) and manufactured by Dongbu Electronics.[1] It uses an array of photosites that consist of three vertically stacked photodiodes. Each of the three stacked photodiodes has a different spectral sensitivity, allowing it to respond differently to different wavelengths.[2] The signals from the three photodiodes are then processed as additive color data that are transformed to a standard RGB color space.

The X3 sensor technology was first deployed in 2002 in the Sigma SD9 DSLR camera, and subsequently in the SD10, SD14, SD15, SD1 (including SD1 Merrill), the original mirrorless compact Sigma DP1 and Sigma DP2 in 2008 and 2009 respectively, the Sigma dp2 Quattro series from 2014, and the Sigma SD Quattro series from 2016. The development of the Foveon X3 technology is the subject of the 2005 book *The Silicon Eye* by George Gilder.

Japanese Patent JPA 1977-837

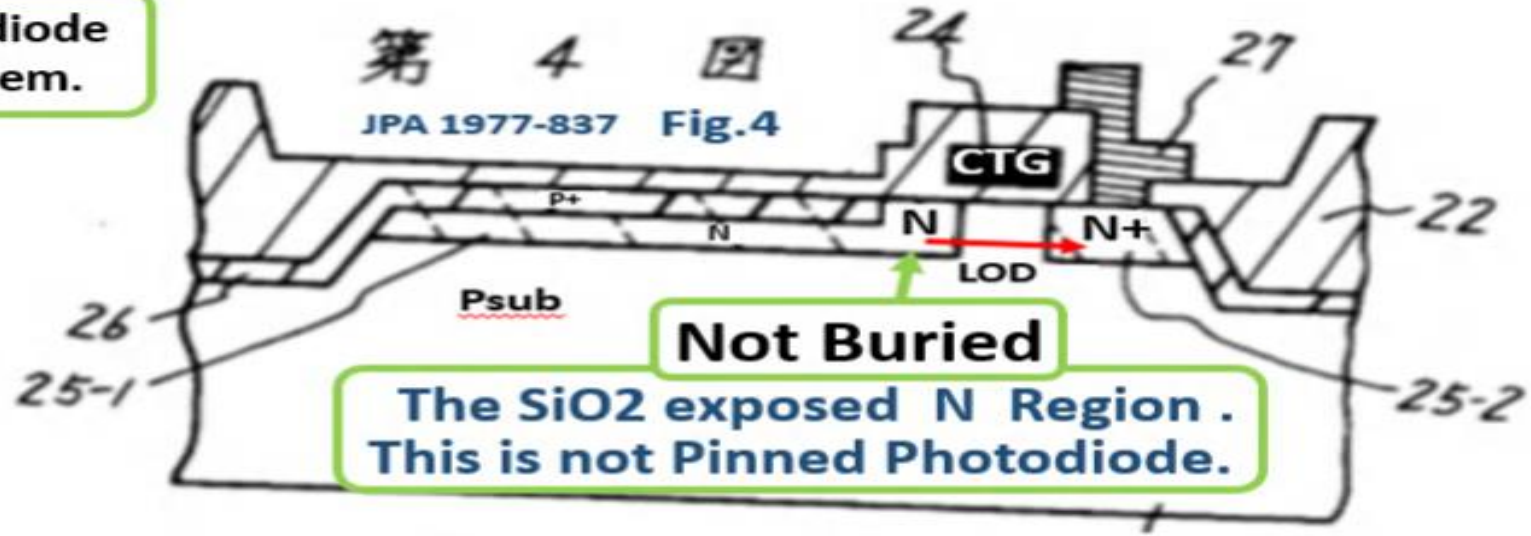
This patent is applied for the lateral overflow drain (LOD) function.
The excess charge is drained to the N+ lateral output drain (LOD).

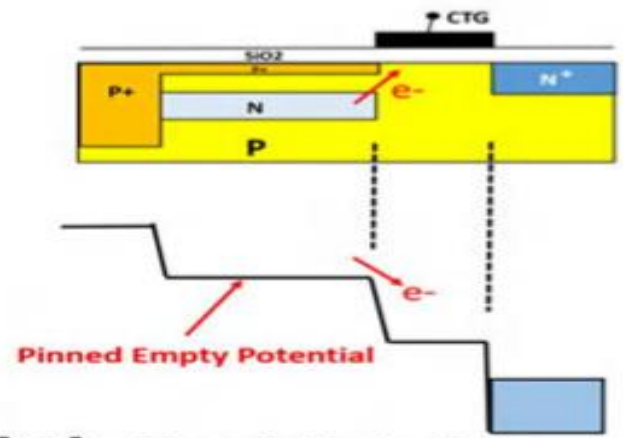
This SiO2 surface exposed photodiode has the serious Image lag problem.

㊵固体撮像装置

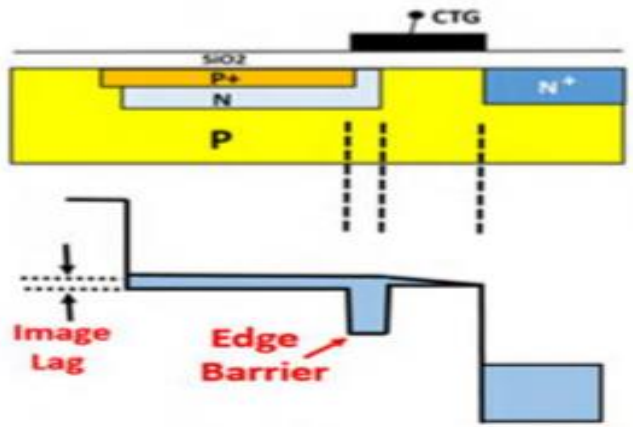
㉑特　　願　昭52—837
㉒出　　願　昭52(1977) 1 月10日
㉗発 明 者　小池紀雄
㊶特許出願公開　昭53—86516

第 4 図
JPA 1977-837 Fig.4

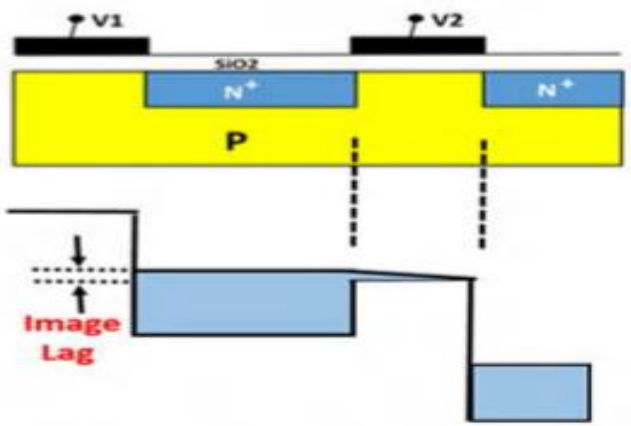




(1) Pinned Photodiode with No Image Lag



(2) Buried Photodiode with BBD Barrier



(3) Bucket Brigade Device (BBD)

JPA1978-1971 by T. Yamada at Toshiba, an invention of the in-pixel anti-blooming using the NPN junction photodiode with the floating N photo charge storage

⑲日本国特許庁(JP)

⑪特許出願公開

⑫公開特許公報(A)

昭54—95116

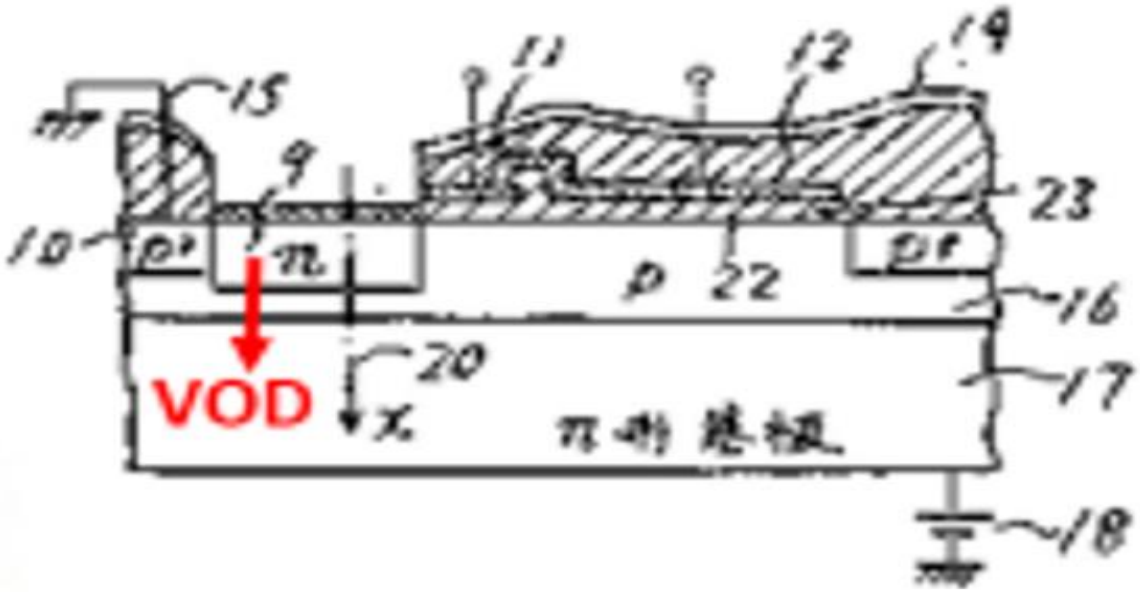
⑤固体撮像装置

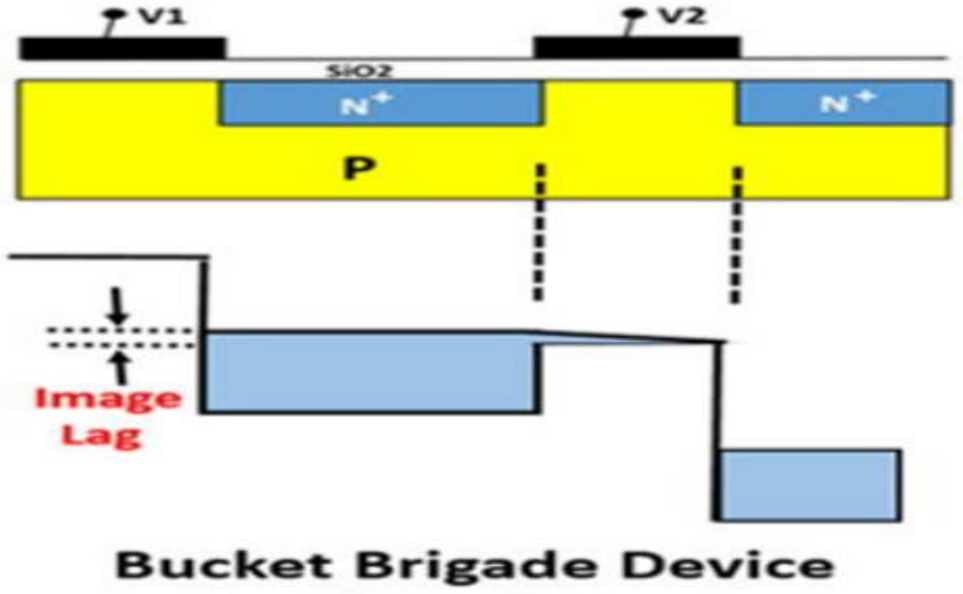
⑳特　　願　昭53—1971

㉒出　　願　昭53(1978)1月13日

㉓発　明　者　山田哲生

⑬公開　昭和54年(1979)7月27日



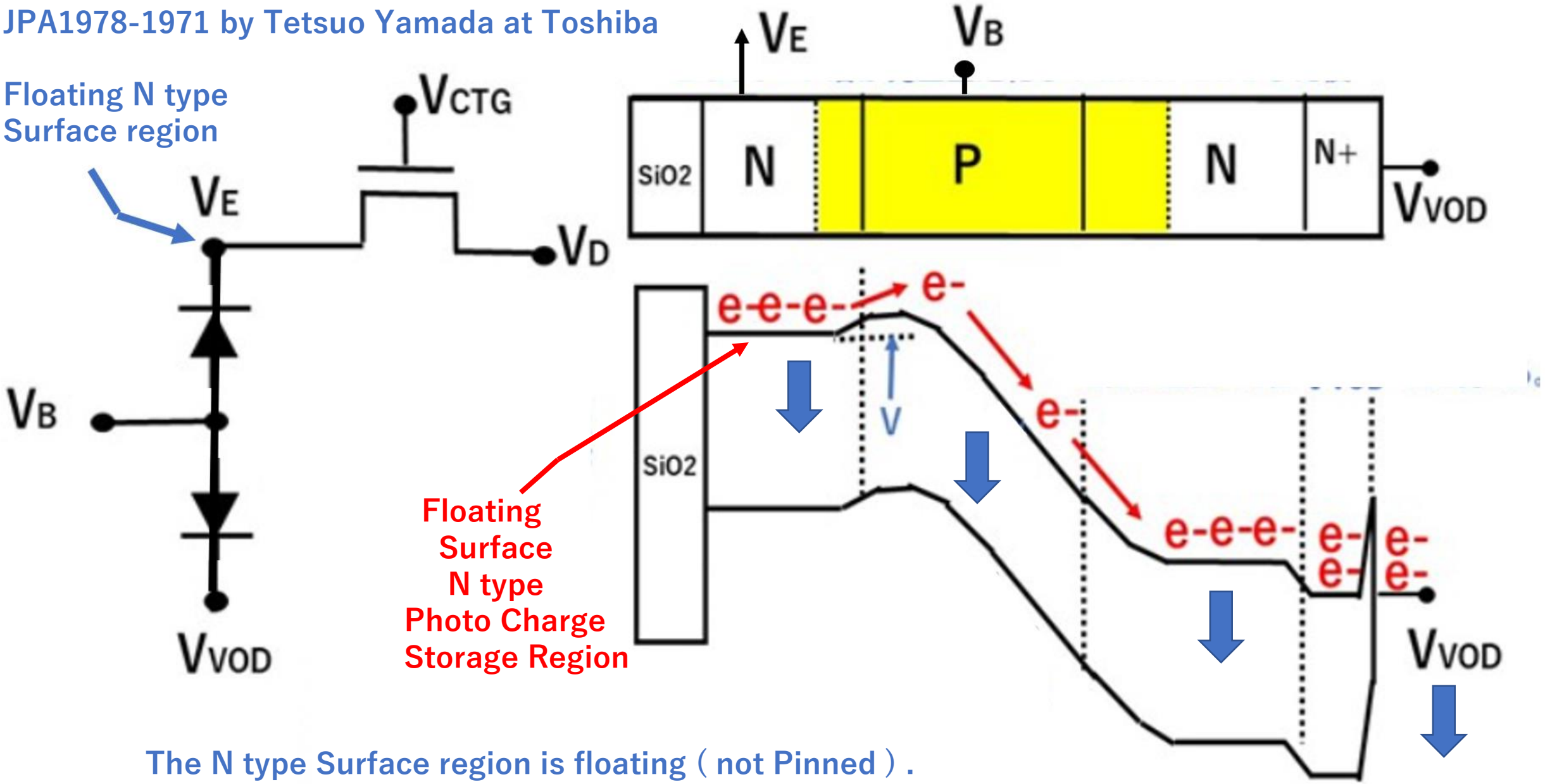


Bucket Brigade Device

This floating surface photodiode operates in the BBD type charge transfer mode with the serious image lag and the truth is that the in-pixel anti-blooming function does not function properly at high frequency.

JPA1978-1971 by Tetsuo Yamada at Toshiba

Floating N type
Surface region



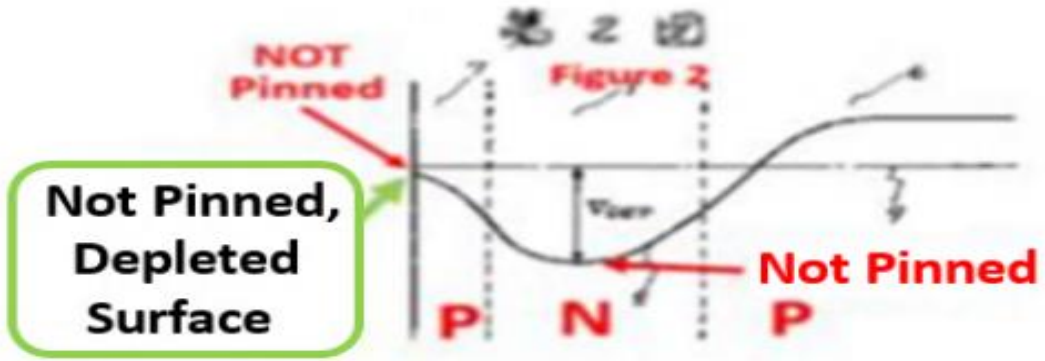
The N type Surface region is floating (not Pinned) .
The anti-blooming VOD does not function well because the N-type surface will also be pulled down as the VOD voltage is pulled down deeper.

JPA1980-138026 by N. Teranishi et al at NEC

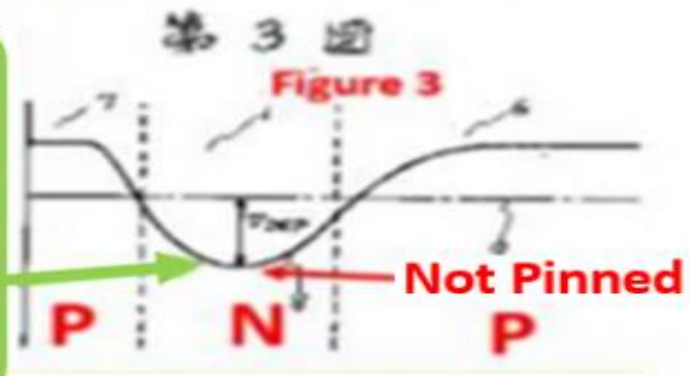
JPA 1980-138026

1980年10月2日出願

⑫特　　願　昭55—138026
⑫出　　願　昭55(1980)10月2日
⑫発　明　者　寺西信一
⑫発　明　者　石原保雄
⑫発　明　者　白木廣光



Not Pinned, Depleted Surface

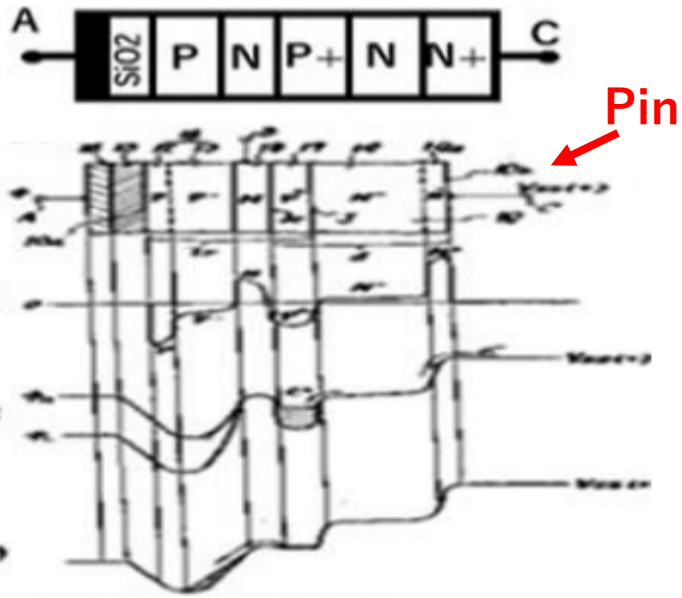


The surface P region is not Pinned. The Buried N region is still floating.

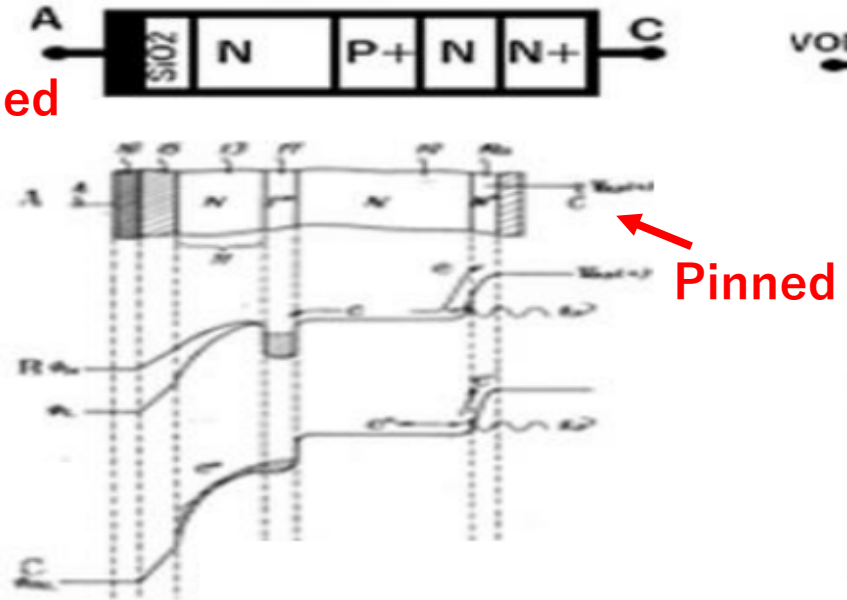
This patent is on the PNP junction type Buried Photodiode but NOT Pinned Photodiode. The surface P region is not pinned and grounded. The surface potential can be of any value depending on the floating buried N region potential, which is actually controlled by the substrate Psub potential which is grounded in this case, but in case of a built-in VOD function P+NPNsub junction photodiode, the P region potential is controlled by the Nsub VOD voltage and can be any value. The surface P region must be pinned by the adjacent P+ channel Stops region or the adjacent metal contact wiring.

Who invented Pinned Photodiode ?

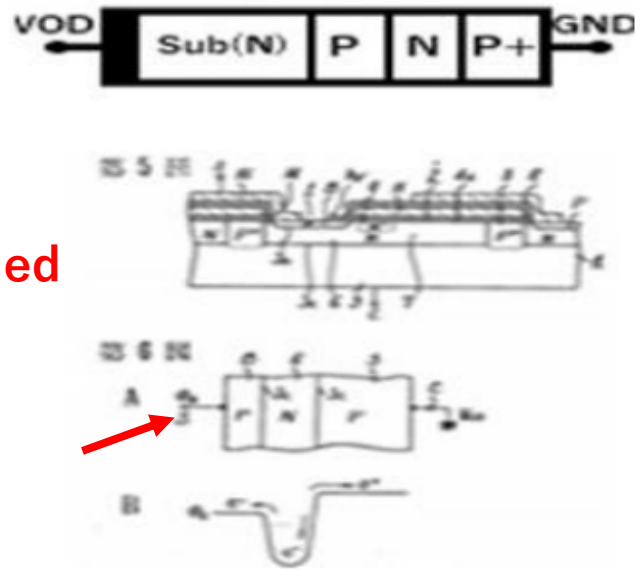
Hagiwara at Sony invented Pinned Photodiode in 1975. The evidence is give by the three Japanese patent applications, JPA1975-127646, JPA1975-127647 and JPA1975-134985. The first Pinned Photodiode was defined in October 23, 1975 as the N+NPNP triple junction(in Fig. 7 of JAP1975-127646) type and the N+NPN double junction type (in Fig. 7 of JAP1975-127647) type photodiodes with the N+ type pinned surface and the P type buried photo charge storage region with the complete charge transfer capability and the no-image-lag feature. The photo charge is transferred and drained to the CCD/MOS type charge storage buffer memory quicky by the strong punch-thru action. The second Pinned Photodiode was defined in November 10, 1975 as the PNP double junction (in Fig. 6 of JAP1975-134985) type photodiode with the vertical overflow drain action also with the complete charge transfer capability and the no-image-lag feature as evidence the empty potential well of the buried photo charge storage, completely depleted of the charge.



JPA1975-127646 Fig. 7



JPA1975-127647 Fig. 7



JPA1975-134985 Fig. 6

Proceedings of the 9th Conference on Solid State Devices, Tokyo, 1977;
Japanese Journal of Applied Physics, Volume 17 (1978) Supplement 17–1, pp. 255–261

Two Phase CCD with Narrow-Channel Transfer Regions

Yoshiaki DAIMON-HAGIWARA

Sony Corporation Research Center Yokohama 240

with no image lag

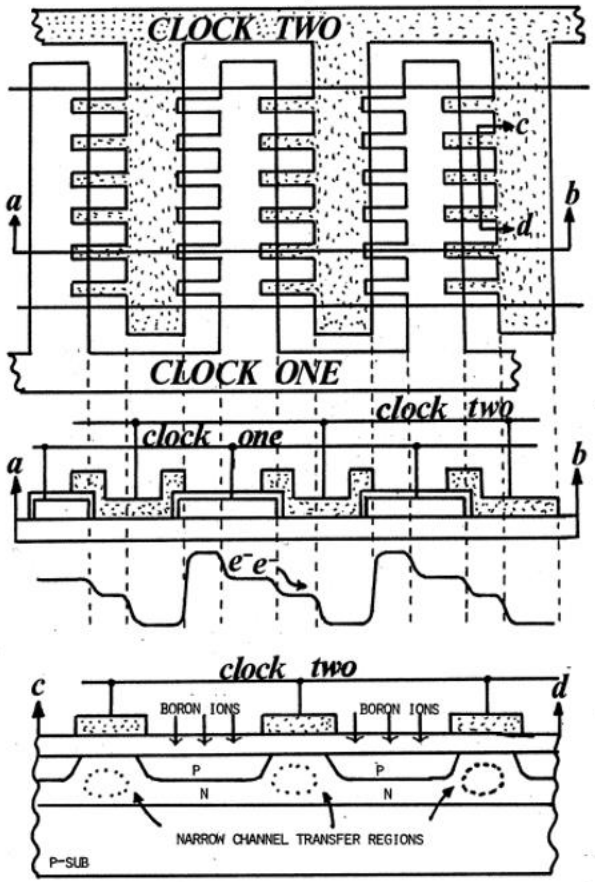


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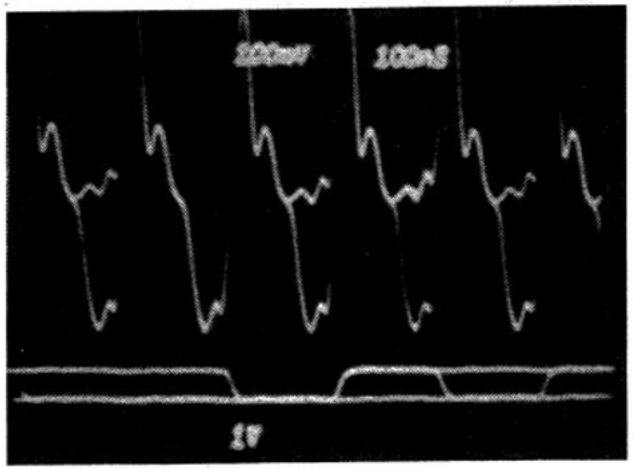


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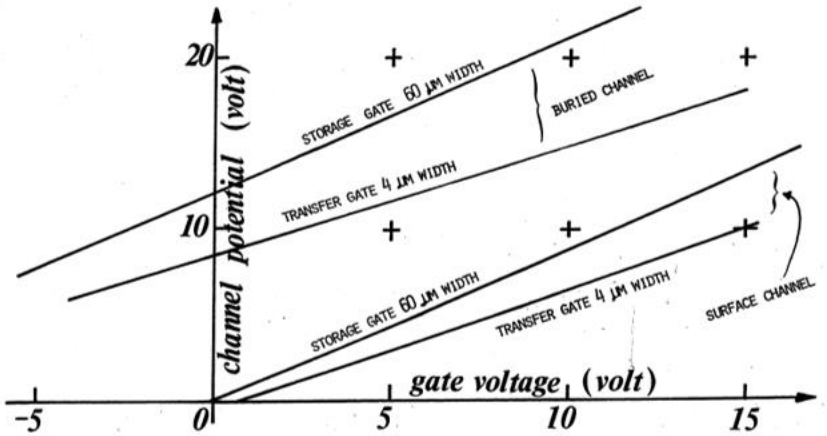


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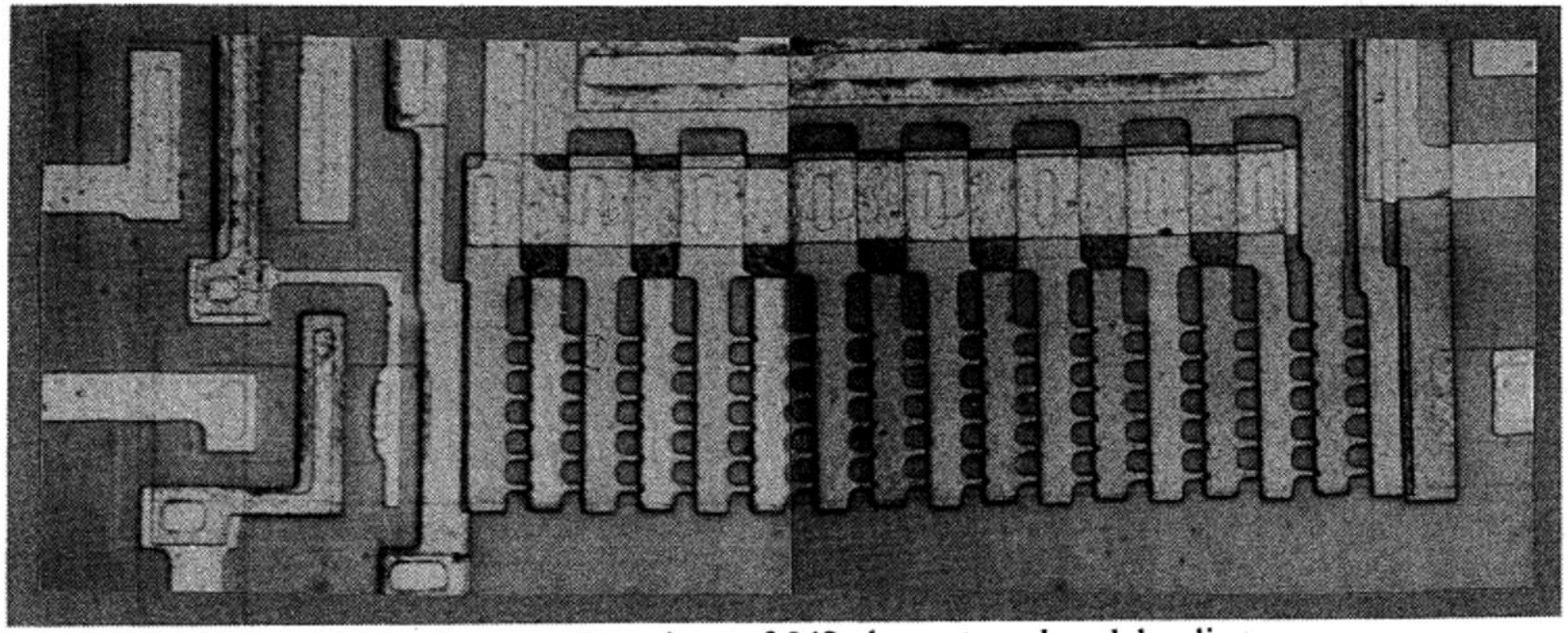
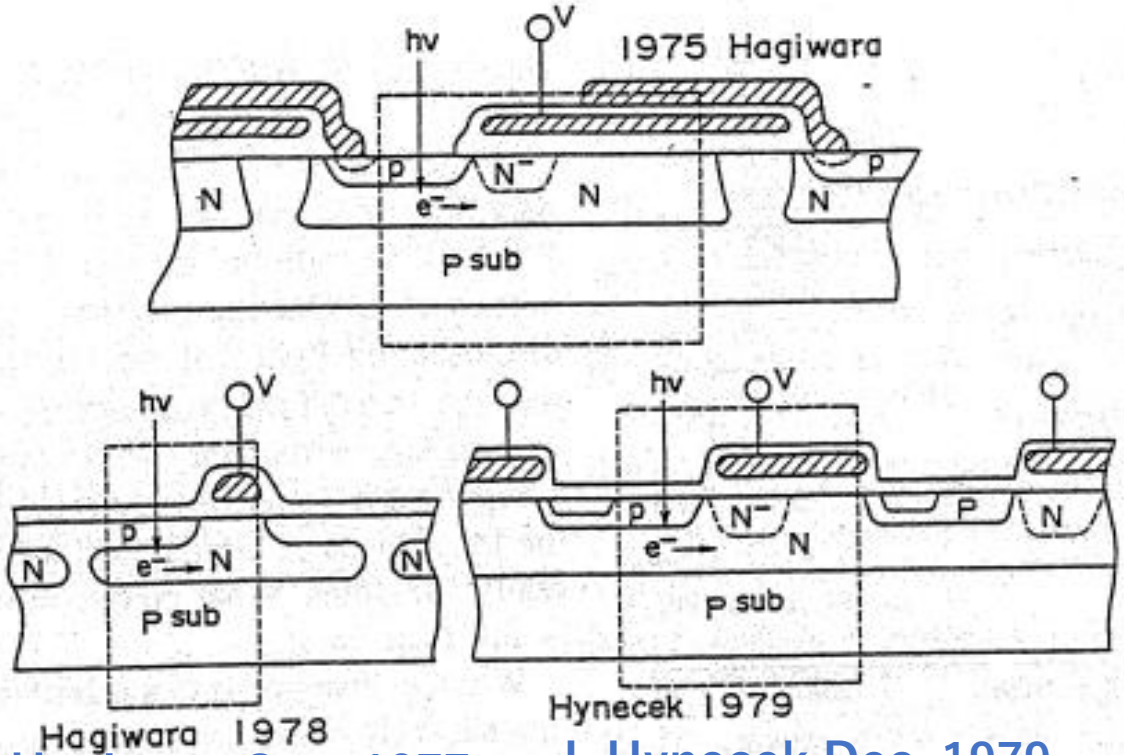


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Yoshiaki Hagiwara, *Member, IEEE*

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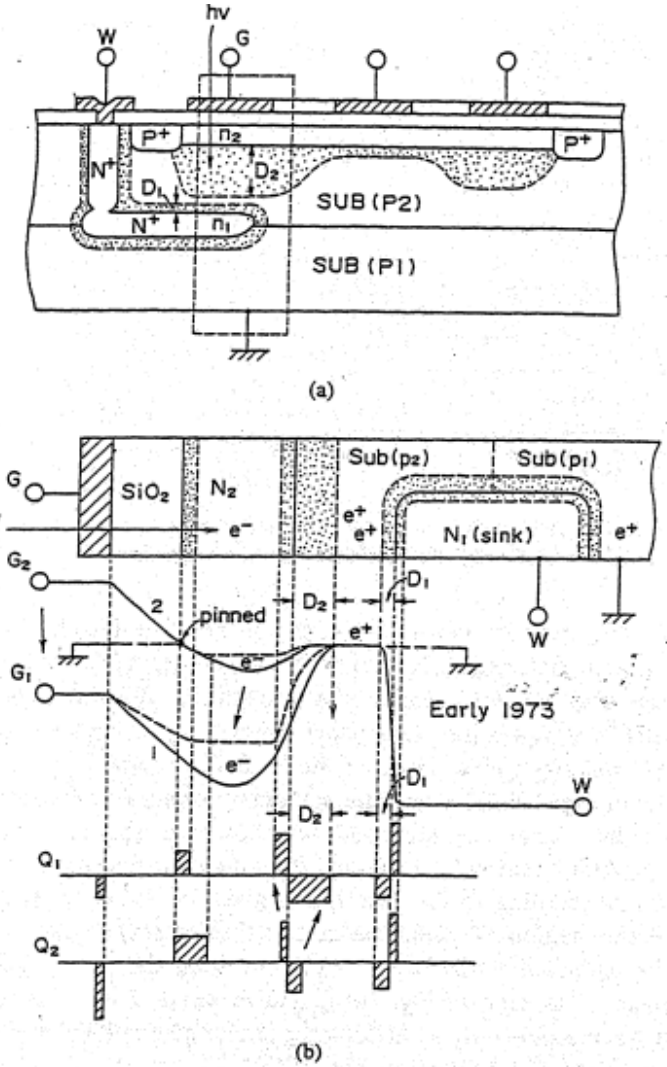


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A 380H × 488V CCD Imager with Narrow Channel Transfer Gates

Yoshiaki Daimon-HAGIWARA, Motoaki ABE† and Chikao OKADA†

Sony Corporation Research Center, Yokohama 240
†Semiconductor Development Division, Yokohama 240

with no image lag

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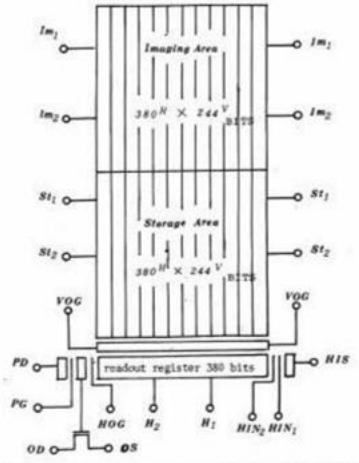


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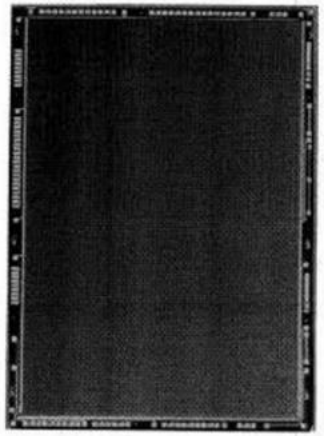


Fig. 3. Photomicrograph of the 380 H×488 V CCD imager. The chip size is 14.6 mm by 10.1 mm.

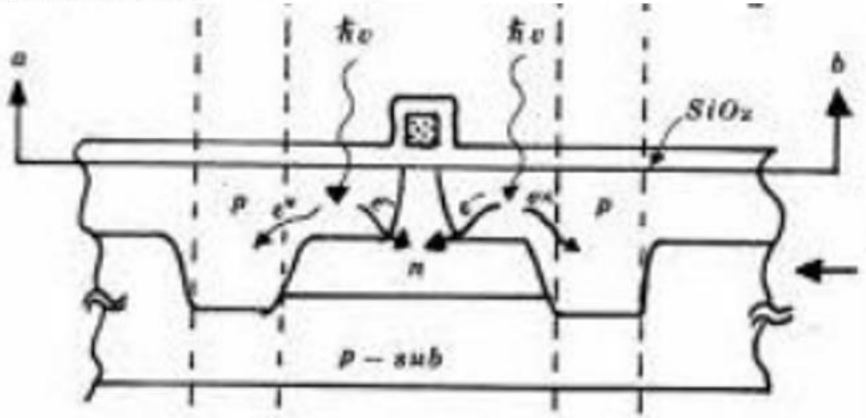


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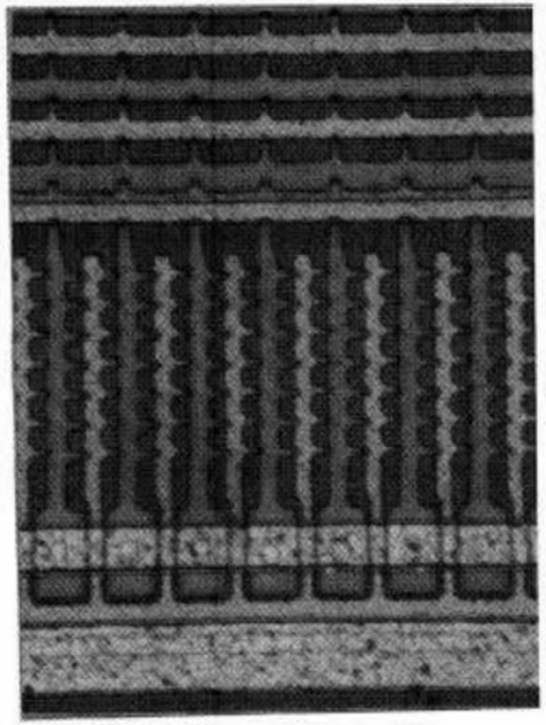


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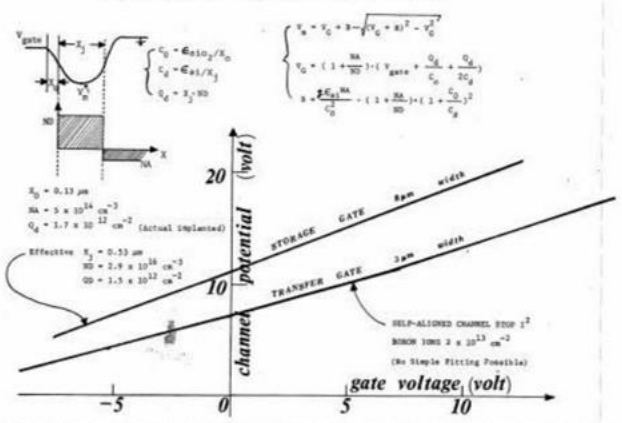


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with no image lag

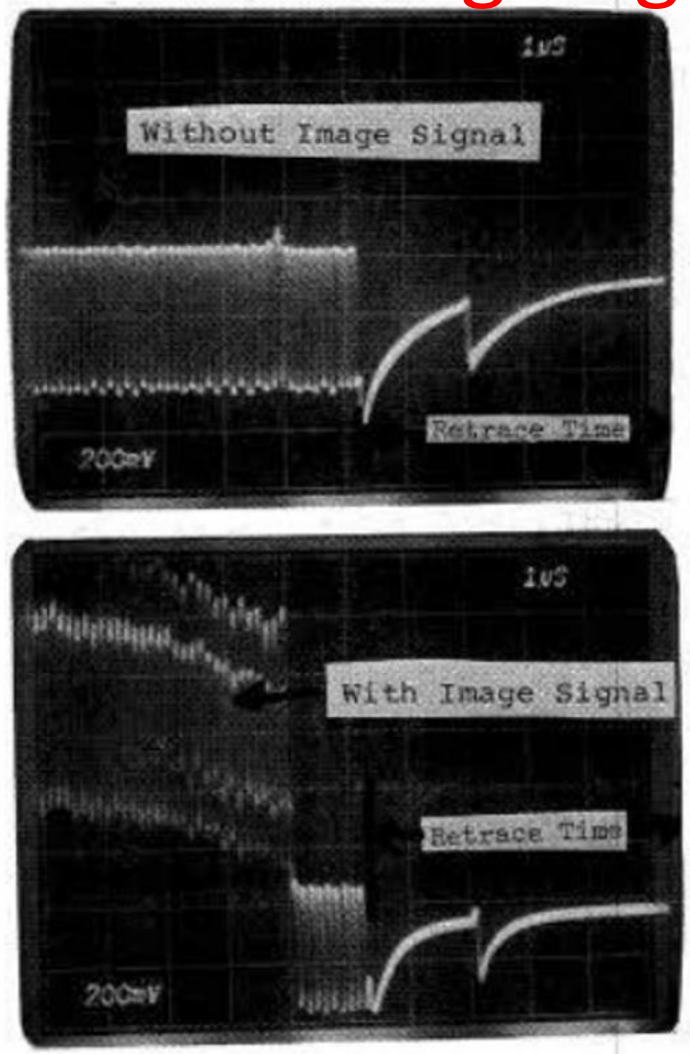
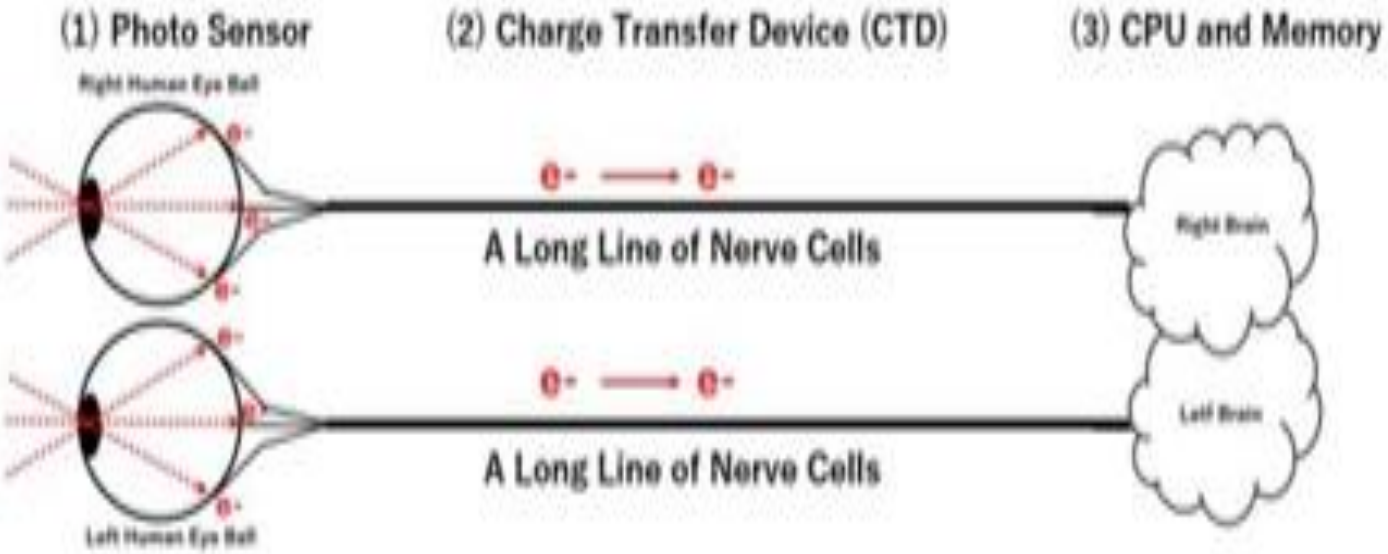


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Three important parts of Image Sensor



History of Charge Transfer Device (CTD)

(1) 1T1C DRAM Cell type MOS Image Sensor

(2) CCD/MOS Capacitor type Image Sensor

(3) CMOS Digital Circuit type Image Sensor

受光面がピン留めされた Double Junction Type New Solar Cell の提案

See JPA2020-131313 invented by Yoshiaki Hagiwara (AIPS) in 2020

The First Pinned Photodiode was invented by Hagiwara at Sony in 1975 in order to realize the in-pixel electric shutter function. The evidence is given in the Japanese patent application JPA1975-127646, which defined the pinned-surface triple-junction dynamic-thyristor type Pinned Photodiode.

The evidence are given in the Japanese Patent Applications, JPA1975-127646, JPA1975-127646 and JPA1975-134985.

Fig 7 in JPA1975-127646

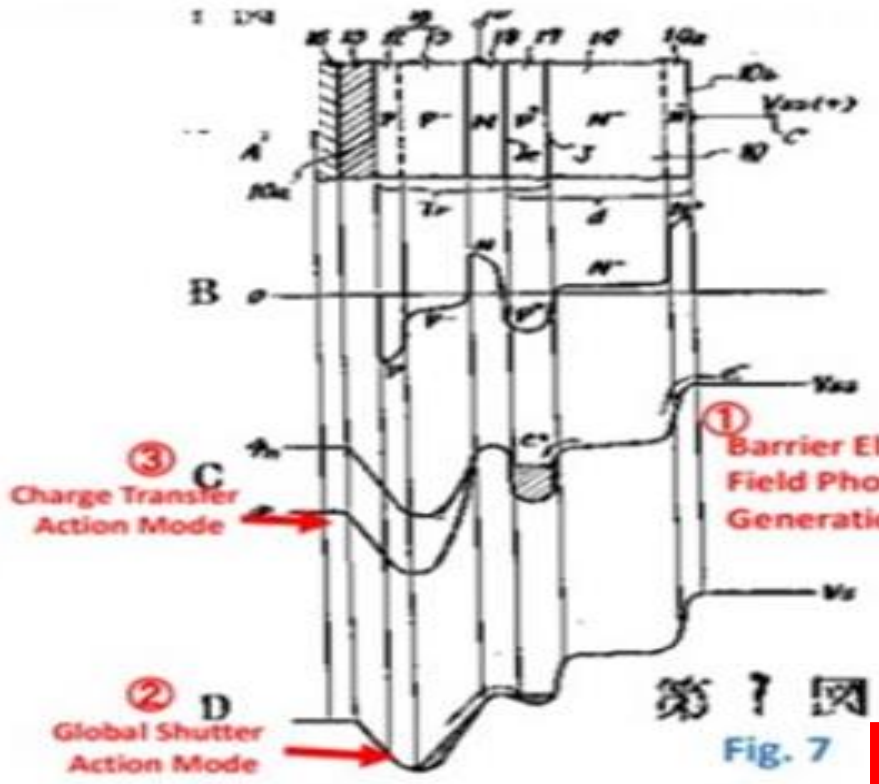


Fig 7 in JPA1975-127647

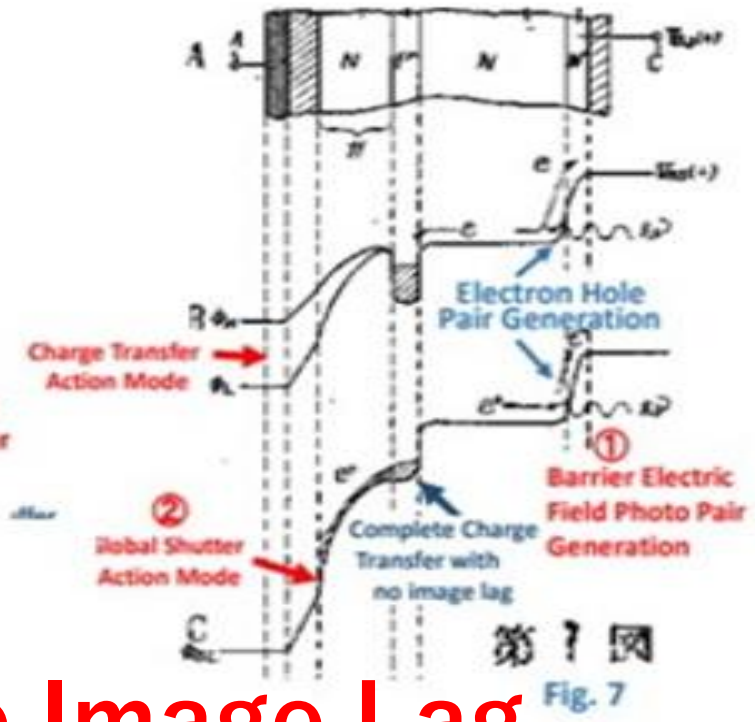
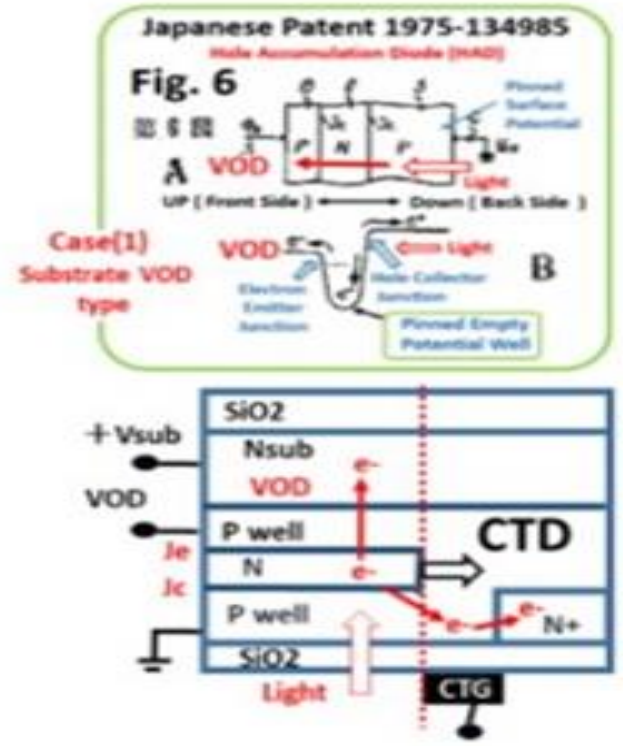


Fig 6 in JPA1975-134985

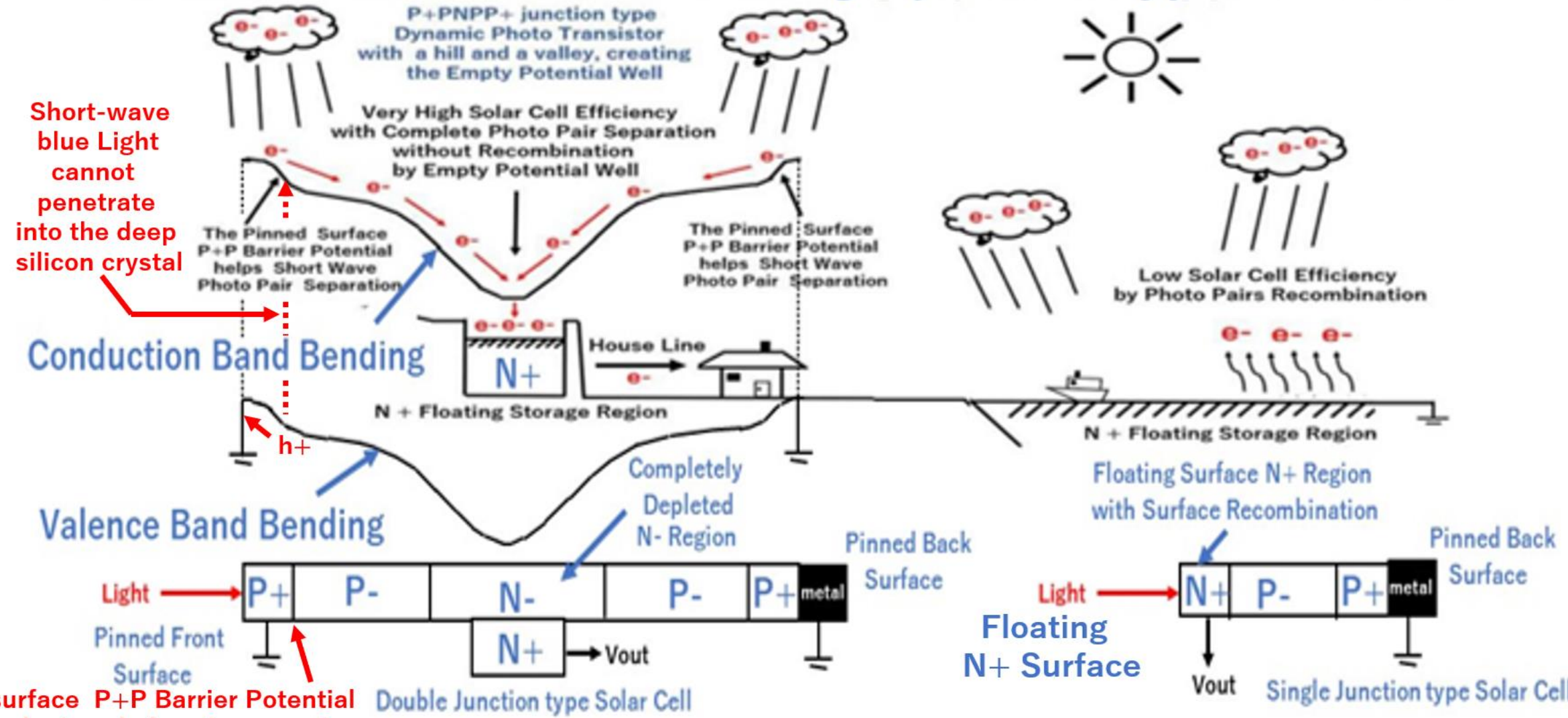


No Image Lag

PPD with in-pixel VOD function was drawn in Hagiwara Lab Note in Feb 1975.

True History of Photodiode

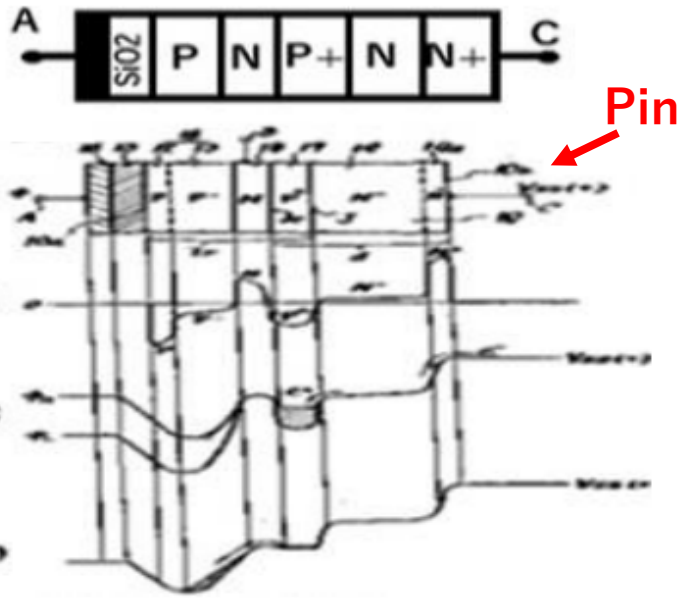
The difference of Double and Single junction type Solar Cells



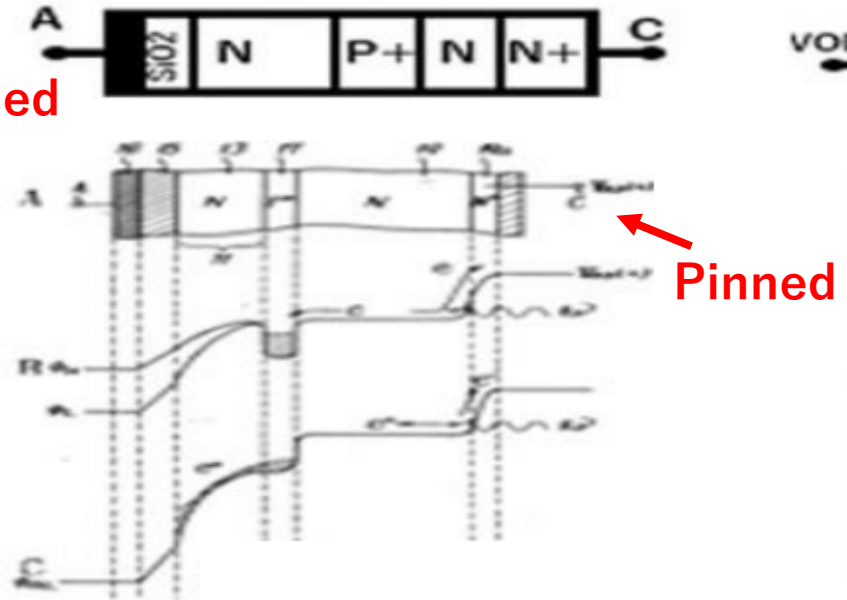
The surface P+P Barrier Potential helps electron-hole pair separations.

Who invented Pinned Photodiode ?

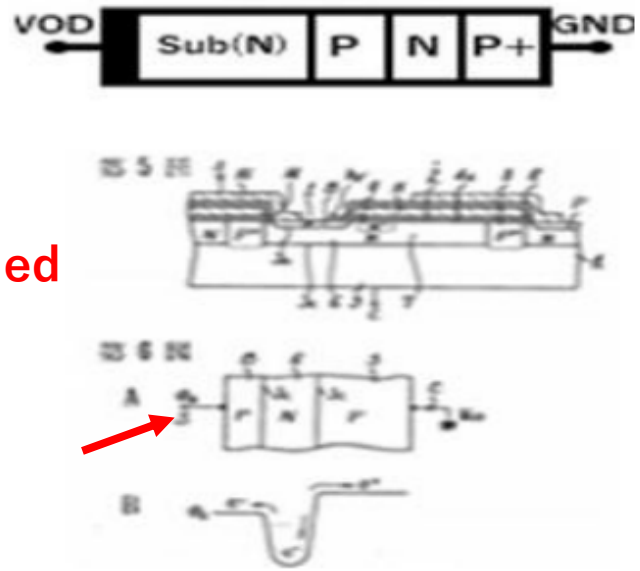
Hagiwara at Sony invented Pinned Photodiode in 1975. The evidence is give by the three Japanese patent applications, JPA1975-127646, JPA1975-127647 and JPA1975-134985. The first Pinned Photodiode was defined in October 23, 1975 as the N+NPNP triple junction(in Fig. 7 of JAP1975-127646) type and the N+NPN double junction type (in Fig. 7 of JAP1975-127647) type photodiodes with the N+ type pinned surface and the P type buried photo charge storage region with the complete charge transfer capability and the no-image-lag feature. The photo charge is transferred and drained to the CCD/MOS type charge storage buffer memory quicky by the strong punch-thru action. The second Pinned Photodiode was defined in November 10, 1975 as the PNP double junction (in Fig. 6 of JAP1975-134985) type photodiode with the vertical overflow drain action also with the complete charge transfer capability and the no-image-lag feature as evidence the empty potential well of the buried photo charge storage, completely depleted of the charge.



JPA1975-127646 Fig. 7



JPA1975-127647 Fig. 7



JPA1975-134985 Fig. 6

Proceedings of the 9th Conference on Solid State Devices, Tokyo, 1977;
Japanese Journal of Applied Physics, Volume 17 (1978) Supplement 17–1, pp. 255–261

Two Phase CCD with Narrow-Channel Transfer Regions

Yoshiaki DAIMON-HAGIWARA

Sony Corporation Research Center Yokohama 240

with no image lag

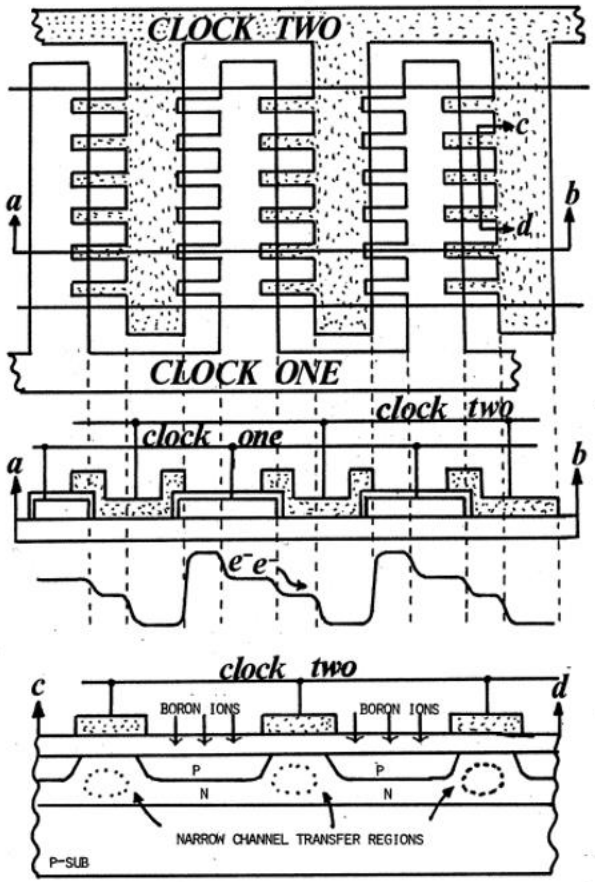


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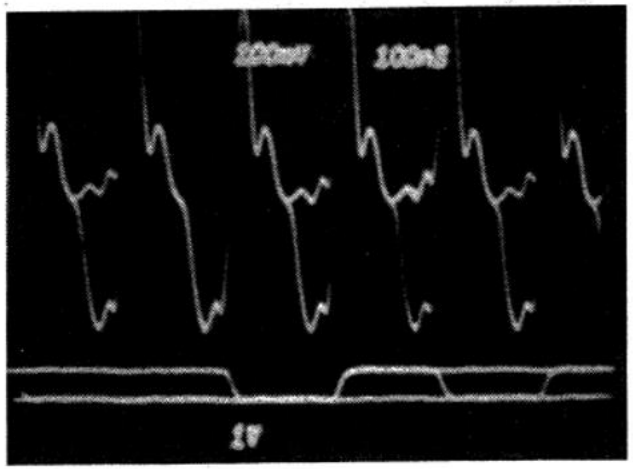


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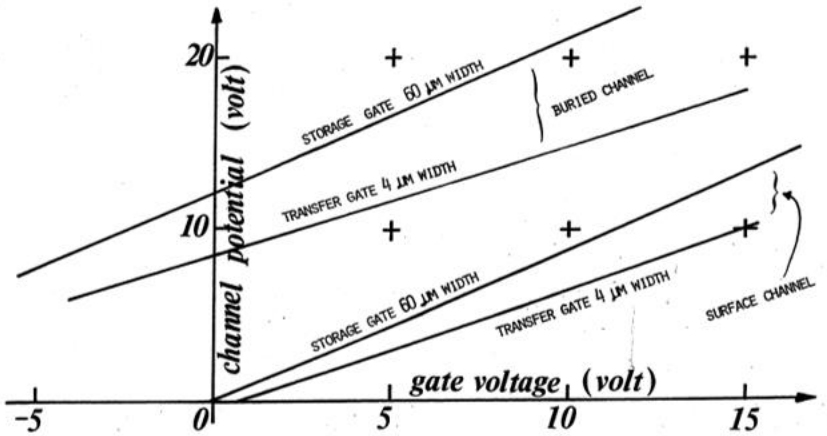


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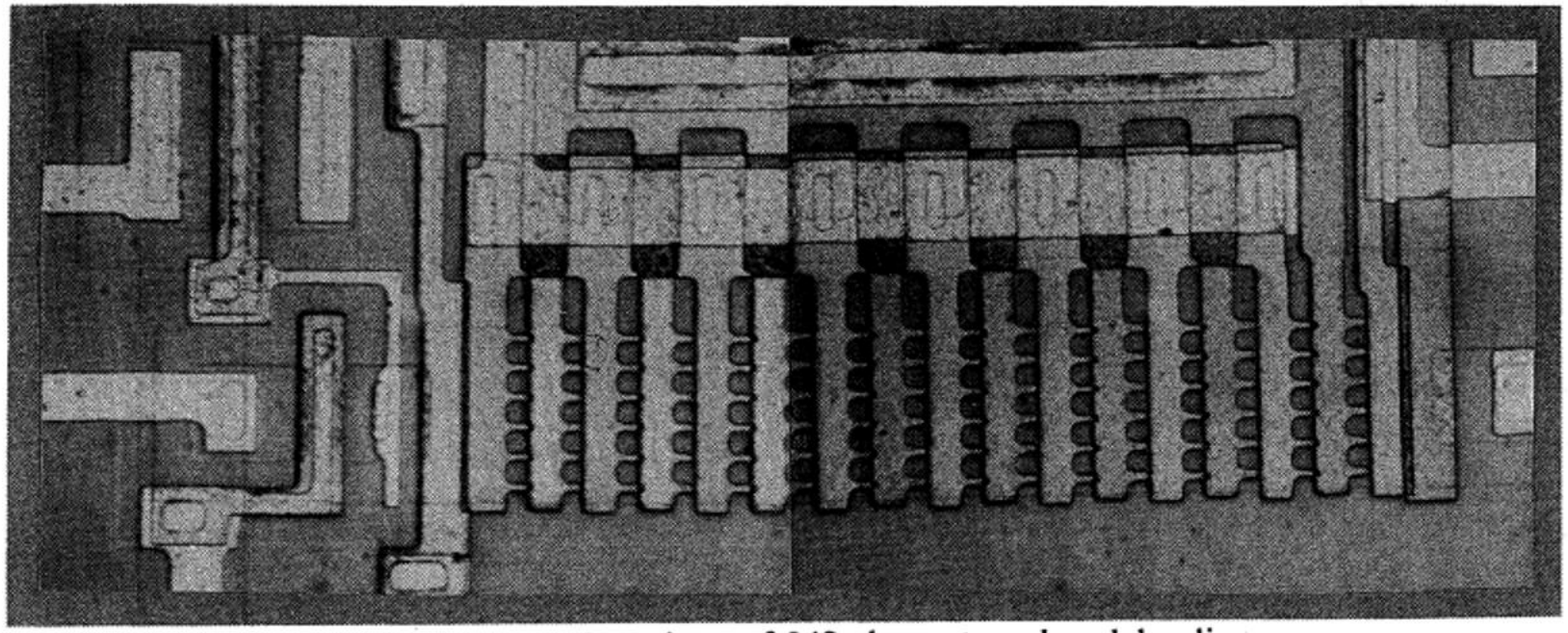
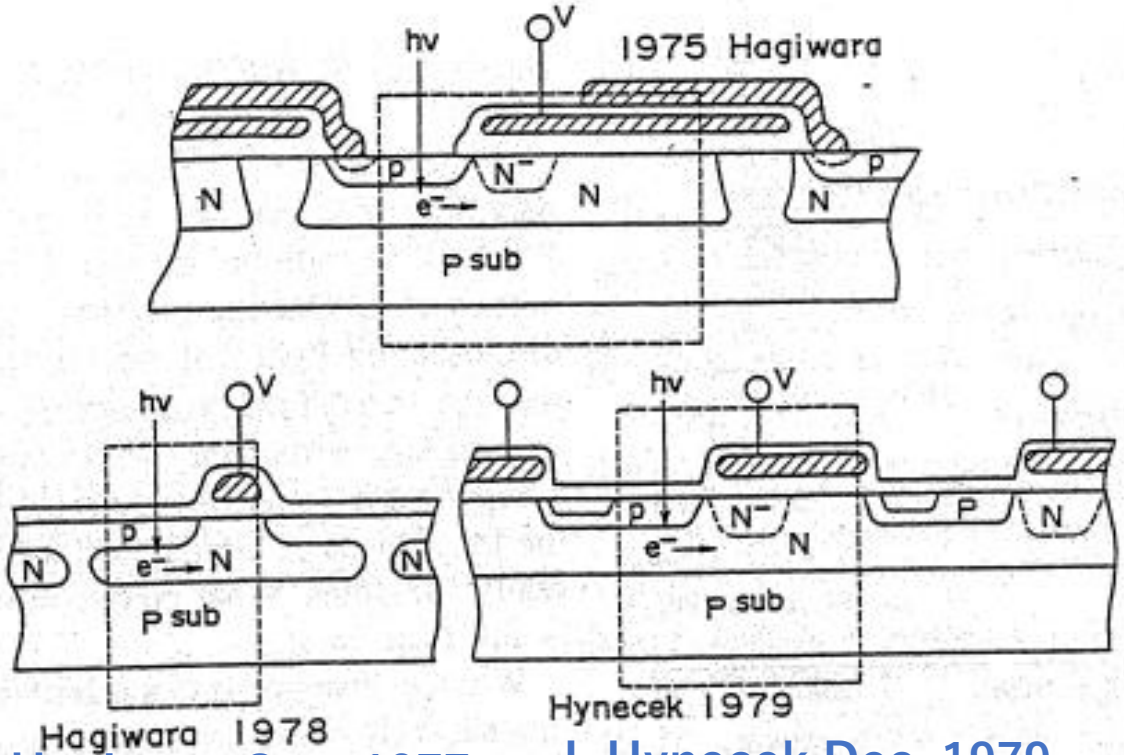


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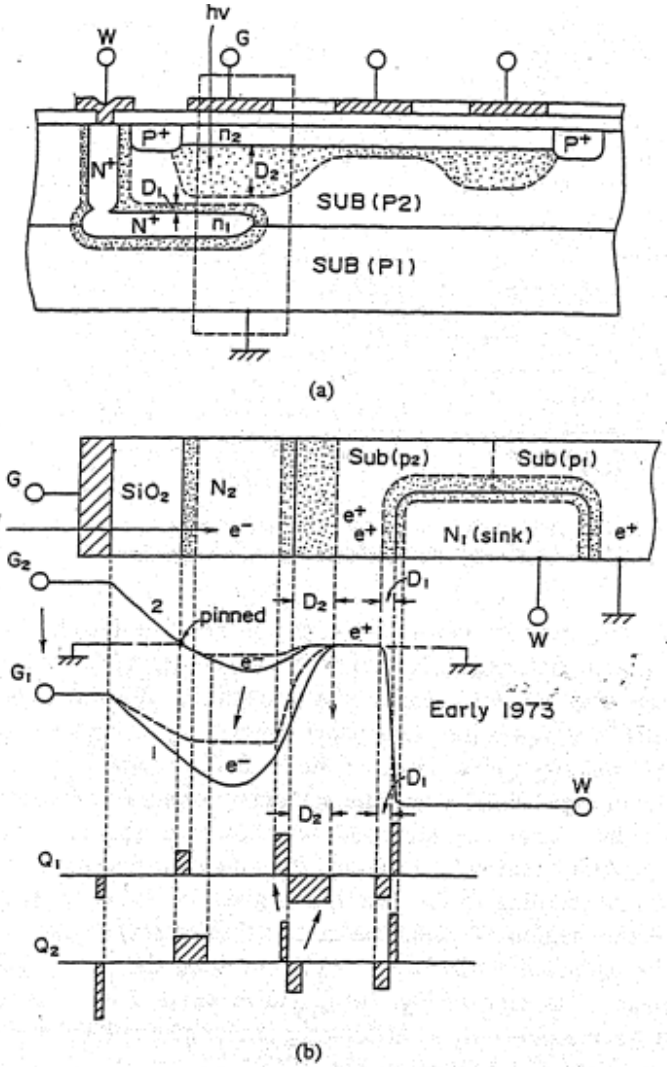


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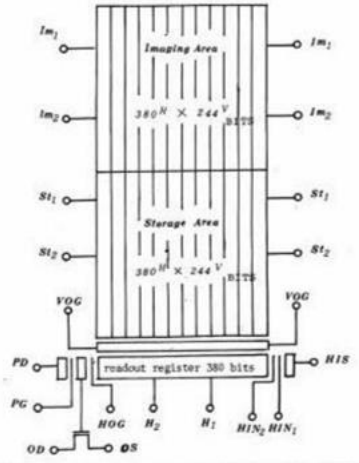


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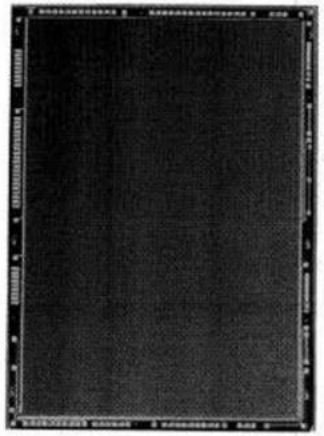


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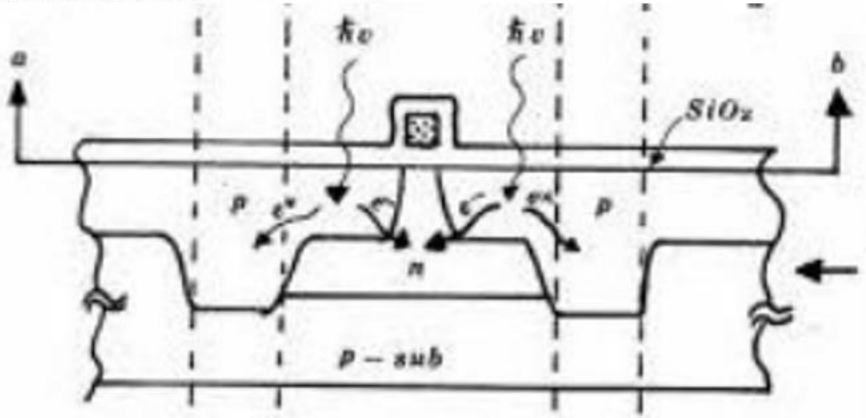


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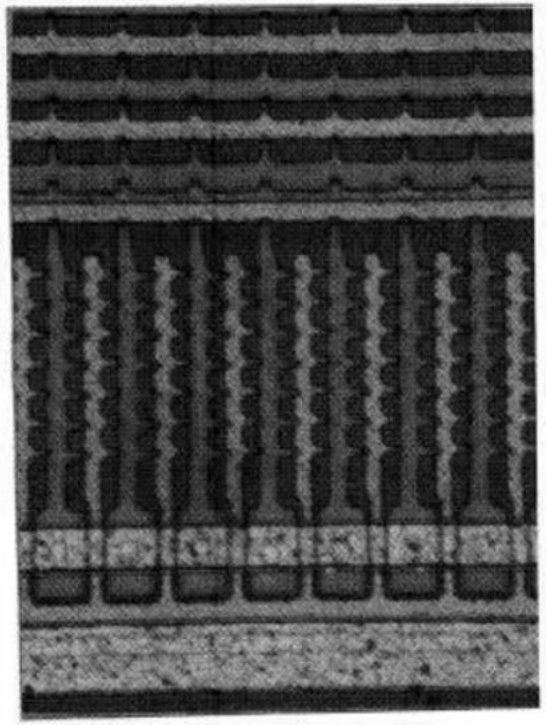


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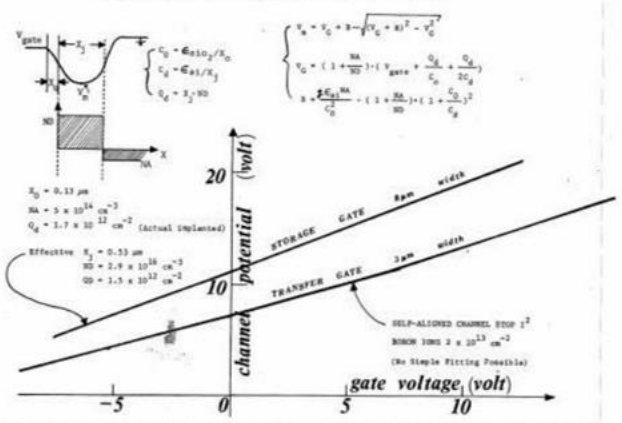


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with no image lag

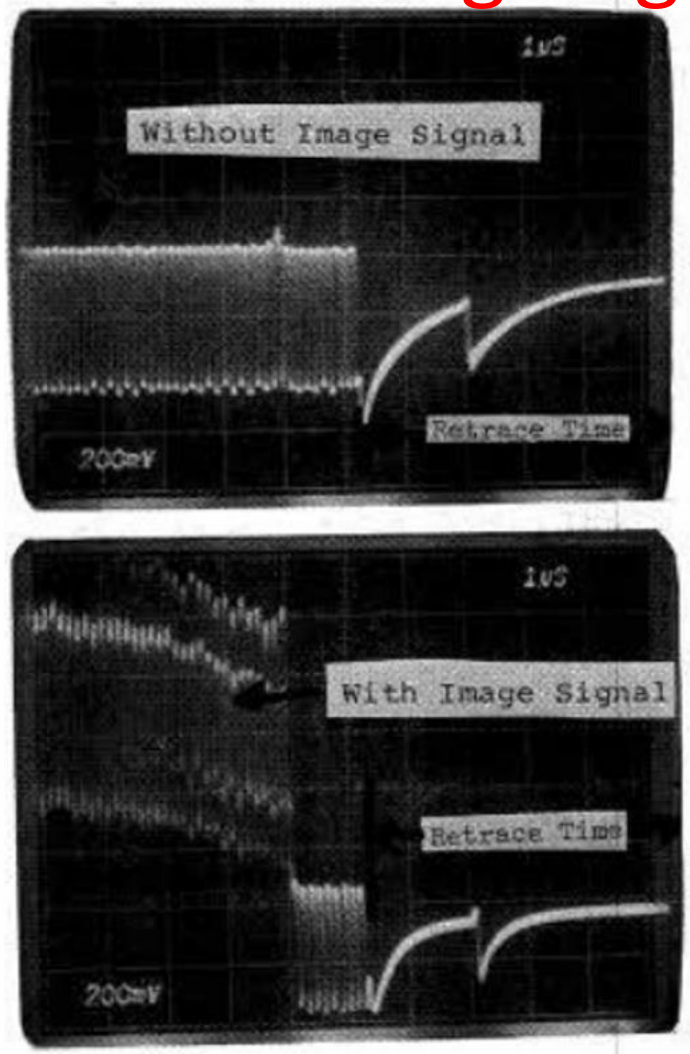
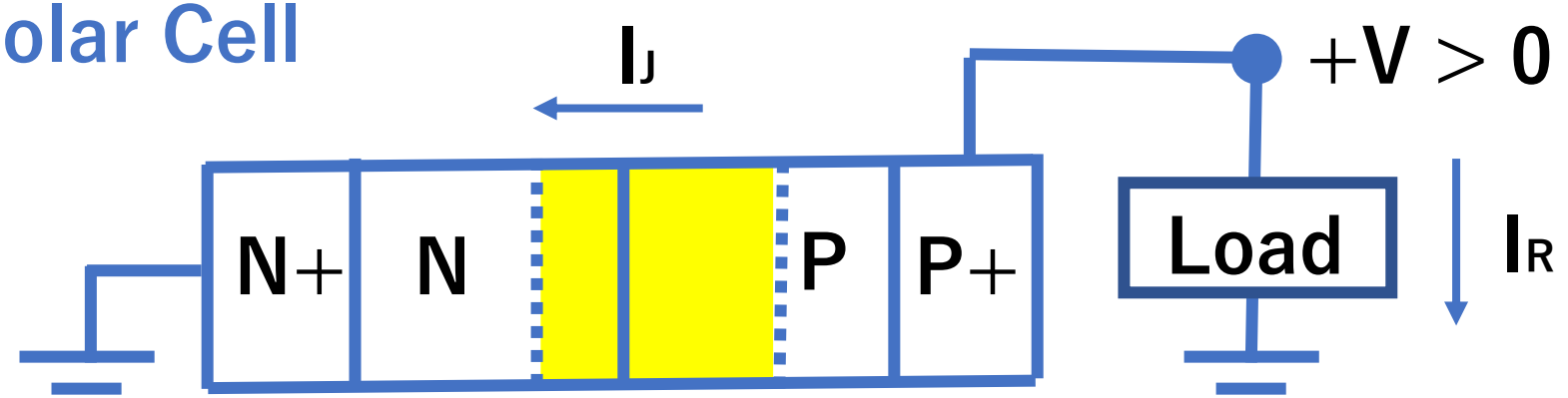


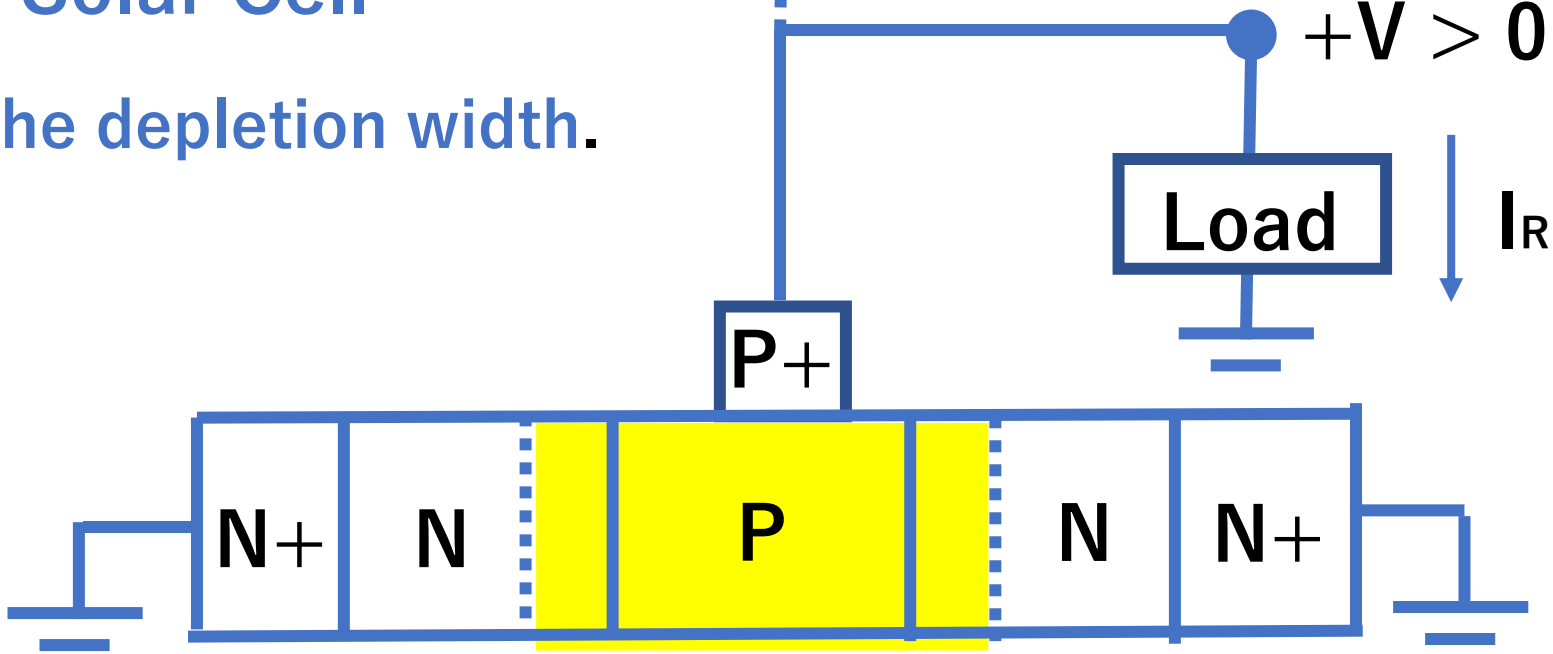
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Single Junction Solar Cell

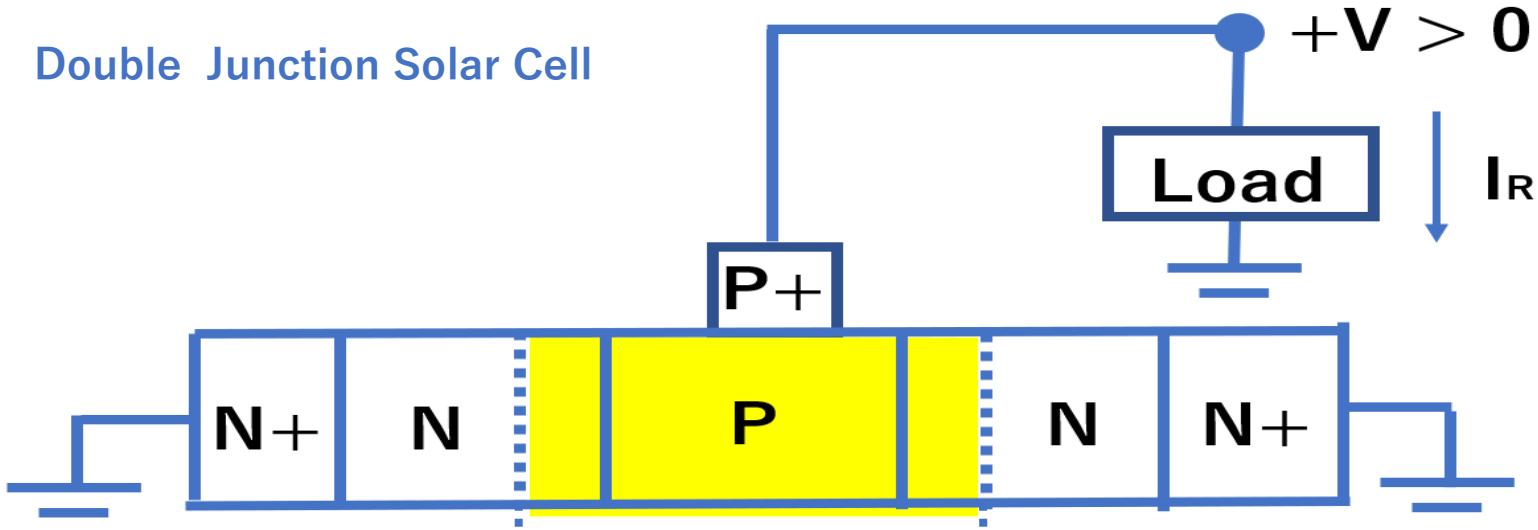


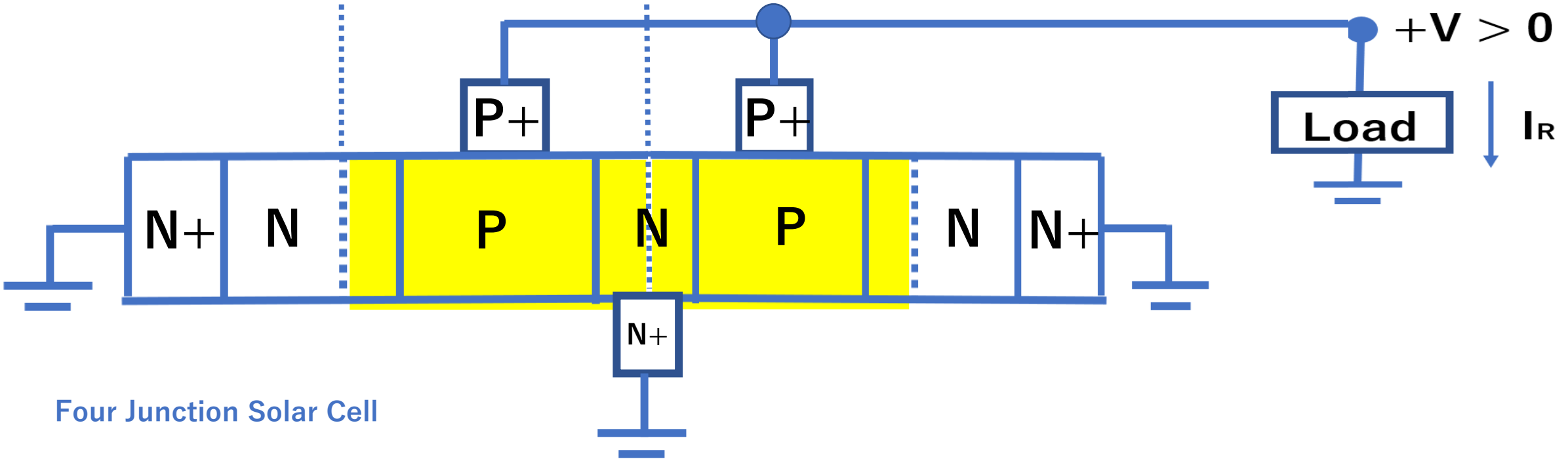
Double Junction Solar Cell

We can double the depletion width.



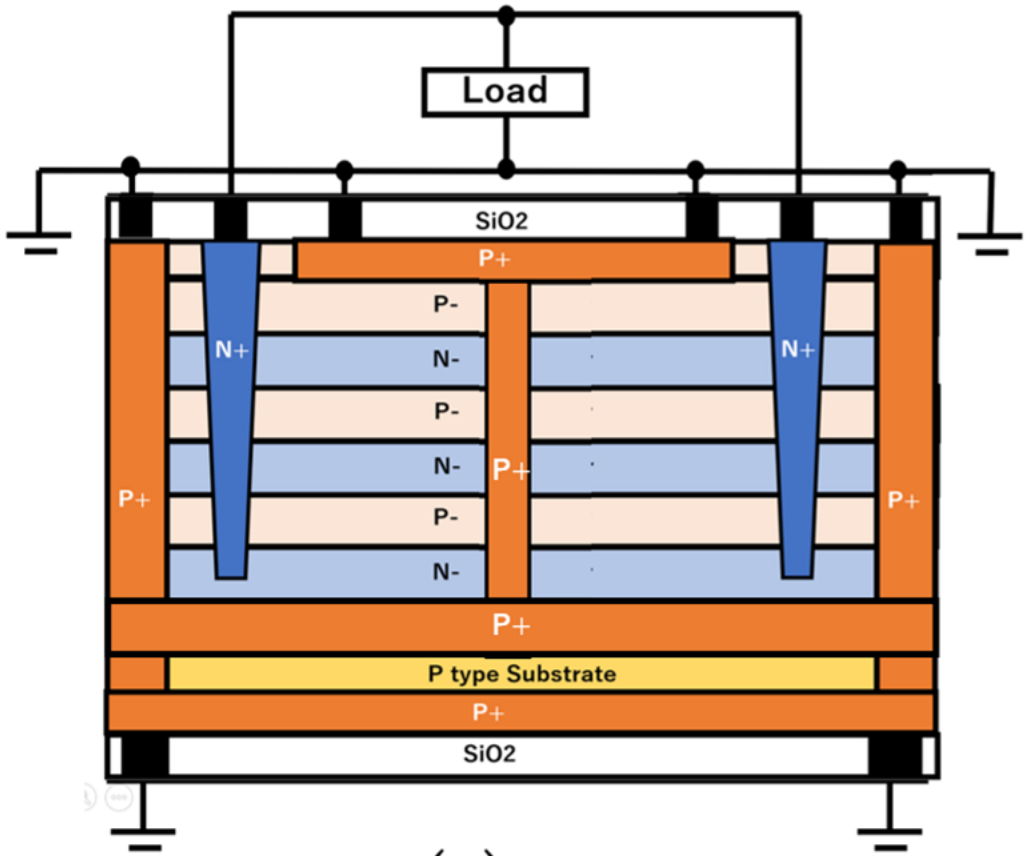
Double Junction Solar Cell





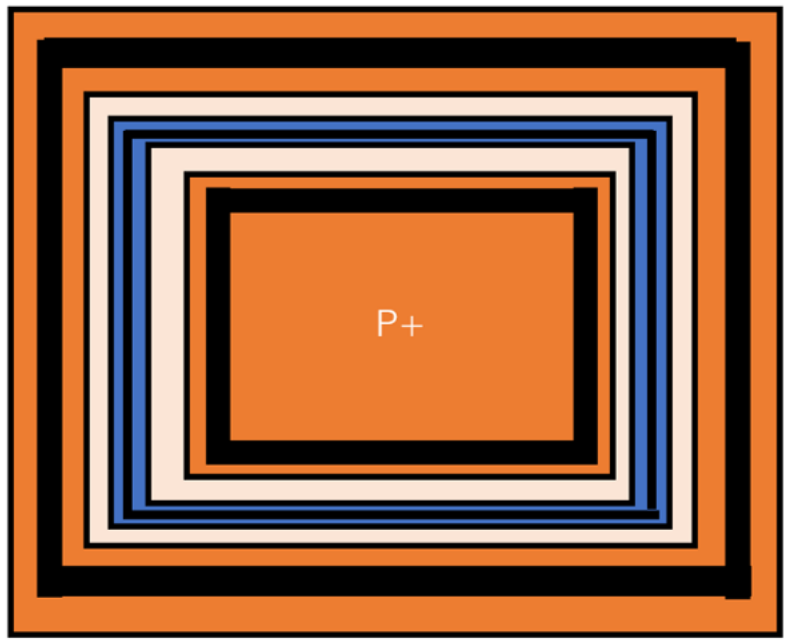
Four Junction Solar Cell

Multi-junction Solar Cell, based on JPA2020-131313 by Yoshiaki Hagiwara, applied on Aug. 1, 2020.



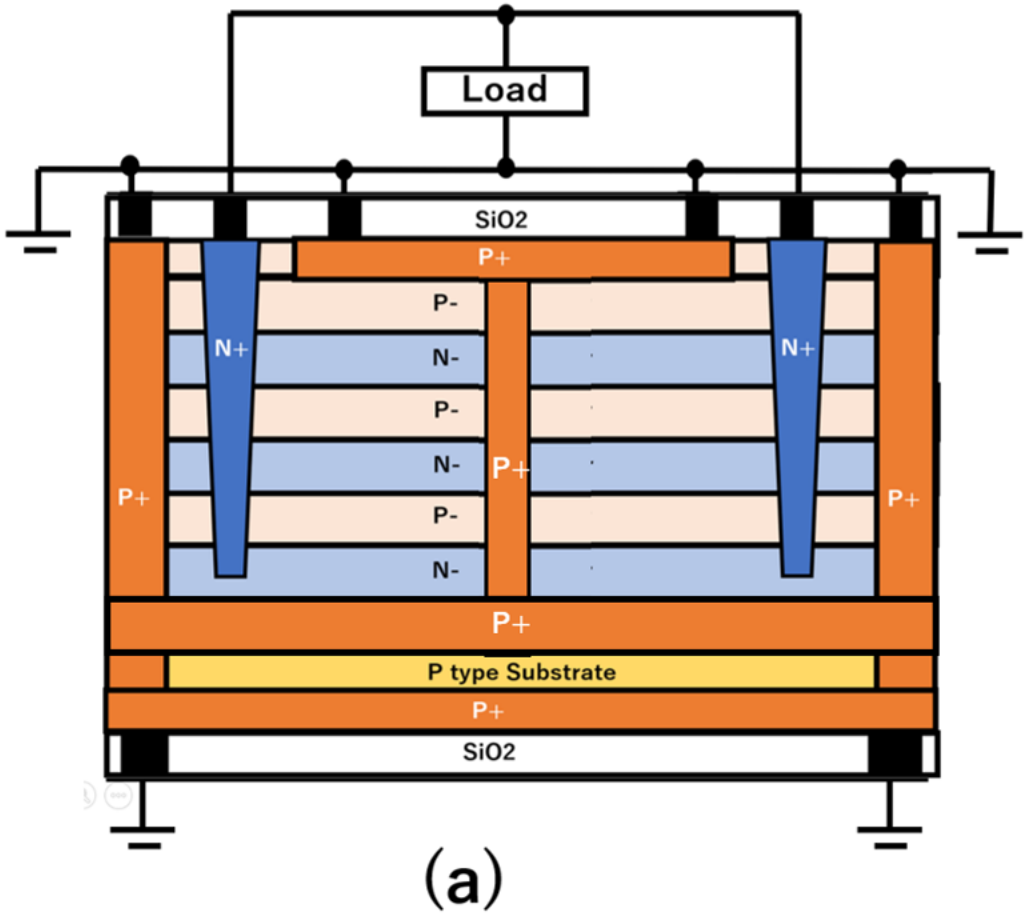
(a)

Top View

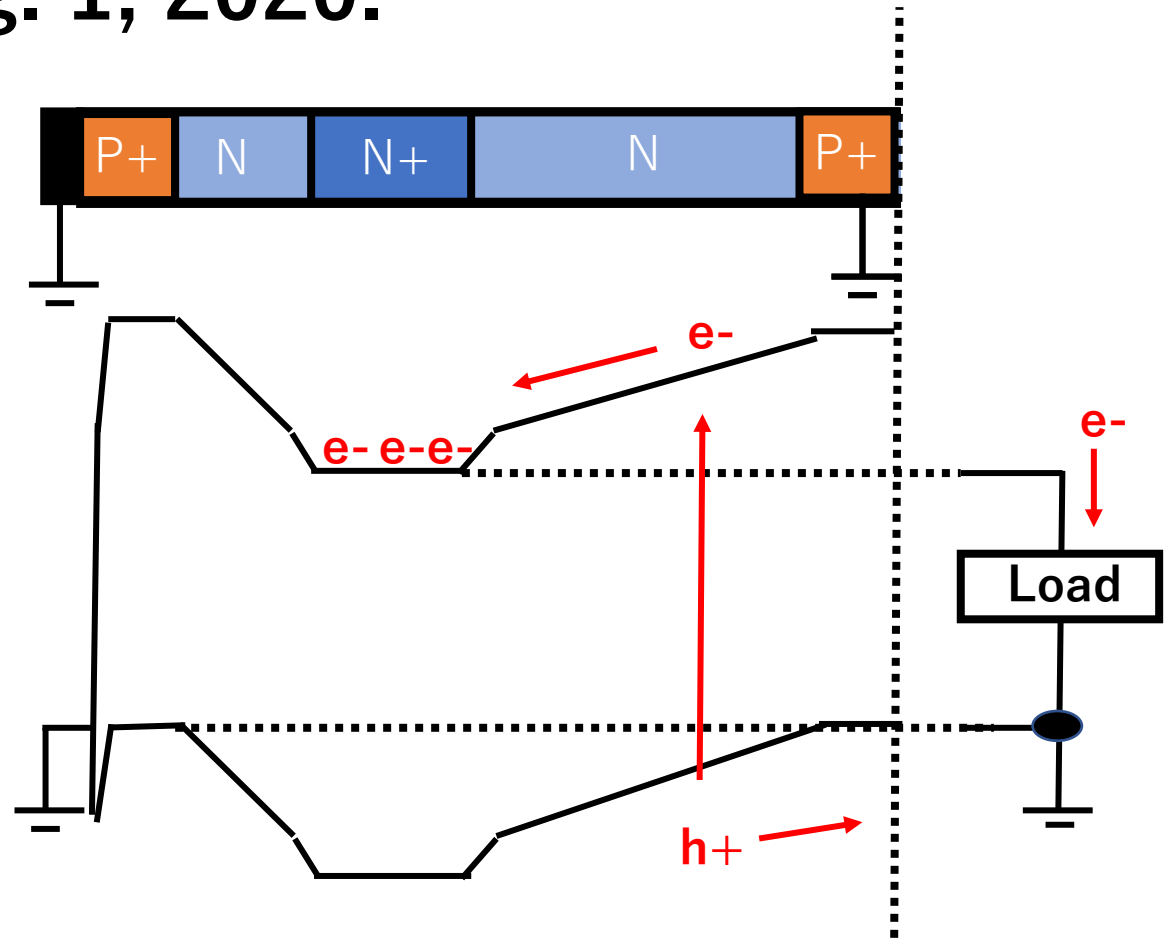


(b)

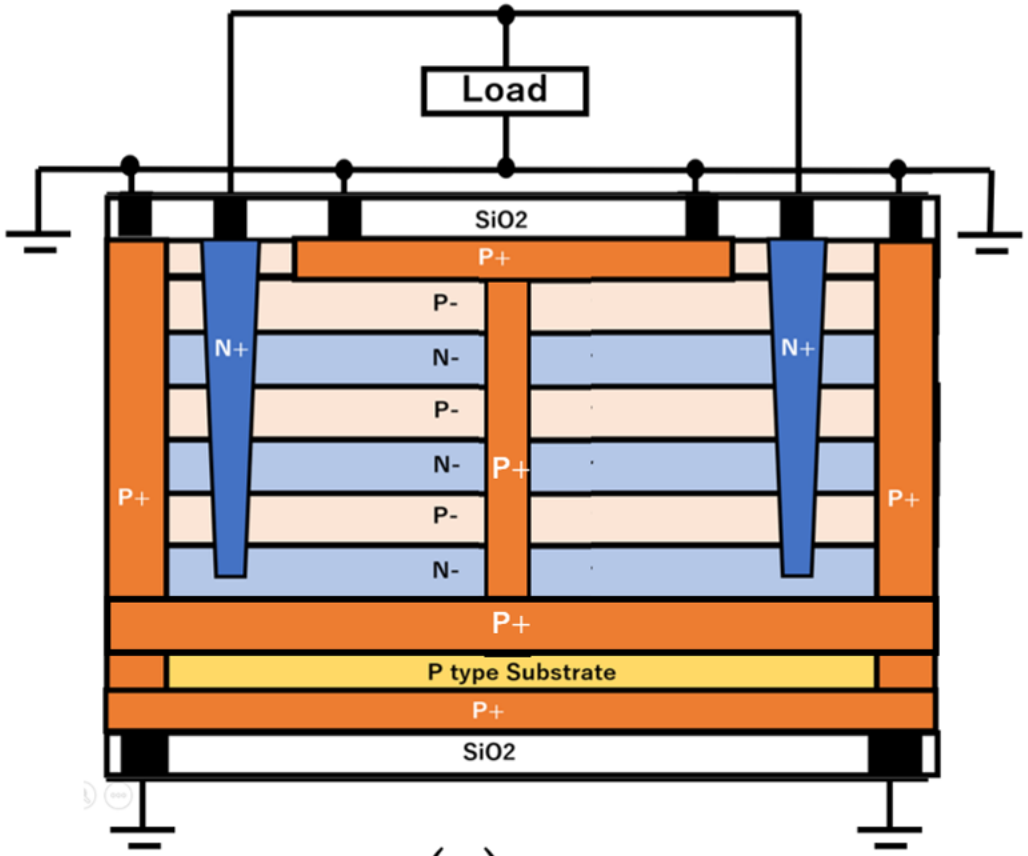
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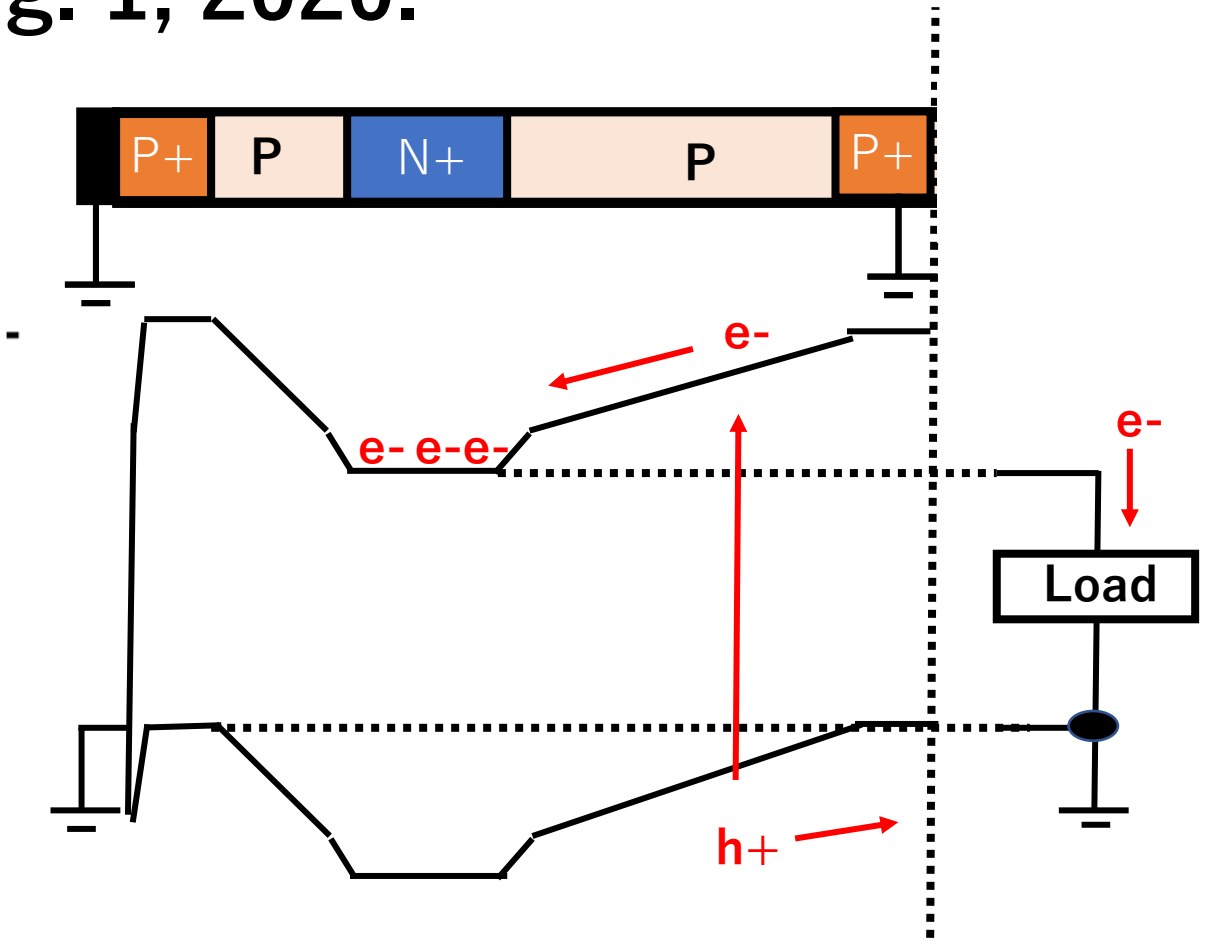
(a)



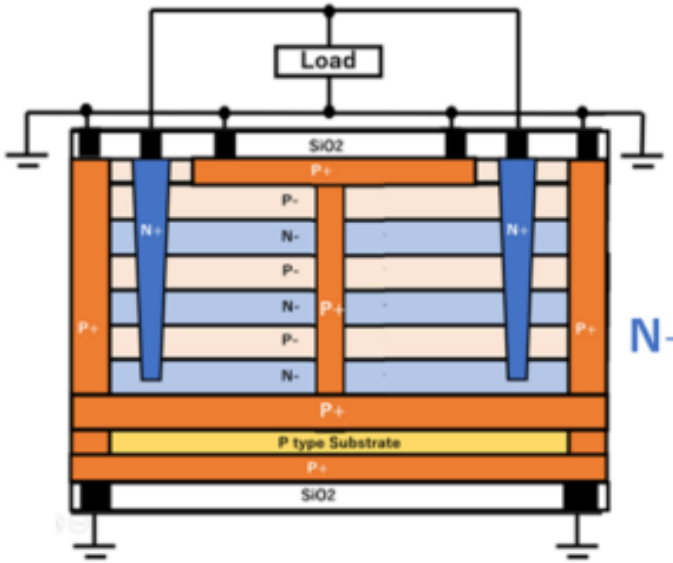
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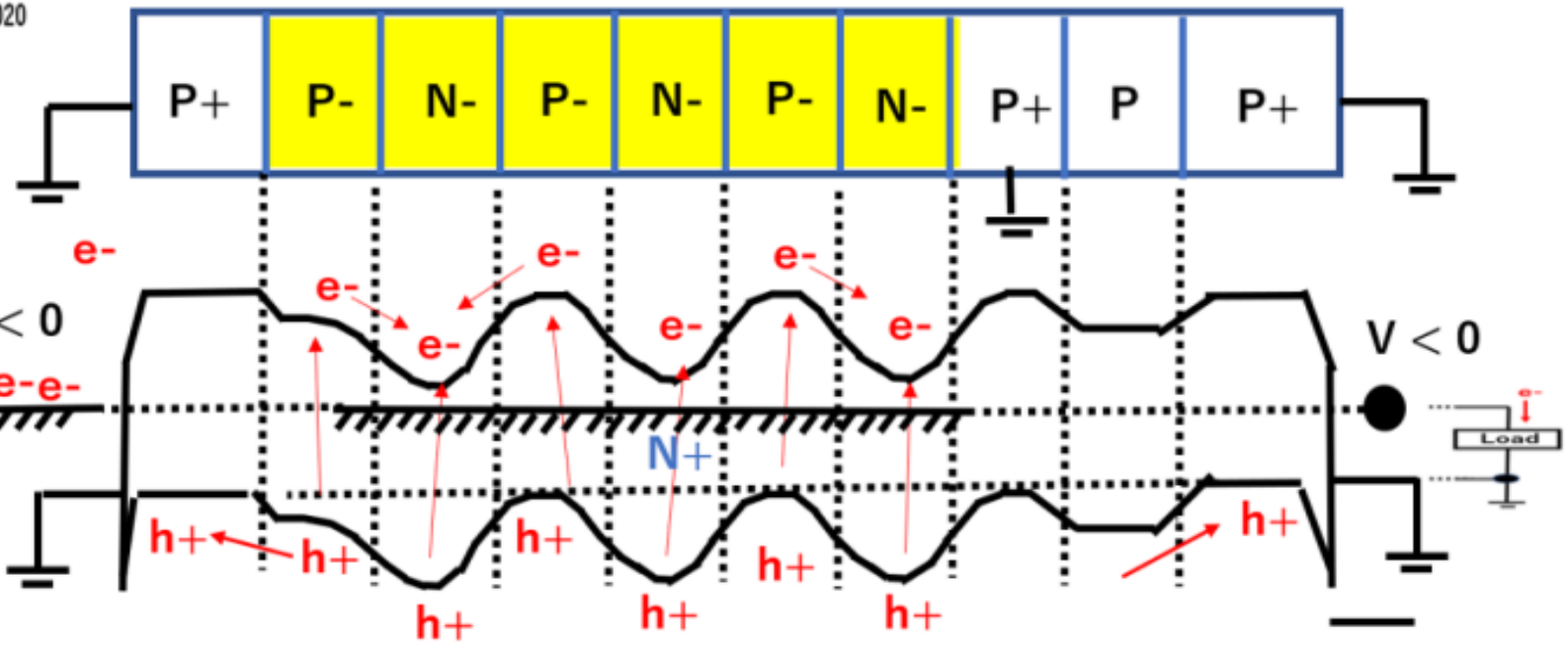
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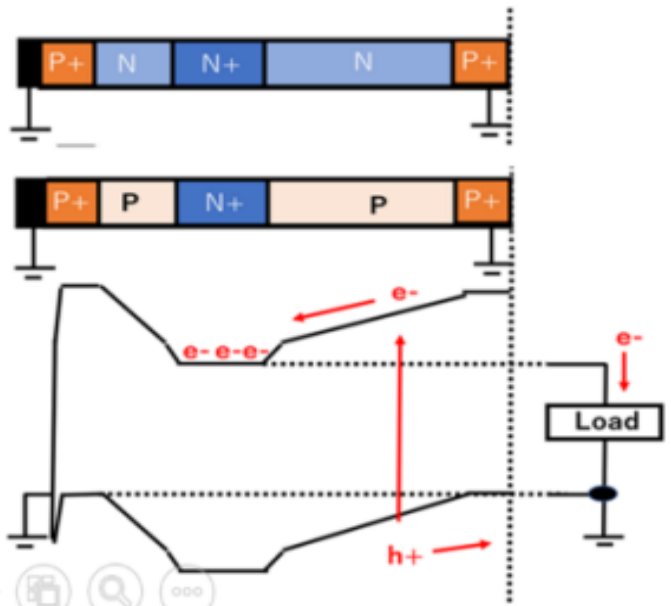


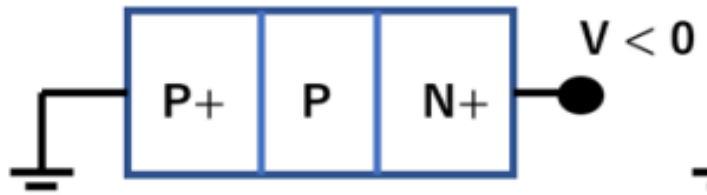
Multi-junction Pinned Photodiode type Solar Cell Structure,
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by Yoshiaki Hagiwara, Sept 12, 2022

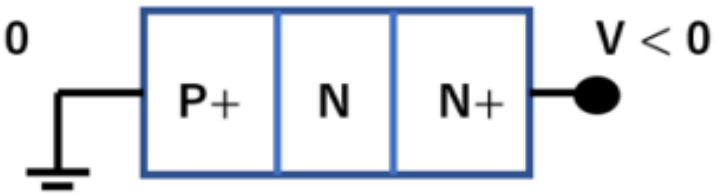


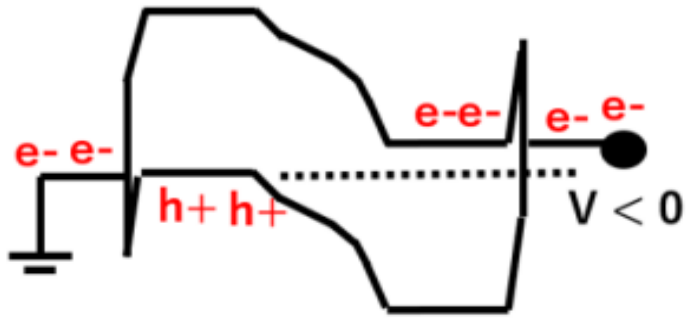
Completely Depleted Muti-Junctions

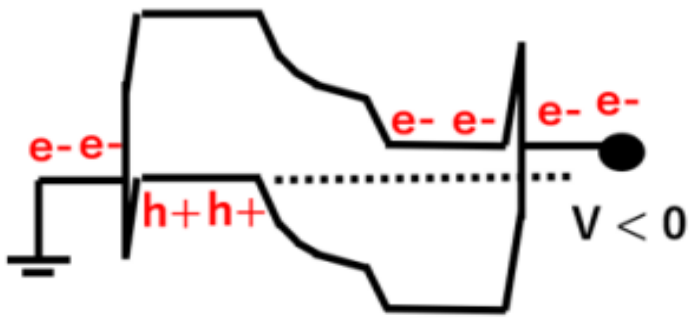




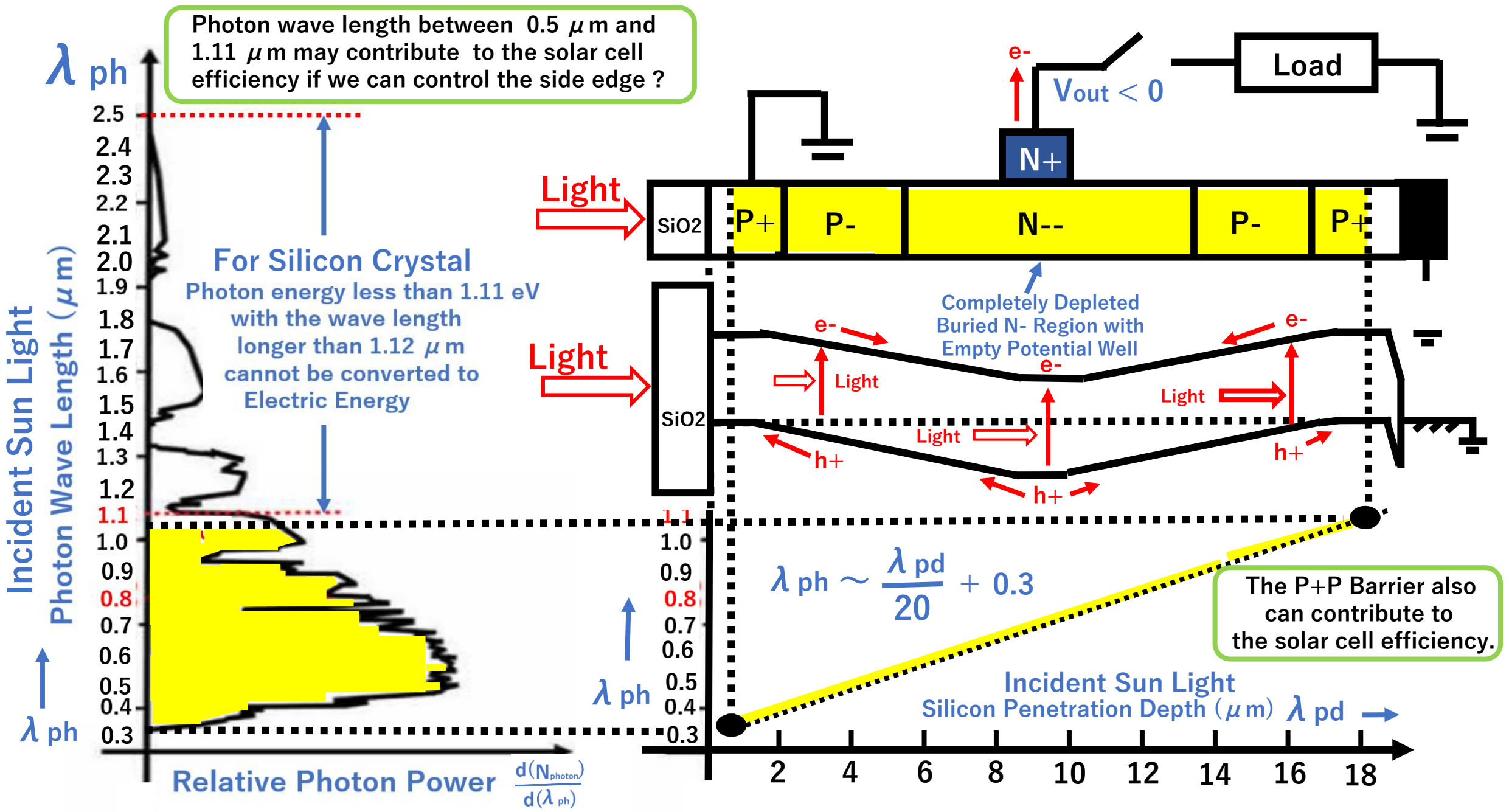






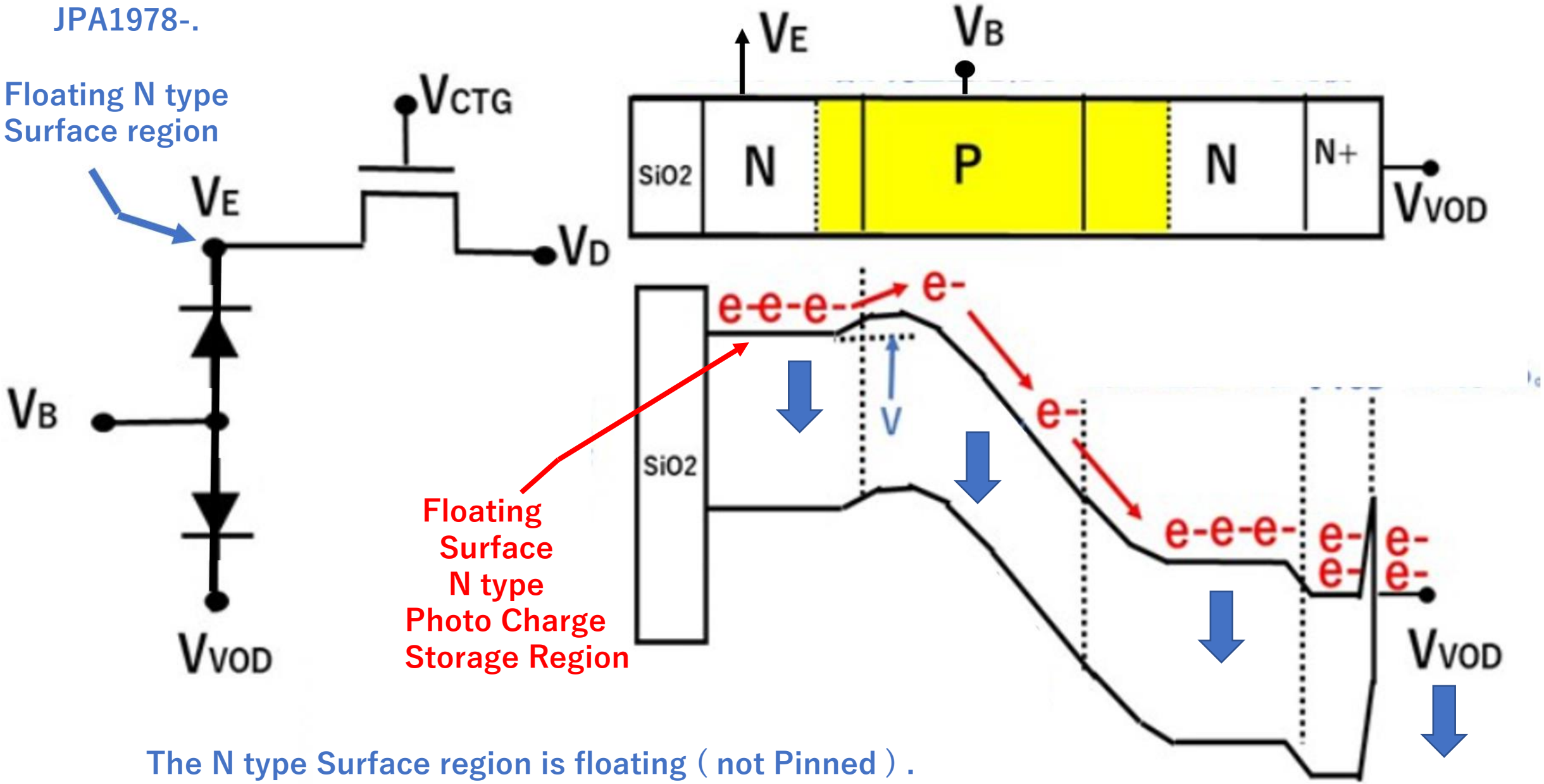


The P+P-N-P-P+ double junction type Solar Cell may have much higher efficiency



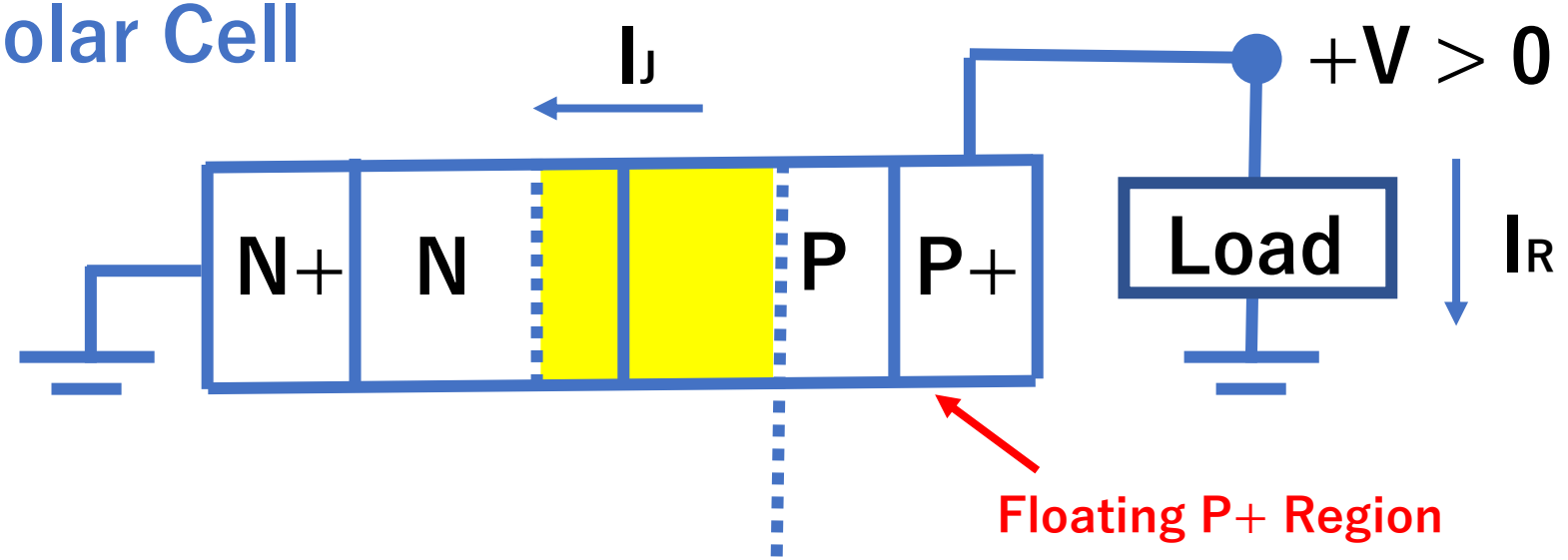
JPA1978-.

Floating N type
Surface region



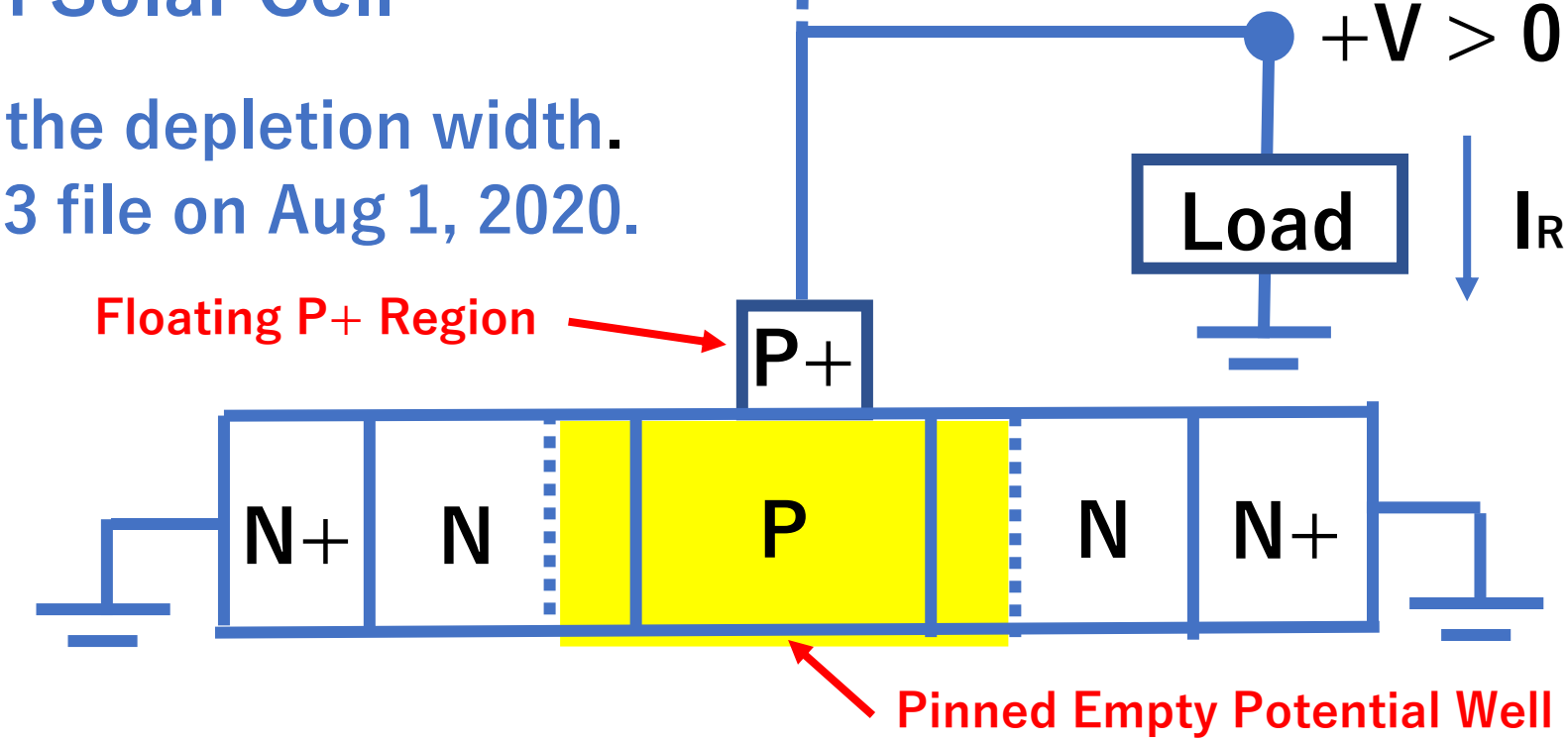
The N type Surface region is floating (not Pinned) .
The anti-blooming VOD does not function well because the N-type surface will also be pulled down as the VOD voltage is pulled down deeper.

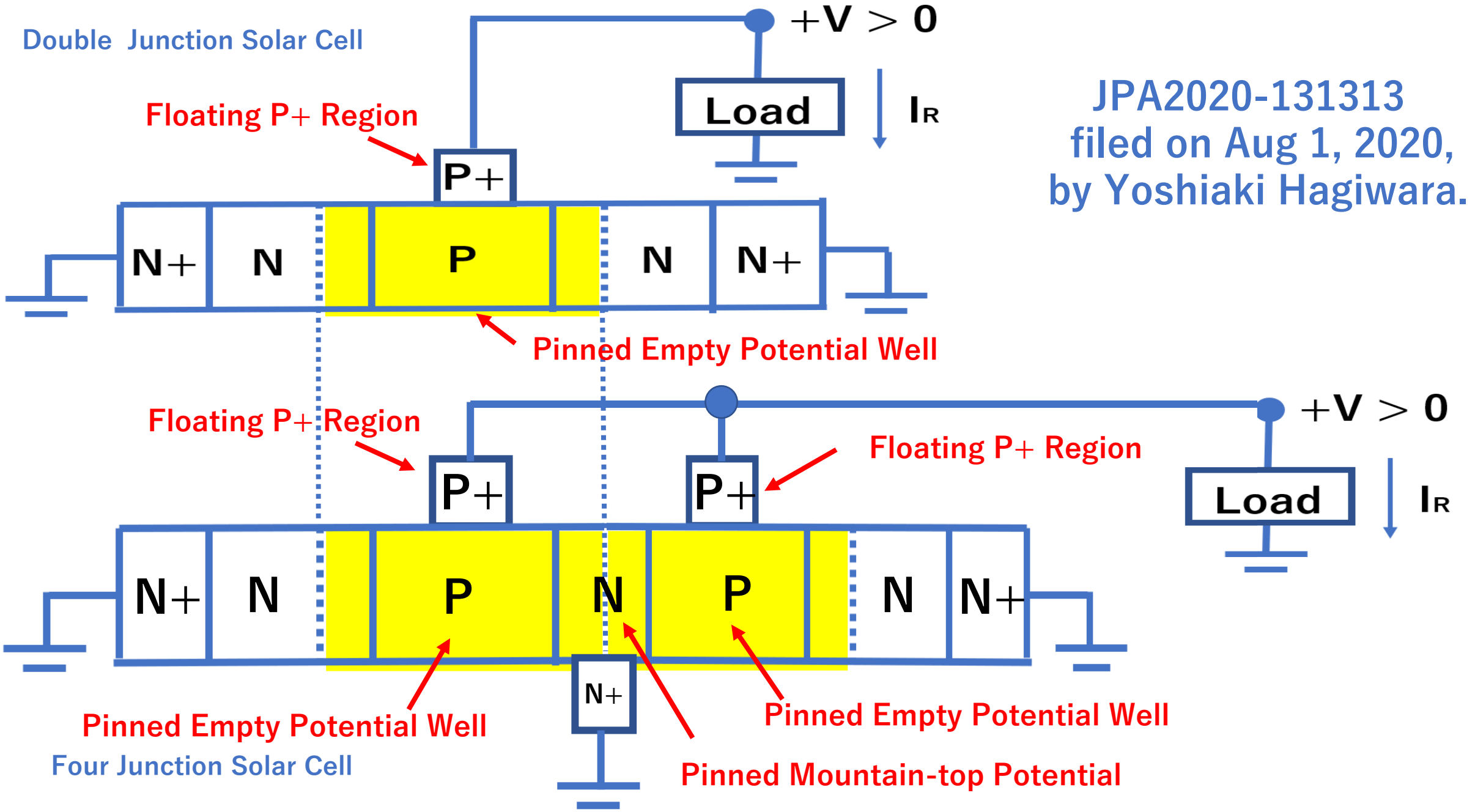
Single Junction Solar Cell



Double Junction Solar Cell

We can double the depletion width.
JPA2020-131313 file on Aug 1, 2020.

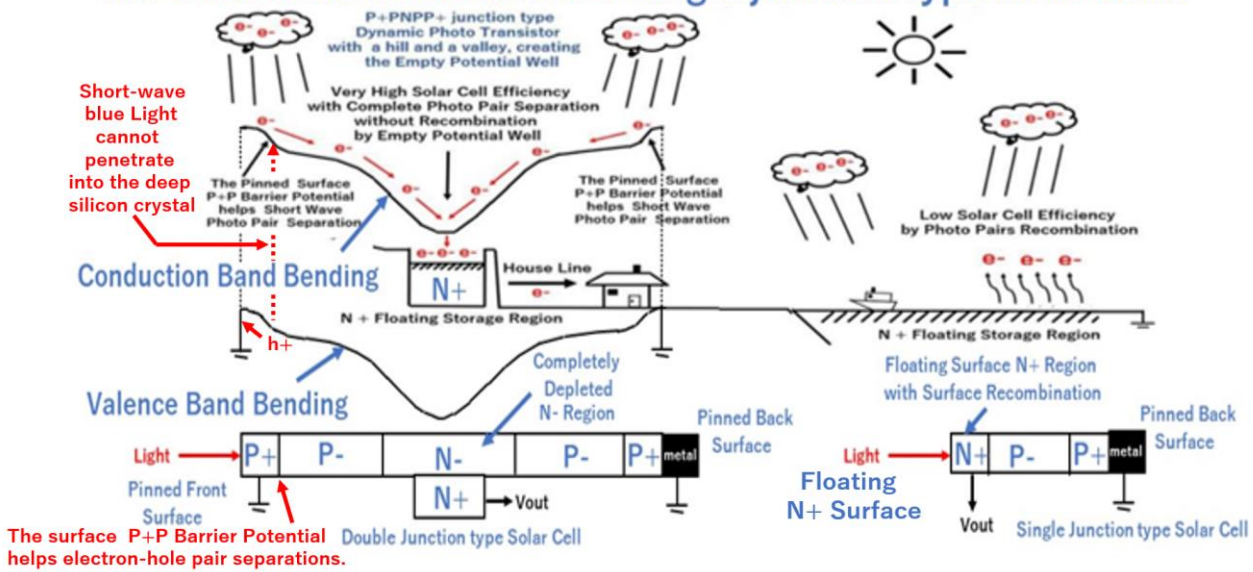




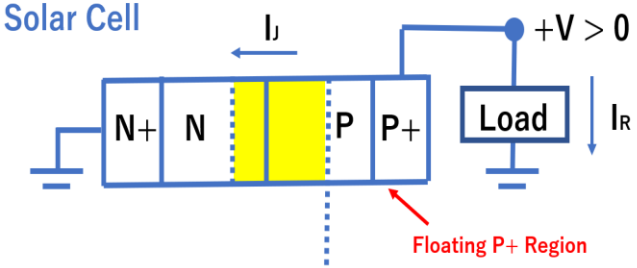
JPA2020-131313
filed on Aug 1, 2020,
by Yoshiaki Hagiwara.

True History of Photodiode

The difference of Double and Single junction type Solar Cells

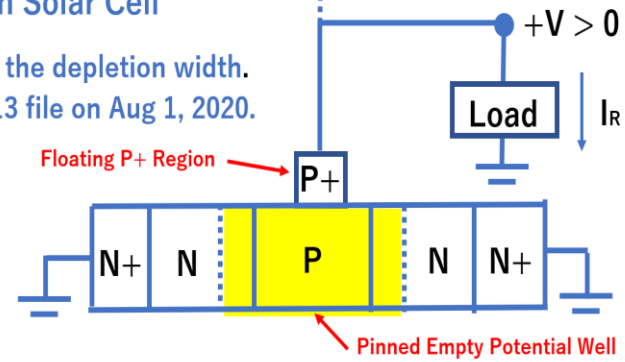


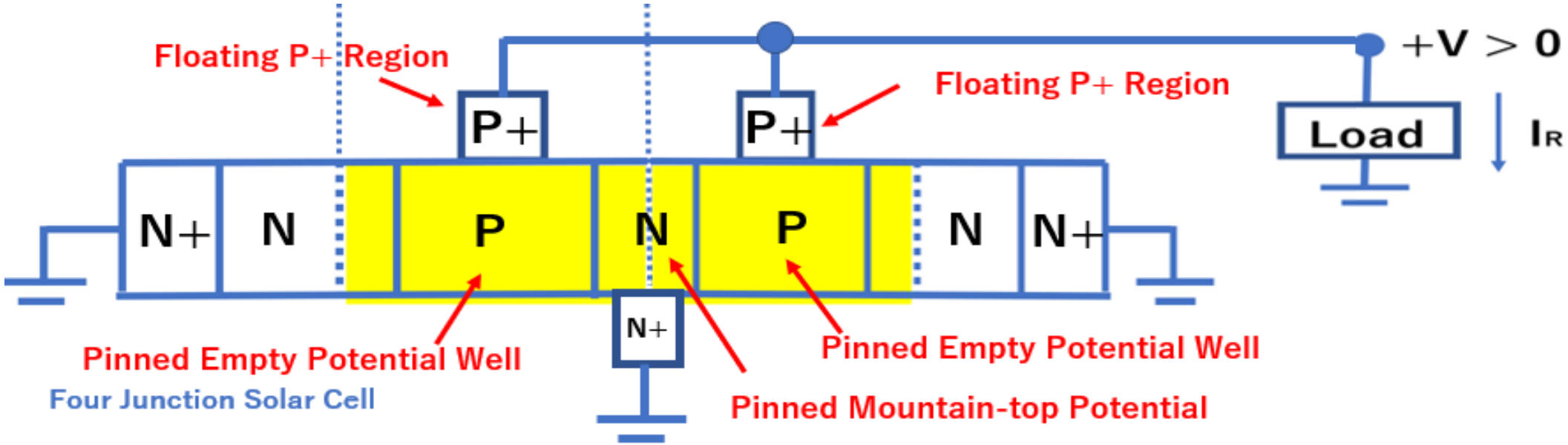
Single Junction Solar Cell



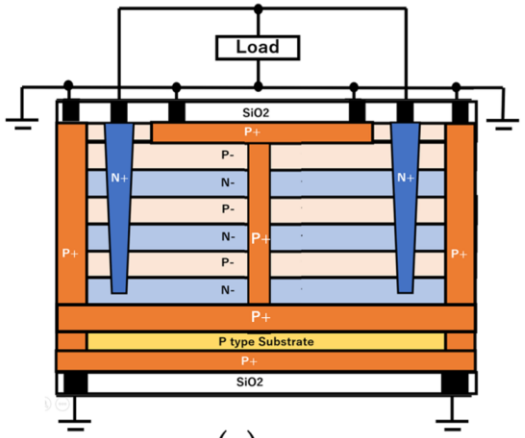
Double Junction Solar Cell

We can double the depletion width.
JPA2020-131313 file on Aug 1, 2020.



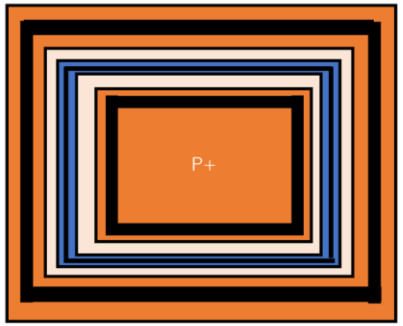


Multi-junction Solar Cell, based on JPA2020-131313 by Yoshiaki Hagiwara, applied on Aug. 1, 2020.



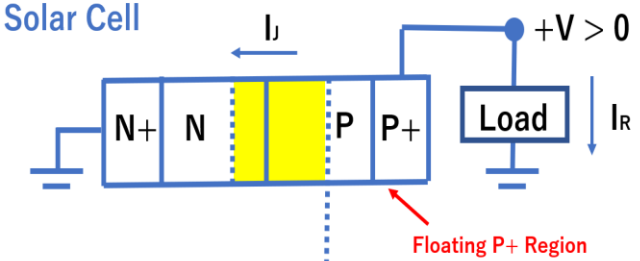
(a)

Top View



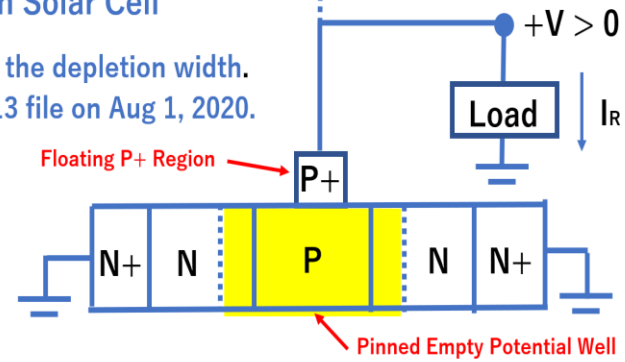
(b)

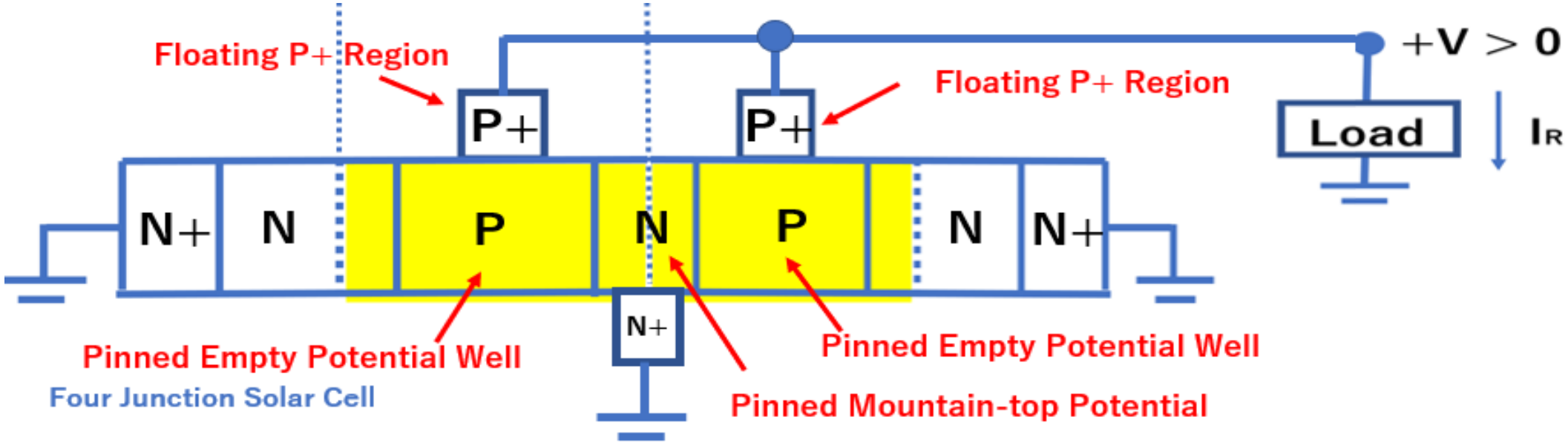
Single Junction Solar Cell



Double Junction Solar Cell

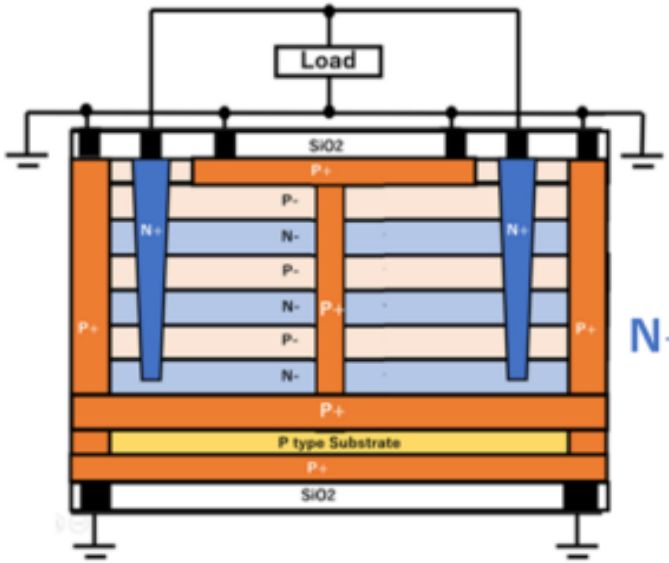
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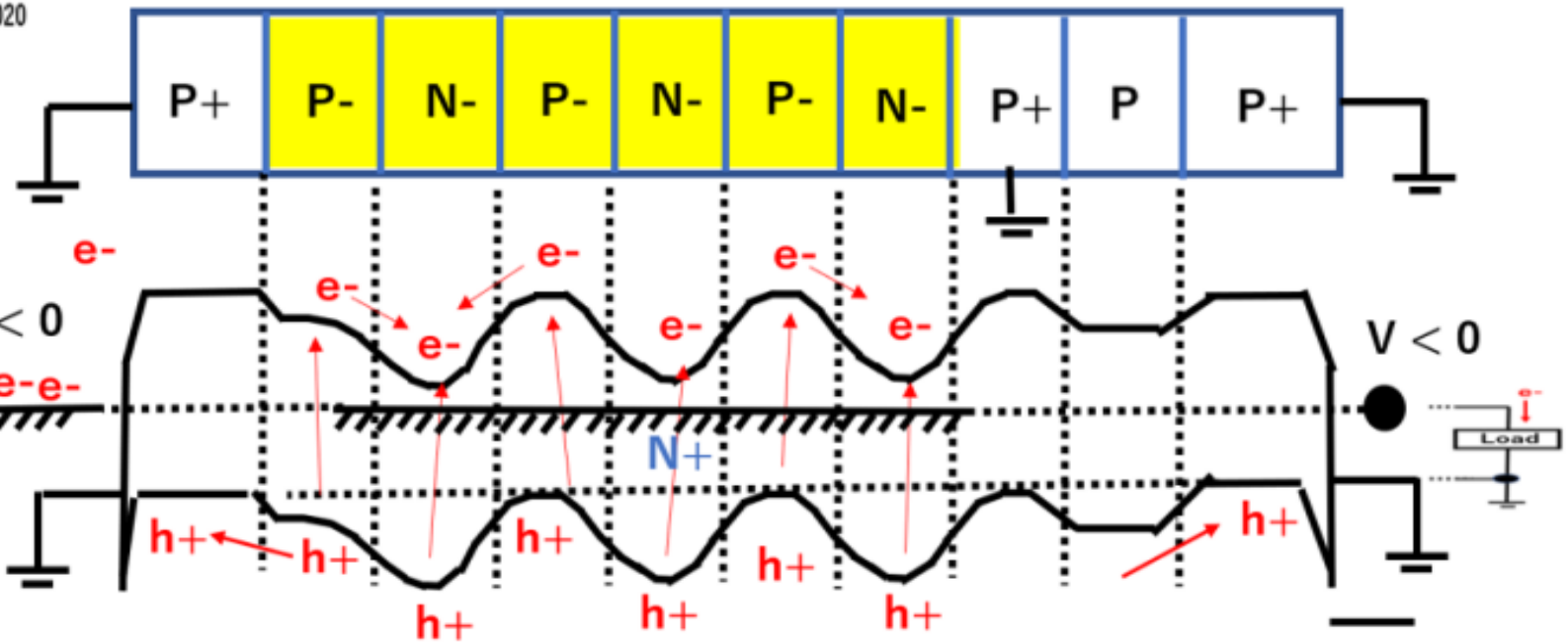


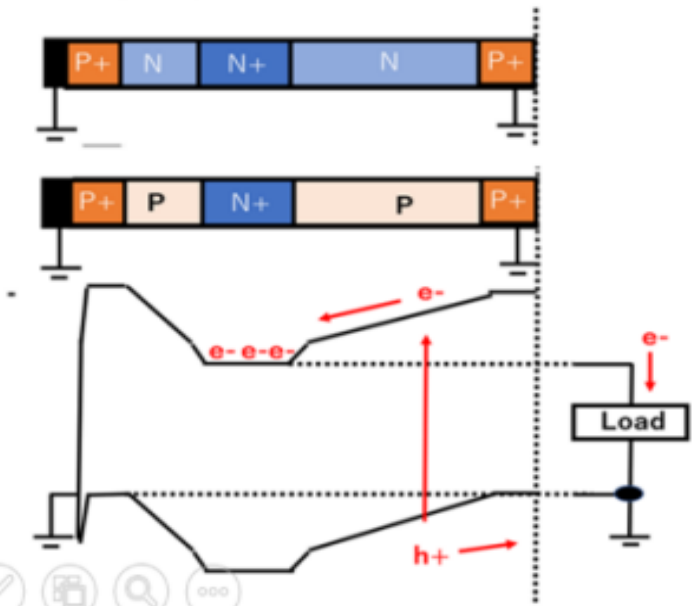


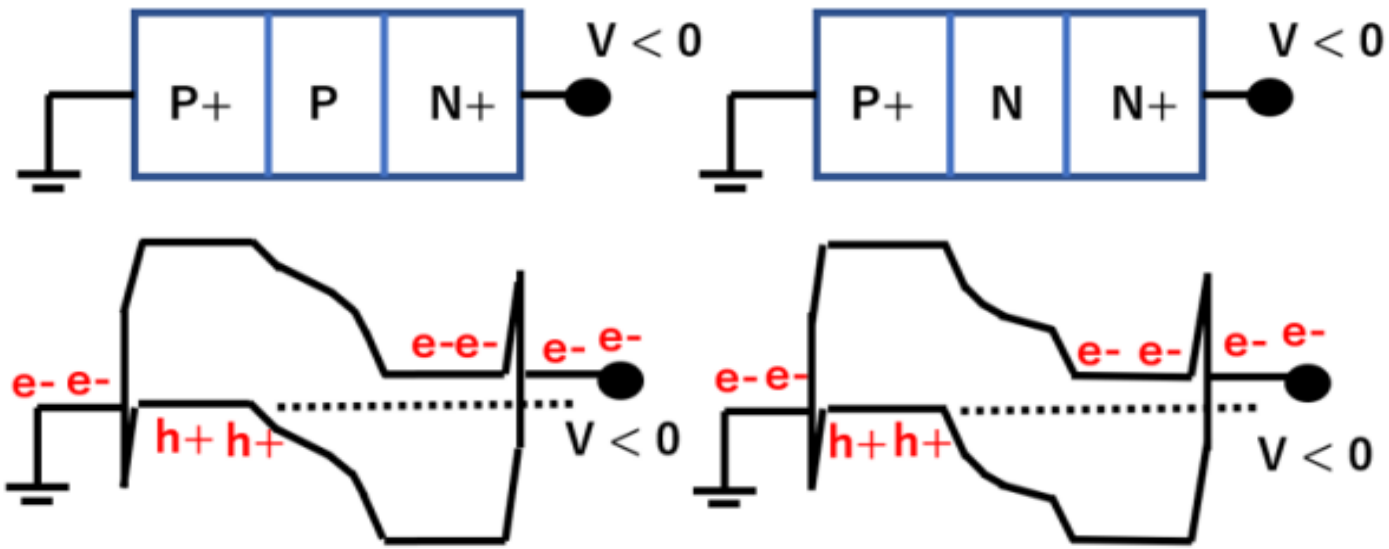
Multi-junction Pinned Photodiode with Completely Depleted of Photo Electron and Hole

Multi-junction Pinned Photodiode type Solar Cell Structure,
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by Yoshiaki Hagiwara, Sept 12, 2022



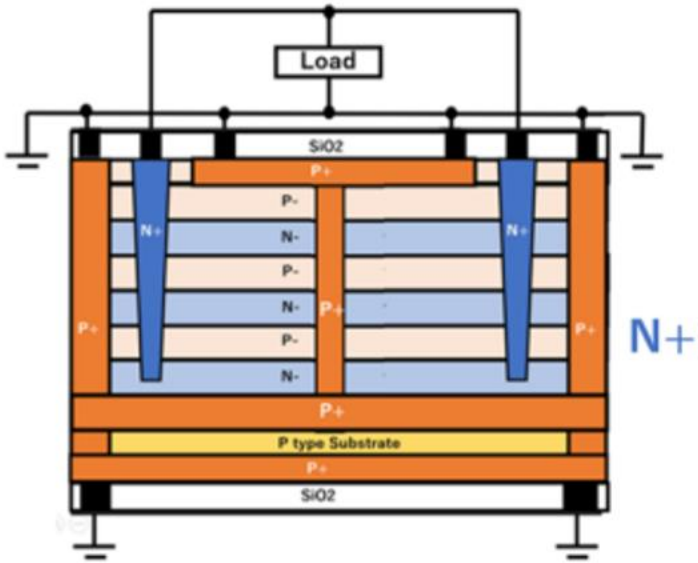


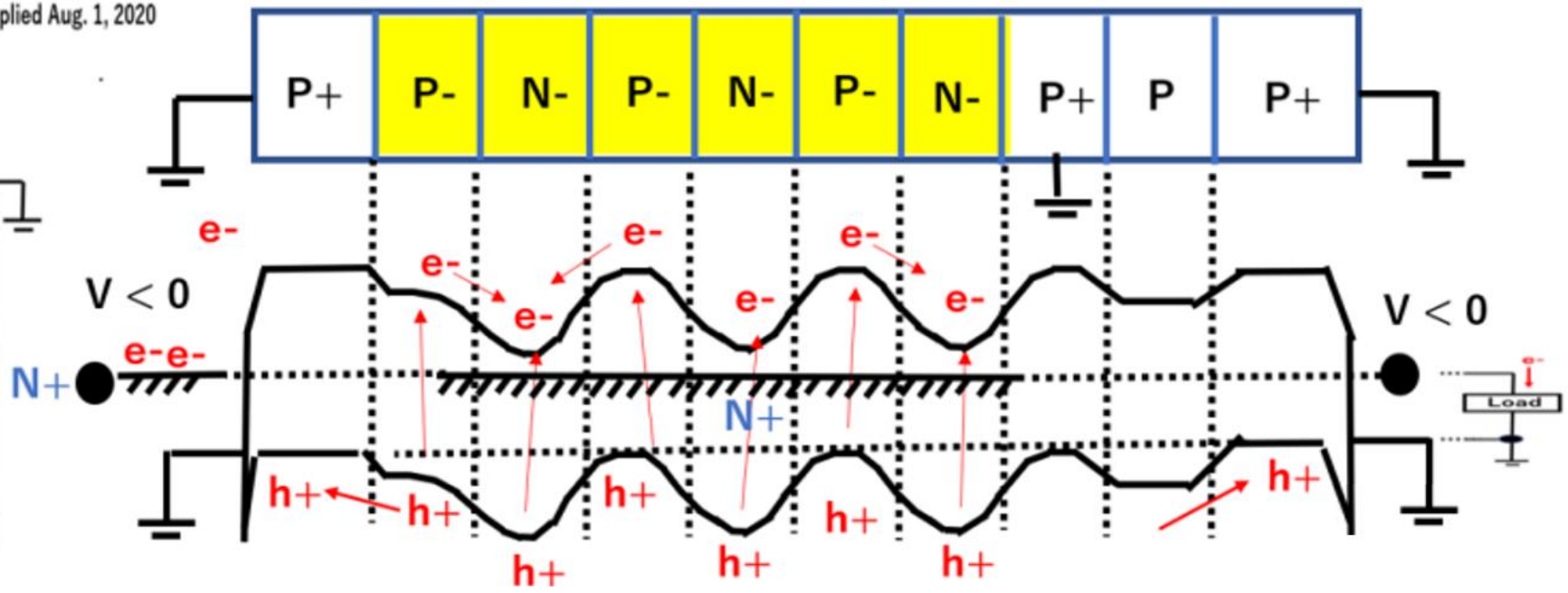


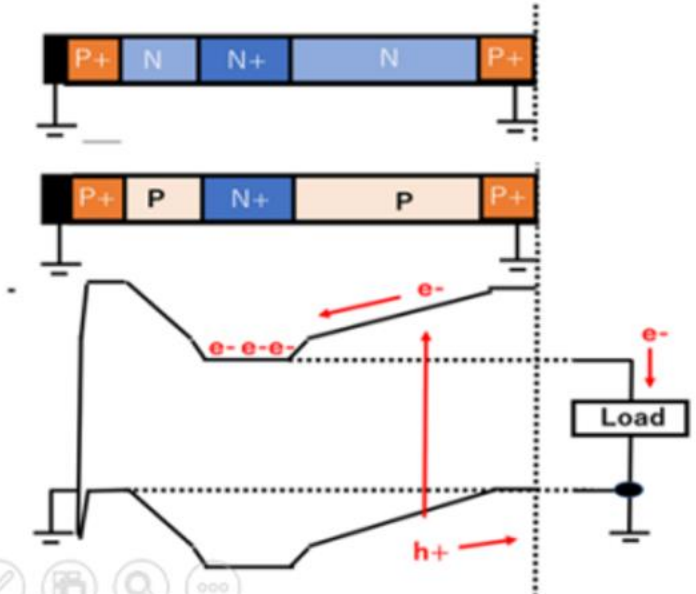


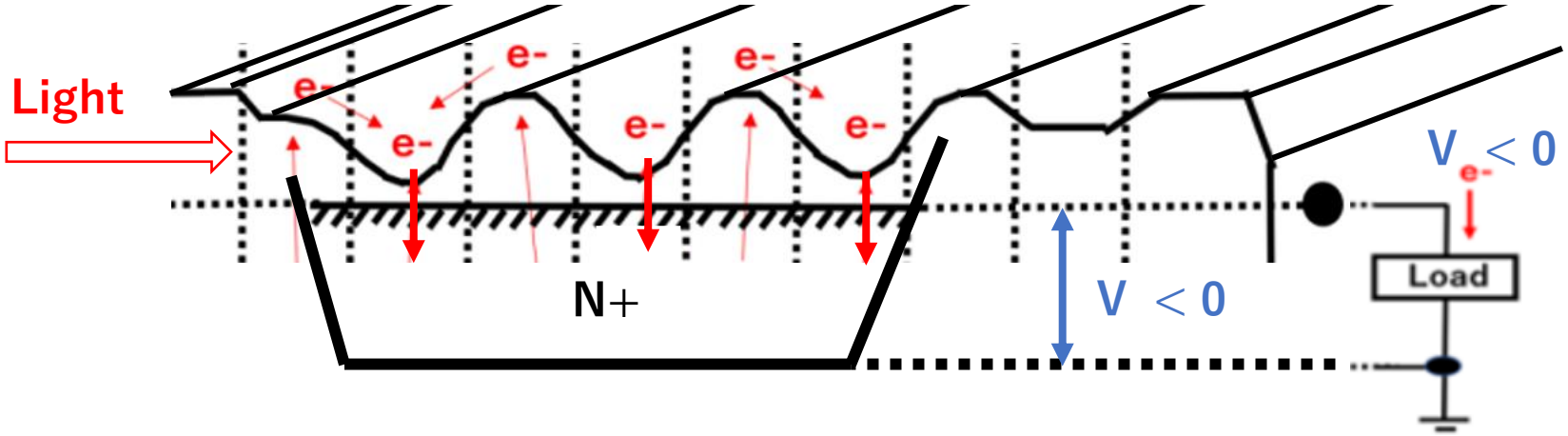
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https://en.wikipedia.org/wiki/Drift-field_transistor- Wikipedia

Invented in 1953 by Herbert Kroemer

Herbert KroemerはBaseの不純物濃度に勾配をつけた Drift Field Transistor を開発した。
さらにヘテロ接合半導体素子の優れた性能を世界で初めて指摘した。

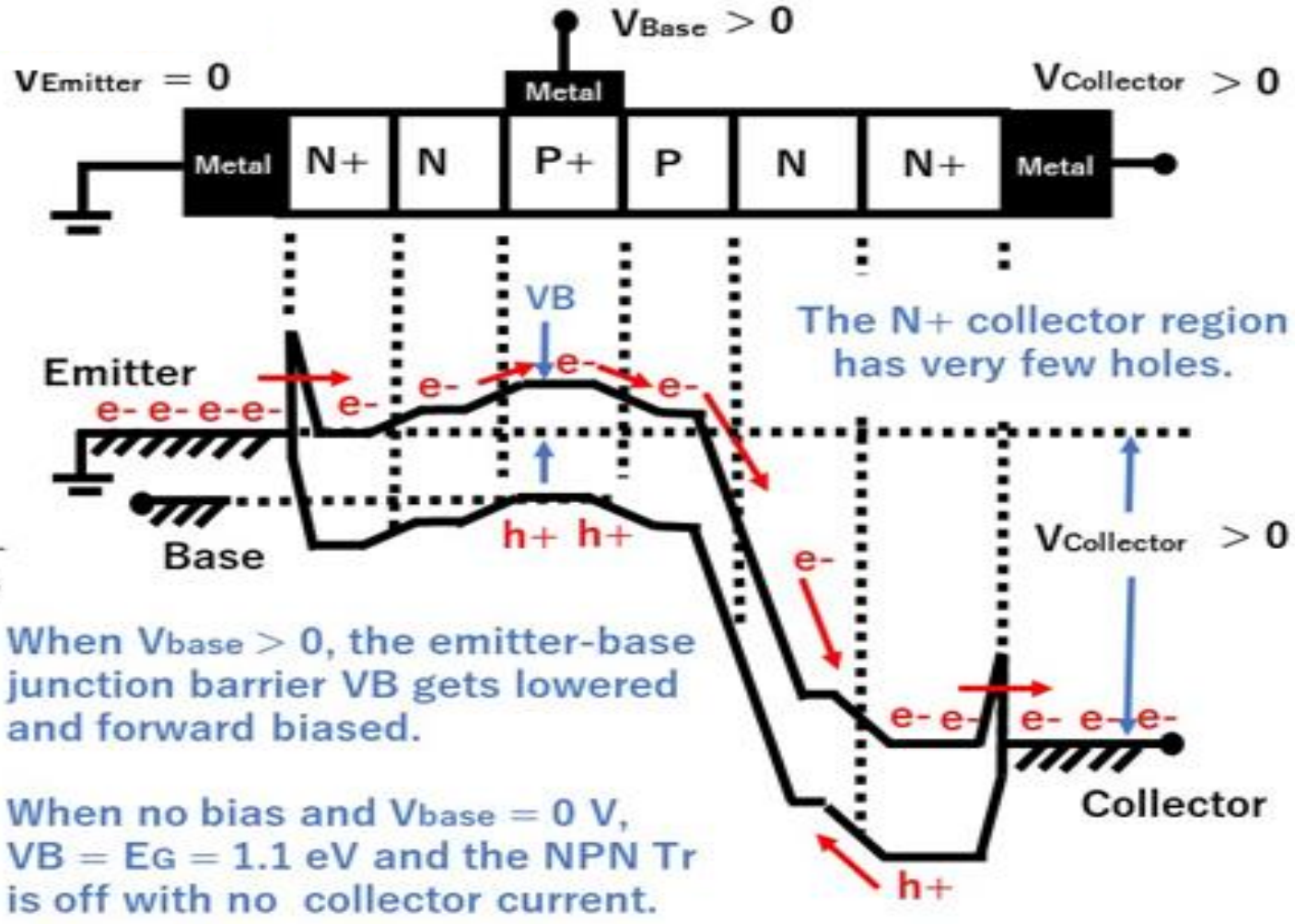
Herbert Kroemer（1928年8月28日生まれ）
ドイツ出身の物理学者。

1952年に、当時の新型トランジスタにおける熱電子効果の論文によってドイツのゲッティンゲン大学で理論物理学の博士号を取得。

1950年代に彼はドリフトトランジスタを開発し、ヘテロ接合を採用した半導体がよりよいパフォーマンスを見せることを初めて指摘した。

さらに有名なのは、1963年にいまや半導体レーザーの中心概念であるダブルのヘテロ接合のレーザーの概念を導入したことである。クレーマーは分子線エピタキシー法の草分けの一人である。

クレーマーとジョレス・アルフョーロフは、2000年、「高速エレクトロニクスおよび光エレクトロニクスに利用される半導体ヘテロ構造の開発」によりノーベル物理学賞を分け合った。



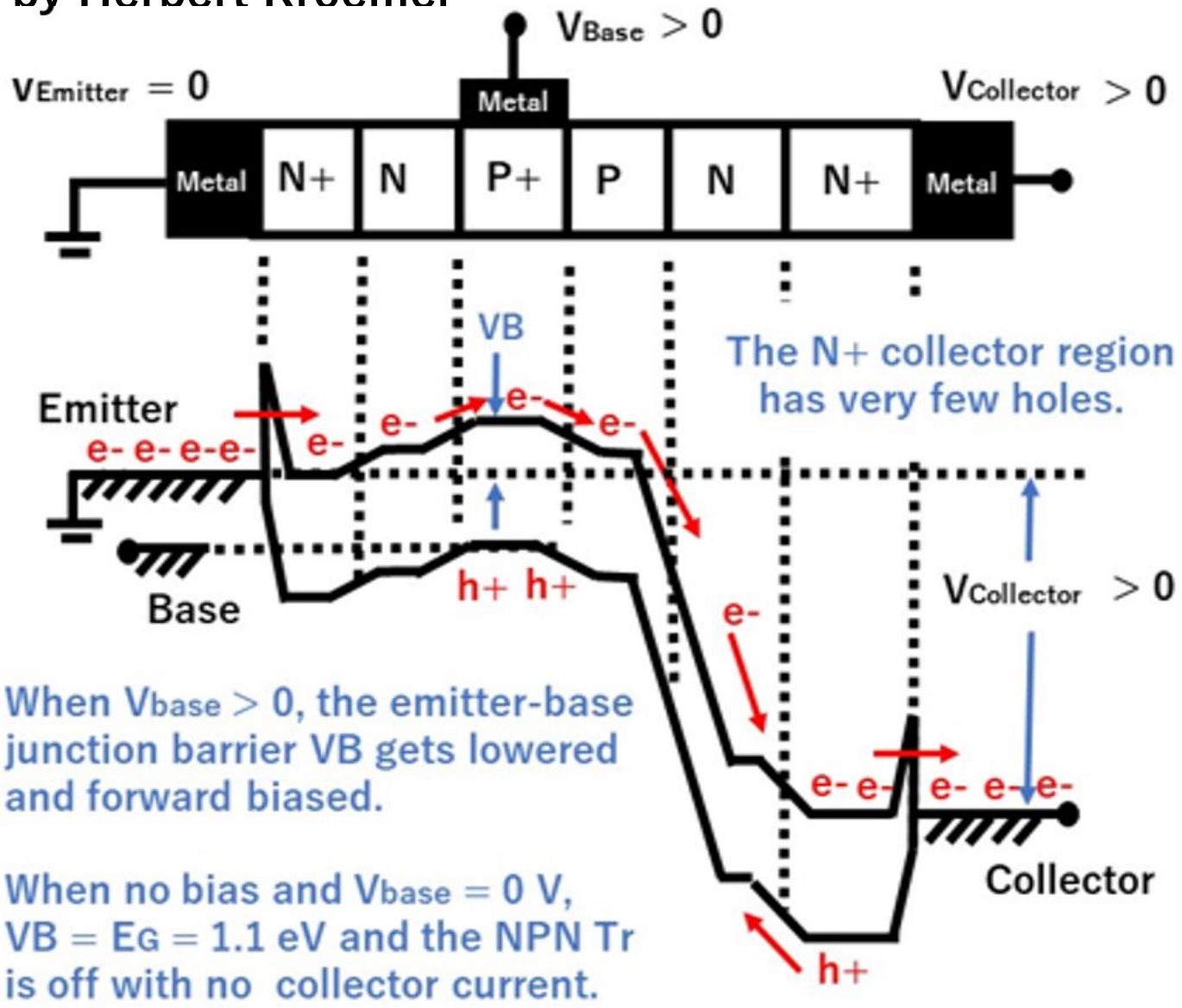
https://en.wikipedia.org/wiki/Drift-field_transistor- Wikipedia

Invented in 1953 by Herbert Kroemer

The drift-field transistor, also called the drift transistor or graded base transistor, is a type of high-speed bipolar junction transistor having a doping-engineered electric field in the base to reduce the charge carrier base transit time.

Invented by Herbert Kroemer at the Central Bureau of Telecommunications Technology of the German Postal Service, in 1953, it continues to influence the design of modern high-speed bipolar junction transistors.

Early drift transistors were made by diffusing the base dopant in a way that caused a higher doping concentration near the emitter reducing towards the collector.



Solid-State Electronics

Volume 24, Issue 12, December 1981, Pages 1161-1165



Theory of back surface field silicon solar cells

S.R. Dhariwal, Arun P. Kulshreshtha

Abstract

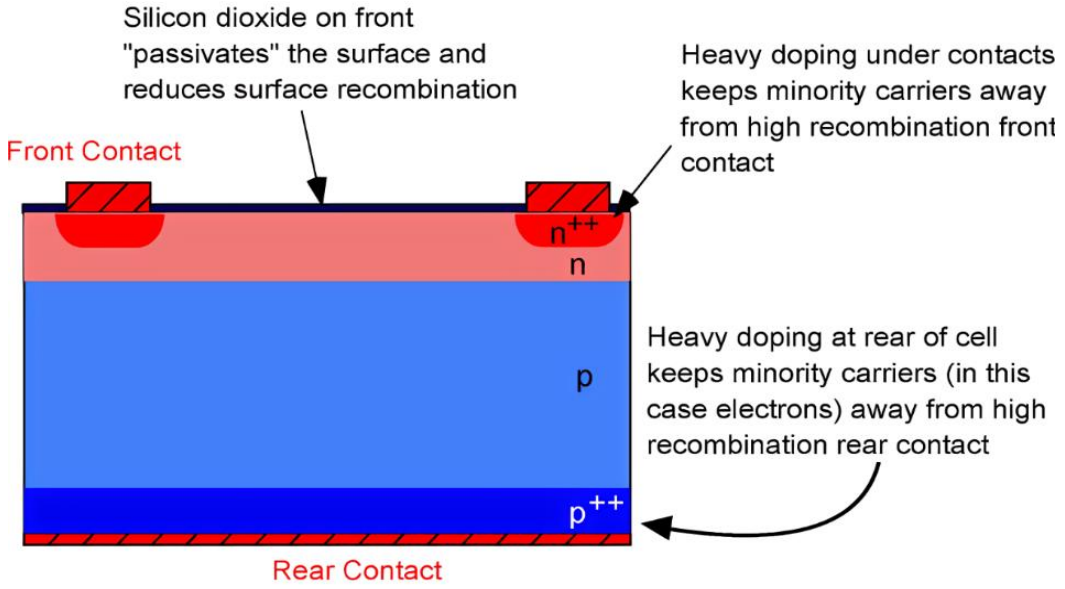
Back surface field silicon solar cells with n^+pp^+ (or sometimes p^+nn^+) structures are found to have better characteristics than the conventional solar cells. The existing theories have not been able to satisfactorily predict the experimentally observed parameters on these cells. A theory, based on the transport of both minority and majority carriers under the charge neutrality condition, has been developed in the present paper which explains the behavior of the back surface field solar cells. Good agreement is achieved between the results obtained by using this theory and the experimental observations of earlier workers.

Back Surface Field Silicon Solar Cell in vented by Wolf in 1963

*M. Wolf, Proc. IEEE, 51 (1963) 674



Conventional N++NPP++ type Solar Cell



https://www.sciencedirect.com/science/article/abs/pii/0038110181901854



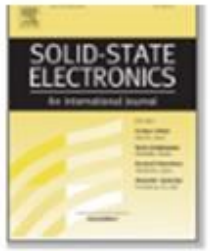
Back Surface Field Silicon Solar Cell の発明

受光表面（N+ またはP +）が浮遊状態にある、 古典的な（N+PまたはP+N）single 接合型のSolar Cell の量子効率は５％程度だった。 1963年に M. Wolf *は そこで裏面にPP+ または NN+ の不純物濃度勾配をつけて、 Band Gap の Bending 効果を利用して、Drift 電界を形成する事により、裏面の再結合を抑圧し、光起電力効果を高める事を 提案した。

Cell 内部で発生した Carrier の外部電極端子への流れを助ける事により裏面での再結合を小さくし、量子効率が高い太陽電池構造として注目された。その結果、金属端子と半導体との間の抵抗値をゼロとし導通性を高めた。その後多くの研究者により、 N+PP+またはP+NN+のSingle 接合型の Solar Cell の理論考察と特性改善が進んだ。現在では、Band Gap のトンネル効果によるオーミク・コンタクトとして理解され広く集積回路での金属配線コンタクトとして応用されている。

*M. Wolf, Proc. IEEE, 51 (1963) 674

Solid-State Electronics
Volume 24, Issue 12, December 1981, Pages 1161-1165



Theory of back surface field silicon solar cells

S.R. Dhariwal, Arun P. Kulshreshtha

Abstract

Back surface field silicon solar cells with n^+pp^+ (or sometimes p^+nn^+) structures are found to have better characteristics than the conventional solar cells. The existing theories have not been able to satisfactorily predict the experimentally observed parameters on these cells. A theory, based on the transport of both minority and majority carriers under the charge neutrality condition, has been developed in the present paper which explains the behavior of the back surface field solar cells. Good agreement is achieved between the results obtained by using this theory and the experimental observations of earlier workers.

裏面にP+層を設けるメリット

熱平衡状態では 電子とホールの密度の積は一定である。濃度の濃い P＋拡層領域内では ホールの密度は P+とほぼ等しい。高電位電子の密度は（P/P+）で減少する。再結合リーク電流が減る。 Solar Cell の量子変換効率を向上する。Solar Cellに寄与する電子は、PN 接合バリアを登れない、低電位電子、運動エネンルギーの小さな静かな電子である。

https://www.sciencedirect.com/science/article/abs/pii/0038110181901854

JPA2020-131313 on Aug 1, 2020　Patent 6818208

整理番号:P0I-202001 特願2020-131313 (Proof) 提出日:令和 2年 8月 1日 1/E

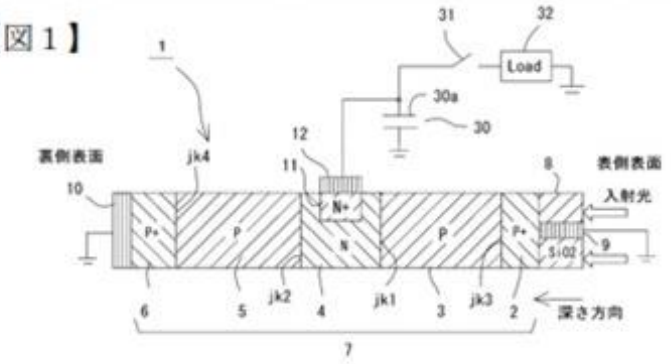
【書類名】 特許願
【整理番号】 P0I-202001
【あて先】 特許庁長官殿
【国際特許分類】 H01L 31/04
【発明者】
【住所又は居所】 神奈川県厚木市上荻野４３１３番地１
【氏名】 萩原 良昭
【特許出願人】
【住所又は居所】 神奈川県厚木市上荻野４３１３番地１
【氏名又は名称】 萩原 良昭

整理番号:P0I-202001 特願2020-131313 (Proof) 提出日:令和 2年 8月 1日 1

【書類名】明細書
【発明の名称】光電変換半導体装置
【技術分野】
【０００１】
本発明は光電変換半導体装置に係り、とくに光電変換半導体装置内に生じた光電子の再結合を抑制することでエネルギー変換効率を改善するようにした光電変換半導体装置に関する。
【背景技術】
【０００２】
地球温暖化を抑制する自然エネルギーとして太陽光発電が注目されている。太陽光発電には、Ｎ型半導体領域とＰ型半導体領域を隣接させたＰＮ接合を有し、光照射で生じた光電子と正孔を各々、ＰＮ接合の空乏層内に生じるＰＮ接合型バリア電界によりＮ型半導体領域側とＰ型半導体領域側に分離させて、Ｎ型半導体領域のＰＮ接合とは反対側端部と、Ｐ型半導体領域のＰＮ接合とは反対側端部の間に光起電力を生じさせるようにした光電変換半導体装置が用いられる。
ところで、太陽光のエネルギー密度は薄く、発電量を増やそうとすると大規模な施設が必要となる。このため、太陽光発電の普及には、太陽電池の変換効率の更なる改善が重要である。

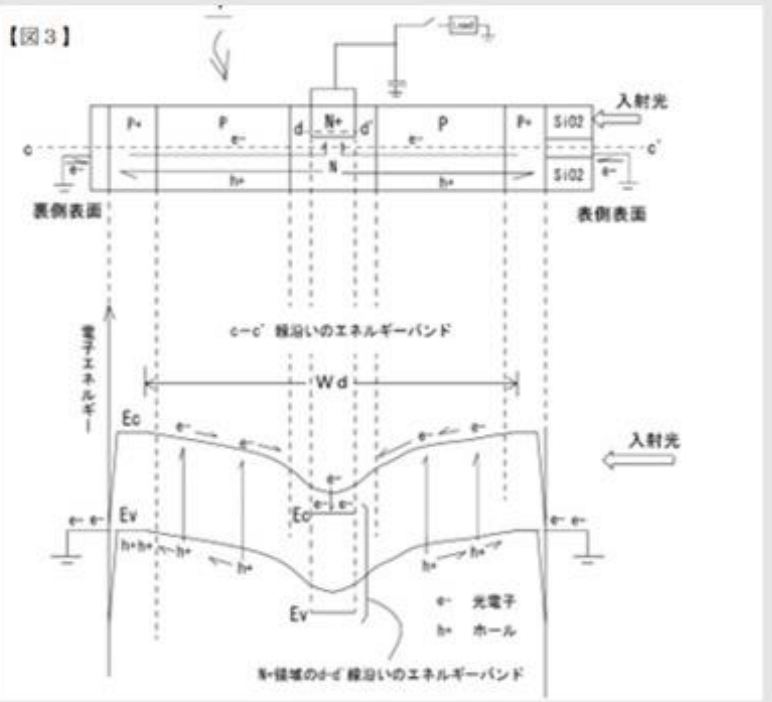
【解決手段】 光電変換半導体装置の深さ方向にＮ領域４の表裏をＰ領域３、５で挟み、更にＰ領域３の表側とＰ領域５の裏側を、濃度勾配型バリア電界生成用のＰ＋領域２とＰ＋領域６で挟んだＰ＋ＰＮＰＰ＋接合部７を設ける。Ｐ＋領域２の表側に受光窓領域８、第１の極性の外面電極９、Ｐ＋領域６の裏側に第１の極性の外面電極１０を設ける。Ｎ領域４の深さ方向の中央部に光電子吸出し用のＮ＋領域１１を設け、Ｎ＋領域１１の外側に第２の極性の外面電極１２を設ける。第１の極性の外面電極９、１０をグランドに接続し、第２の極性の外面電極１２とグランドの間に、電荷蓄積用の容量３０を接続する。

【図１】

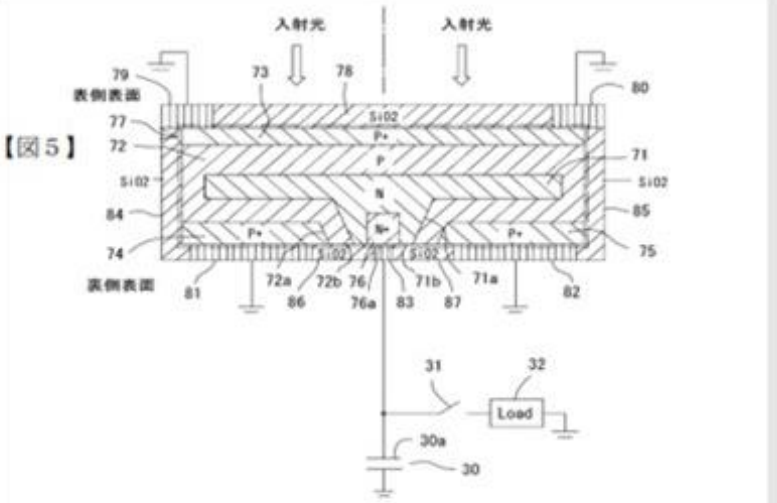




【図３】

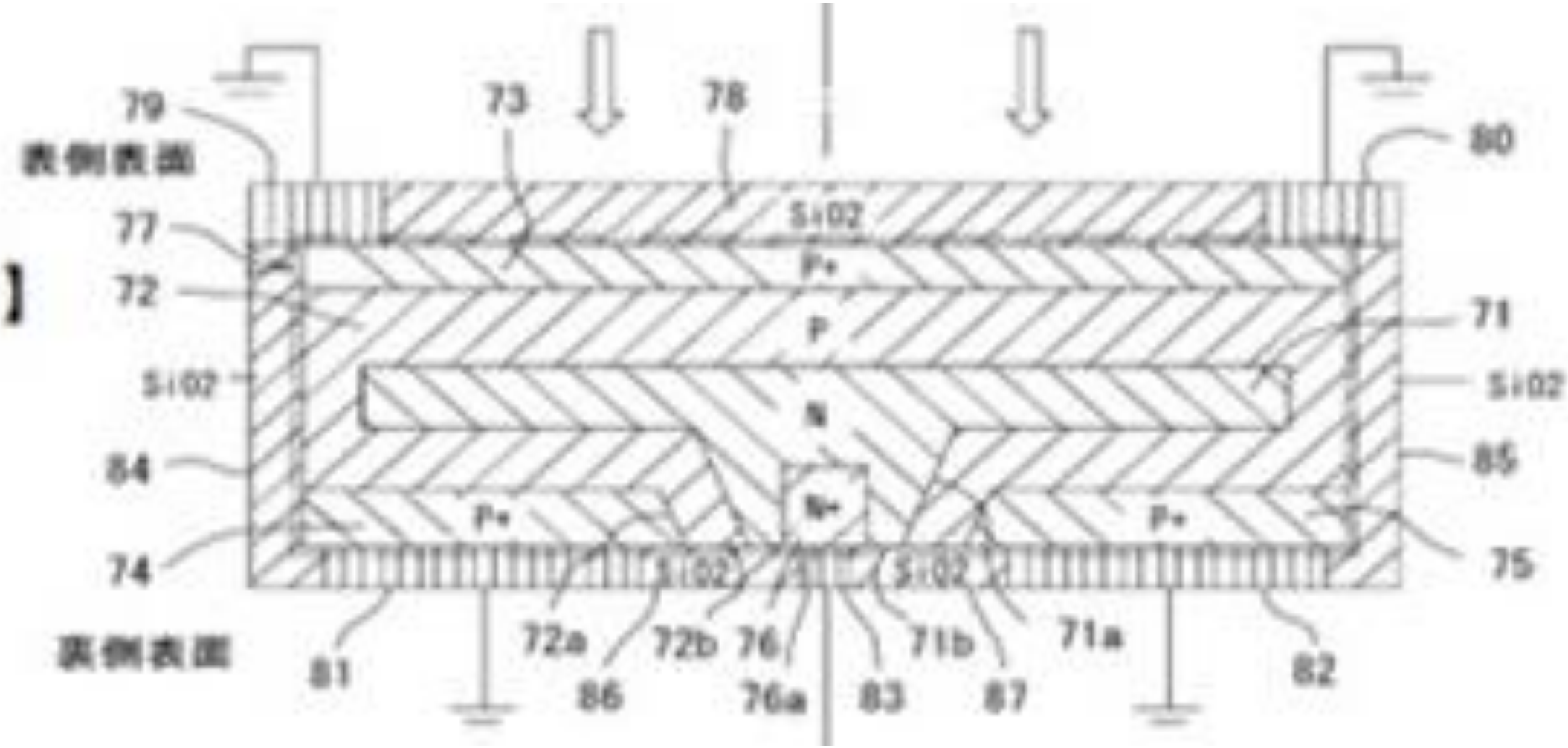


【図５】



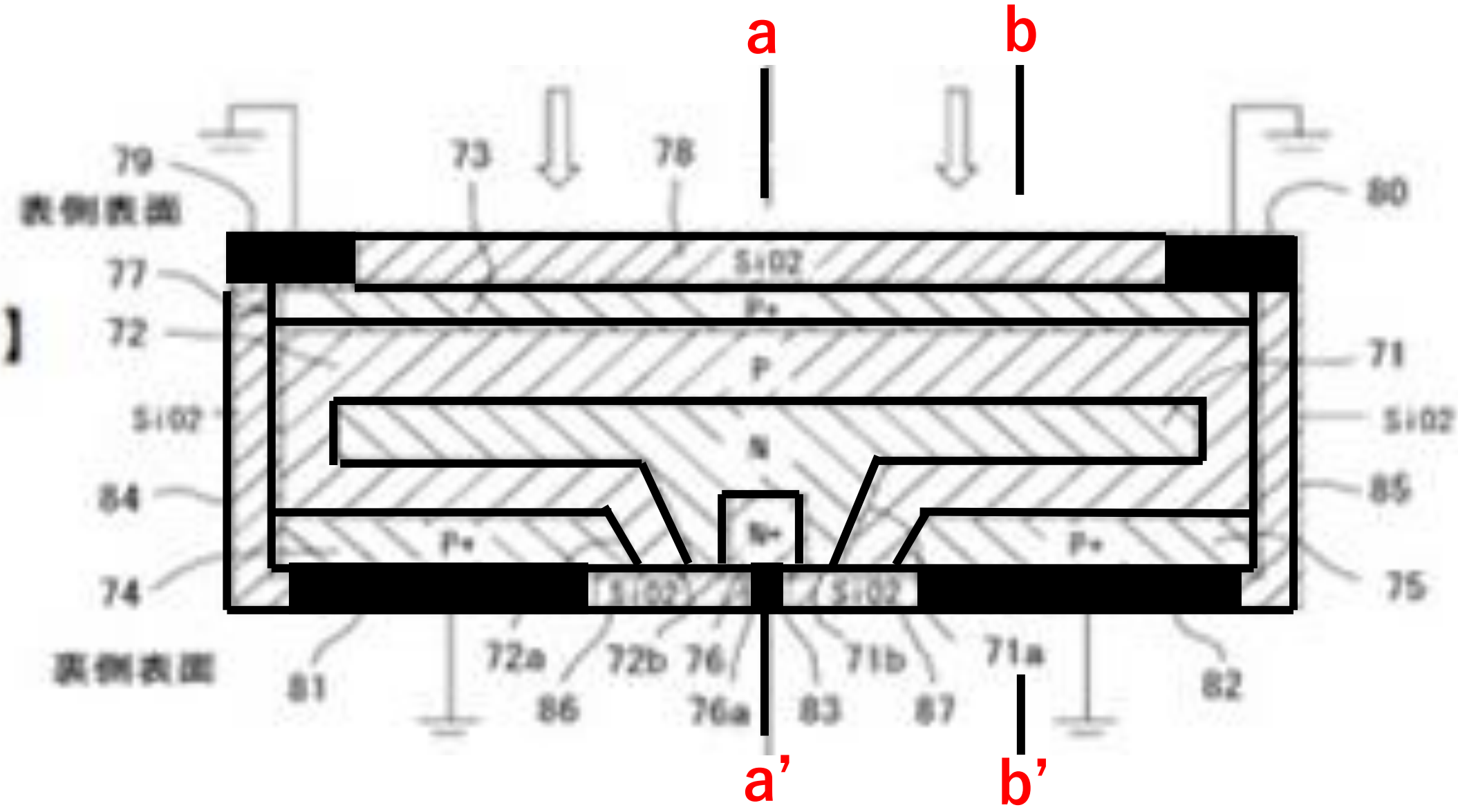
JPA2020-131313 on Aug 1, 2020　Patent 6818208

【図５】

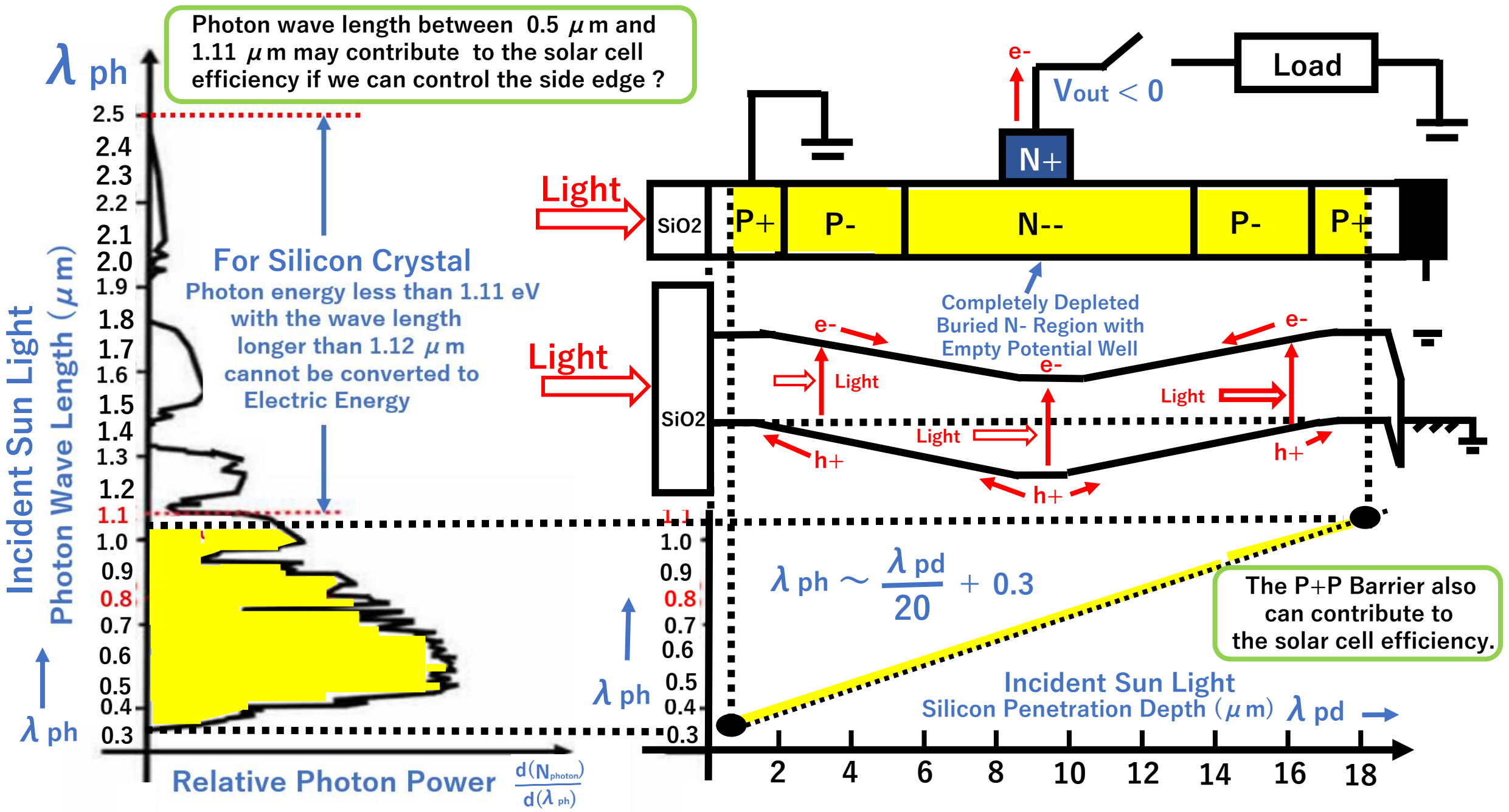


JPA2020-131313 on Aug 1, 2020　Patent 6818208

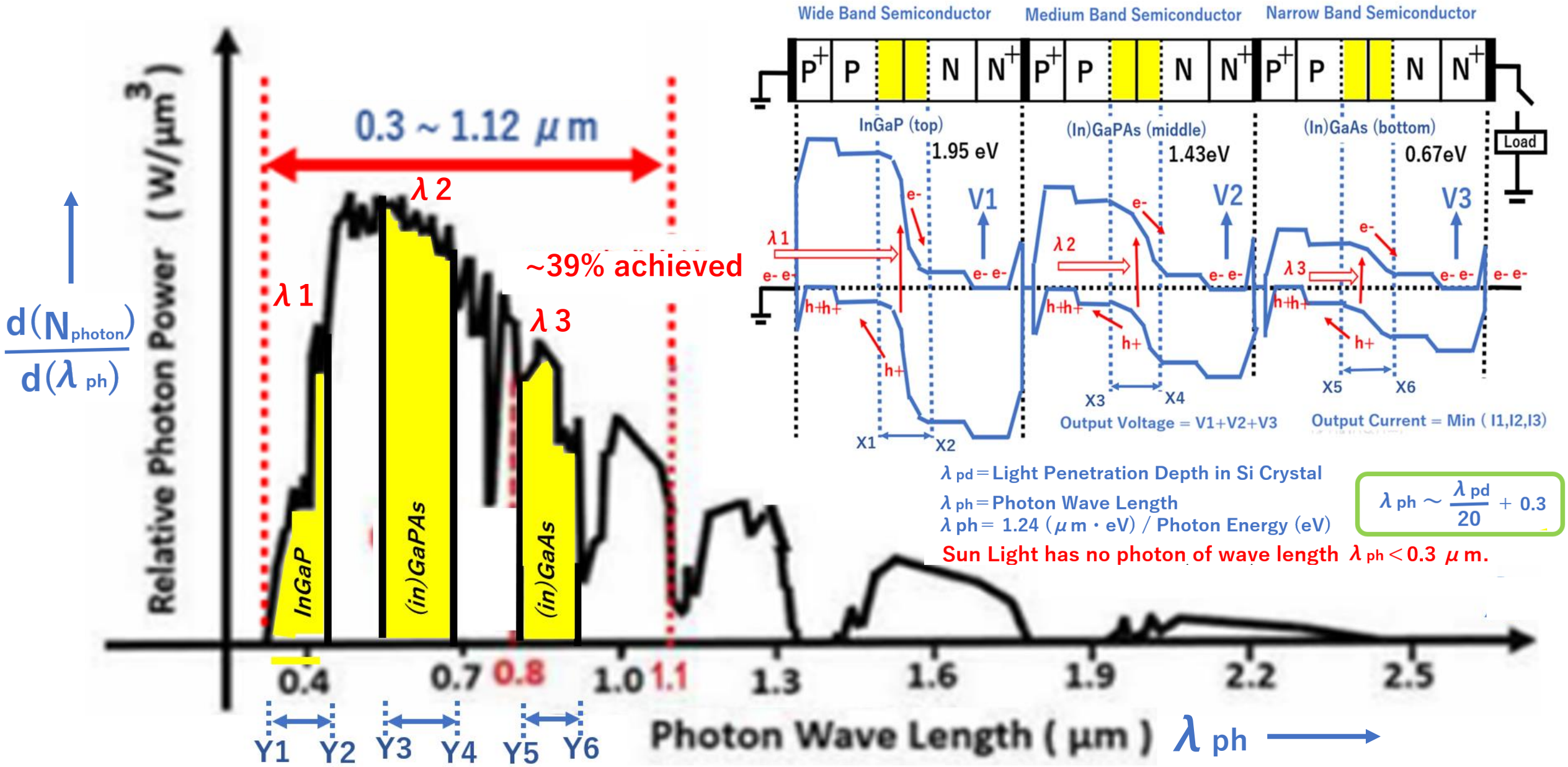
【図５】



The P+P-N-P-P+ double junction type Solar Cell may have much higher efficiency



Triple Junction Solar Cell with Wide Band Gap Compound Semiconductors achieved ~39% Quantum Efficiency



λ pd = Light Penetration Depth in Si Crystal

λ ph = Photon Wave Length

λ ph = 1.24 (μm・eV) / Photon Energy (eV)

$$\lambda_{ph} \sim \frac{\lambda_{pd}}{20} + 0.3$$

Sun Light has no photon of wave length $\lambda_{ph} < 0.3\ \mu m$.

太陽電池の変換効率の限界

変換効率は、使用される半導体材料が吸収できる太陽光の波長領域と、PN接合の空乏層領域での吸収量で求まります。シリコン結晶では、波長が 0.29μmから 1.20μm までの太陽光を吸収できます。Single PN 接合型での変換効率の限界理論値は 28% です。実際には20%程度です。その理由は(1)受光面での反射や(2)受光表面再結合や(3)PN接合の空乏層内での結晶欠陥による再結合や(4)裏面再結合などが生じ、光電変換された光電子とホールのペアが再結合し無駄になる為です。

Silicon のBand Gap は　1.1 eV

InP のBand Gap は　1.34 eV

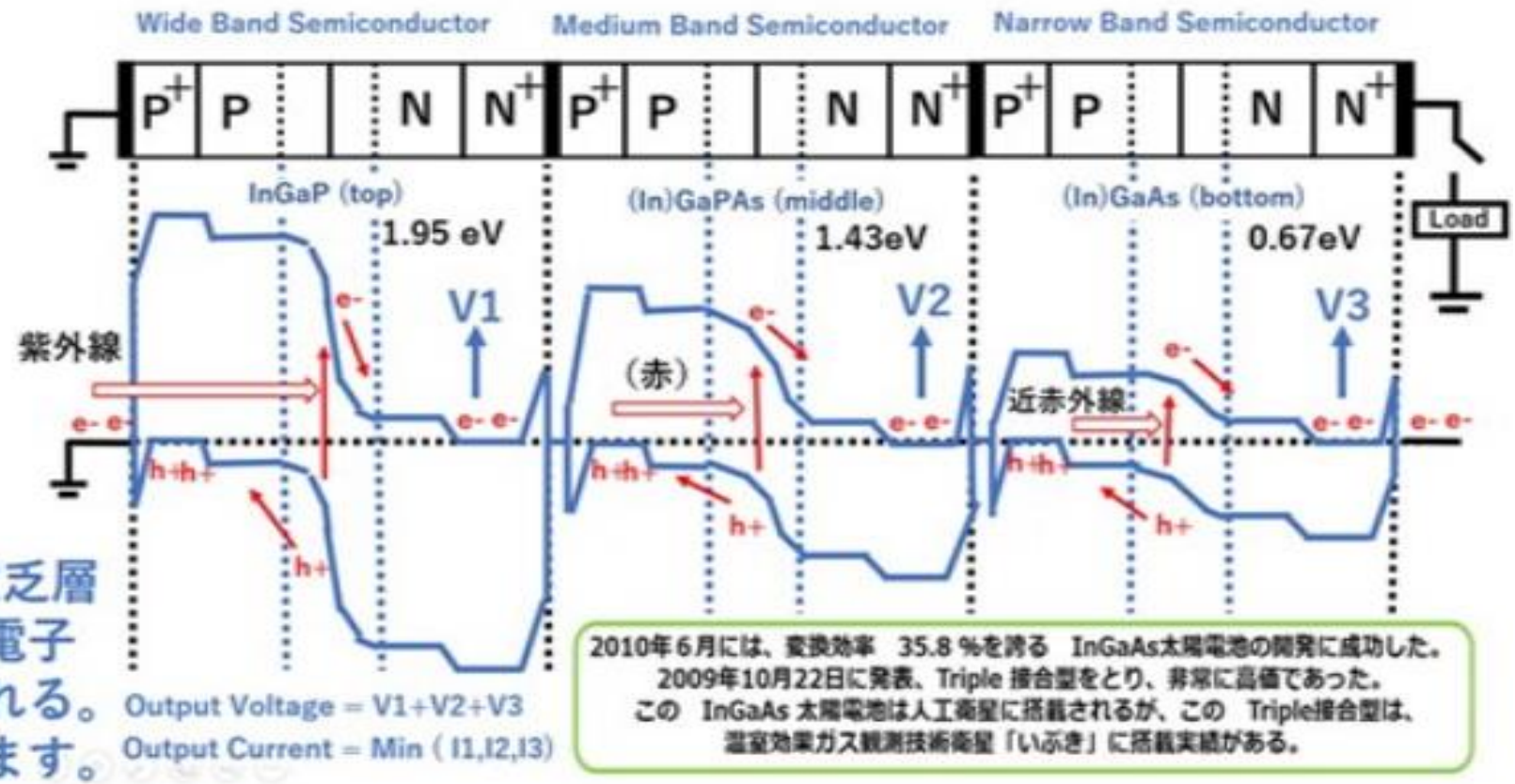
GaAs のBand Gap は　1.42 eV

CdTe のBand Gap は　1.48 eV

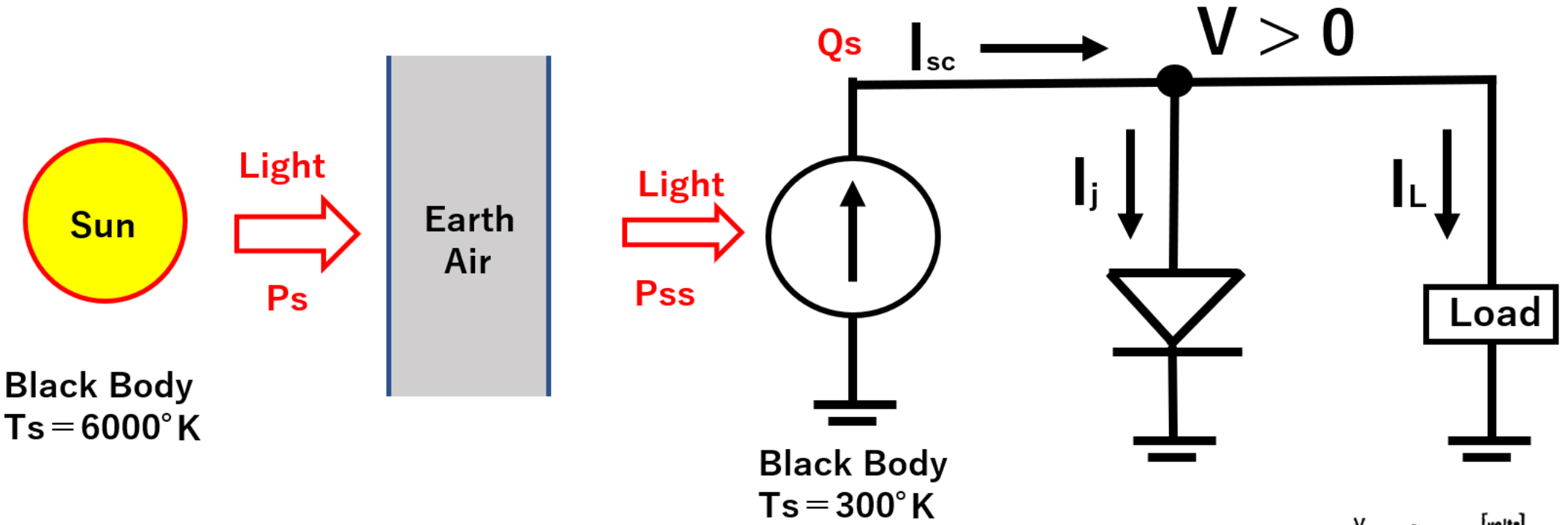
GaN のBand Gap は　3.4 eV

β-Ga_2O_3 のBand Gap は 4.5 eV

バリア電界が存在するPN接合の空乏層領域内でのみ、光電変換による光電子とホールのペアは効率良く分離される。と言う事が、今の常識となっています。



2010年6月には、変換効率　35.8 %を誇る　InGaAs太陽電池の開発に成功した。
2009年10月22日に発表、Triple 接合型をとり、非常に高価であった。
この　InGaAs 太陽電池は人工衛星に搭載されるが、この　Triple接合型は、
温室効果ガス観測技術衛星「いぶき」に搭載実績がある。



$$Ps = 2\pi h/c^2 \int_0^\infty \nu^3 d\nu/[\exp(h\nu/kT_s)-1]$$

$$Qs = (2\pi/c^2) \int_{\nu_g}^\infty [\exp(h\nu/kT_s)-1]^{-1}\nu^2 d\nu$$

$$E_g = h\nu_g = qV_g$$

$$\text{(Solar Cell Efficiency)} \sim \frac{(h\nu_g)Qs}{Ps} = \frac{(h\nu_g)(2\pi/c^2)\int_{\nu_g}^\infty [\exp(h\nu/kT_s)-1]^{-1}\nu^2 d\nu}{2\pi h/c^2 \int_0^\infty \nu^3 d\nu/[\exp(h\nu/kT_s)-1]}$$

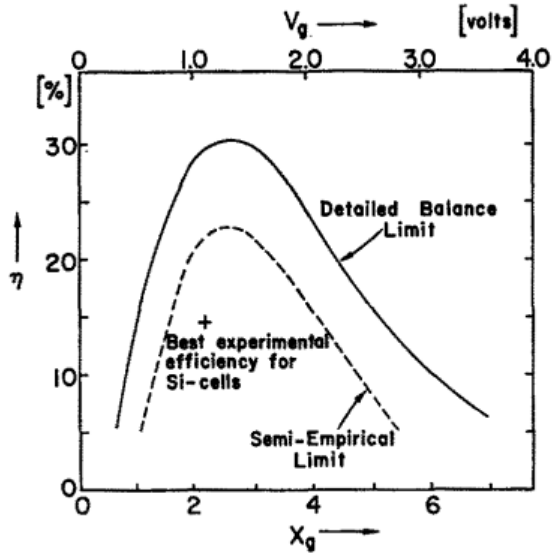


FIG. 1. Comparison of the "semiempirical limit" of efficiency of solar cells with the "detailed balance limit," derived in this paper. + represents the "best experiment efficiency to date" for silicon cells. (See footnote 6.)

Journal of Applied Physics

Detailed Balance Limit of Efficiency of *p-n* Junction Solar Cells

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William Shockley and Hans J. Queisser

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JOURNAL OF APPLIED PHYSICS VOLUME 32, NUMBER 3 MARCH, 1961

Detailed Balance Limit of Efficiency of *p-n* Junction Solar Cells*

WILLIAM SHOCKLEY AND HANS J. QUEISSER
Shockley Transistor, Unit of Clevite Transistor, Palo Alto, California
(Received May 3, 1960; in final form October 31, 1960)

In order to find an upper theoretical limit for the efficiency of *p-n* junction solar energy converters, a limiting efficiency, called the *detailed balance limit* of efficiency, has been calculated for an ideal case in which the only recombination mechanism of hole-electron pairs is radiative as required by the principle of detailed balance. The efficiency is also calculated for the case in which radiative recombination is only a fixed fraction f_c of the total recombination, the rest being nonradiative. Efficiencies at the matched loads have been calculated with band gap and f_c as parameters, the sun and cell being assumed to be blackbodies with temperatures of 6000°K and 300°K, respectively. The maximum efficiency is found to be 30% for an energy gap of 1.1 ev and $f_c=1$. Actual junctions do not obey the predicted current-voltage relationship, and reasons for the difference and its relevance to efficiency are discussed.

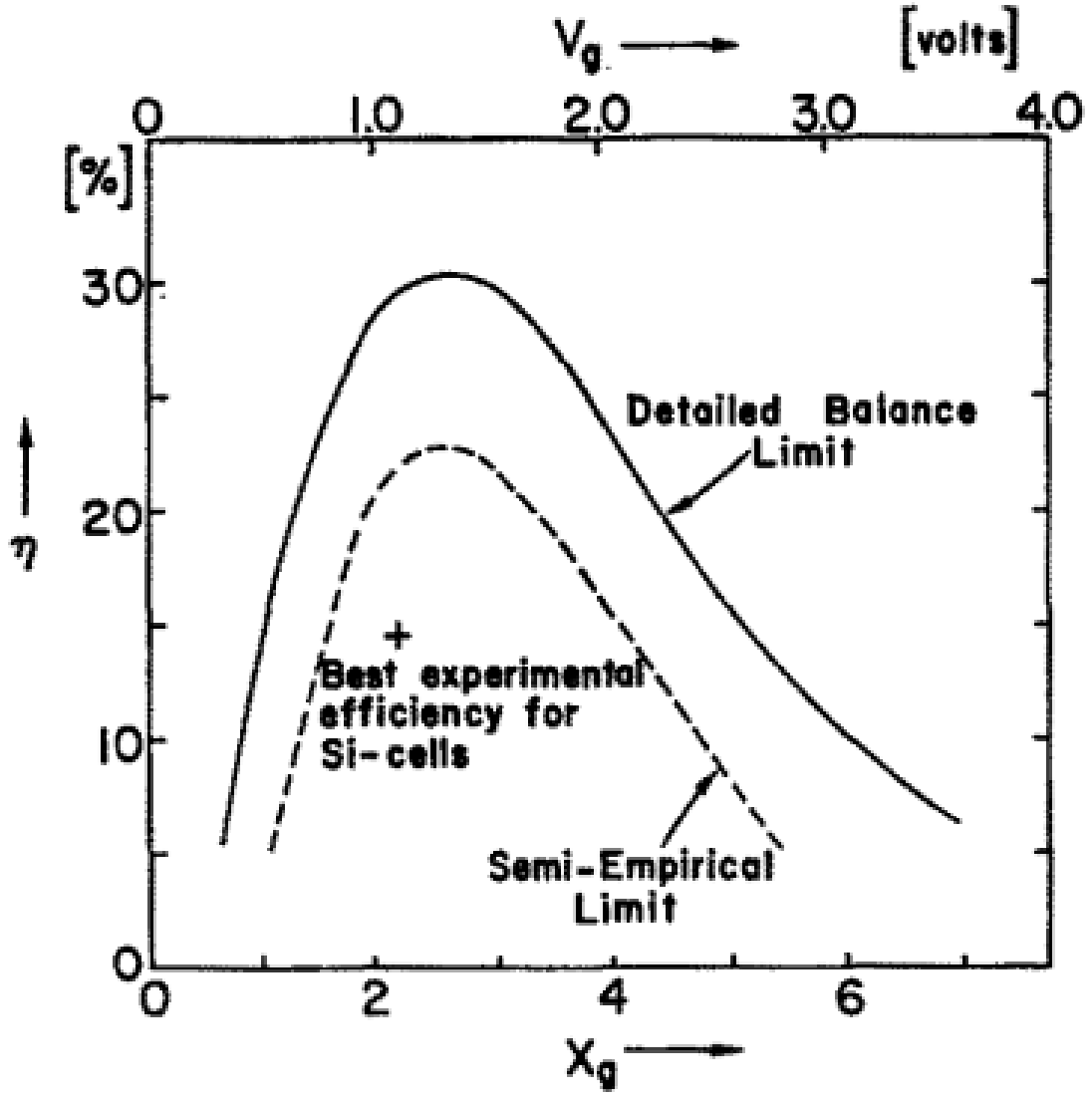


FIG. 1. Comparison of the "semiempirical limit" of efficiency of solar cells with the "detailed balance limit," derived in this paper. + represents the "best experiment efficiency to date" for silicon cells. (See footnote 6.)

t_s = the probability that a photon with $h\nu > E_g$ incident on the surface will produce a hole-electron pair. (1.6)

For the detailed balance efficiency limit to be reached, t_s must be unity.

These variables are: the temperature of the sun T_s,

$$kT_s = qV_s; \tag{1.1}$$

the temperature of the solar cell T_c,

$$kT_c = qV_c; \tag{1.2}$$

and the energy gap E_g,

$$E_g = h\nu_g = qV_g, \tag{1.3}$$

where k is Boltzmann's constant, $q = |q|$ is the electronic charge, and h is Planck's constant. The efficiency is found to involve only the two ratios

$$x_g = E_g/kT_s \tag{1.4}$$

$$x_c = T_c/T_s. \tag{1.5}$$

Each photon with energy greater than $h\nu_g$ produces one electronic charge q at a voltage of $V_g = h\nu_g/q$. (2.1)

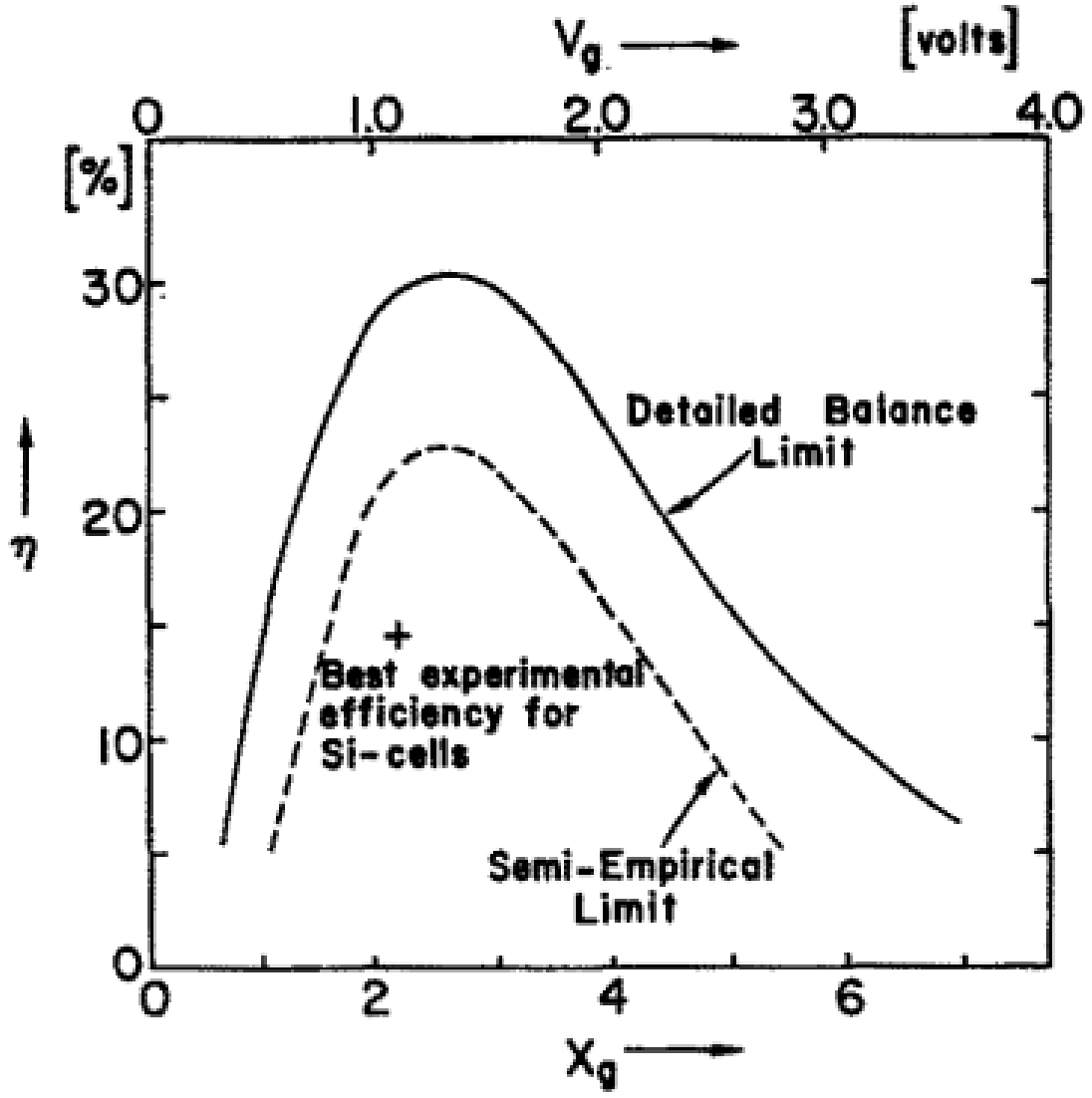


FIG. 1. Comparison of the "semiempirical limit" of efficiency of solar cells with the "detailed balance limit," derived in this paper. + represents the "best experiment efficiency to date" for silicon cells. (See footnote 6.)

The number of photons incident from the solar radiation in Fig. 2 is readily calculated in accordance with the formulas of the Planck distribution. We denote by Q_s the number of quanta of frequency greater than ν_g incident per unit area per unit time for blackbody radiation of temperature T_s. For later purposes we shall also introduce the symbol $Q(\nu_g,T_s)$ in order to be able to represent situations for different values of the limiting frequency. In accordance with this notation and well-known formulas, we have

$$Q_s \equiv Q(\nu_g,T_s) = (2\pi/c^2)\int_{\nu_g}^{\infty} [\exp(h\nu/kT_s)-1]^{-1}\nu^2 d\nu$$

$$= [2\pi(kT_s)^3/h^3c^2]\int_{x_g}^{\infty} x^2 dx/(e^x-1), \quad (2.2)$$

Each photon with energy greater than $h\nu_g$ produces one electronic charge q at a voltage of $V_g = h\nu_g/q$. (2.1)

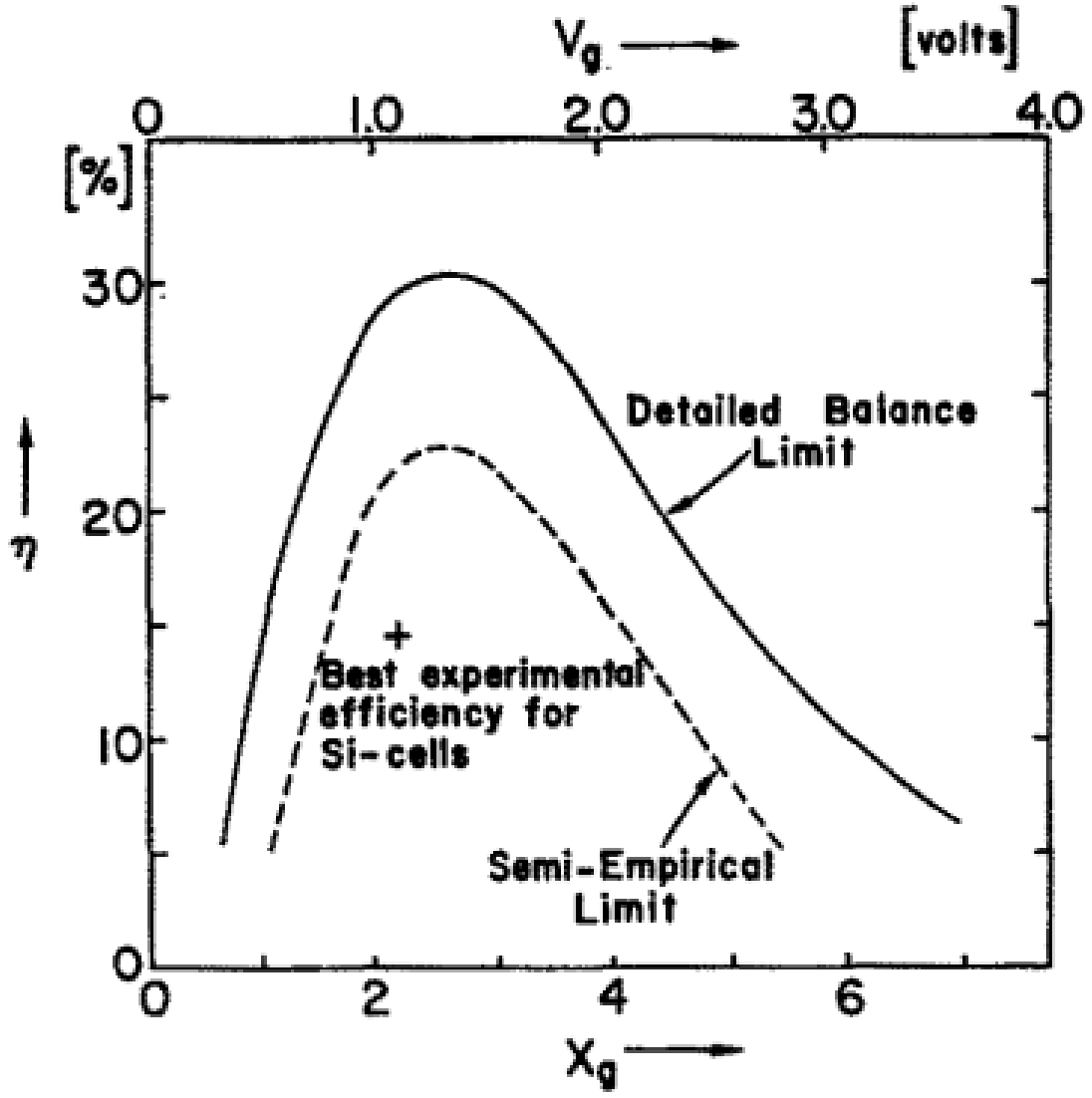


FIG. 1. Comparison of the "semiempirical limit" of efficiency of solar cells with the "detailed balance limit," derived in this paper. + represents the "best experiment efficiency to date" for silicon cells. (See footnote 6.)

P_s is the total energy density falling upon unit area in unit time for blackbody radiation at temperature T_s. In accordance with well-known formulas for the Planck distribution, P_s is given by

$$P_s = 2\pi h/c^2 \int_0^\infty \nu^3 d\nu/[\exp(h\nu/kT_s)-1]$$

$$= 2\pi (kT_s)^4/h^3c^2 \int_0^\infty x^3 dx/(e^x-1)$$

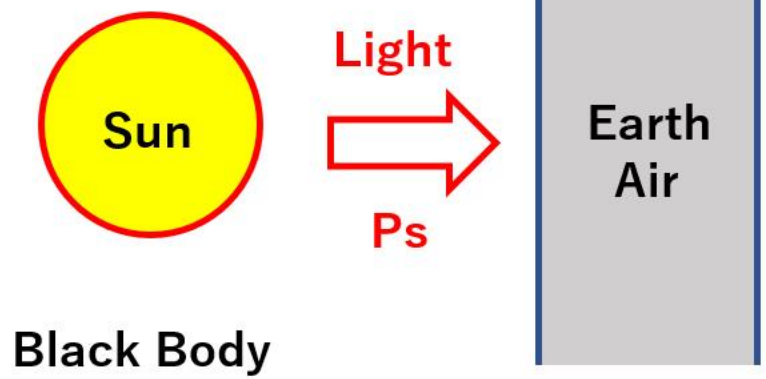
$$= 2\pi^5 (kT_s)^4/15h^3c^2. \qquad (2.6)$$

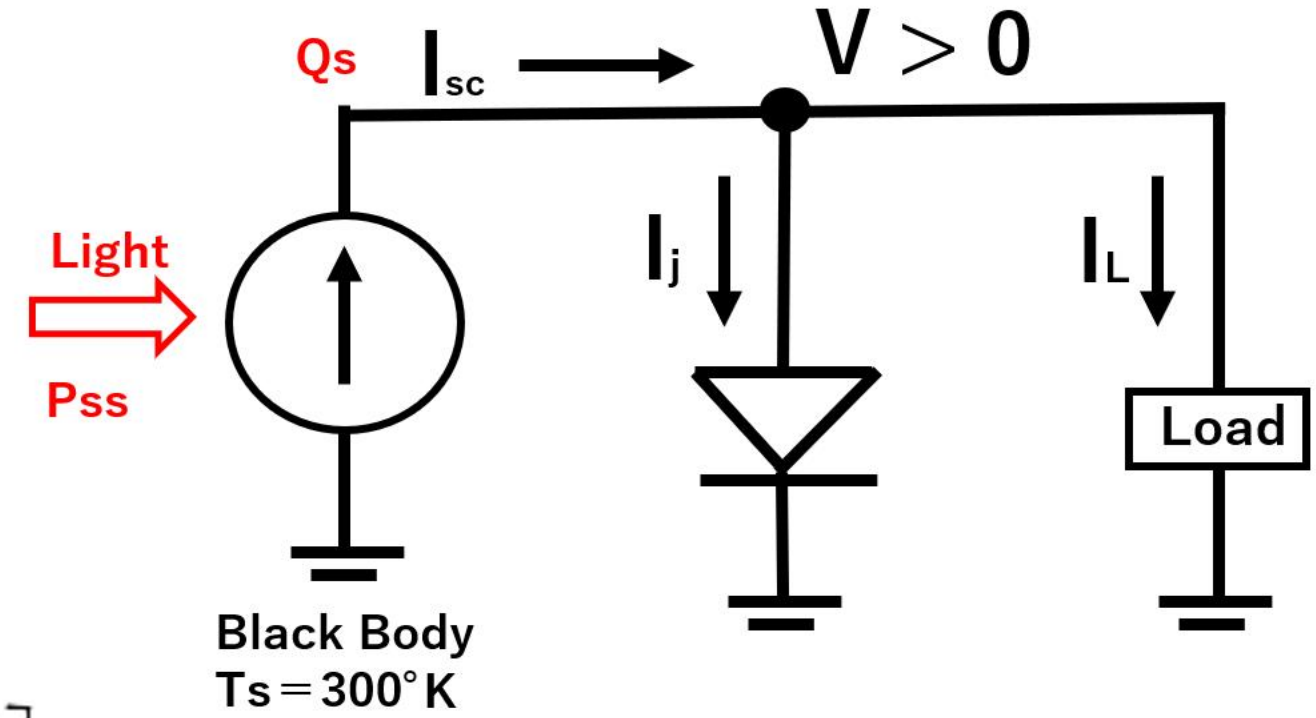
In accordance with the above definitions, the ultimate efficiency is a function only of x_g and is

$$u(x_g) = h\nu_g Q_s/P_s$$

$$= \left[x_g \int_{x_g}^\infty x^2 dx/(e^x-1)\right] \Big/ \int_0^\infty x^3 dx/(e^x-1). \quad (2.8)$$

Each photon with energy greater than $h\nu_g$ produces one electronic charge q at a voltage of $V_g = h\nu_g/q$. (2.1)



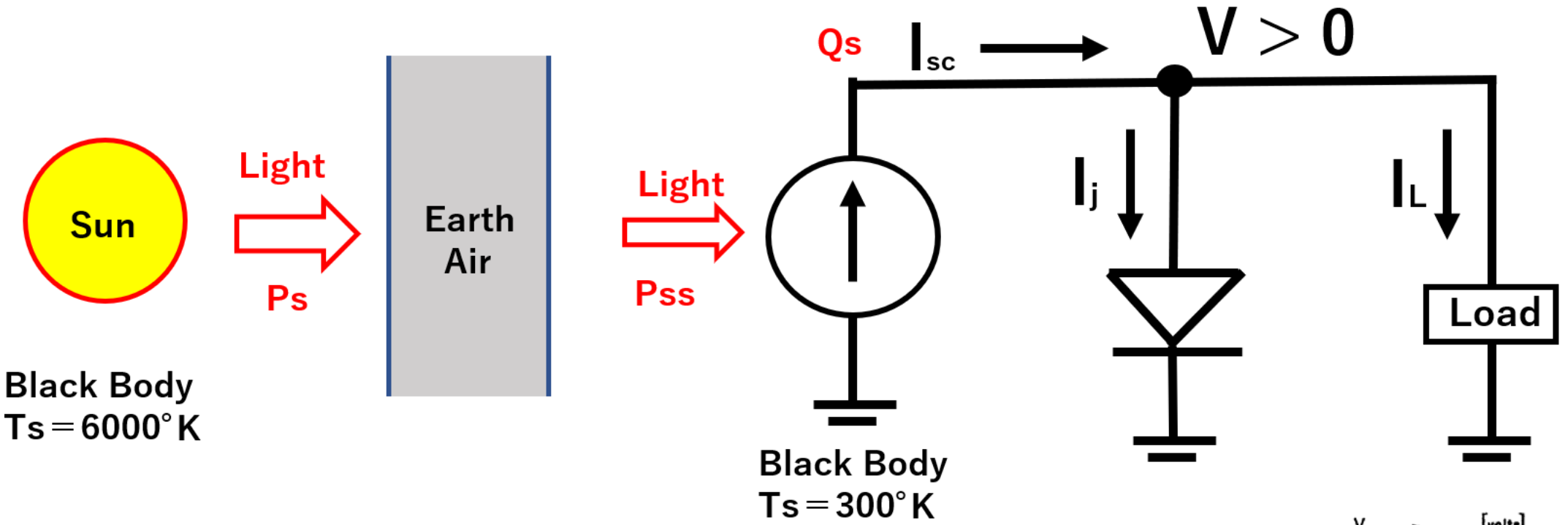


$$Ps = 2\pi h/c^2 \int_0^\infty \nu^3 d\nu / [\exp(h\nu/kT_s) - 1]$$

$$Qs = (2\pi/c^2) \int_{\nu_g}^\infty [\exp(h\nu/kT_s) - 1]^{-1} \nu^2 d\nu$$

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$$Ps = 2\pi h/c^2 \int_0^\infty \nu^3 d\nu/[\exp(h\nu/kT_s)-1]$$

$$Qs = (2\pi/c^2) \int_{\nu_g}^\infty [\exp(h\nu/kT_s)-1]^{-1}\nu^2 d\nu$$

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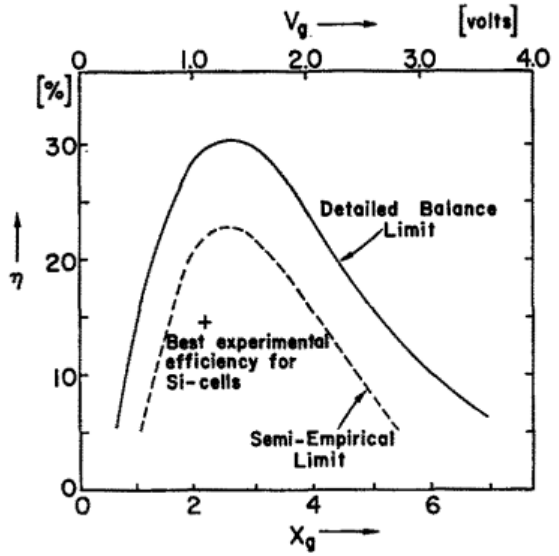


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Invention and Historical Development Efforts of Pinned Photodiode and Electric Shutter

2019 熊本テックの皆様



Hagiwara at Sony Kumamoto Tech Center
in 2017, 2019 and 2022.

2001



1. Introduction
2. Patent Wars on Pinned Photodiode
3. Double Junction type Solar Cell
4. Physics of Image Sensor and Solar Cell

1980



1996



Hagiwara also visited Sony Atsugi-Tech Center in July 2020.

Invention and Historical Development Efforts of Pinned Photodiode and Electric Shutter

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1980

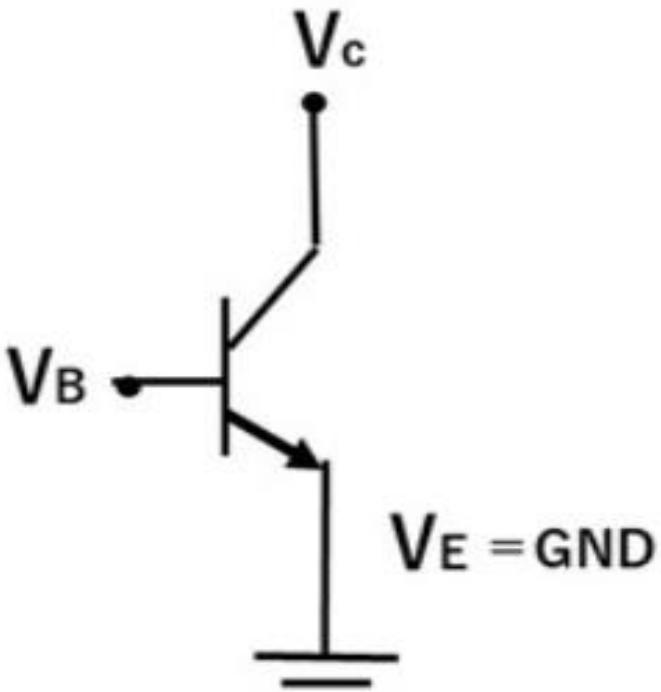


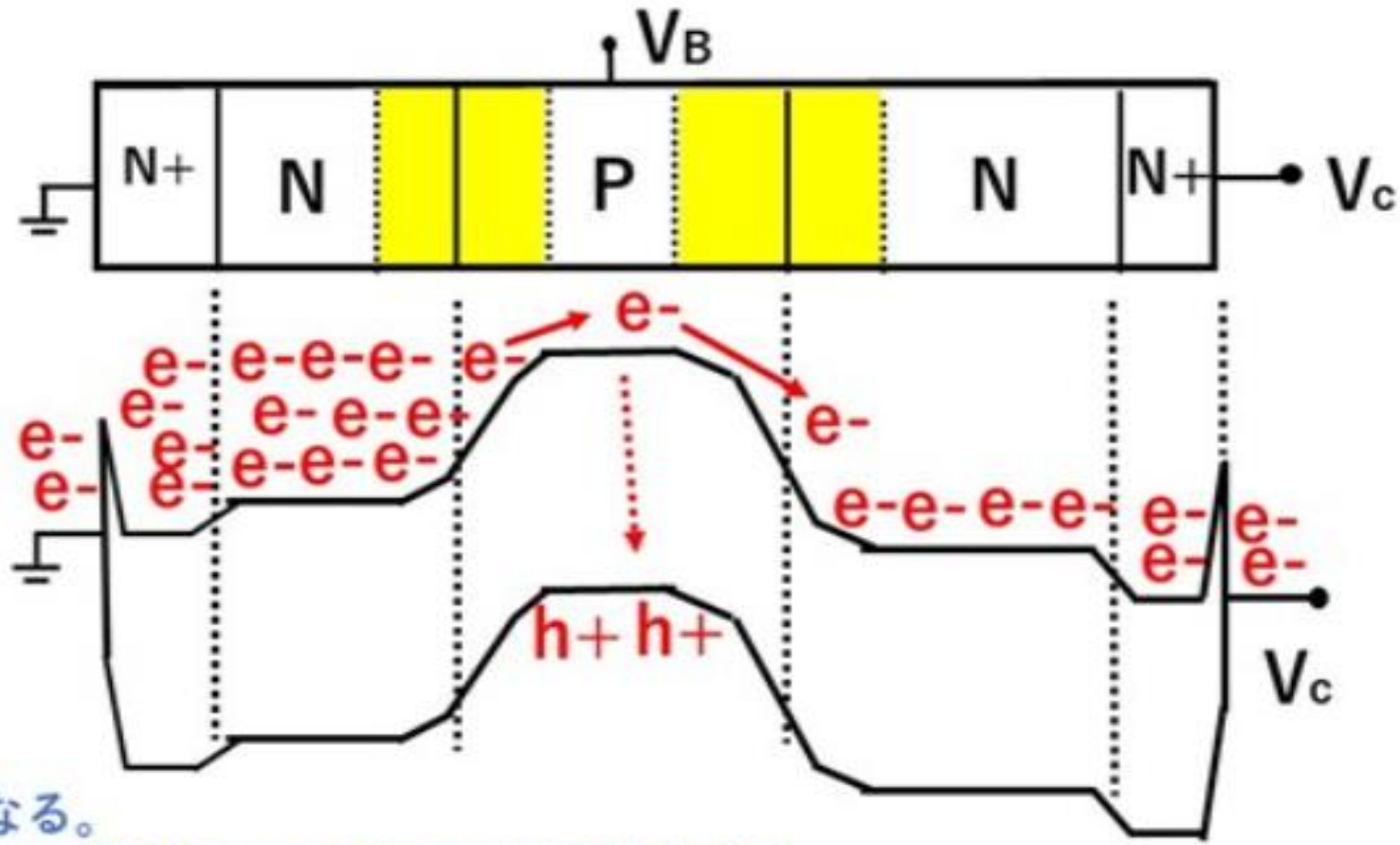
Hagiwara also visited Sony Atsugi-Tech Center in July 2020.

1996



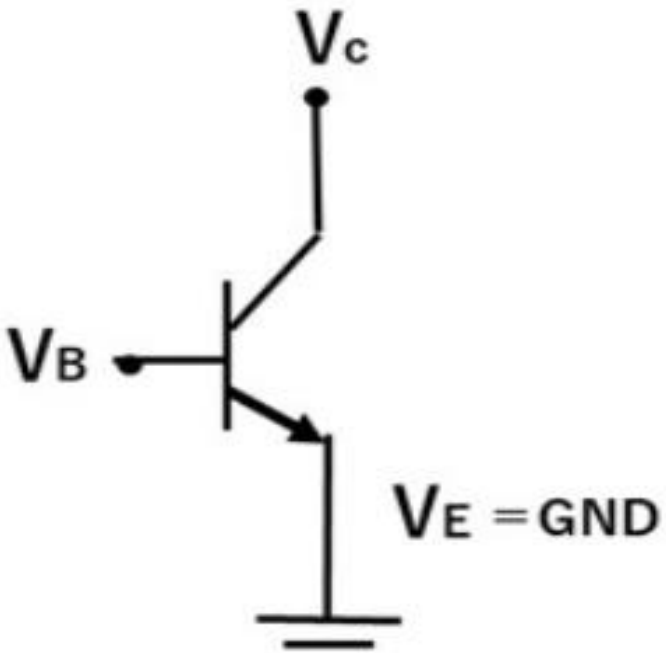
通常のNPN Bipolar Transistorの動作原理

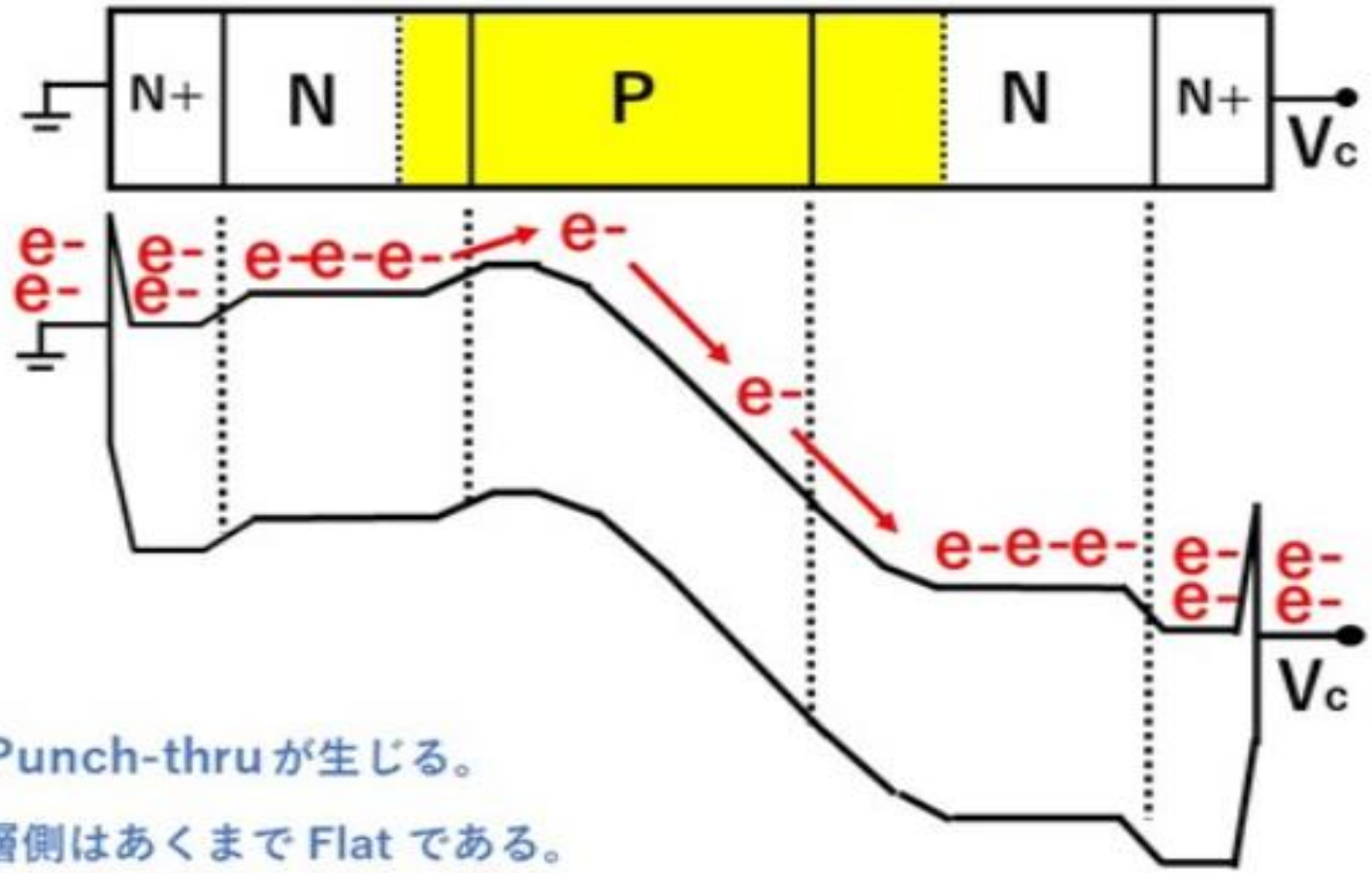




Emitter/Base間の接合が順方向になる。
電子の雲が丘（Base)を乗り越える。一部はBaseでホールと再結合する。
ほとんどの元気な電子は、隣接するCollector端子側の絶壁を電子が滝のように流れ落ちる。
太平洋に低気圧がある時に、山を乗り越えて、雪雲が日本海側（新潟）から関東平野に流れるこむ様子に似ている。

BaseのP層が完全空乏化し Punch-thru している Bipolar Transistor





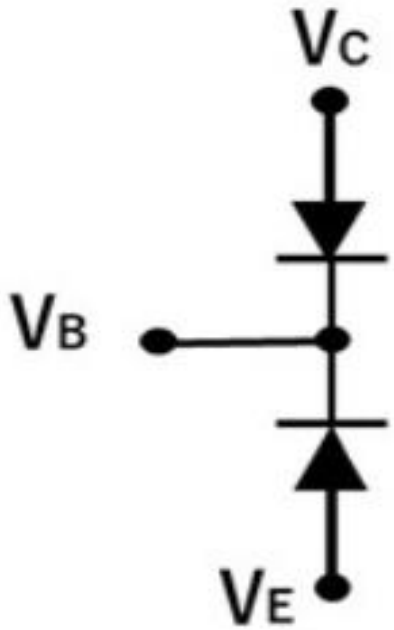
BaseのP層が完全空乏化すると、Punch-thruが生じる。

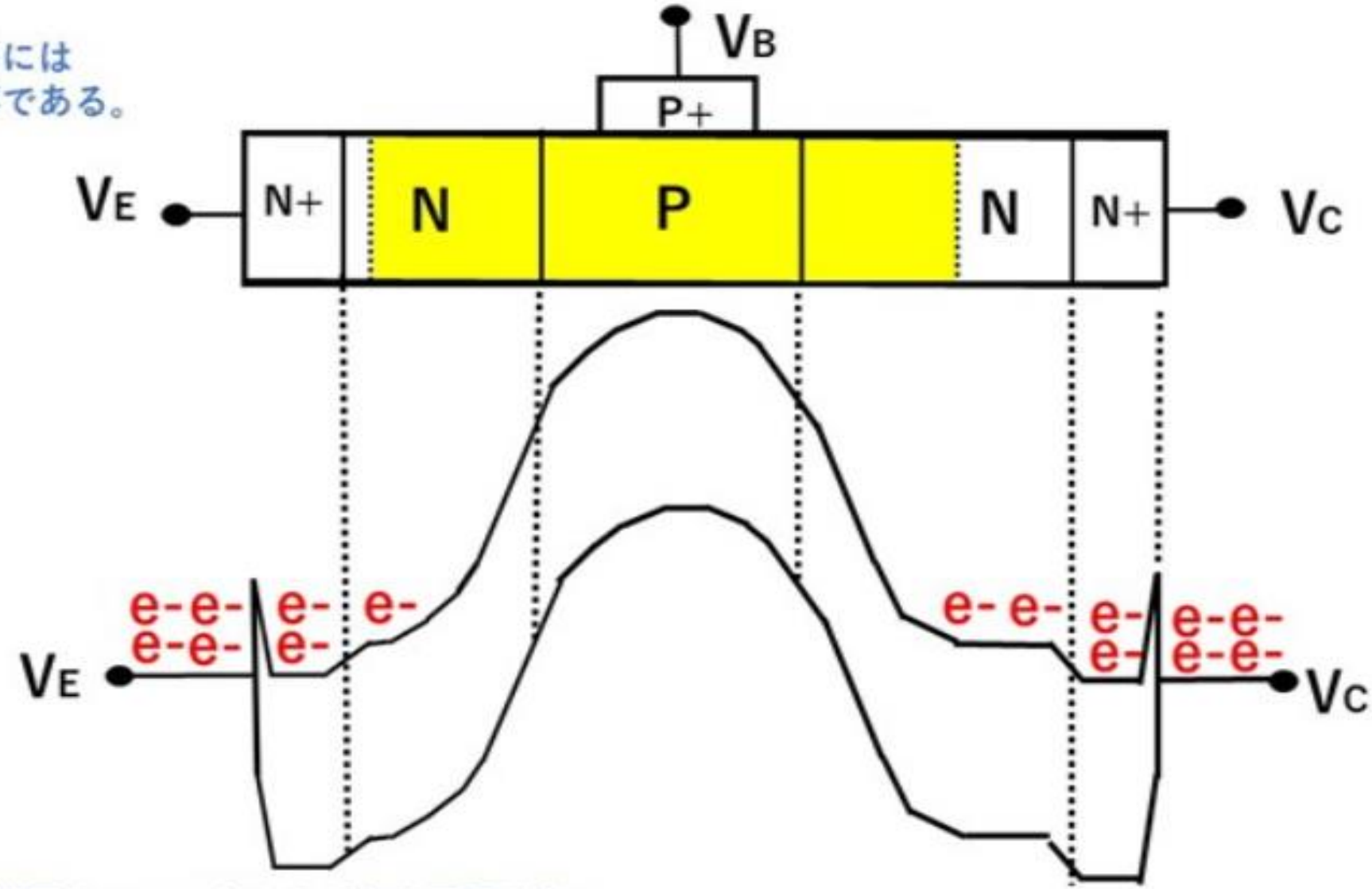
Barrier は下がるが、Emitter のN層側はあくまで Flat である。

Emitter のN層の表面には金属端子とのコンタクトがあり電界がない。
深い電圧が必要となり、通常の電圧では、Emitter のN層は完全空乏化できない。

両端ともに逆バイアスされた NPN Double 接合の電位 Profile

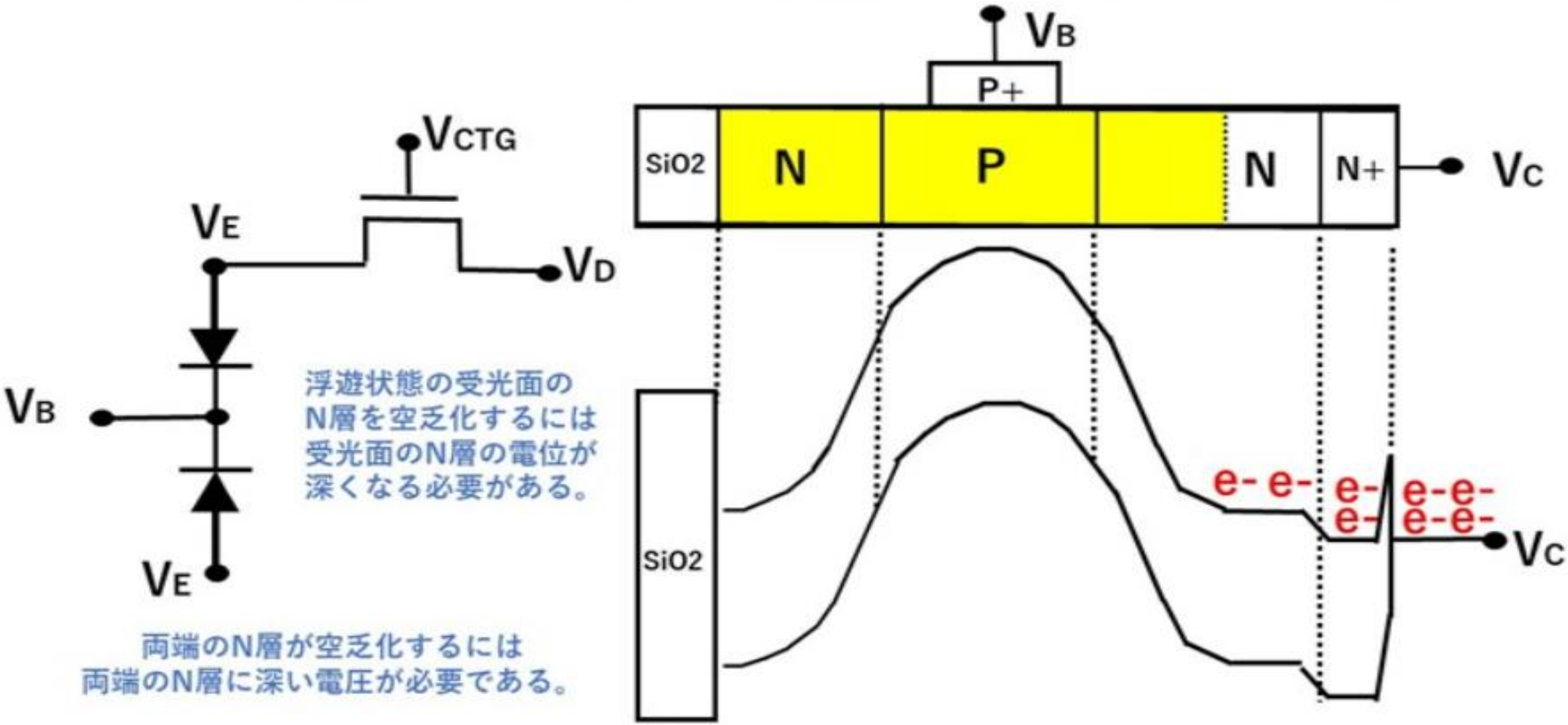
両端のN層が空乏化するには
両端のN層に深い電圧が必要である。





Emitter のN層の表面には金属端子とのコンタクトがあり電界がない。
深い電圧が必要となり、通常の電圧では、Emitter のN層は完全空乏化できない。

受光表面のN層が浮遊状態（Floating Surface）のありかつ完全空乏化している場合



浮遊状態の受光面の
N層を空乏化するには
受光面のN層の電位が
深くなる必要がある。

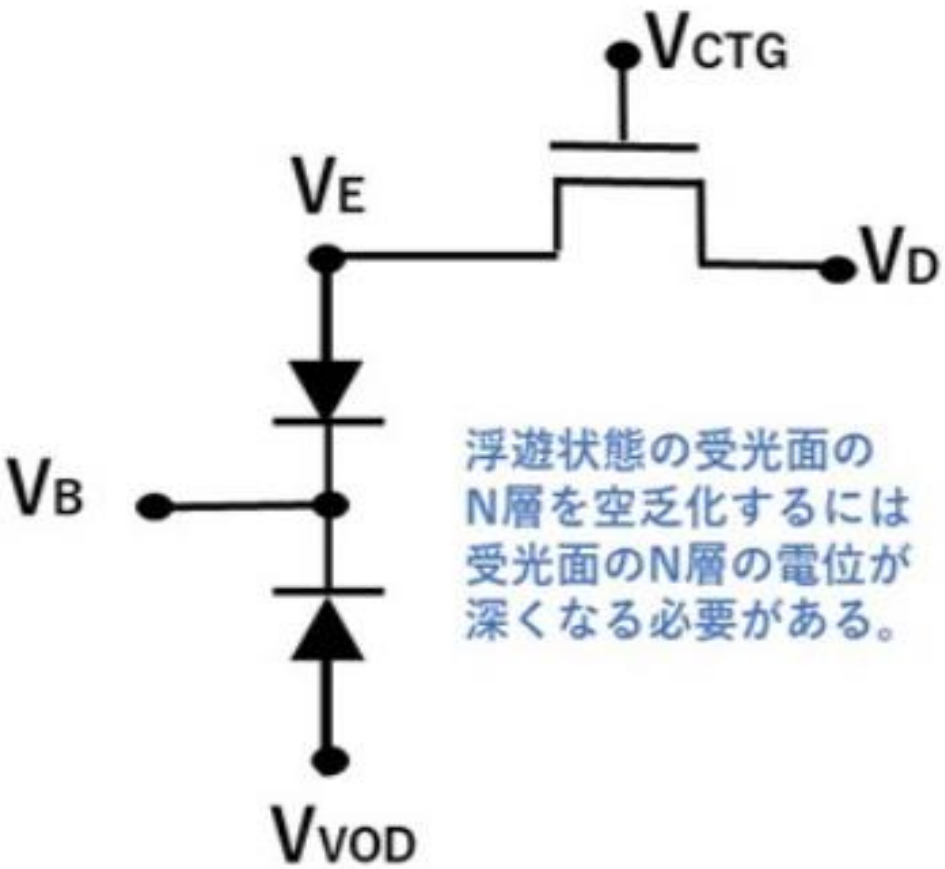
両端のN層が空乏化するには
両端のN層に深い電圧が必要である。

深い電圧が必要となり、通常の電圧では、Emitter のN層は完全空乏化できない。

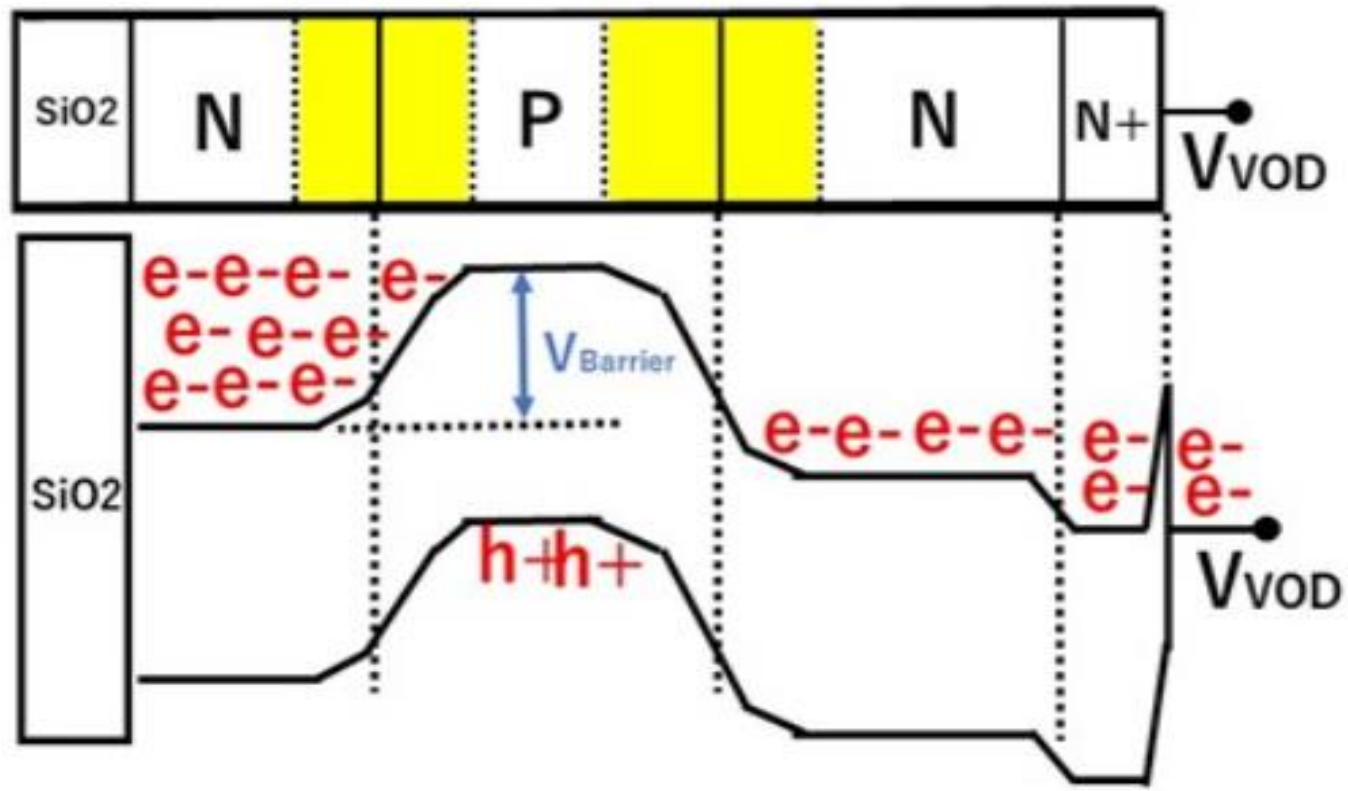
表面が浮状態（Floating Surface）の NPNN+ Double 接合型受光素子

（東芝1977）JPA1978-1971 特許 on Vertical Overflow Drain (VOD)

VOD として機能するが電子シャッター機能はない。



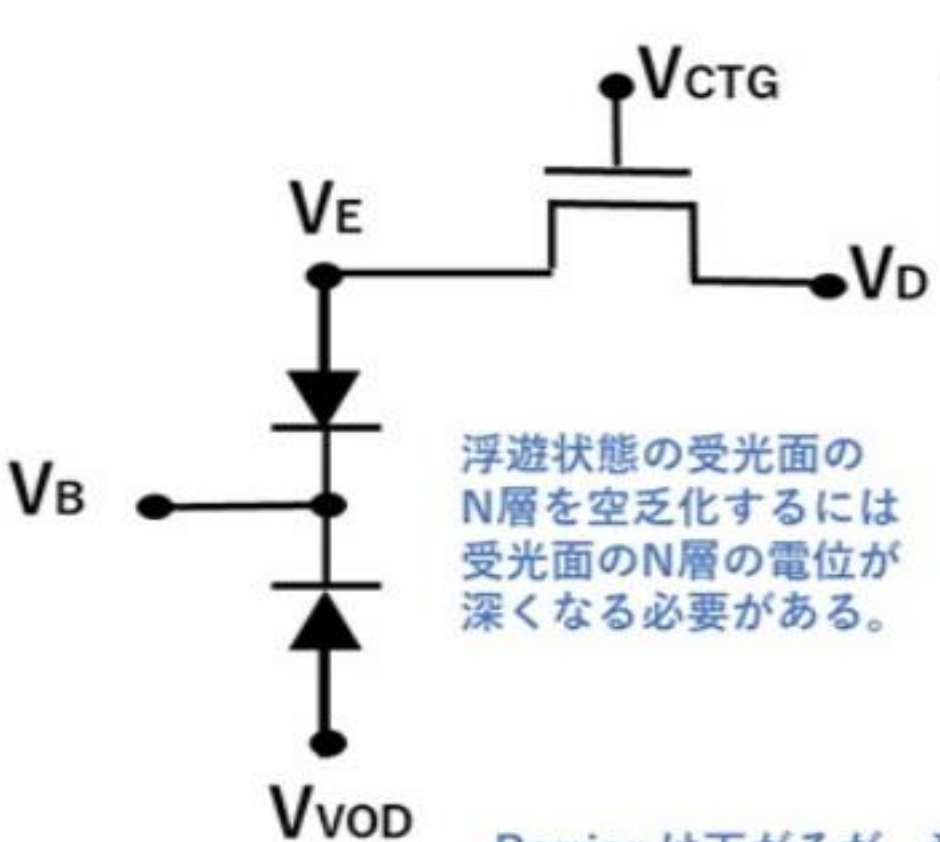
浮遊状態の受光面の
N層を空乏化するには
受光面のN層の電位が
深くなる必要がある。



表面が浮状態（Floating Surface）の NPNN+ Double 接合型受光素子

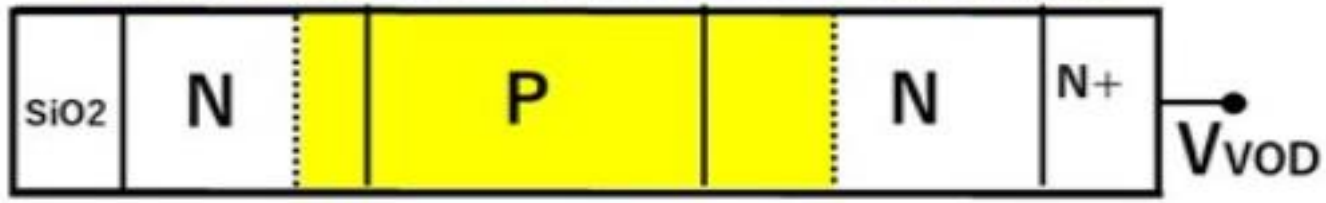
（東芝1977）JPA1978-1971 特許 on Vertical Overflow Drain (VOD)

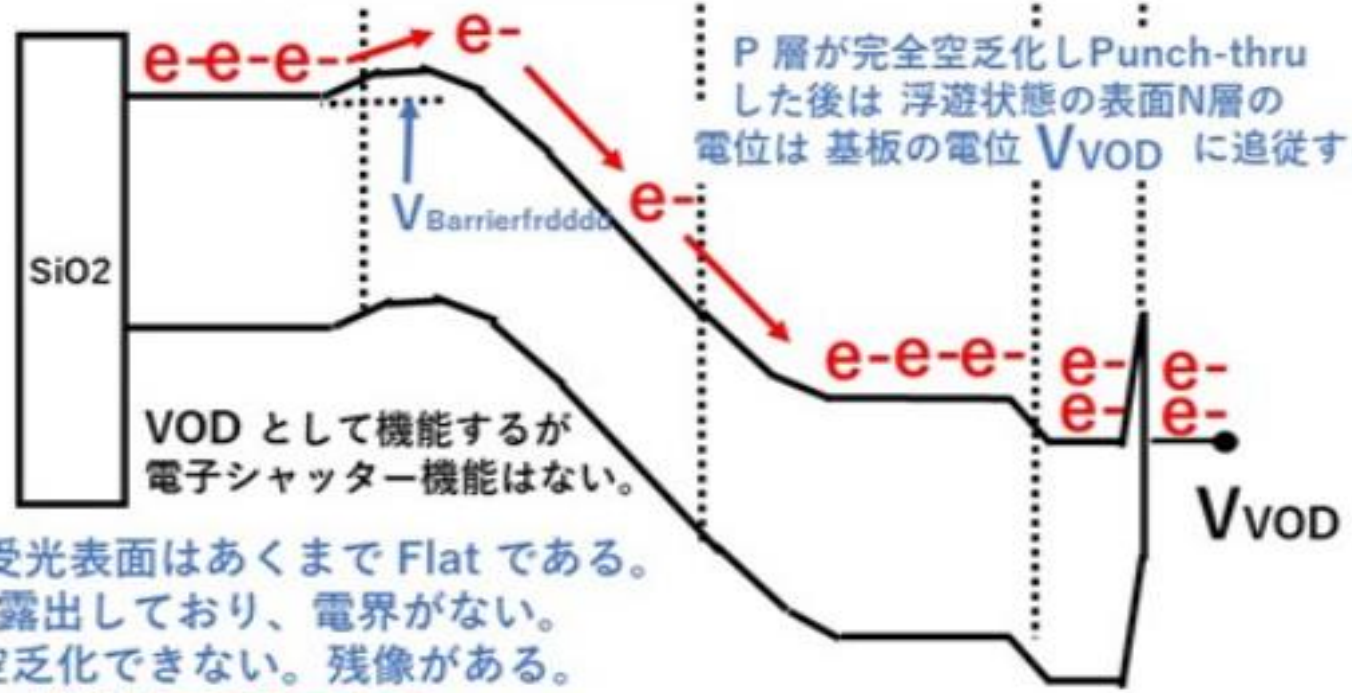
VOD として機能するが電子シャッター機能はない。



浮遊状態の受光面の
N層を空乏化するには
受光面のN層の電位が
深くなる必要がある。

BaseのP層が完全空乏化し Punch-thru した後





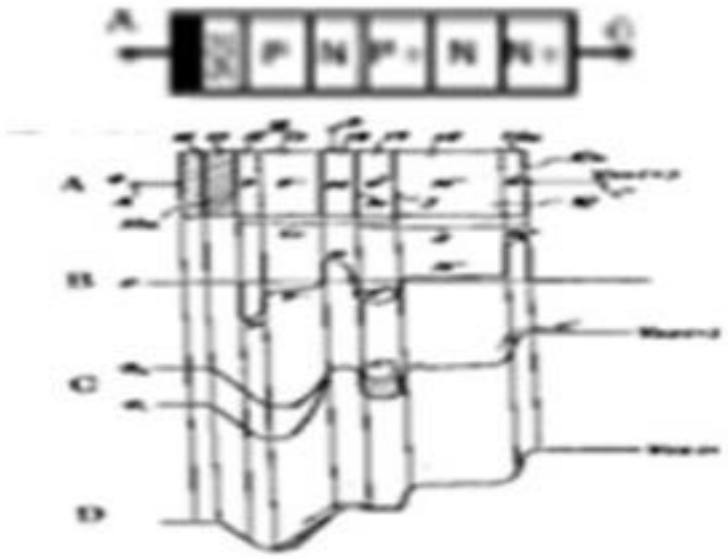
P 層が完全空乏化しPunch-thru
した後は 浮遊状態の表面N層の
電位は 基板の電位 VVOD に追従する。

VOD として機能するが
電子シャッター機能はない。

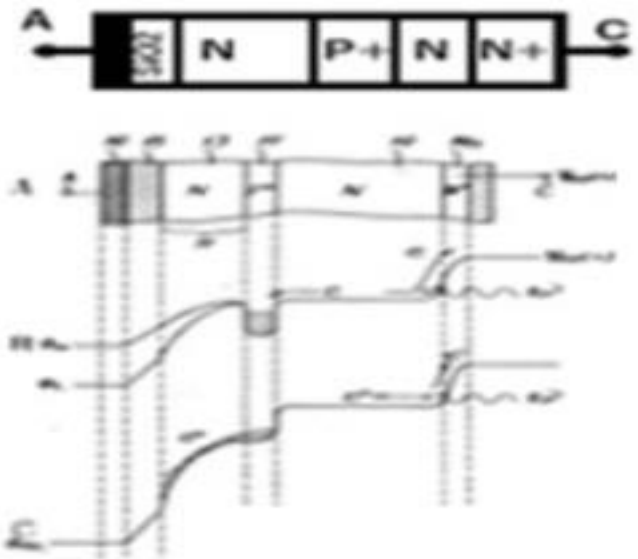
Barrier は下がるが、受光表面はあくまで Flat である。
受光表面はSiO2に露出しており、電界がない。
表面受光層(N)は完全空乏化できない。残像がある。
電子シャッター機能は不可能である。

Who invented Pinned Photodiode ?

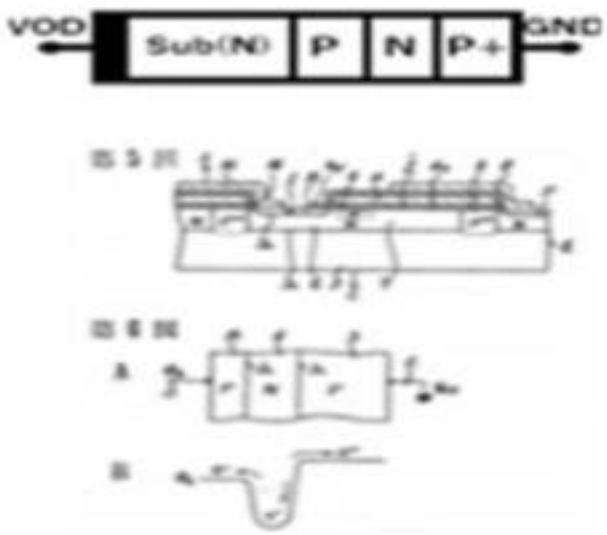
Hagiwara at Sony invented Pinned Photodiode in 1975. The evidence is give by the three Japanese patent applications, JPA1975-127646, JPA1975-127647 and JPA1975-134985. The first Pinned Photodiode was defined in October 23, 1975 as the N+NPNP triple junction(in Fig. 7 of JAP1975-127646) type and the N+NPN double junction type (in Fig. 7 of JAP1975-127647) type photodiodes with the N+ type pinned surface and the P type buried photo charge storage region with the complete charge transfer capability and the no-image-lag feature. The photo charge is transferred and drained to the CCD/MOS type charge storage buffer memory quicky by the strong punch-thru action. The second Pinned Photodiode was defined in November 10, 1975 as the PNP double junction (in Fig. 6 of JAP1975-134985) type photodiode with the vertical overflow drain action also with the complete charge transfer capability and the no-image-lag feature as evidence the empty potential well of the buried photo charge storage, completely depleted of the charge.



JPA1975-127646 Fig. 7



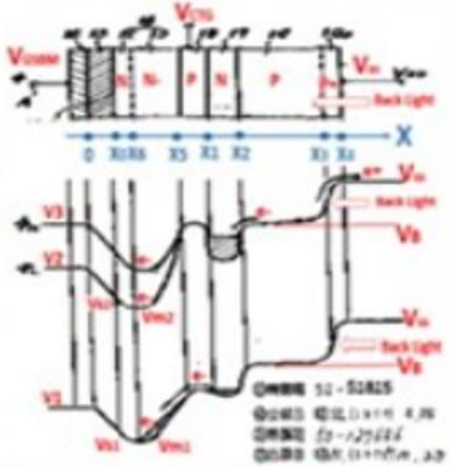
JPA1975-127647 Fig. 7

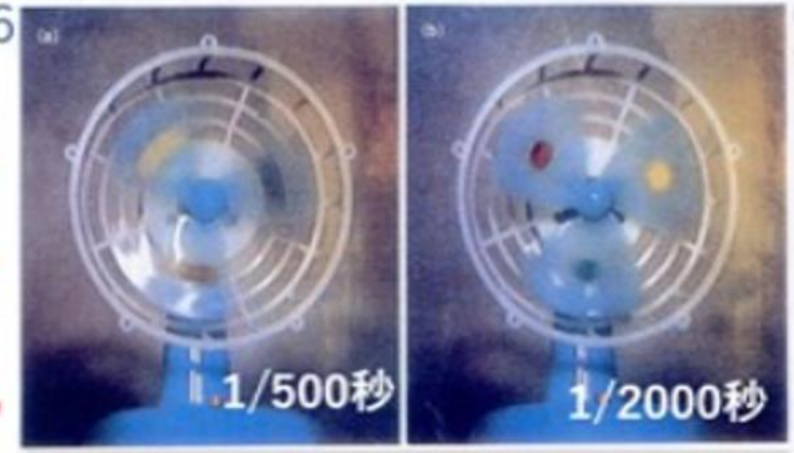


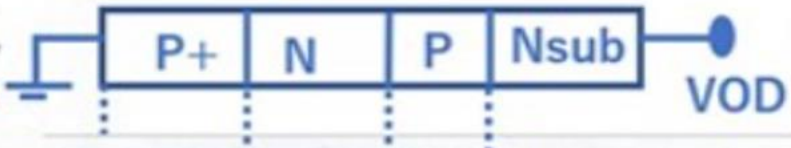
JPA1975-134985 Fig. 6

NIKKEI MICRODEVICES 1987年10月号
pp.60～67

JPA1975-127646







JPA1975-127646の図7と同一受光構造である。受光表面はGNDにピン留めされた、P+NPNsub 接合型、すなわちTriple 接合型の Pinned Photodiode.

38万画素に達した固体撮像素子

最低照度51xの高感度インターライン型CCD

基板に余剰電荷を掃き出し,可変電子シャッタを実現

ソニー 半導体事業本部 CCD 事業部
浜崎 正治
鈴木 智行
賀川 能明
石川 貴久枝
宮田 克郎
ソニー国分セミコンダクタ CCD 製造部
神戸 秀夫

最も一般的な固体撮像素子であるインターライン型 CCD で,
2/3 インチで 38 万と大規模な画素数を持つ素子をソニーが製品化した。
画素面積が小さくなることで減少する信号量を確保するため,
縦型オーバーフロー・ドレインを採用して開口率を上げ,
補色フィルタで光の利用効率を上げた。
さらに界面準位からの暗電流を抑えている。
この結果,81 dB のダイナミック・レンジが得られた。



図4 電子shutterの動作原理の説明図

SONYの1987年発表の電子シャッター機能付き
Hole Accumulation Diode (HAD) 受光素子構造

P+PN-PP+接合型太陽電池の提案

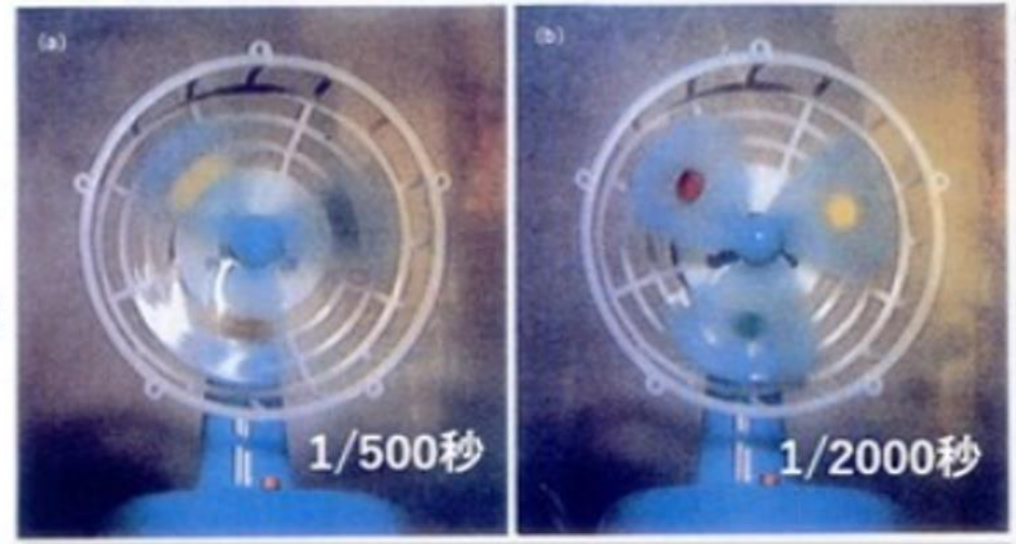
萩原良昭(AIPS)

題目：　人工知能ロボットを支える、超光感度の賢い電子の目を太陽電池に応用する

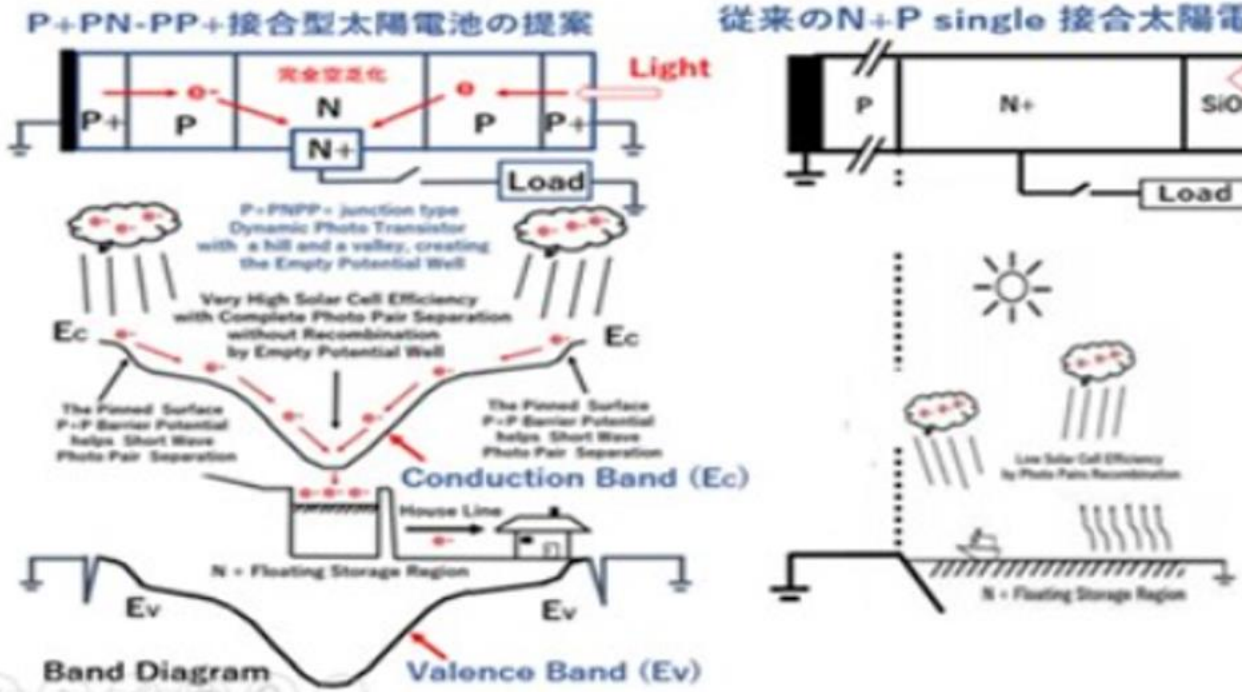
概要

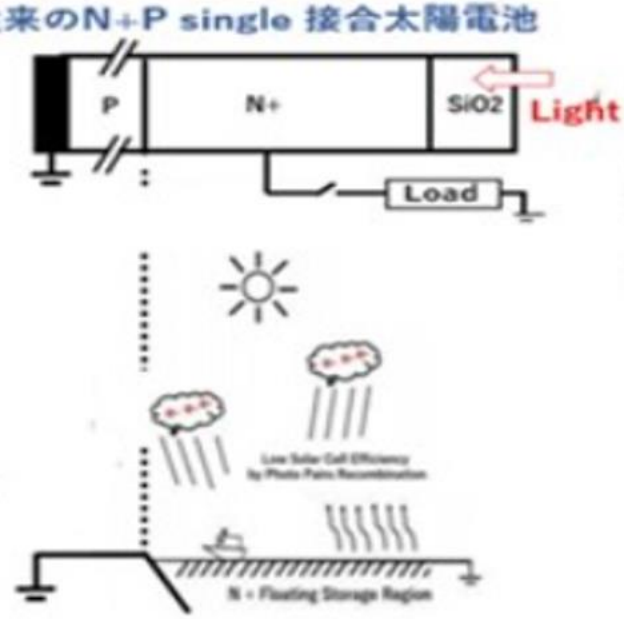
1975年に萩原良昭が発明(JPA1975-127646,JPA1975-127647,JPA1975-134985)

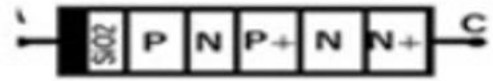
考案した超光感度のイメージセンサーの受光素子構造は、Double 接合型の受光素子である。通称、Pinned Photodiodeと呼ばれる受光素子である。短波長青色光に対する感度特性が優れている事が知られているが、その受光素子構造を太陽電池の光電変換効率向上のために採用することを提案する。

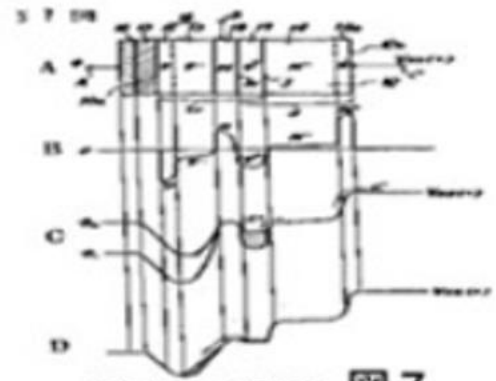


電子シャッター機能付きビデオカメラ　Sony 1987

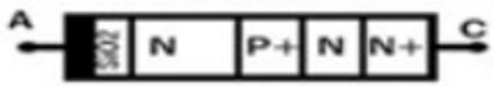


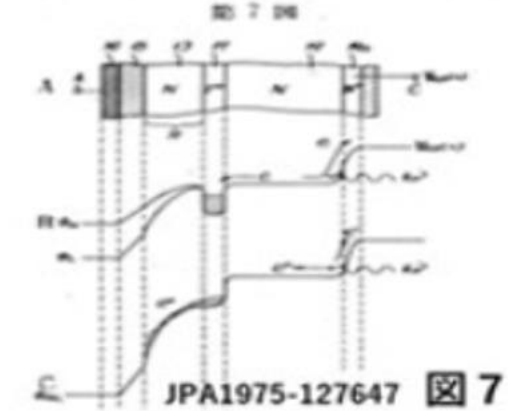






JPA1975-127646 図 7





JPA1975-127647 図 7

太陽電池の変換効率の限界

変換効率は、使用される半導体材料が吸収できる太陽光の波長領域と、PN接合の空乏層領域での吸収量で求まります。シリコン結晶では、波長が 0.29μmから 1.20μm までの太陽光を吸収できます。Single PN 接合型での変換効率の限界理論値は 28% です。実際には20%程度です。その理由は(1)受光面での反射や(2)受光表面再結合や(3)PN接合の空乏層内での結晶欠陥による再結合や(4)裏面再結合などが生じ、光電変換された光電子とホールのペアが再結合し無駄になる為です。

Silicon のBand Gap は　1.1 eV

InP のBand Gap は　1.34 eV

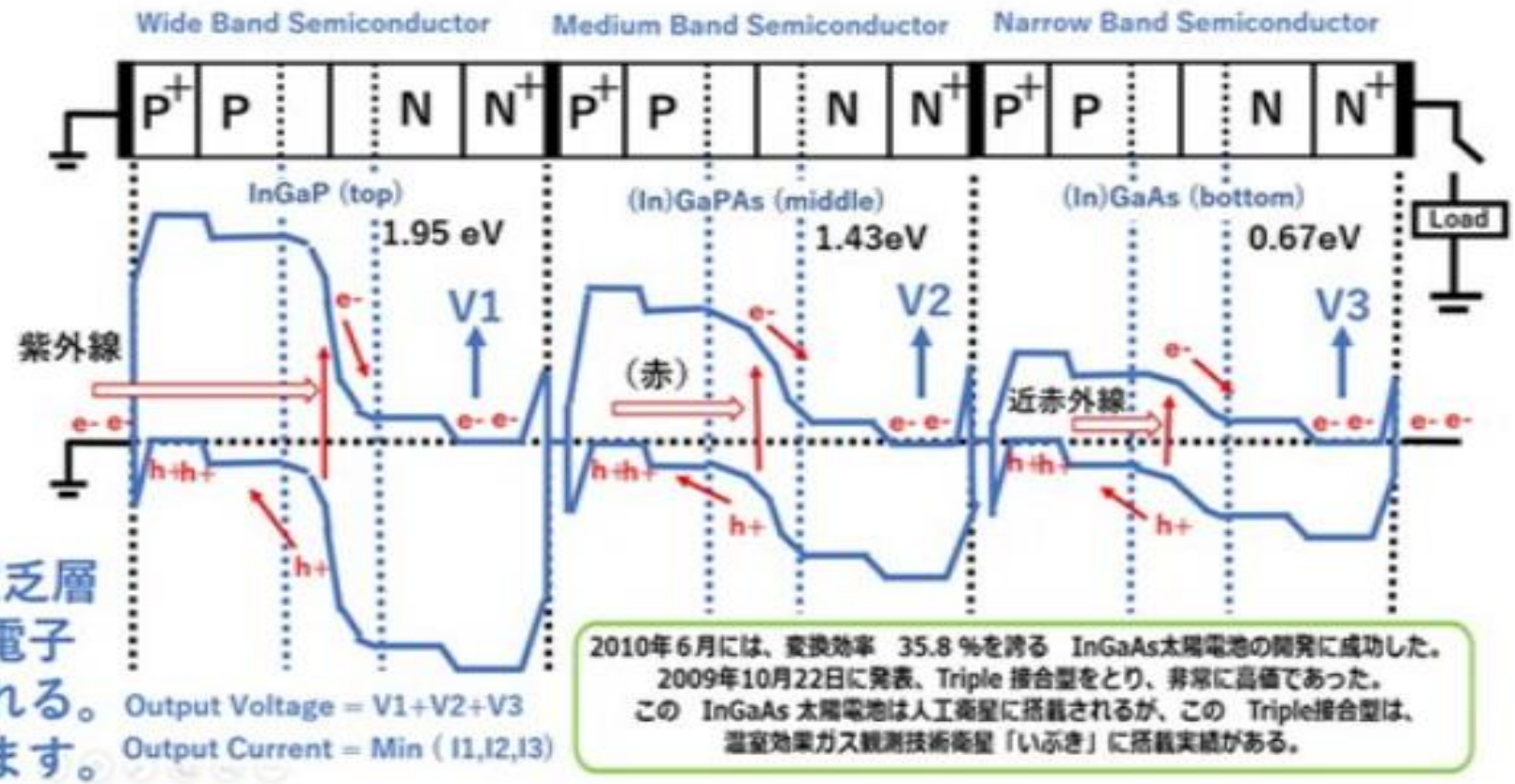
GaAs のBand Gap は　1.42 eV

CdTe のBand Gap は　1.48 eV

GaN のBand Gap は　3.4 eV

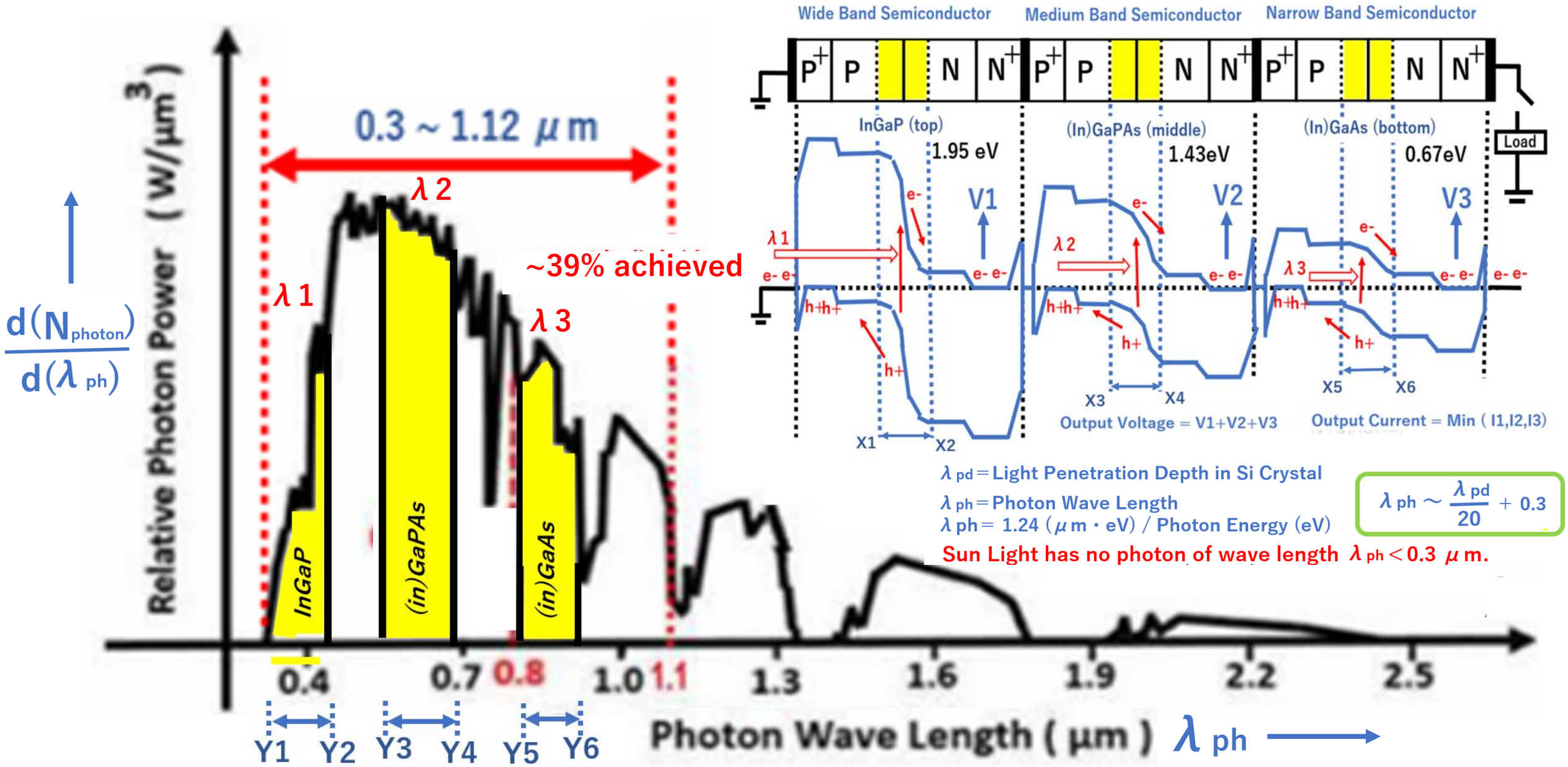
β-Ga_2O_3 のBand Gap は 4.5 eV

バリア電界が存在するPN接合の空乏層領域内でのみ、光電変換による光電子とホールのペアは効率良く分離される。と言う事が、今の常識となっています。



2010年6月には、変換効率　35.8 %を誇る　InGaAs太陽電池の開発に成功した。
2009年10月22日に発表、Triple 接合型をとり、非常に高価であった。
この　InGaAs 太陽電池は人工衛星に搭載されるが、この　Triple接合型は、
温室効果ガス観測技術衛星「いぶき」に搭載実績がある。

Triple Junction Solar Cell with Wide Band Gap Compound Semiconductors achieved ~39% Quantum Efficiency



λ pd = Light Penetration Depth in Si Crystal

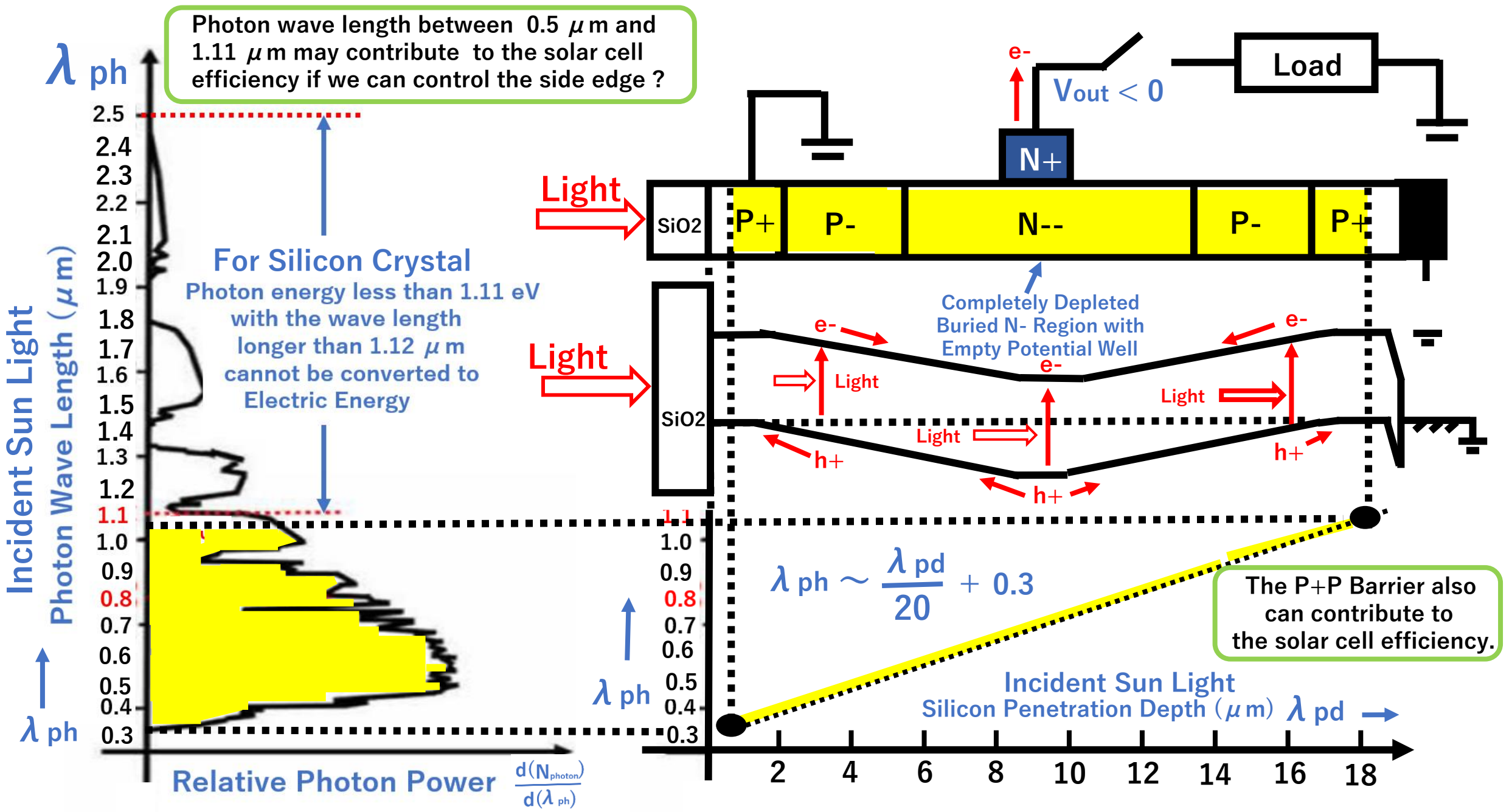
λ ph = Photon Wave Length

λ ph = 1.24 (μm・eV) / Photon Energy (eV)

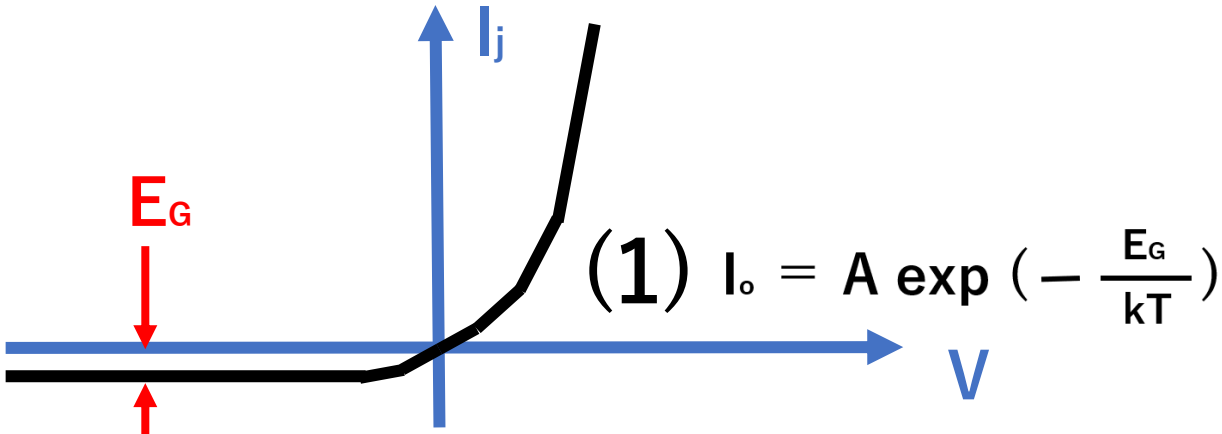
$$\lambda_{ph} \sim \frac{\lambda_{pd}}{20} + 0.3$$

Sun Light has no photon of wave length $\lambda_{ph} < 0.3\ \mu m$.

The P+P-N-P-P+ double junction type Solar Cell may have much higher efficiency



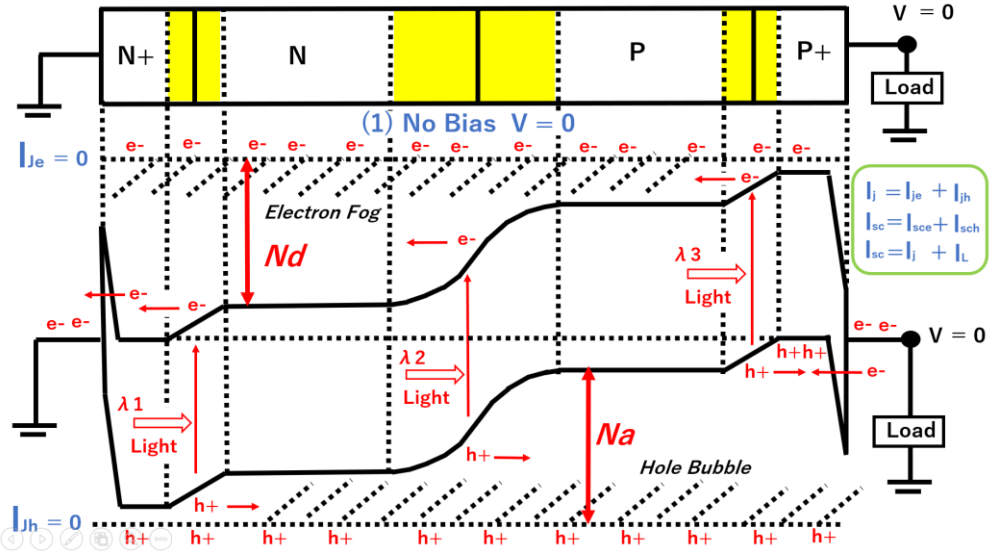
P+PNN+接合Diodeの電流(Ij)電圧(V)特性

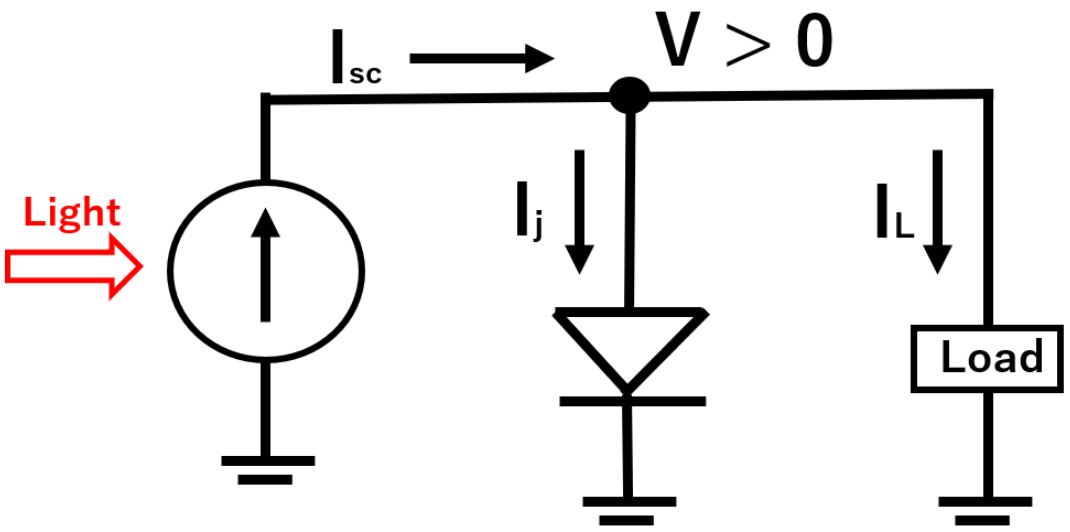


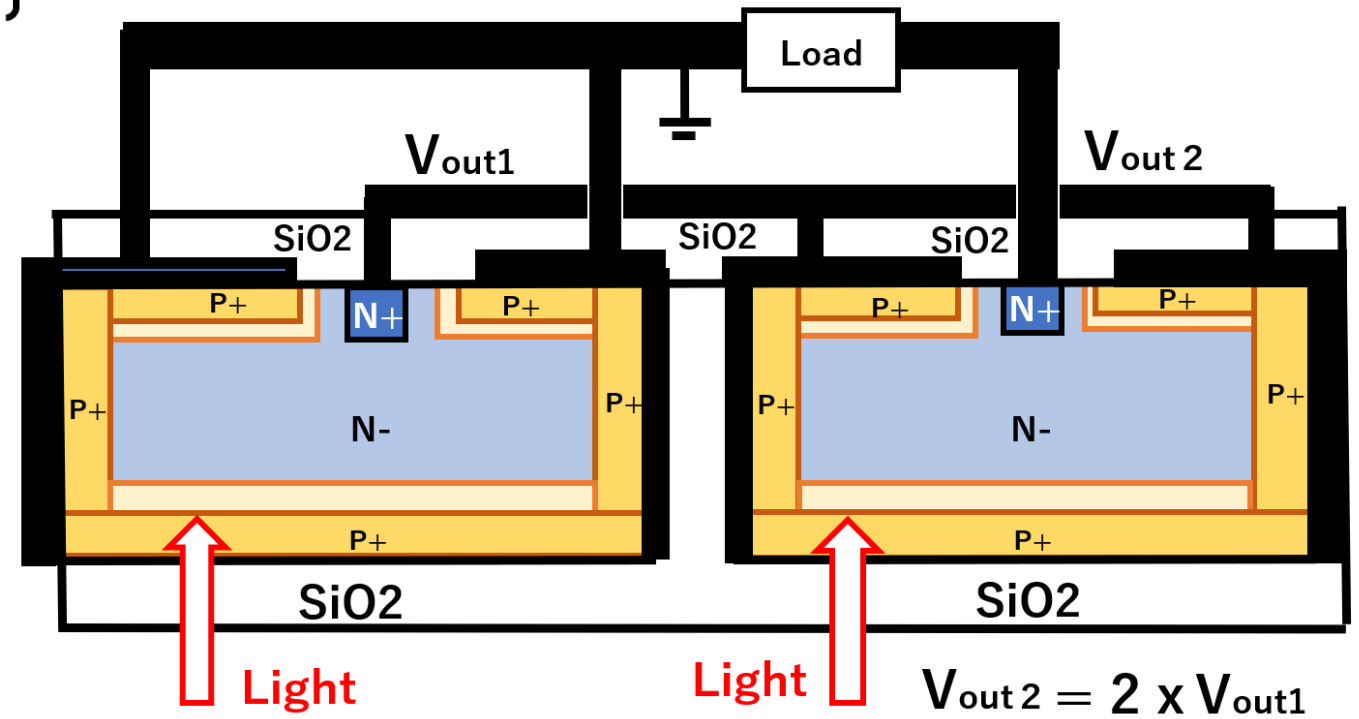
$$(1)\ I_o = A \exp\left(-\frac{E_G}{kT}\right)$$

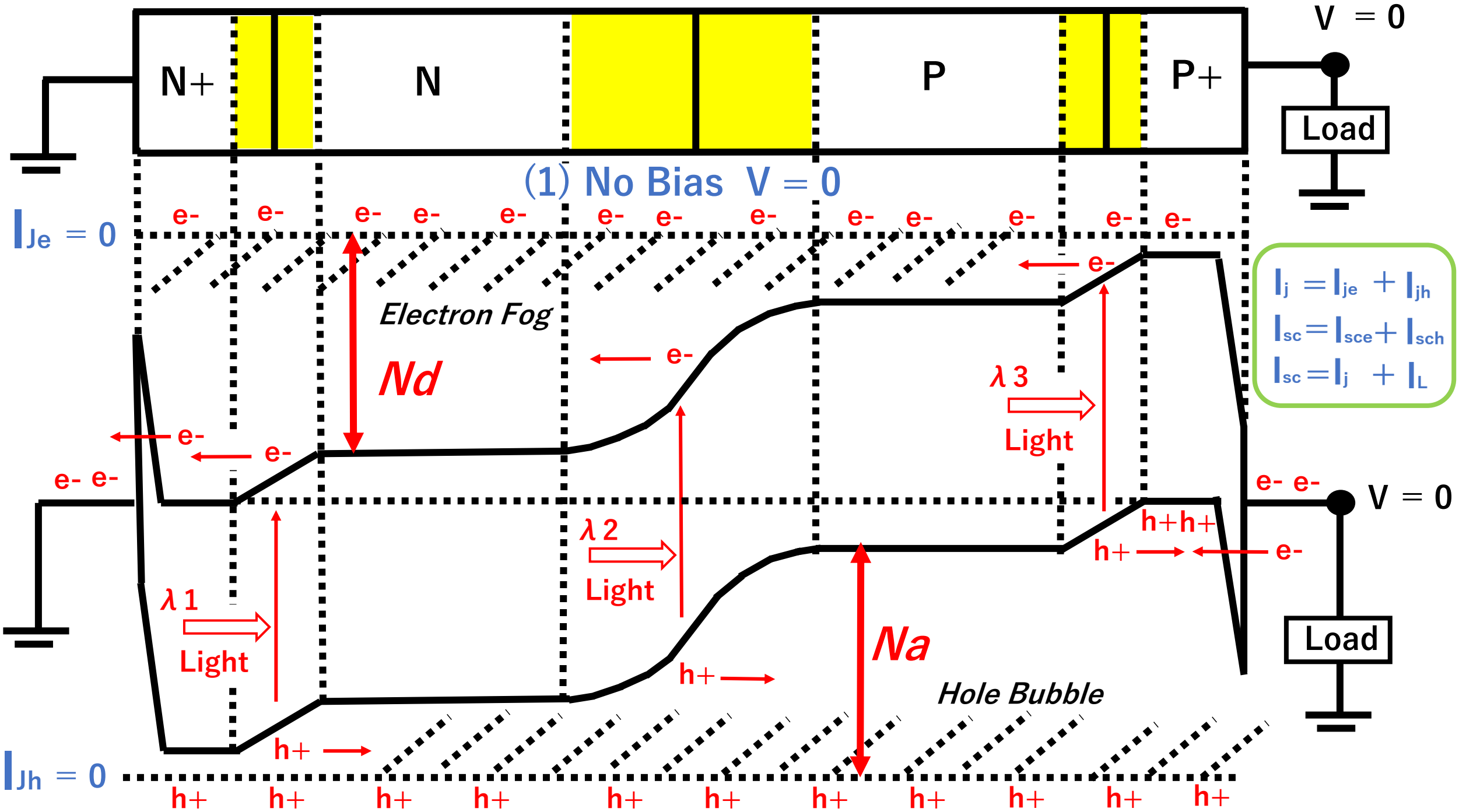
$$(2)\ I_j = (I_o)\left\{\exp\left(\frac{V}{kT}\right) - 1\right\}$$

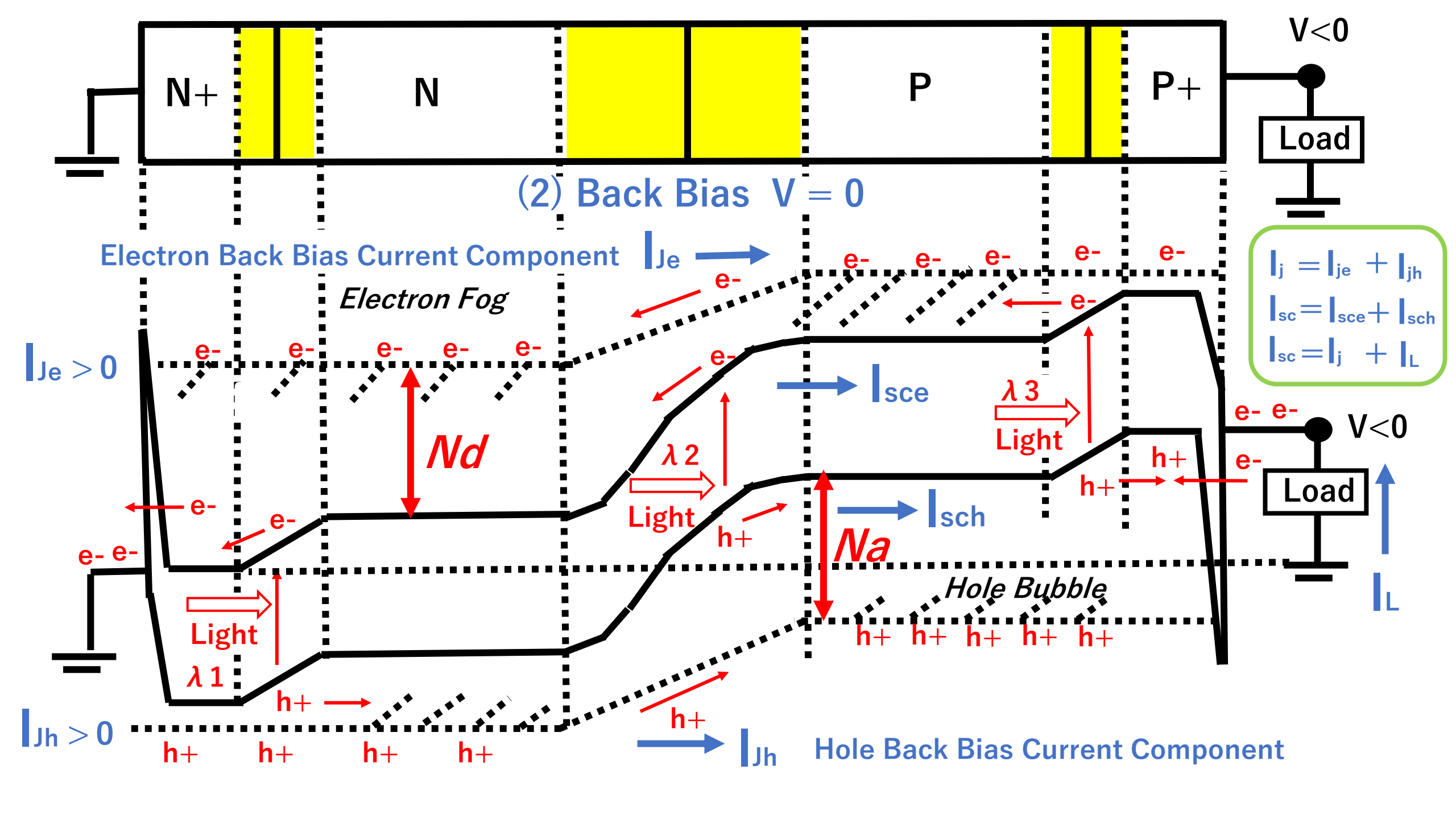
(1) No Bias V = 0

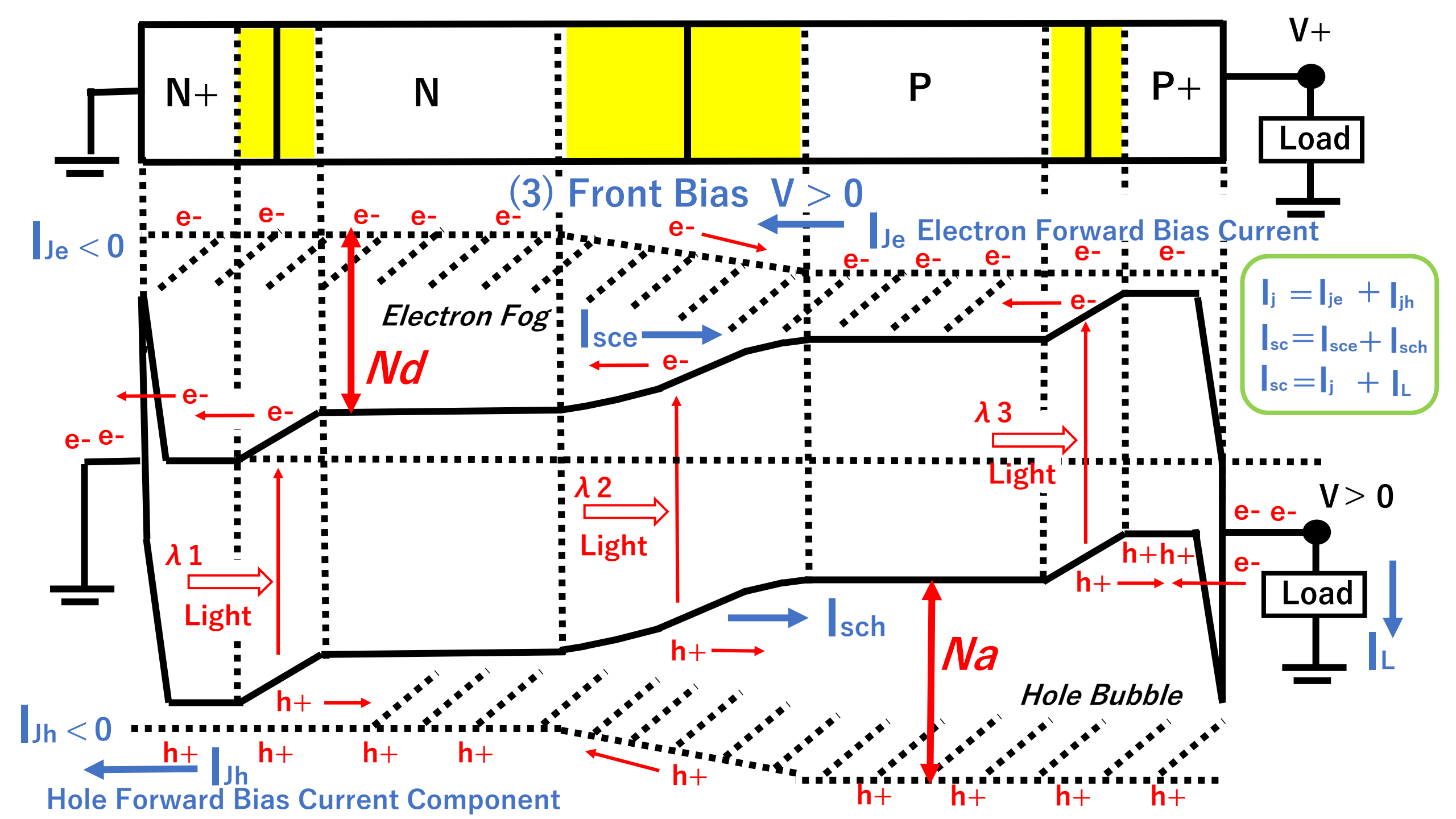




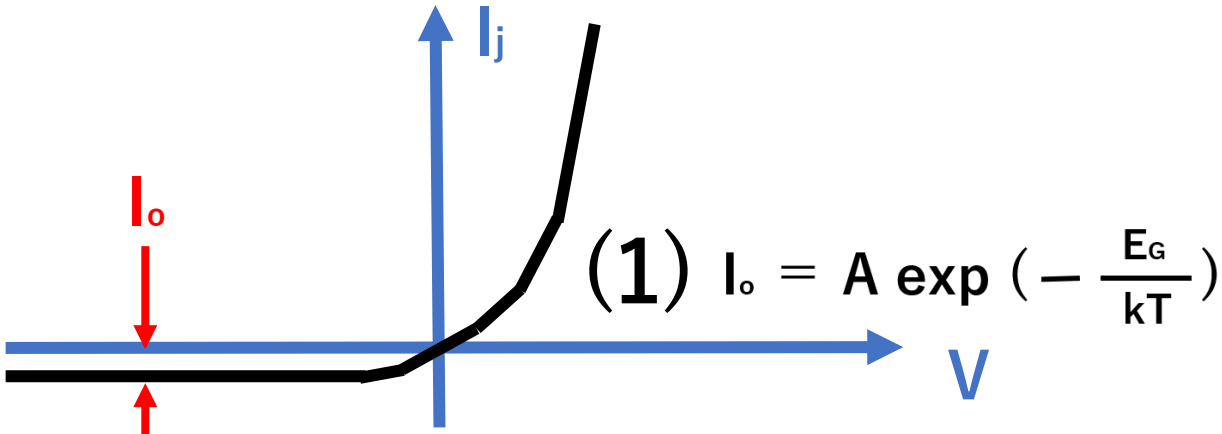



N+
N
P
P+
V = 0
Load
(1) No Bias V = 0
$I_{Je} = 0$
e-
Electron Fog
Nd
$I_j = I_{je} + I_{jh}$
$I_{sc} = I_{sce} + I_{sch}$
$I_{sc} = I_j + I_L$
λ 3
Light
λ 2
Light
λ 1
Light
h+
Na
Hole Bubble
V = 0
Load
$I_{Jh} = 0$


N+
N
P
P+
V<0
Load
(2) Back Bias V = 0
Electron Back Bias Current Component
Ije
Electron Fog
Ije > 0
e-
Nd
λ 1
Light
h+
Ijh > 0
Ijh
Hole Back Bias Current Component
λ 2
Light
Isce
λ 3
Light
Isch
Na
Hole Bubble
V<0
Load
IL
Ij = Ije + Ijh
Isc = Isce + Isch
Isc = Ij + IL


N+
N
P
P+
V+
Load
(3) Front Bias V > 0
IJe Electron Forward Bias Current
IJe < 0
e-
Electron Fog
Nd
Isce
λ 3
Light
λ 2
Light
λ 1
Light
Isch
Na
Hole Bubble
V > 0
Load
IL
h+
IJh < 0
IJh
Hole Forward Bias Current Component
Ij = Ije + Ijh
Isc = Isce + Isch
Isc = Ij + IL

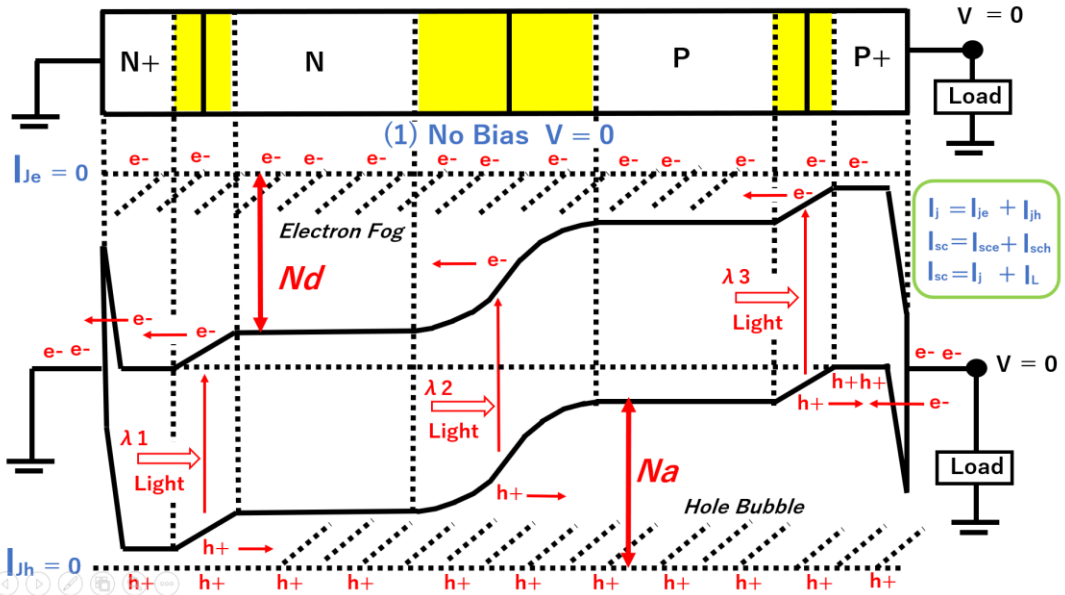
P+PNN+接合Diodeの電流(Ij)電圧(V)特性



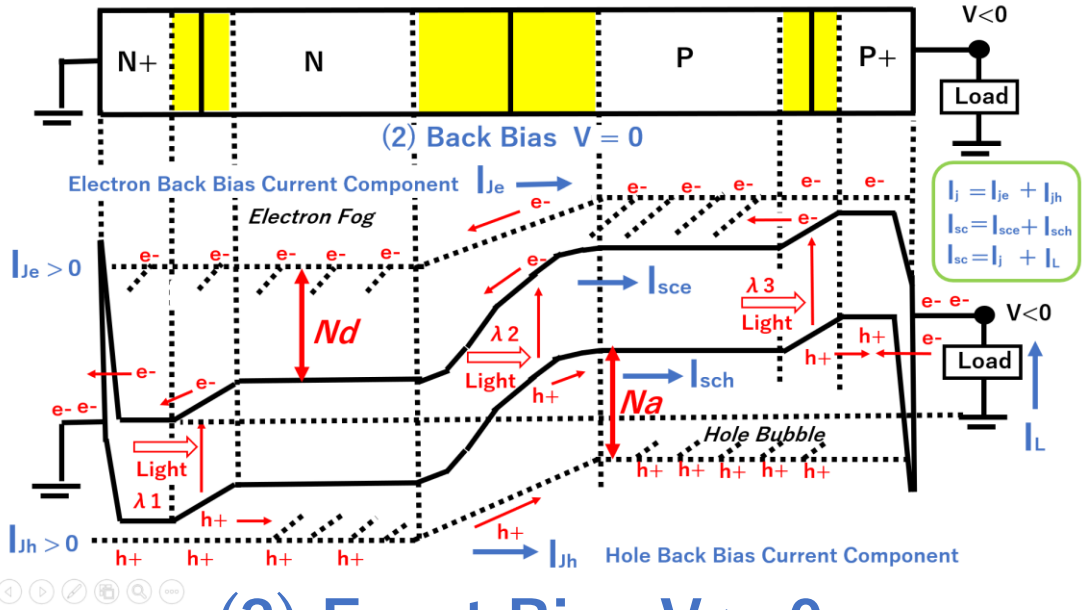
$$(1)\ I_o = A \exp\left(-\frac{E_G}{kT}\right)$$

$$(2)\ I_j = (I_o)\left[\exp\left(\frac{V}{kT}\right) - 1\right]$$

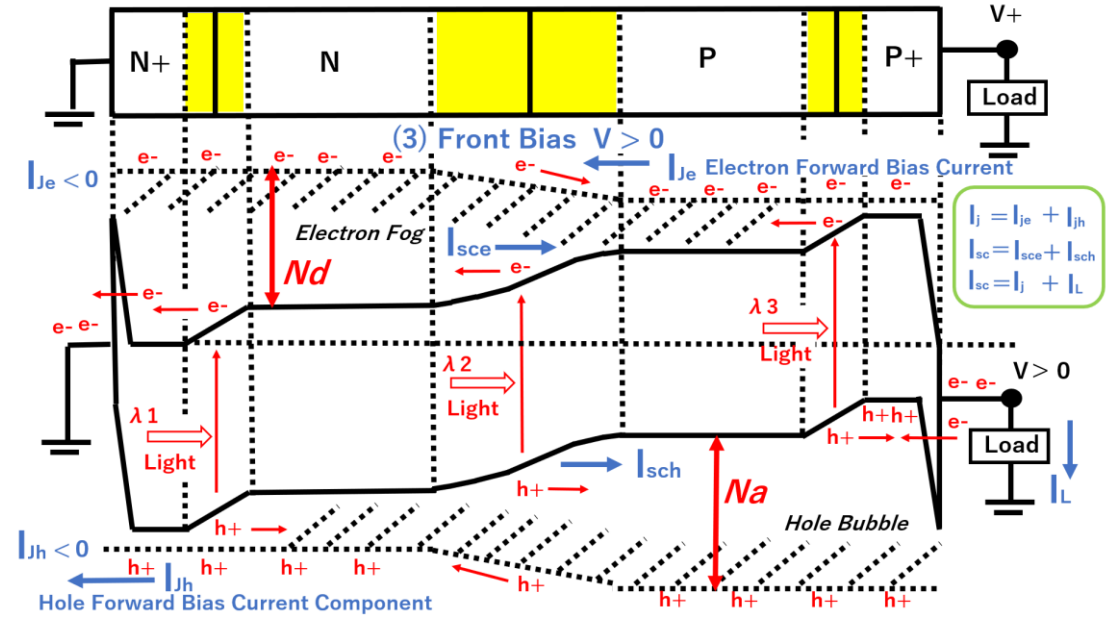
(1) No Bias V = 0



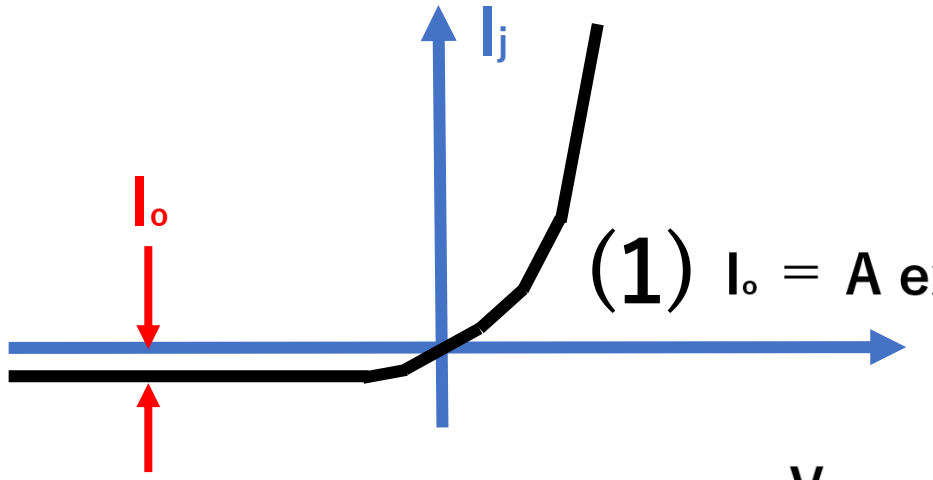
(2) Back Bias V < 0



(3) Front Bias V > 0

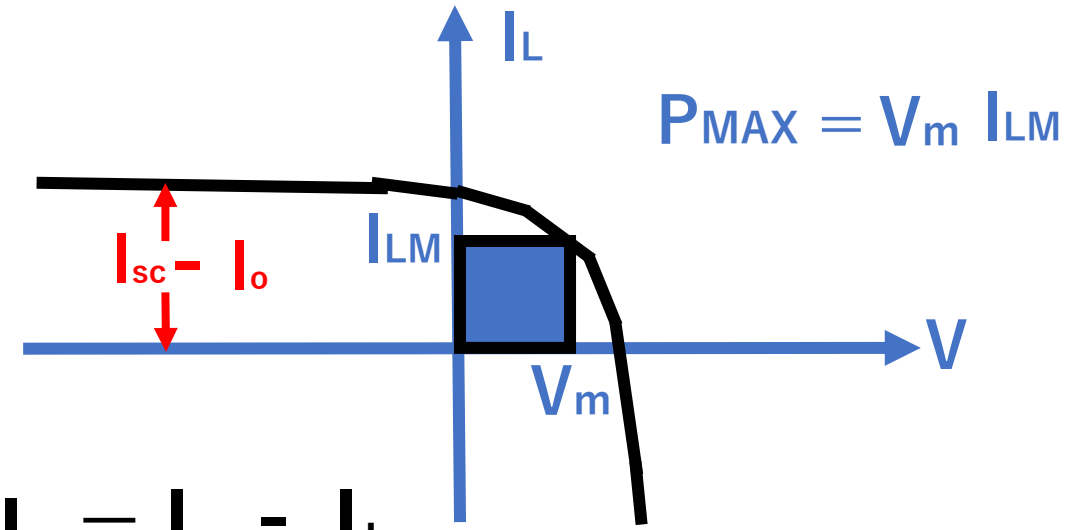


P+PNN+接合Diodeの電流(I_j)電圧(V)特性

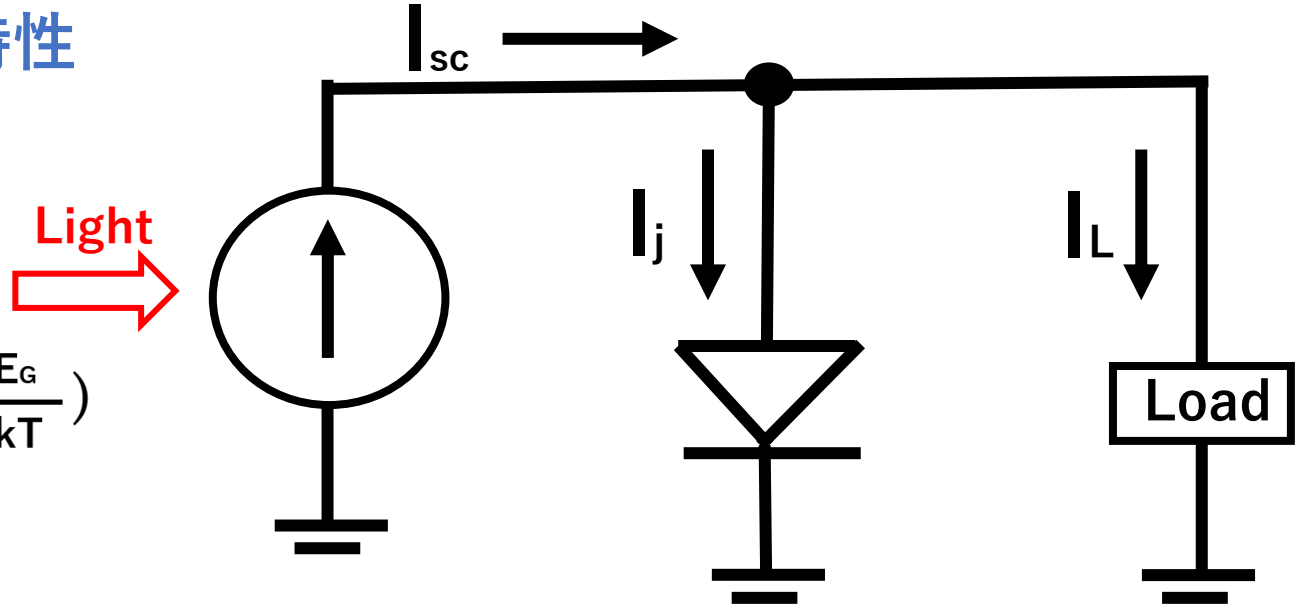


(1) $I_o = A \exp\left(-\frac{E_G}{kT}\right)$

(2) $I_j = (I_o)\left[\exp\left(\frac{V}{kT}\right) - 1\right]$



$I_L = I_{sc} - I_J$



(3) $I_{sc} = I_J + I_L$

(4) $(\text{Power}) = (V)(I_L)$

(5) $\frac{d(I_{sc})}{d(V)} = 0$

(6) $\frac{d(I_j)}{d(V)} + \frac{d(I_L)}{d(V)} = 0$

Obtain $0.5 < \frac{I_{Load}}{I_{SolarCell}} < 1.0$

(1) $I_o = A \exp\left(-\frac{E_G}{kT}\right)$

(2) $I_j = (I_o)\left[\exp\left(\frac{V}{kT}\right) - 1\right]$

(3) $I_{sc} = I_J + I_L$

(4) $(\text{Power}) = (V)(I_L)$

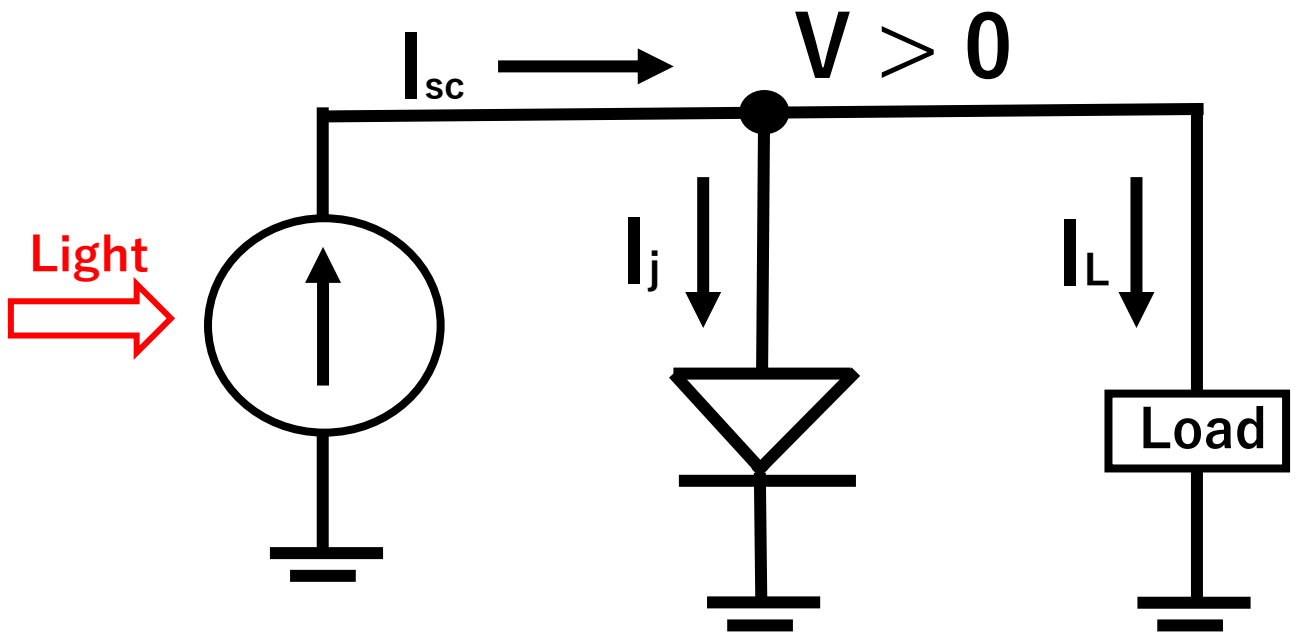
(5) $\frac{d(I_{sc})}{d(V)} = 0$

(6) $\frac{d(I_j)}{d(V)} + \frac{d(I_L)}{d(V)} = 0$

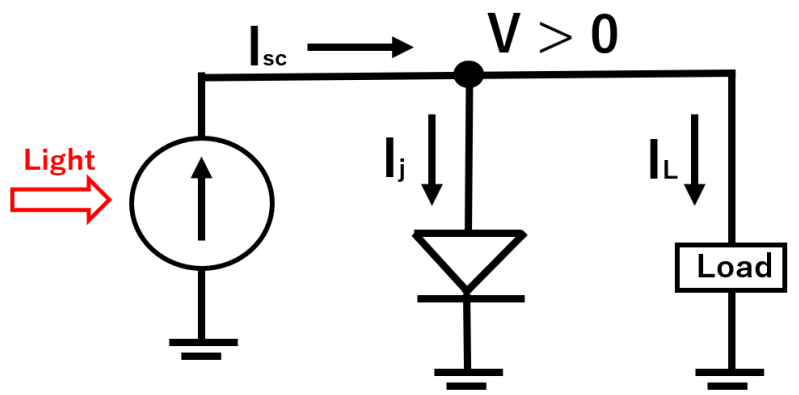
(7) $\frac{d(\text{Power})}{d(V)} = 0$

(8) $(I_L) + (V)\frac{d(I_L)}{d(V)} = 0$

(9) $(I_L) = (V)\frac{d(I_j)}{d(V)}$



Obtain $0.5 < \frac{I_{Load}}{I_{SolarCell}} < 1.0$



$$(9)\quad (I_L) = (V)\frac{d(I_j)}{d(V)}$$

$$(2)\quad I_j = (I_o)\left[\exp\left(\frac{V}{kT}\right) - 1\right]$$

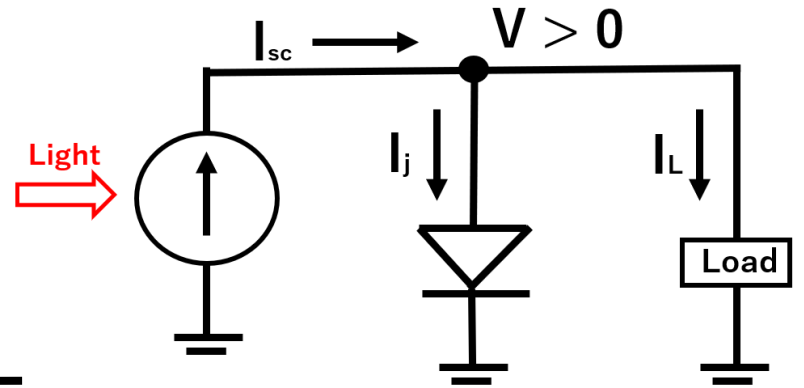
$$(10)\quad (I_L) = \frac{(V\, I_o)}{kT}\exp\left(\frac{V}{kT}\right)$$

$$(1)\quad I_{sc} = I_J + I_L$$

$$(11)\quad \frac{(I_L)}{(I_{sc})} = \frac{(I_L)}{(I_L) + (I_j)}$$

$$(12)\quad \frac{(I_L)}{(I_{sc})} = \frac{\frac{V\, I_o}{kT}\exp\left(\frac{V}{kT}\right)}{\frac{V\, I_o}{kT}\exp\left(\frac{V}{kT}\right) + (I_o)\left[\exp\left(\frac{V}{kT}\right) - 1\right]}$$

Obtain $0.5 < \frac{I_{Load}}{I_{SolarCell}} < 1.0$



E_G=1.11 eV
kT=0.0256 eV

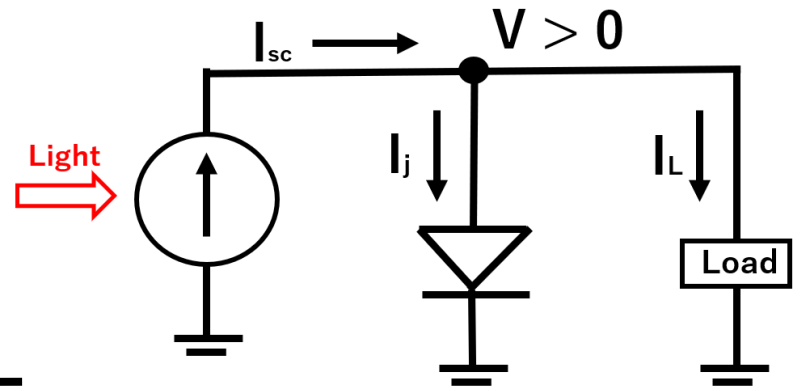
(13) $$\frac{(I_L)}{(I_{sc})} = \frac{\frac{V}{kT}}{1 + (\frac{V}{kT}) - \exp(\frac{-V}{kT})}$$

(14) $$\frac{(V\ I_L)}{(V\ I_{sc})} = \frac{(\frac{V}{kT})}{1 + (\frac{V}{kT}) - \exp(\frac{-V}{kT})} = (0.5 \sim 1.0)$$

for $0<V<E_G$

(12) $$\frac{(I_L)}{(I_{sc})} = \frac{\frac{V\ I_o}{kT} \exp(\frac{V}{kT})}{\frac{V\ I_o}{kT} \exp(\frac{V}{kT}) + (I_o)\left[\exp(\frac{V}{kT}) - 1\right]}$$

Obtain $0.5 < \frac{I_{Load}}{I_{SolarCell}} < 1.0$



$$(13)\quad \frac{(I_L)}{(I_{sc})} = \frac{\frac{V}{kT}}{1 + (\frac{V}{kT}) - \exp(\frac{-V}{kT})}$$

$E_G = 1.11$ eV
$kT = 0.0256$ eV

$$(14)\quad \frac{(V\,I_L)}{(V\,I_{sc})} = \frac{(\frac{V}{kT})}{1 + (\frac{V}{kT}) - \exp(\frac{-V}{kT})} = (0.5 \sim 1.0)$$

for $0 < V < E_G$

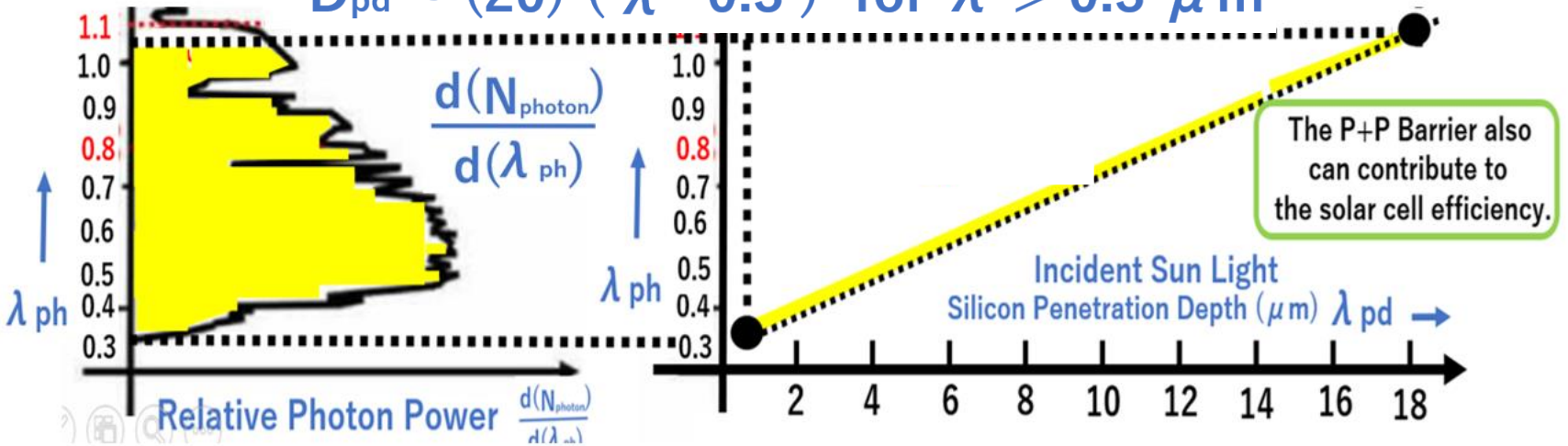
$B < 1.0$

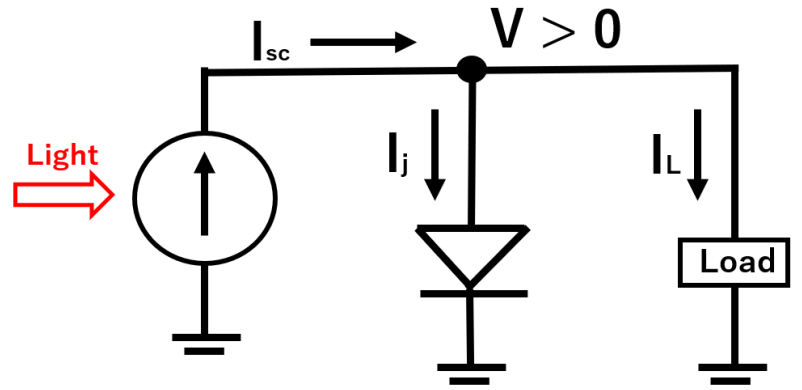
E = Photon Energy (eV)
$E\,(eV) = 1.24\,(\mu m \cdot eV) / \lambda_{ph}\,(\mu m)$

$\lambda_{ph} = 1.24\,(\mu m \cdot eV) / E\,(eV)$
$d(\lambda_{ph})/dE = -1.24/E^2$

$$d(I_{sc}) = \frac{(hc)}{(\lambda)} \{ 1 - \exp(-a\,D_{pd}(\lambda)) \} \frac{dN_{ph}}{d\lambda} d\lambda$$

$$D_{pd} \sim (20)\,(\lambda - 0.3) \quad \text{for } \lambda > 0.3\ \mu m$$





$E_G = 1.11$ eV

$kT = 0.0256$ eV

$$(14)\quad \frac{(V\ I_L)}{(V\ I_{sc})} = \frac{\left(\frac{V}{kT}\right)}{1 + \left(\frac{V}{kT}\right) - \exp\left(\frac{-V}{kT}\right)} = (0.5 \sim 1.0)$$

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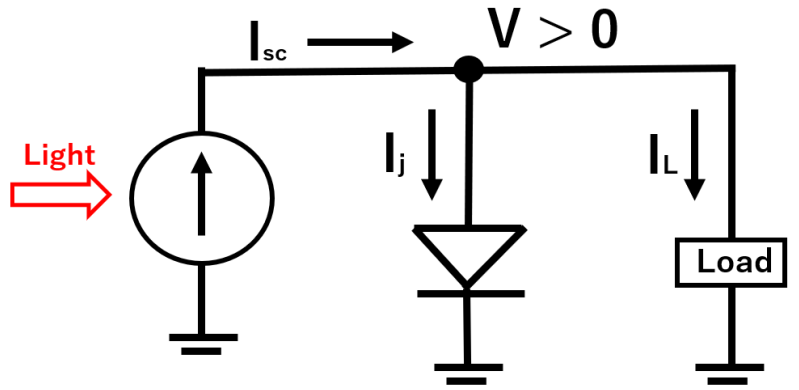
E = Photon Energy (eV)

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$\lambda_{pd} \sim (20)\,(\lambda_{ph} - 0.3)$

$$d(I_{sc}) = \frac{(hc)}{(\lambda)} \{\ 1 - \exp(-a\,D_{pd}(\lambda))\ \} \frac{dN_{ph}}{d\lambda}\, d\lambda$$

$$d(I_{sc}) = (hf)\, dN_{sc} \qquad c = (f\lambda)$$

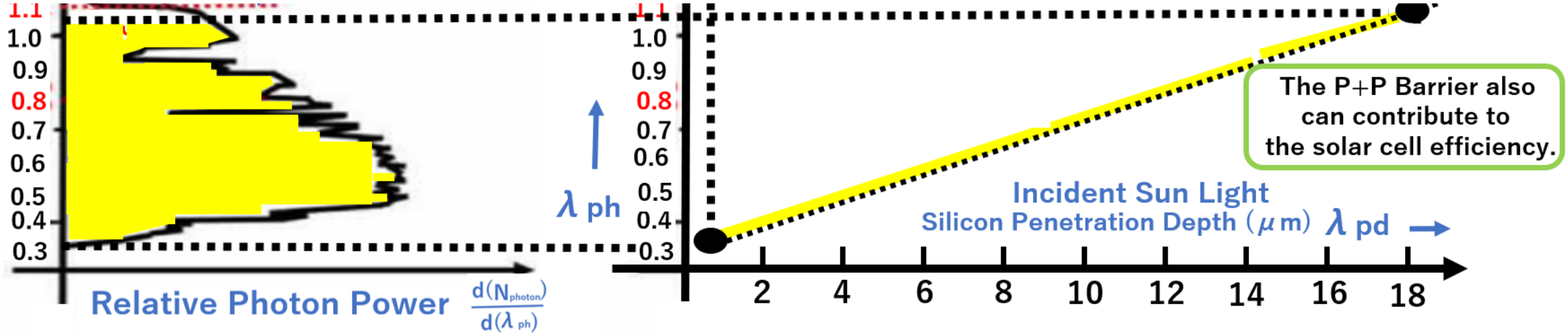


$$d(I_{sc}) = \frac{(hc)}{(\lambda)} \frac{dN_{sc}}{d\lambda} d\lambda$$

$E_G = 1.11$ eV

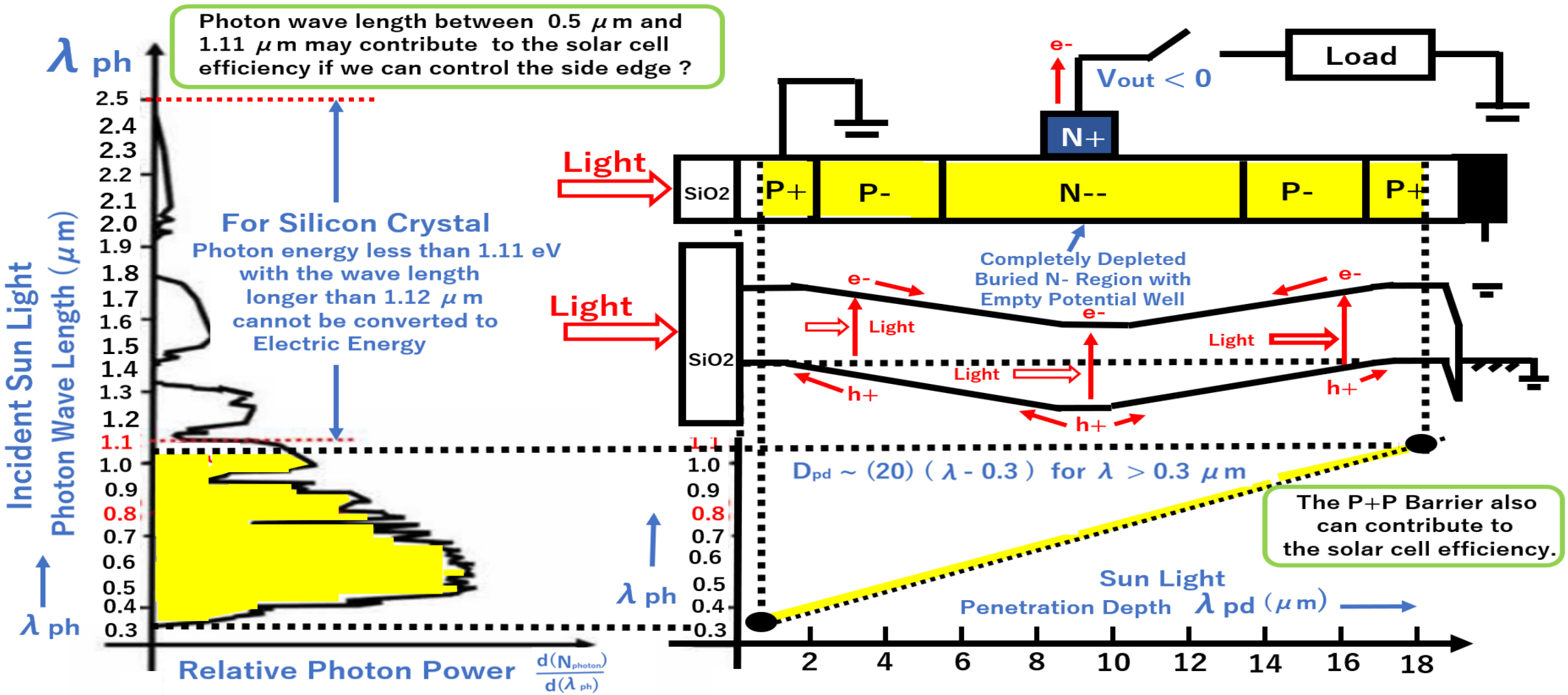
$kT = 0.0256$ eV

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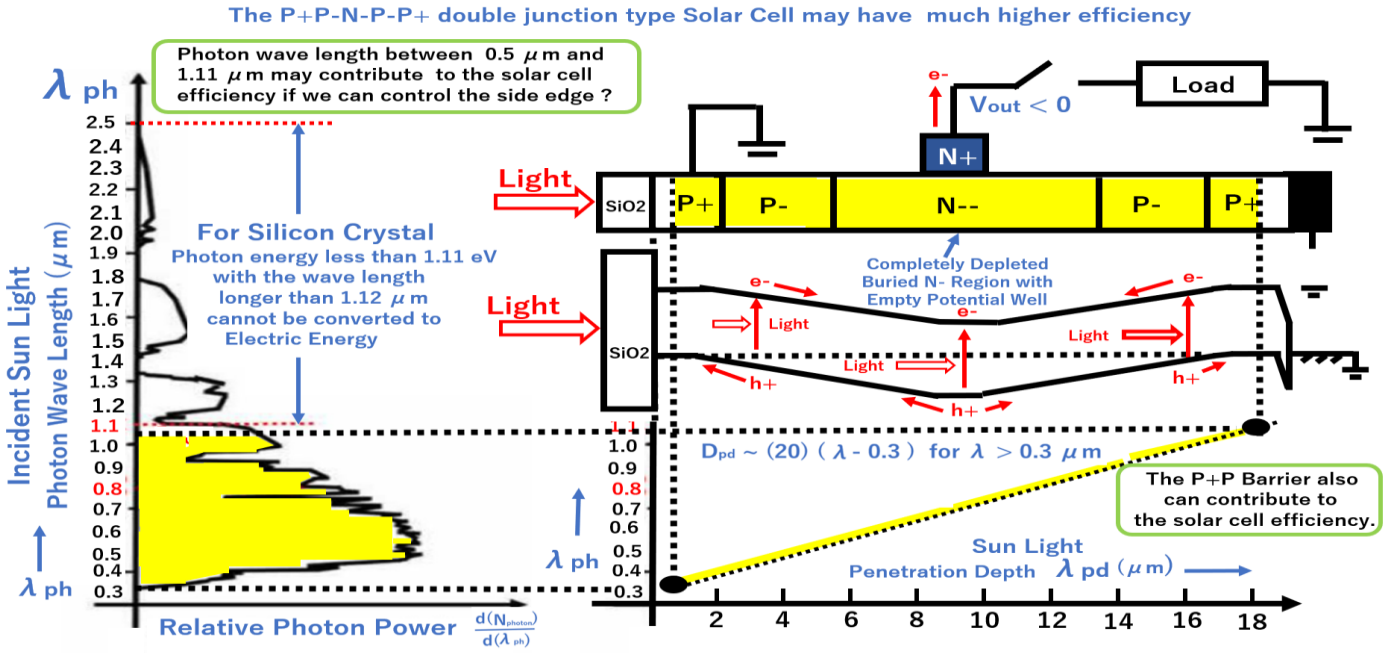
$$d(I_{sc}) = \frac{(hc)}{(\lambda)} \{ 1 - \exp(-a D_{pd}(\lambda)) \} \frac{dN_{ph}}{d\lambda} d\lambda$$

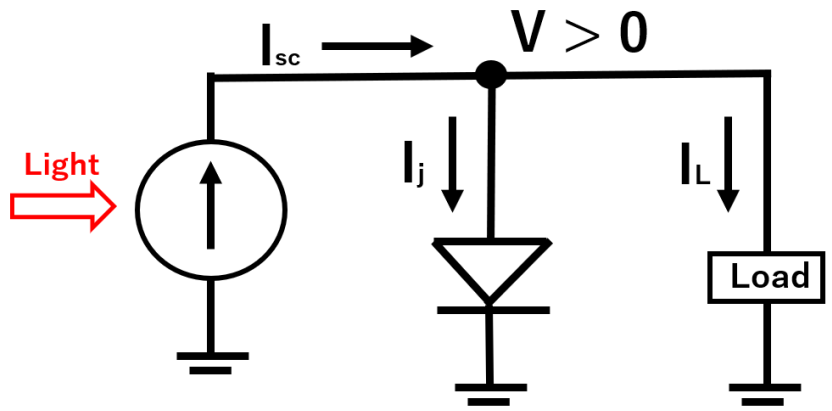
The P+P-N-P-P+ double junction type Solar Cell may have much higher efficiency



$$d(I_{sc}) = \frac{(hc)}{(\lambda)} \{ 1 - \exp(- a D_{pd}(\lambda)) \} \frac{dN_{ph}}{d\lambda} d\lambda$$

P+PNN+接合Diodeの電流(Ij)電圧(V)特性

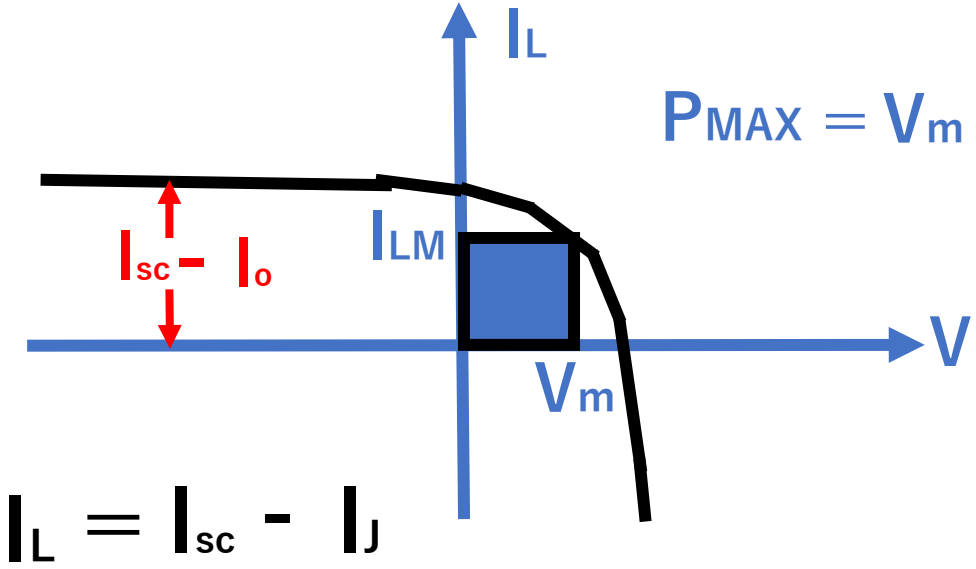




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$$(3)\quad I_{sc} = I_J + I_L$$



$$P_{MAX} = V_m I_{LM}$$

$$I_L = I_{sc} - I_J$$

$$\frac{(V I_L)}{(V I_{sc})} = \frac{\left(\frac{V}{kT}\right)}{1 + \left(\frac{V}{kT}\right) - \exp\left(\frac{-V}{kT}\right)} = (0.5 \sim 1.0)$$

$$d(I_{sc}) = \frac{(hc)}{(\lambda)}\left\{1 - \exp\left(-a D_{pd}(\lambda)\right)\right\}\frac{dN_{ph}}{d\lambda}\, d\lambda$$

太陽電池の変換効率の限界

変換効率は、使用される半導体材料が吸収できる太陽光の波長領域と、PN接合の空乏層領域での吸収量で求まります。シリコン結晶では、波長が 0.29μmから 1.20μm までの太陽光を吸収できます。Single PN 接合型での変換効率の限界理論値は 28% です。実際には20%程度です。その理由は(1)受光面での反射や(2)受光表面再結合や(3)PN接合の空乏層内での結晶欠陥による再結合や(4)裏面再結合などが生じ、光電変換された光電子とホールのペアが再結合し無駄になる為です。

Silicon のBand Gap は　1.1 eV

InP のBand Gap は　1.34 eV

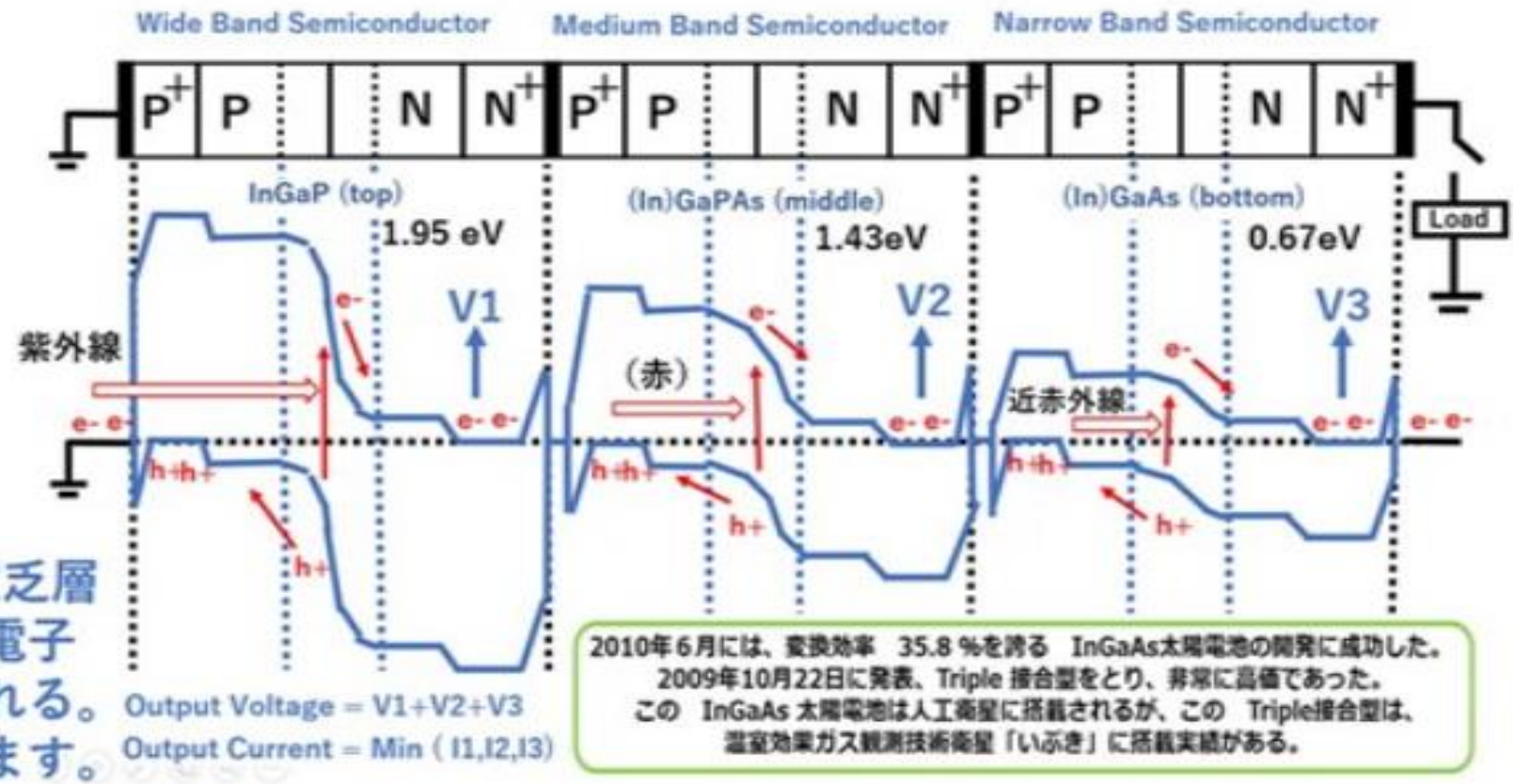
GaAs のBand Gap は　1.42 eV

CdTe のBand Gap は　1.48 eV

GaN のBand Gap は　3.4 eV

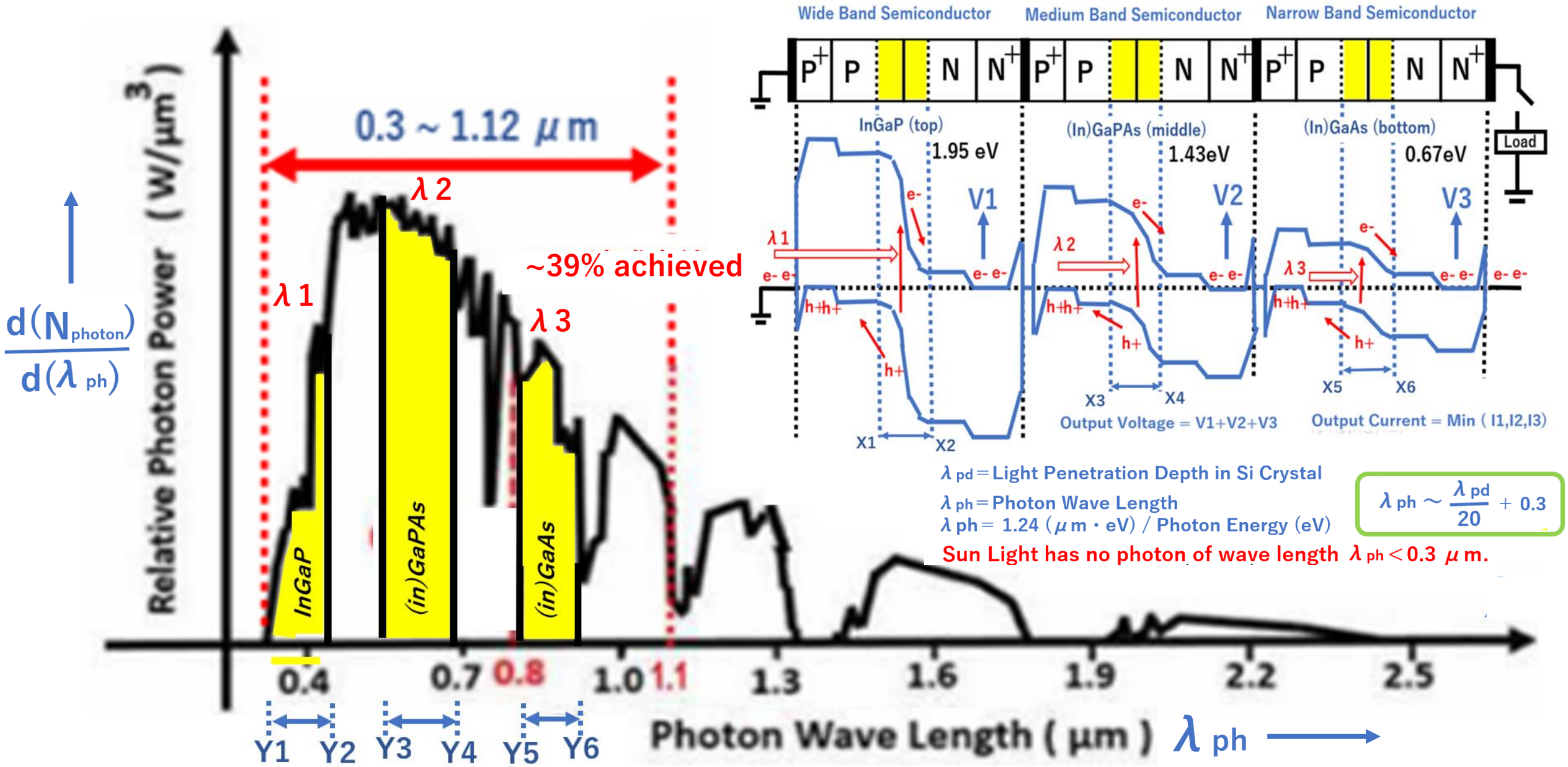
β-Ga_2O_3 のBand Gap は 4.5 eV

バリア電界が存在するPN接合の空乏層領域内でのみ、光電変換による光電子とホールのペアは効率良く分離される。と言う事が、今の常識となっています。



2010年6月には、変換効率　35.8 %を誇る　InGaAs太陽電池の開発に成功した。
2009年10月22日に発表、Triple 接合型をとり、非常に高価であった。
この　InGaAs 太陽電池は人工衛星に搭載されるが、この　Triple接合型は、
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Triple Junction Solar Cell with Wide Band Gap Compound Semiconductors achieved ~39% Quantum Efficiency



λ pd = Light Penetration Depth in Si Crystal

λ ph = Photon Wave Length

λ ph = 1.24 (μm・eV) / Photon Energy (eV)

$$\lambda_{ph} \sim \frac{\lambda_{pd}}{20} + 0.3$$

Sun Light has no photon of wave length $\lambda_{ph} < 0.3\ \mu m$.

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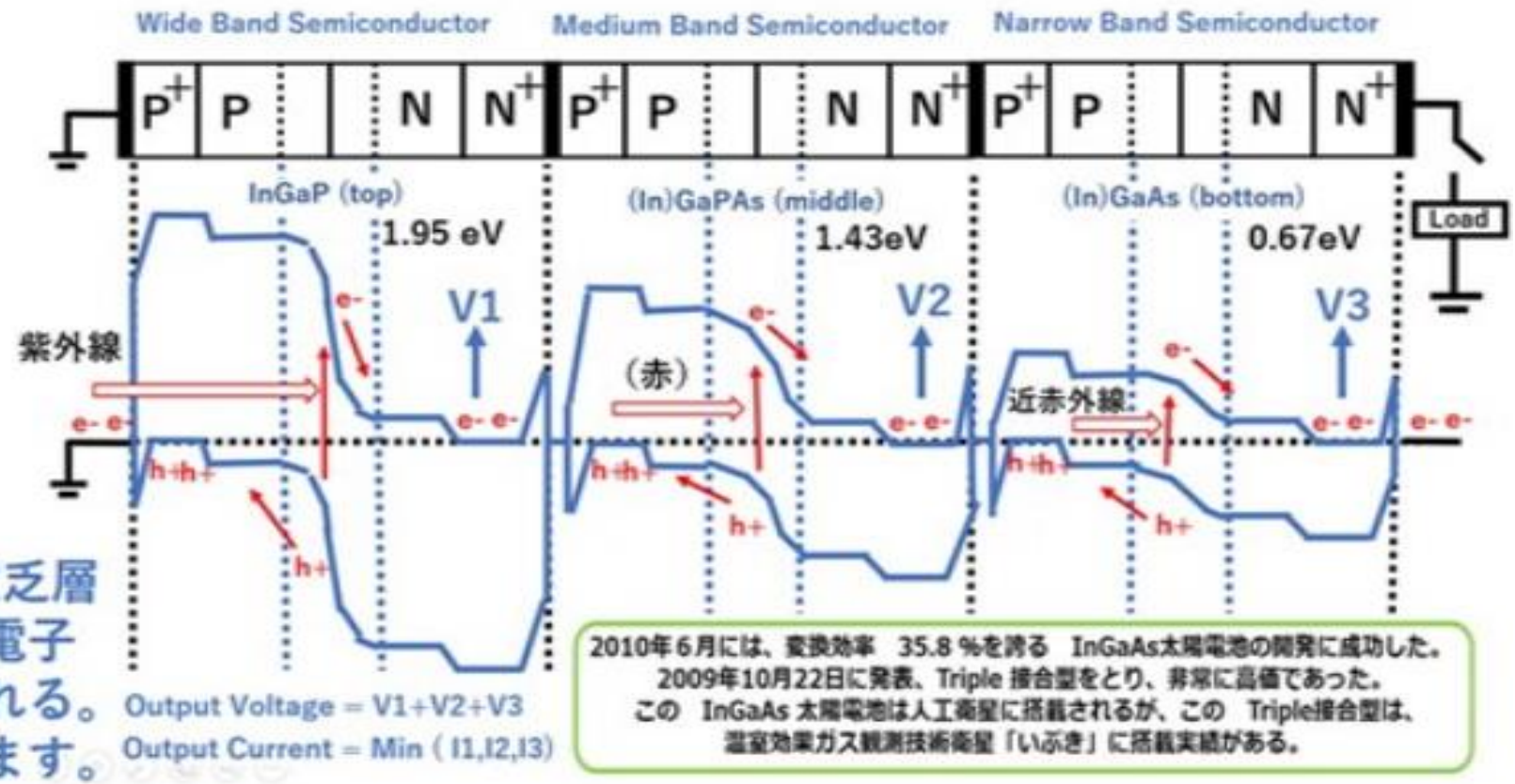
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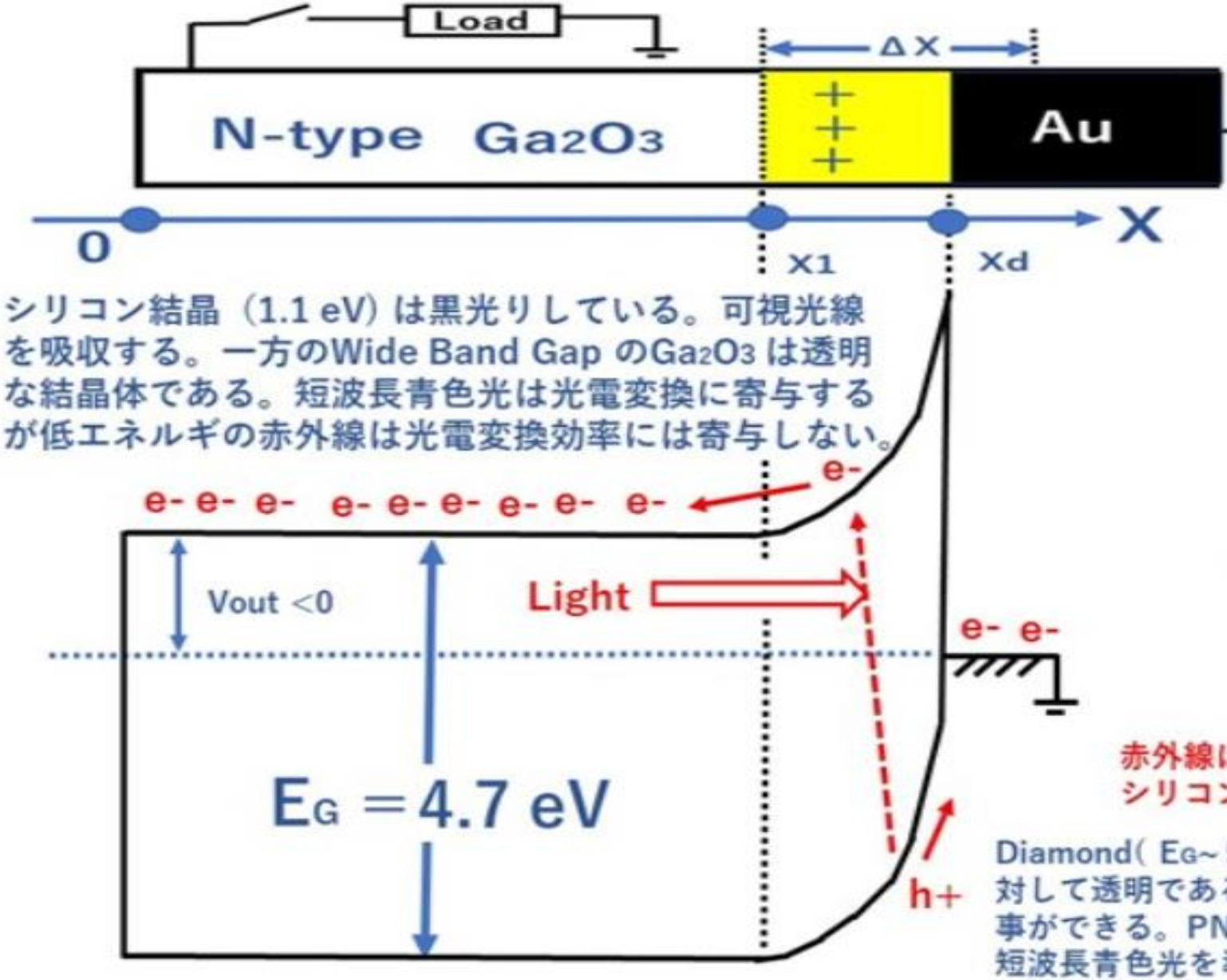
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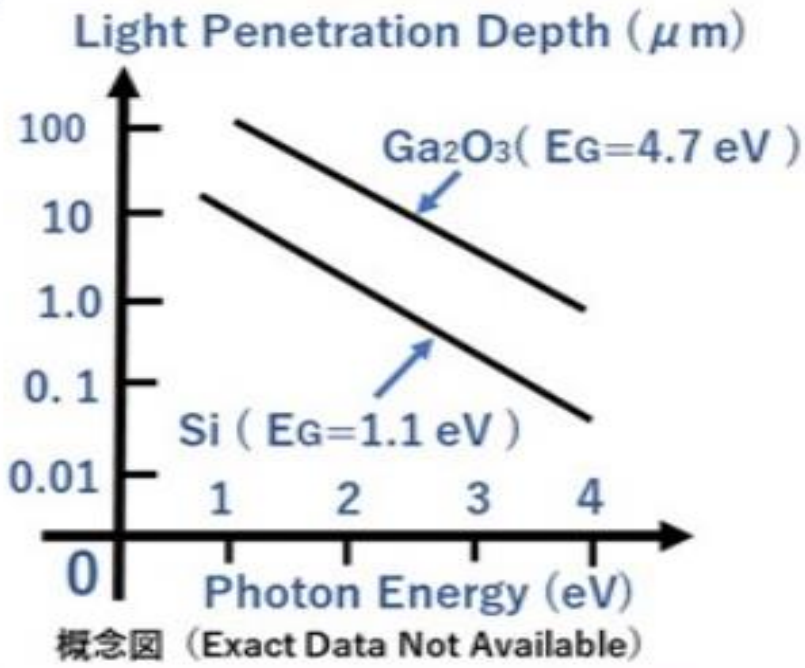


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シリコン結晶（1.1 eV）は黒光りしている。可視光線を吸収する。一方のWide Band Gap のGa2O3 は透明な結晶体である。短波長青色光は光電変換に寄与するが低エネルギの赤外線は光電変換効率には寄与しない。

$$(\text{Photon Energy}) = \frac{1.24\ (\text{eV}/\mu\text{m})}{(\text{Wave Length})}$$



概念図（Exact Data Not Available）

赤外線は結晶奥深く迄透過するが一方の紫外線はシリコンの結晶表面近傍で吸収されて熱になる。

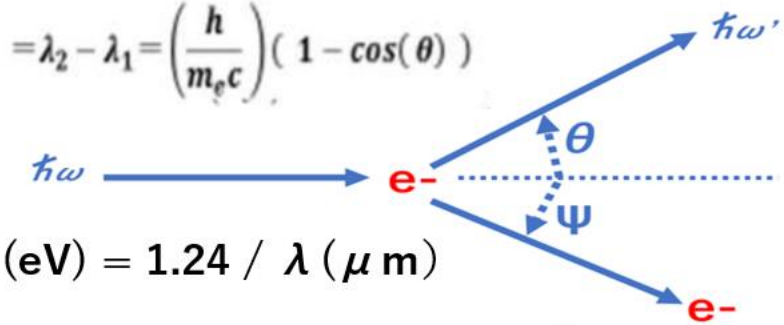
Diamond(EG~ 5 eV)やGa2O3 (EG~ 4 7 eV)などは可視光線に対して透明である。結晶内の奥深く迄短波長青色光を透過する事ができる。PN接合の空乏層領域 X1<X<X2 迄、奥深く迄、短波長青色光を導く事が可能で太陽電池の効率向上に寄与する。

Arthur H. Compton (1892～1962), while at Washington University at St. Louis found that x-rays increase in wave length when scattered, which he explained in 1923 on the basis of the quantum theory of light.

●光は波でもあり、また粒子（光子）でもある (Albert Einstein 1900)

●玉突きと同じ古典物理モデルで記述できる。
●反射光の角度と波長の関係から**電子の質量**が求まる！

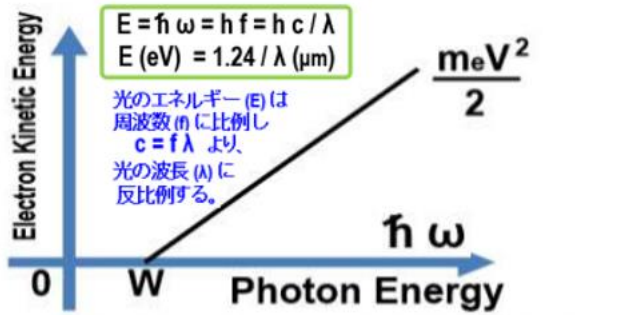
$$\Delta\lambda = \lambda_2 - \lambda_1 = \left(\frac{h}{m_e c}\right)(1 - \cos(\theta))$$



$$E\ (eV) = 1.24 / \lambda\ (\mu m)$$

光が電子とぶつからない時は
Θ=0 で光は直進し波長の変化はない。

光の速度 C = 2.99792458 x 10^{10} cm/sec
Plank 定数 h = 6. 62606957 x 10^{-34} Joule･sec
電子の質量 m_e = 9.10938291 x 10^{-31} kg

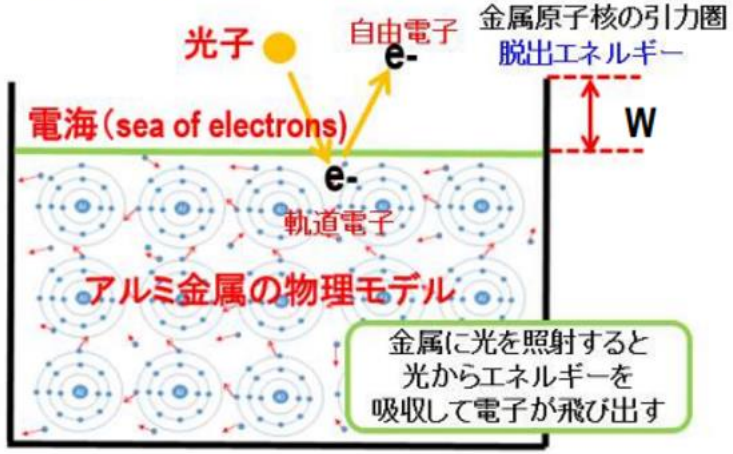


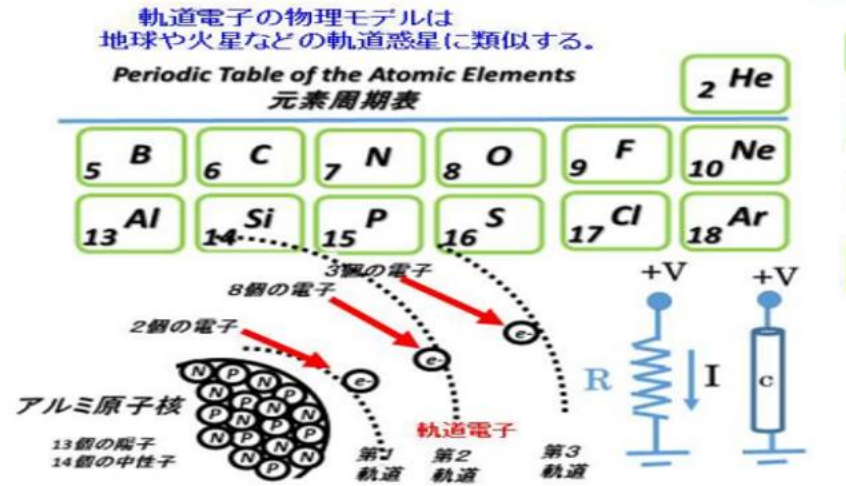
Work Function (W)の値から金属の種類が判明する。

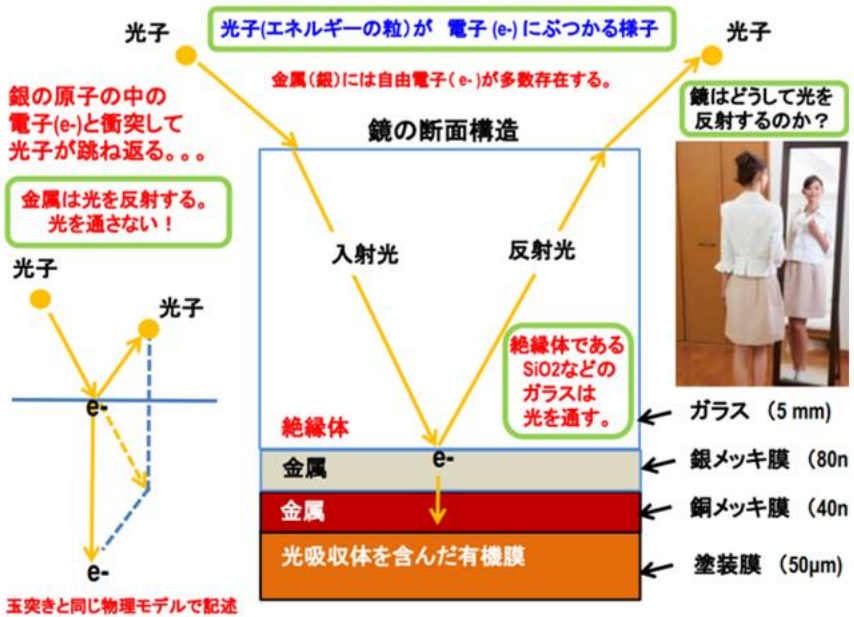


（脱出エネルギー）＝半導体のEnergy Gap
Silicon, E_G = 1.10 eV and λ = 1.12 μm

●金属の物理モデル（器の中に入った水モデル）





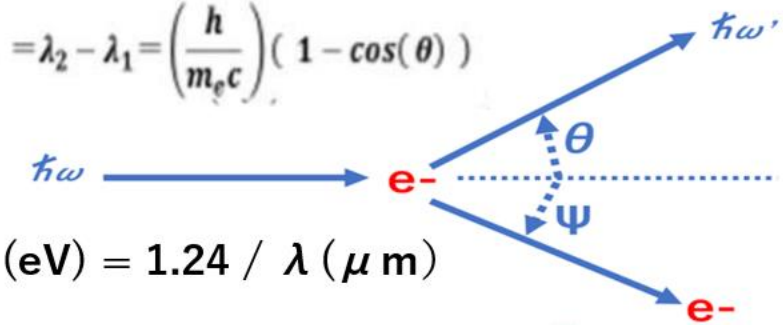


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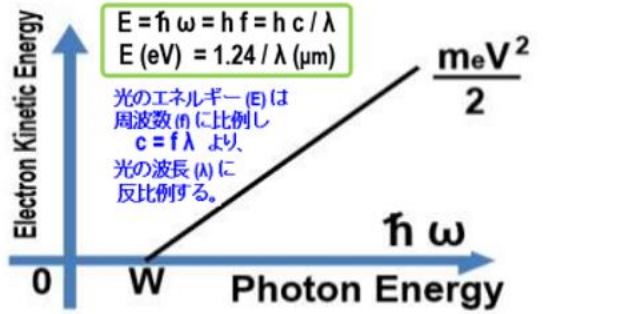
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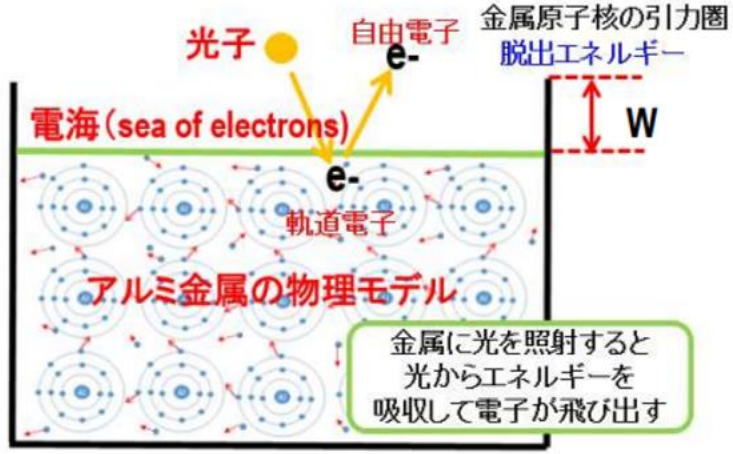


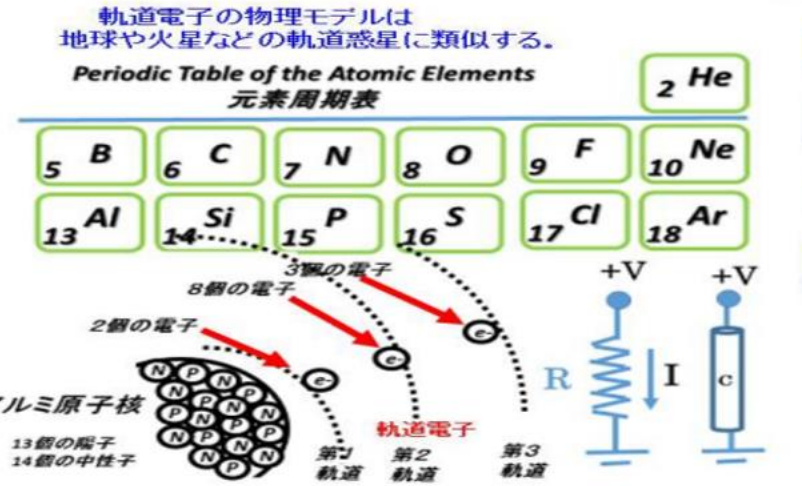
Work Function (W)の値から金属の種類が判明する。

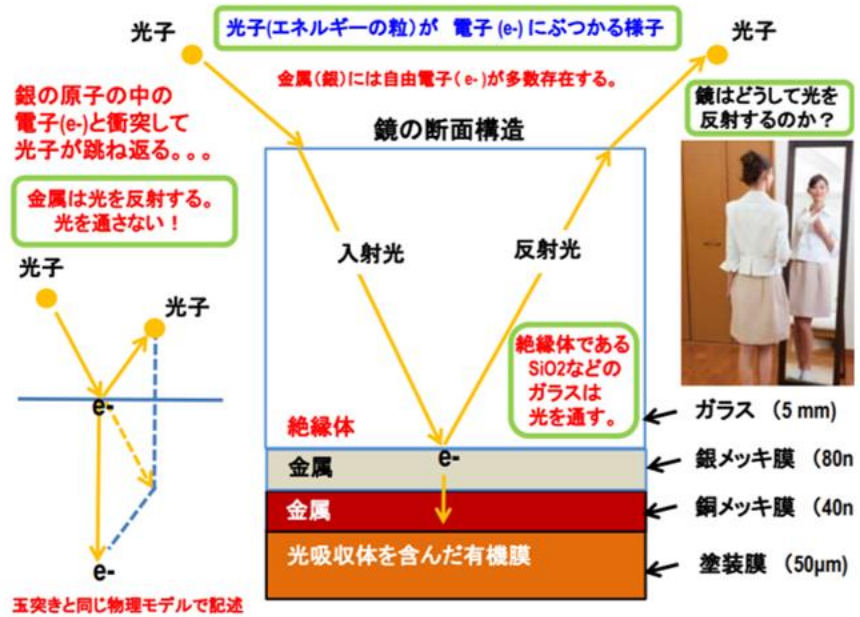


（脱出エネルギー）＝半導体のEnergy Gap
Silicon, E_G = 1.10 eV and λ = 1.12 μm

●金属の物理モデル（器の中に入った水モデル）



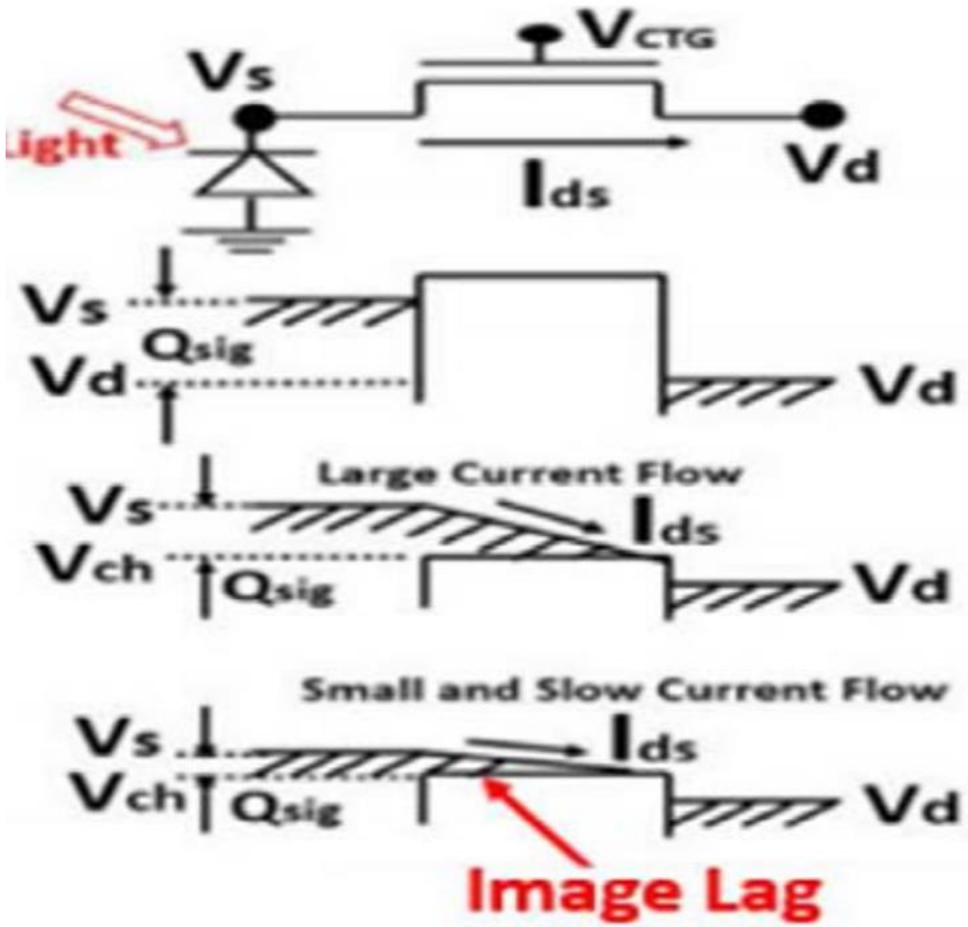




$(Light)_4 = \hbar \cdot (\omega, Kx, Ky, Kz)$ $(Electron)_4 = (E, Px, Py, Pz)$ $E^2 - c^2 P^2 = E_o^2$ $E = \hbar\omega$ and $P = \hbar K$

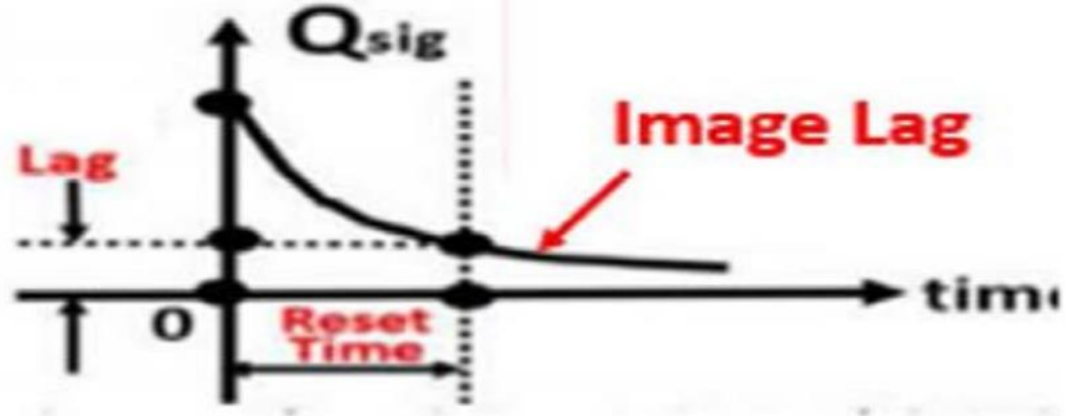
True History of Photodiode

(1) Single Junction Type Dynamic Photodiode before 1970



$$I_{ds}(t) = I_o \left(V_s - V_{ch} \right)^2$$

$$Q_{sig}(t) = Q_o \exp\left(-t / \tau \right)$$



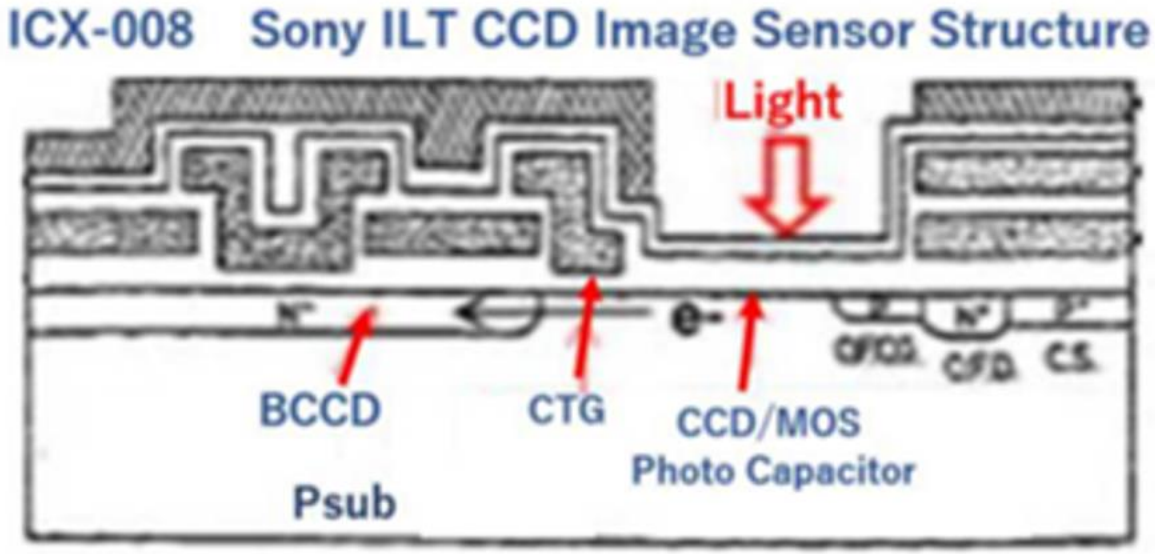
(1) Single 接合型は残像が大問題だった。

. Serious Image Lag of Floating N+P Single Junction Photodiode.

True History of Photodiode

(2) CCD/MOS容量型は光感度と暗電流白点欠陥多発が大問題だった。

(2) CCD/Mos type dynamic Photodiode invented in 1970







SONY 1980 Two-chip CCD Color Video Camera XC-1.

True History of Photodiode

(3) Double 接合型は、RC遅延による光残像が生じ電子シャッター機能が不可だった。

(3) Double Junction type Dynamic Photodiode invented by Philips in June 9, 1975



⑪特開昭 51－150288

⑬公開日 昭51.(1976) 12 23

㉑特願昭 51－65705

㉒出願日 昭51.(1976) 6.7

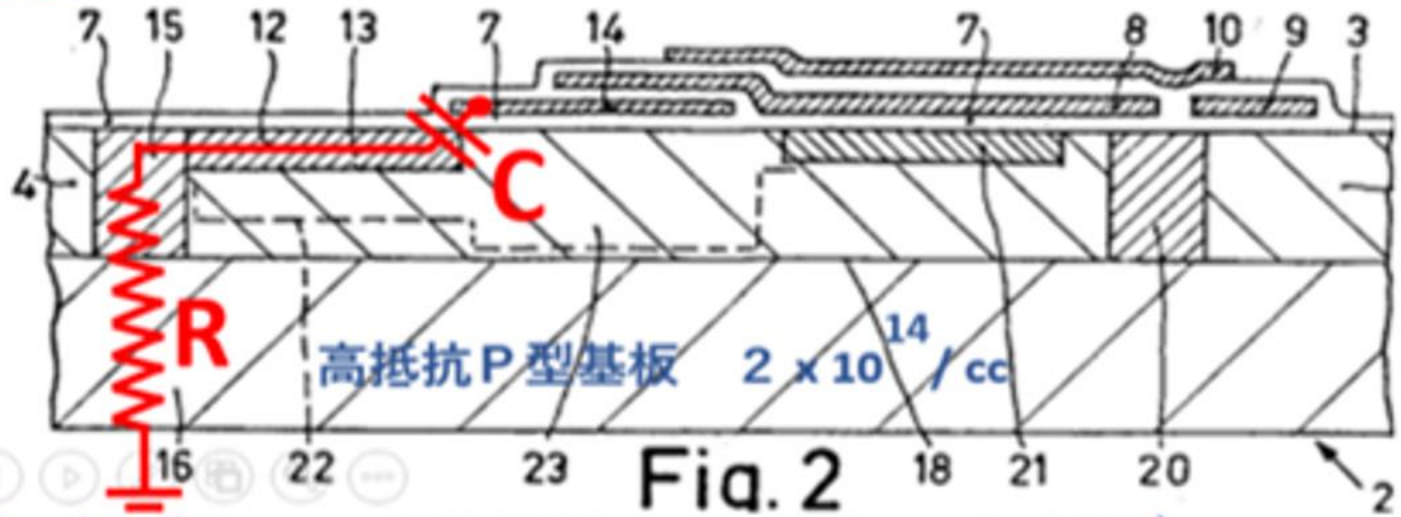


Fig. 2

JPA1976-150288(Netherland Patent 7506795, priority June 9, 1975)

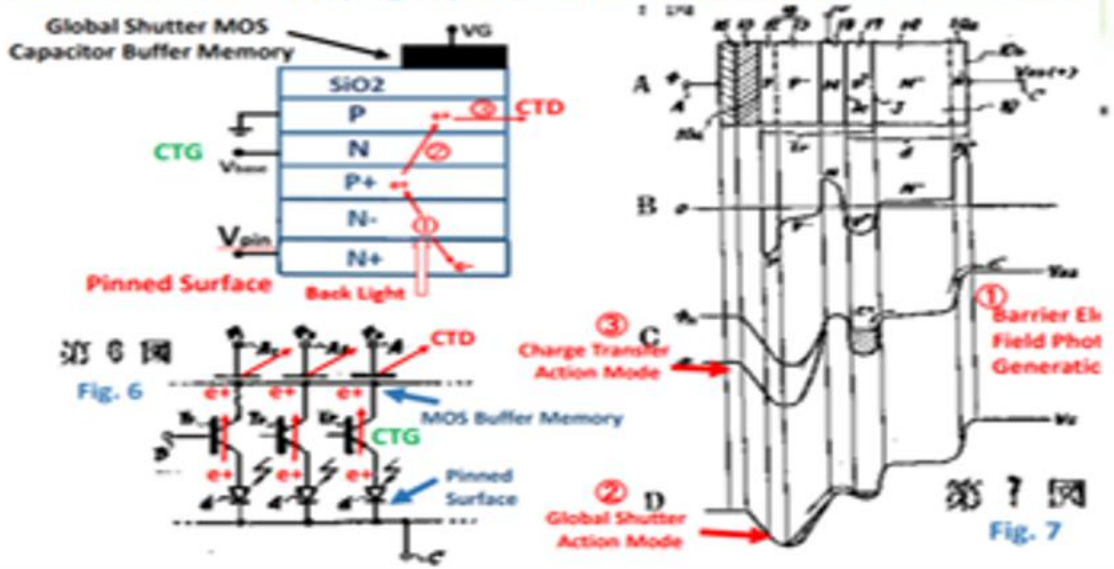
すこしでも RC 遅延があると、10万ぶんの1秒などの超高速な電子のシャッター機能は実現不可能である。
通常は 1 秒間に 60 frame 程度が必要撮像条件である。この埋め込み型のBuried Photodiodeでは、
受光面が完全にはピン留めされていない。それでは、十分に残像が取り切れない。 1 秒間に 60 frame 程度のシャッター速度でも残像がのこる。
事実1982年に、NECの寺西は IEDM1982の論文（このPhilips社発明と同構造)においても、残像があることを報告している。
1978年のSSDM1978の国際会議で、Sonyは、High Energy Ion Implantation技術を使い、高濃度のP+のChannel Stops領域を受光表面に隣接させて形成した。
それで受光表面をピン留めし、この受光素子は完全に電荷転送を実現しており、残像のない特性を持つ事を報告した。
1984年のIEDM1984の国際会議でKODAKは、LOCOS素子間分離を使って、受光表面を完全にGNDにピン留めした受光素子を開発し、
KODAK社は「受光表面がピン留めされて電圧が固定されること」の必要性を強調し、Pinned Photodiodeと命名した。

True History of Photodiode

(4) Triple Junction type Dynamic Photodiode with the pinned surface invented by Sony in Oct 23, 1975.

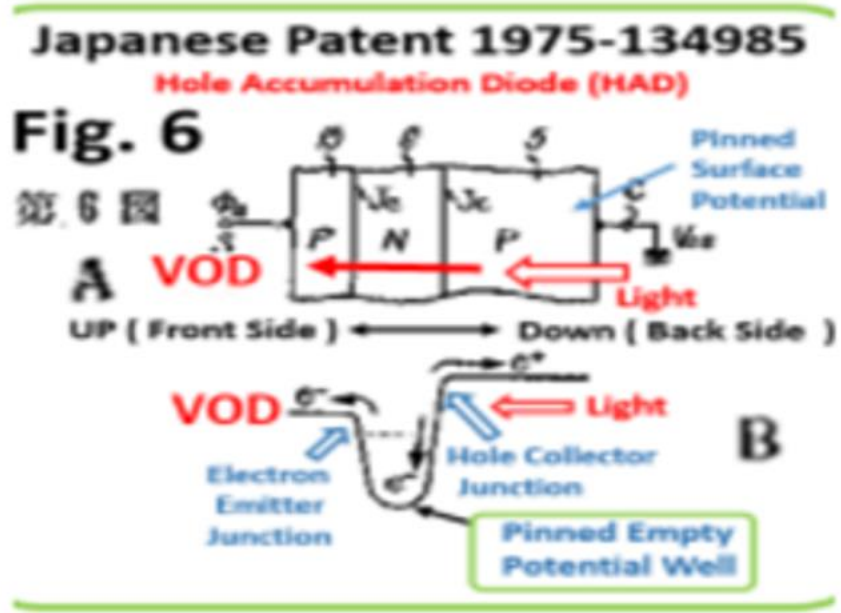
Japanese Patent 1975-127646

N+NP+NP junction type Buried Pinned Photodiode
with Built-in MOS Capacitor Buffer Memory Global Shutter Function
and the surface N+N doping slope Barrier Electric Field Photo Pair Generation



Japanese Patent 1975-134985

Hole Accumulation Diode (HAD)



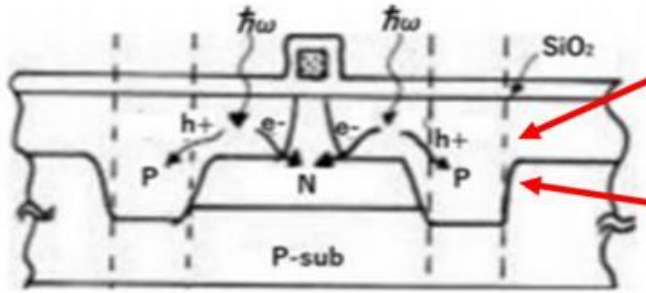
(4) Triple 接合型受光素子となり、初めて垂直型電子シャッター機能が実現した。
電子シャッター機能の実現には、受光面が電圧固定（ピン留め）されて
いる事が不可欠だった。実は、Pinned Photodiodeは、電子シャッター実現
のためにTriple 接合型受光素子として最初に１９７５年１０月に考案された。

True Historv of Photodiode

First Pinned Photodiode was invented by Hagiwara in 1975 and reported at SSDM1978 by Sony.

Sony never used LOCOS isolation nor Shallow Trench Isolation. Both suffer the yield problem of Dark Current and White Defects. Instead, Sony used high energy ion implantation to form the adjacent heavily doped P+ channel stops region with the Lamp Anneal Technology invented by Kazuo Nishiyama at Sony.

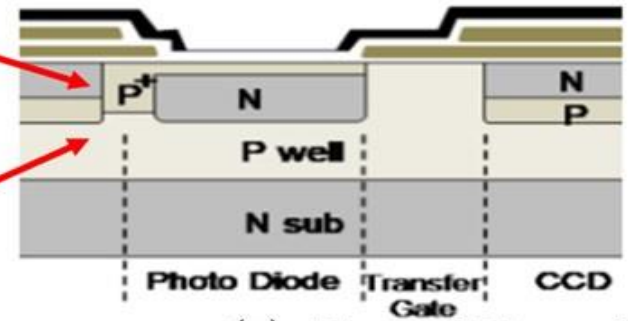
(1) The first Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation invented and reported at SSDM1978 by Hagiwara.



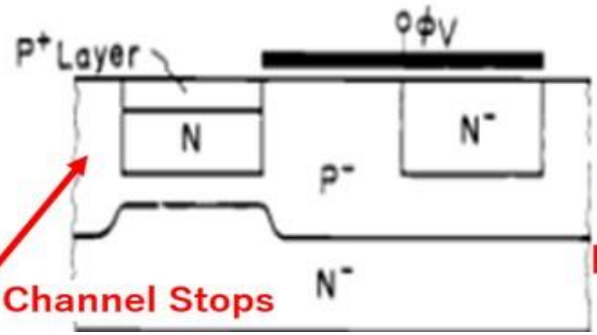
No LOCOS Isolation

No Shallow Trench Isolation

(2) Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation as explained by ssis.or.jp in the official Semiconductor History Museum WEB site.

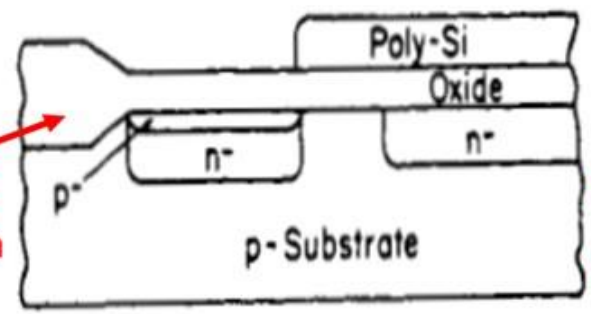


(3) Buried Photodiode reported at IEDM1982 by NEC



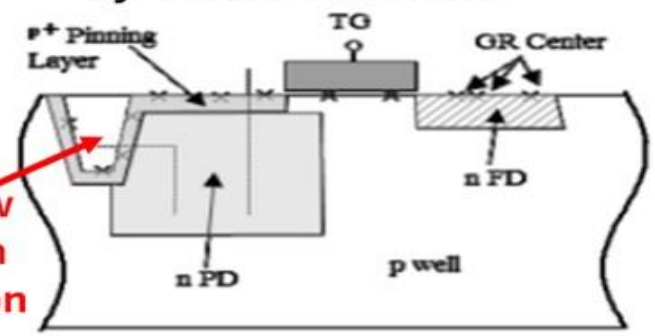
No Channel Stops

(4) Pinned Photodiode reported at IEDM1984 by KODAK



LOCOS Isolation

(5) Pinned Photodiode reported by Teranishi in 2014



Shallow Trench Isolation

Sony Pinned Photodiode has the adjacent P+ heavily doped channel stops always directly grounded to the metal wire at the surface since 1978. Sony never used LOCOS isolation nor Shallow Trench Isolation.

The First Pinned Photodiode was invented by Hagiwara at Sony in 1975 in order to realize the in-pixel electric shutter function. The evidence is given in the Japanese patent application JPA1975-127646, which defined the pinned-surface triple-junction dynamic-thyristor type Pinned Photodiode.

The evidence are given in the Japanese Patent Applications, JPA1975-127646, JPA1975-127646 and JPA1975-134985.

Fig 7 in JPA1975-127646

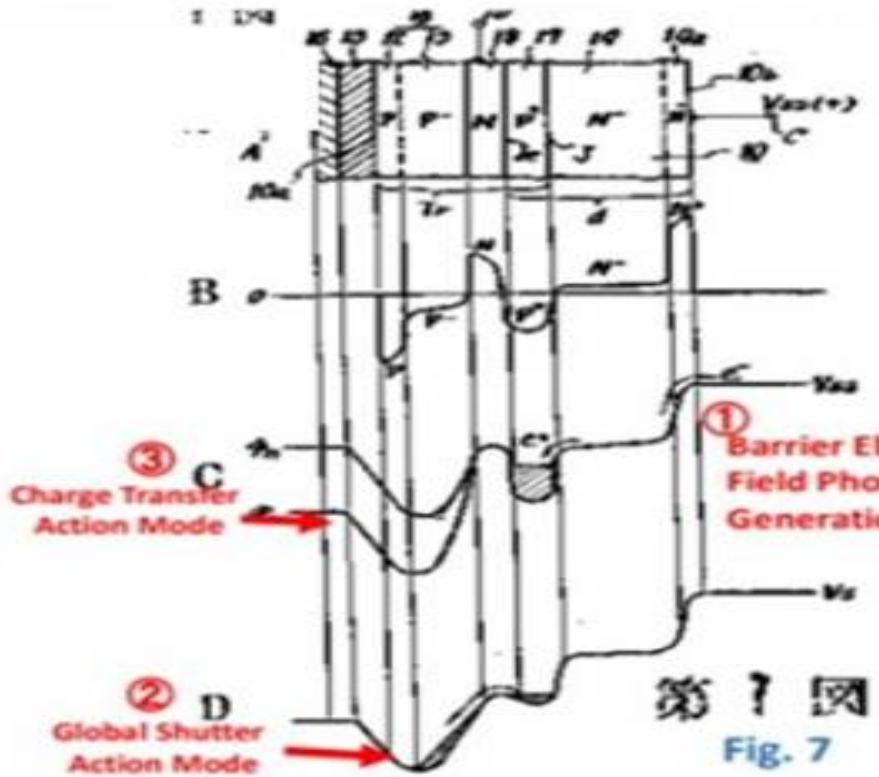


Fig 7 in JPA1975-127647

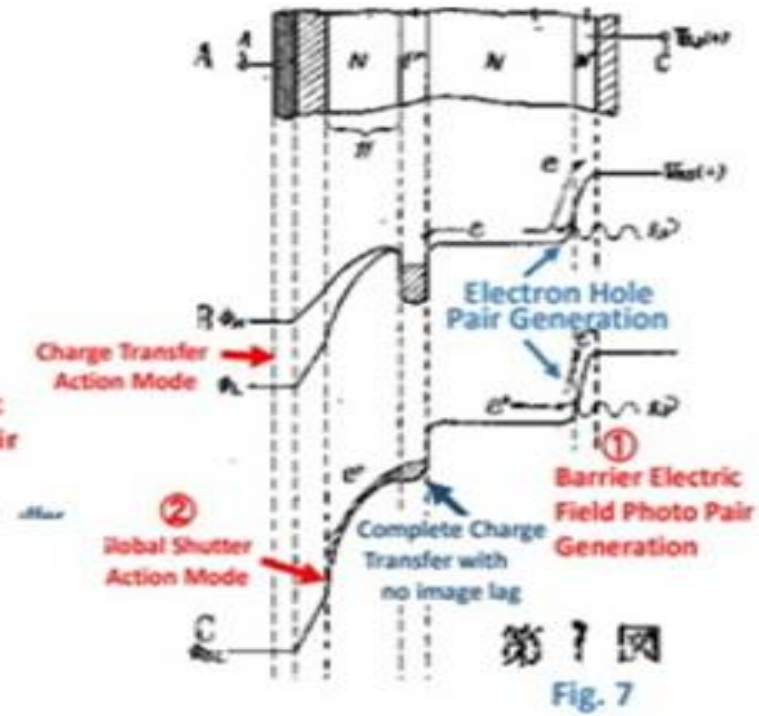
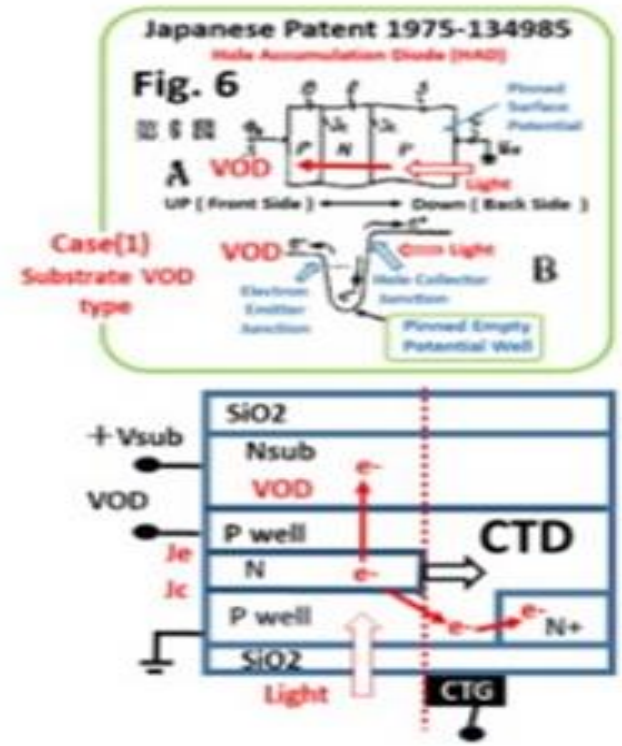


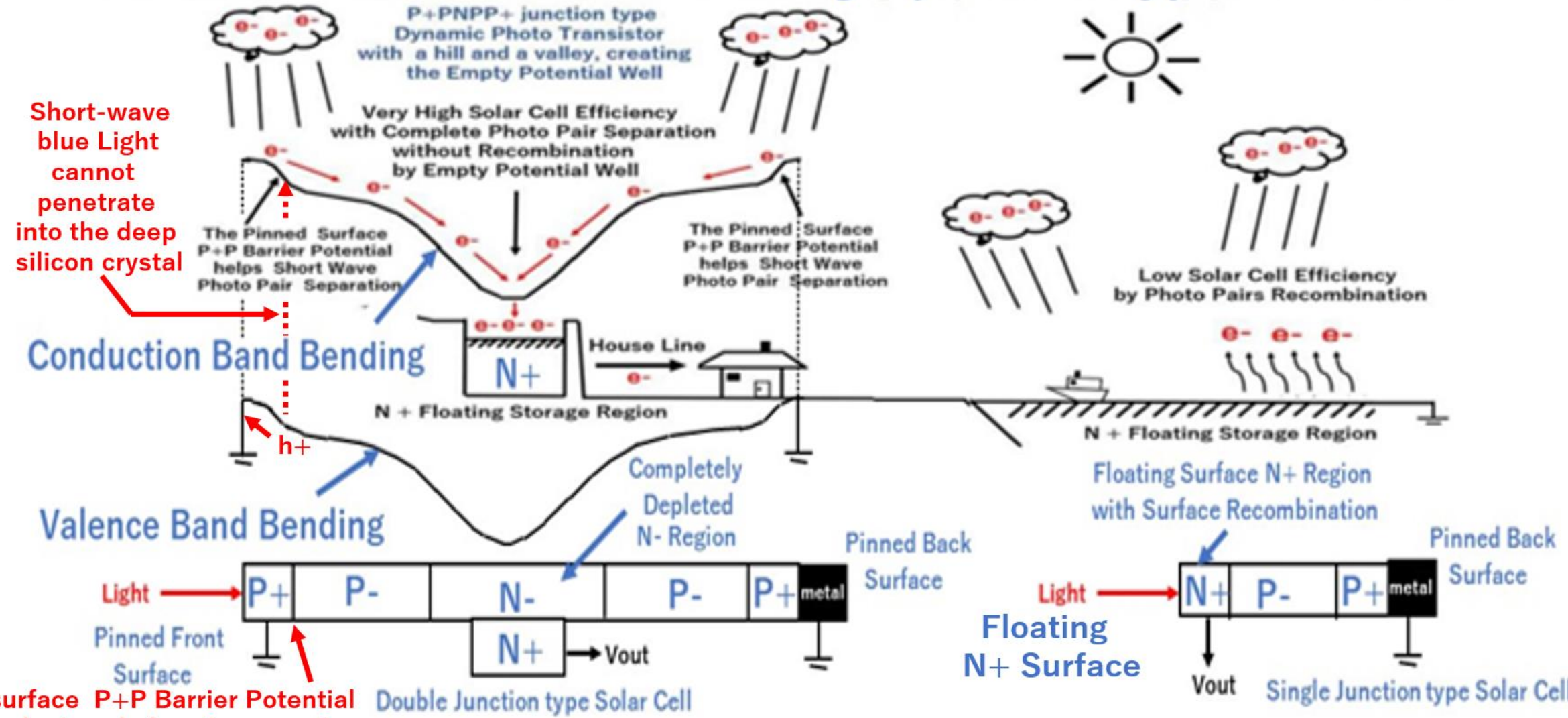
Fig 6 in JPA1975-134985



PPD with in-pixel VOD function was drawn in Hagiwara Lab Note in Feb 1975.

True History of Photodiode

The difference of Double and Single junction type Solar Cells



The surface P+P Barrier Potential helps electron-hole pair separations.

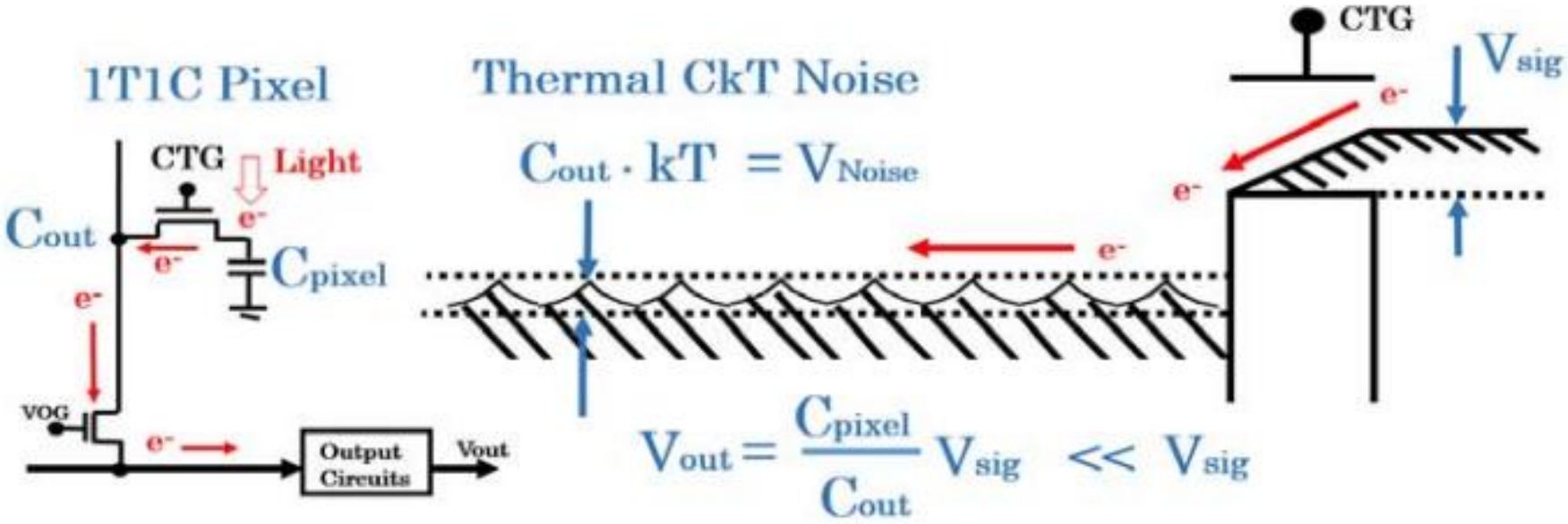
True History of Photodiode

(1) Single Junction Type Dynamic Photodiode before 1970

(2) CCD/Mos type dynamic Photodiode invented in 1970

(3) Double Junction type Dynamic Photodiode invented by Philips in June 6, 1975

(4) Triple Junction type Dynamic Photodiode with the pinned surface invented by Sony in Oct 23, 1975.



1T1C type MOS Image Sensor with a Large Output Data Line Capacitance.

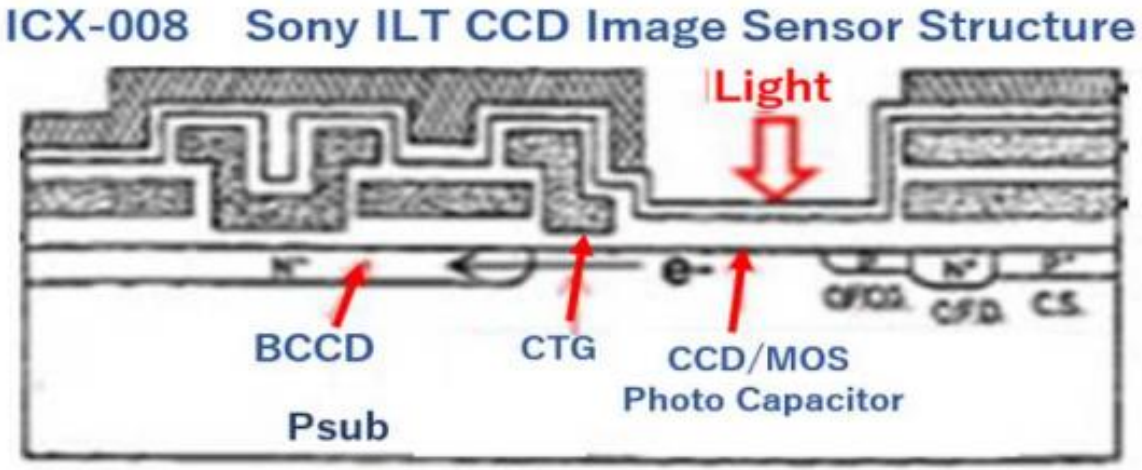
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SONY 1980 Two-chip CCD Color Video Camera XC-1.





True History of Photodiode

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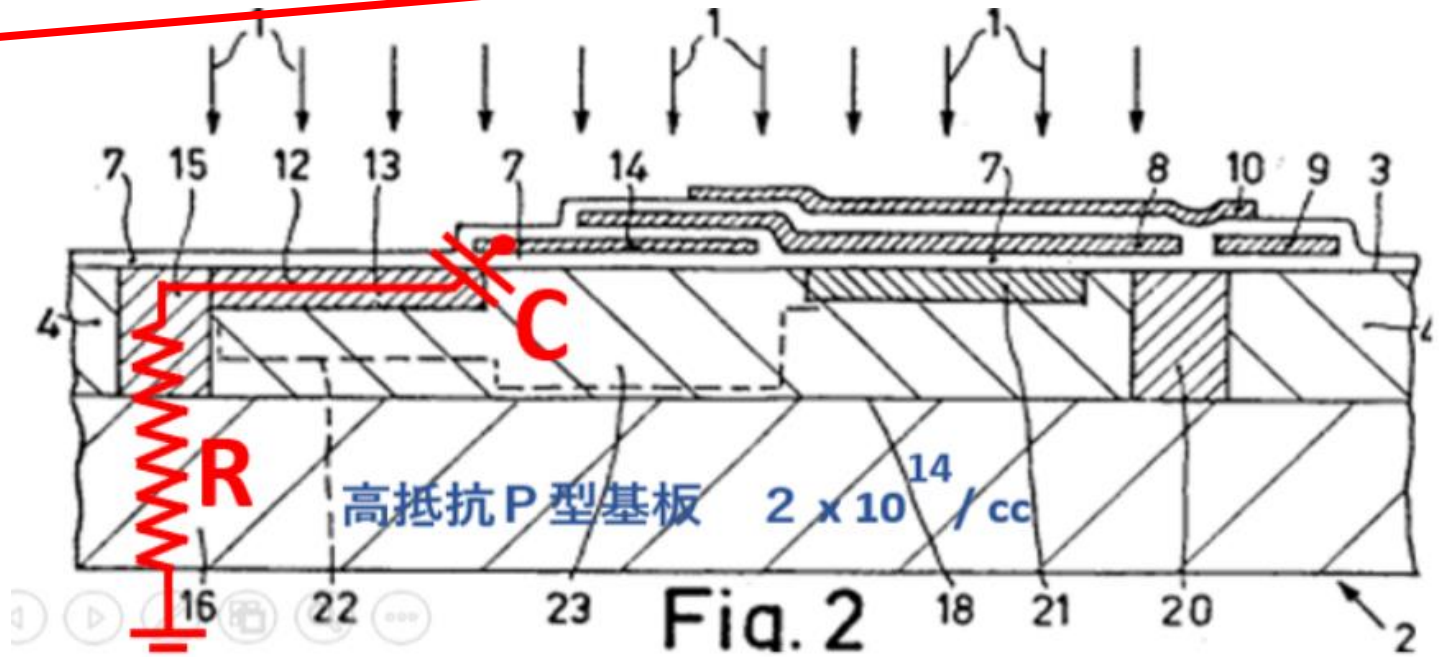


Fig. 2

JPA1976-150288(Netherland Patent 7506795, priority June 7, 1975)

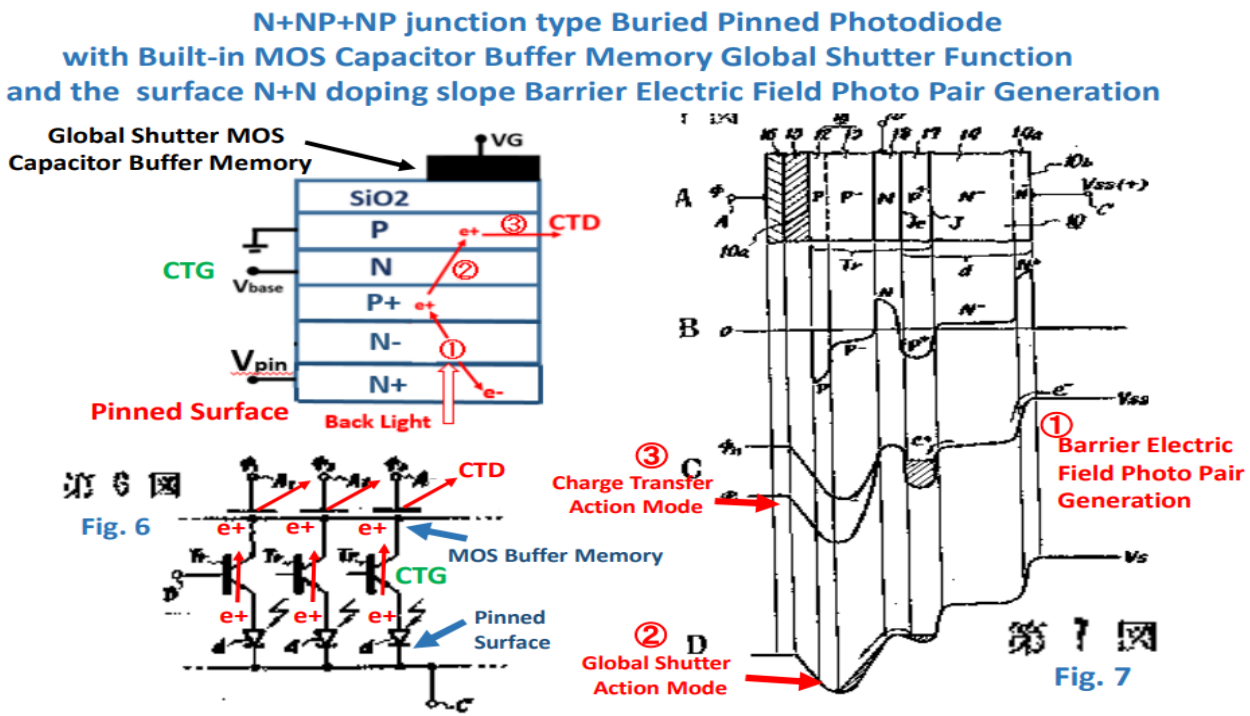
True History of Photodiode

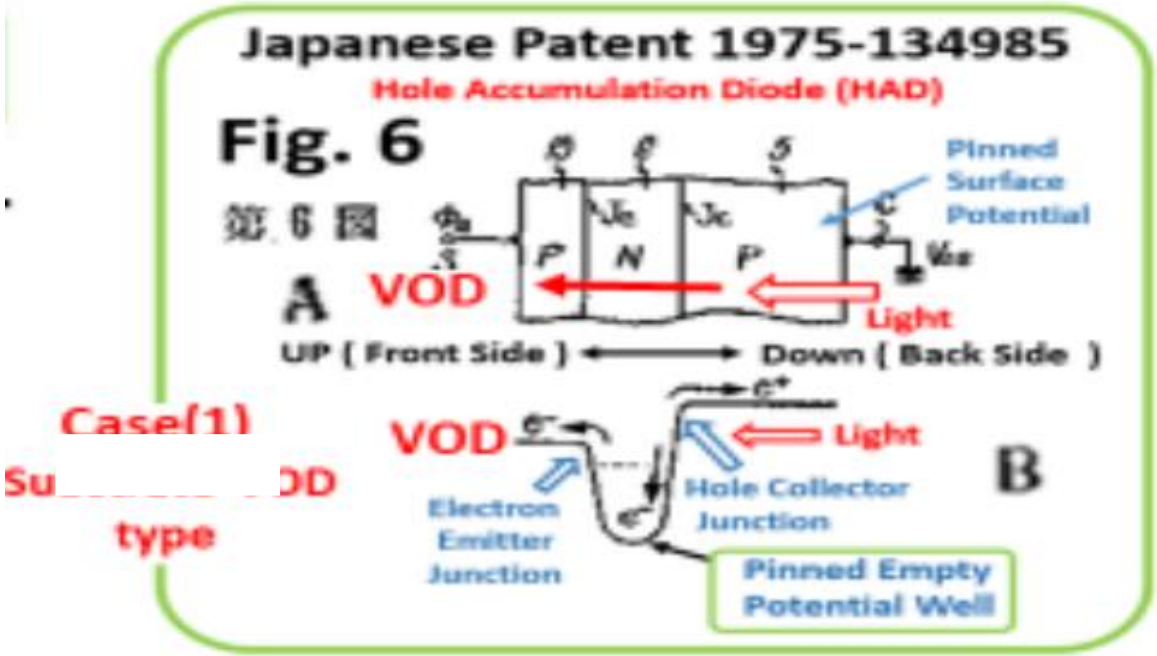
(1) Single Junction Type Dynamic Photodiode before 1970

(2) CCD/Mos type dynamic Photodiode invented in 1970

(3) Double Junction type Dynamic Photodiode invented by Philips in June 6, 1975

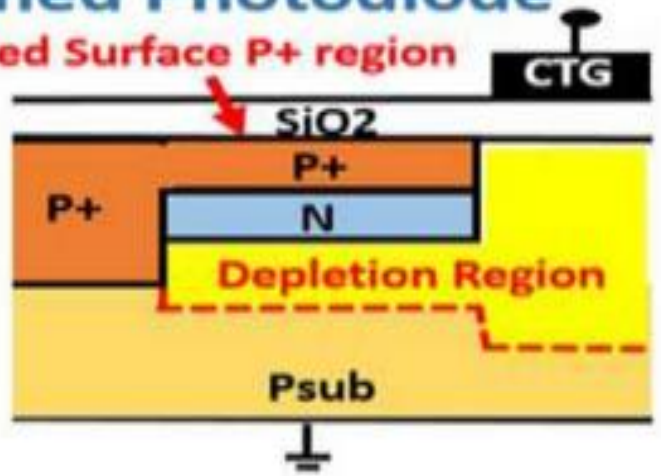
(4) Triple Junction type Dynamic Photodiode with the pinned surface invented by Sony in Oct 23, 1975.



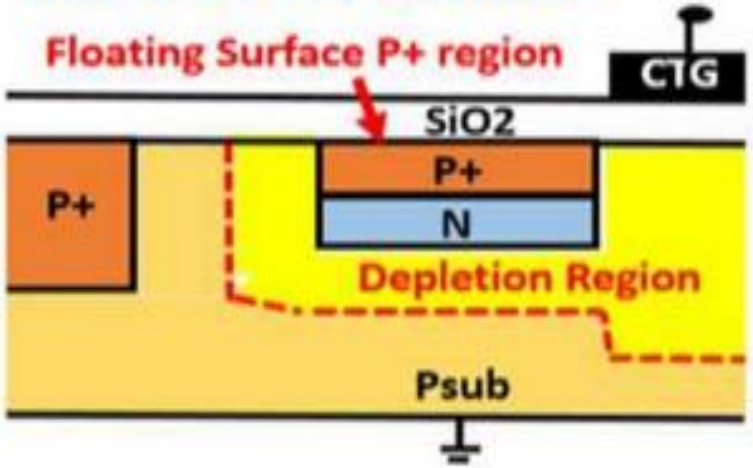


Comparison of Sony 1978, NEC 1982 and Kodak 1984 Photodiodes.

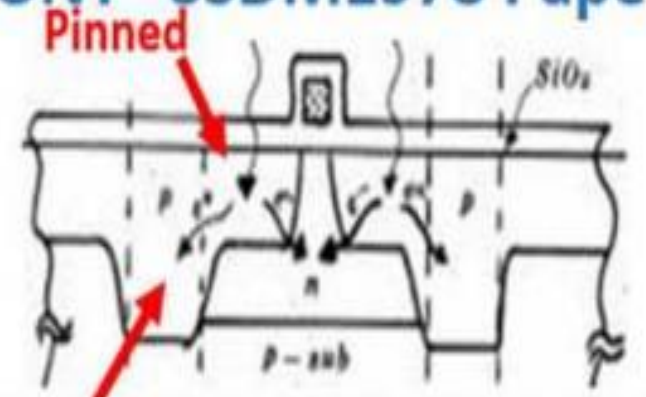
Pinned Photodiode



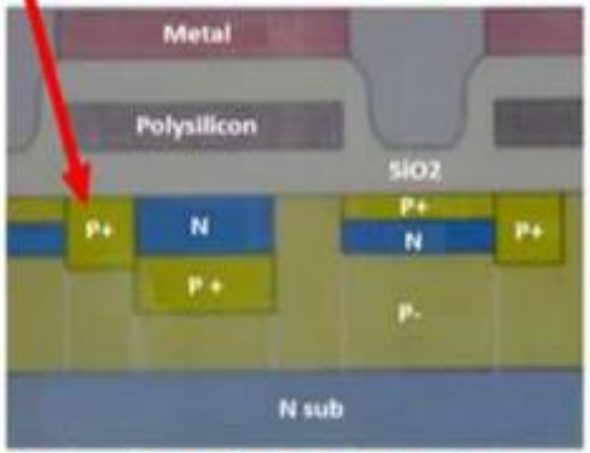
Buried Photodiode



SONY SSDM1978 Paper



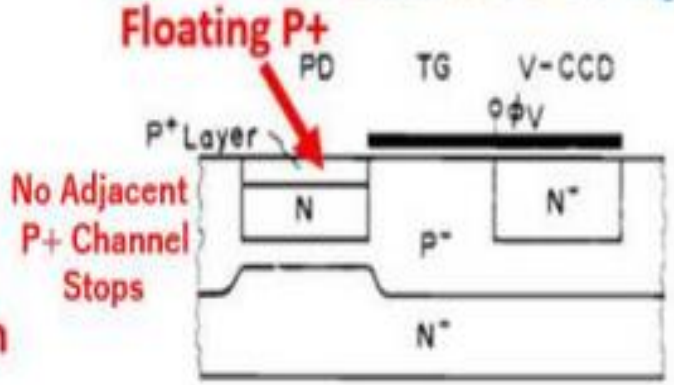
P+ Channel Stops and no Image Lag Problem

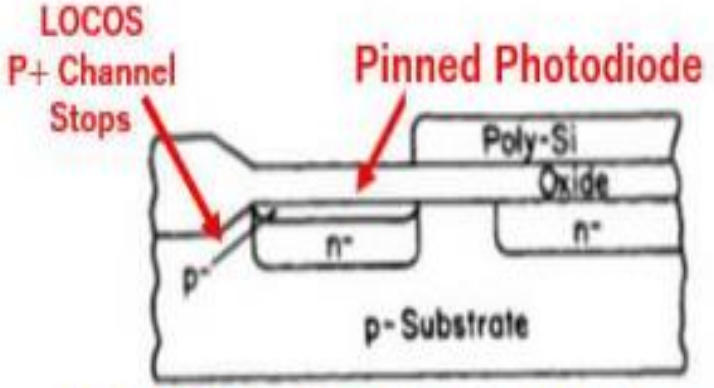


SONY 1987 HAD Sensor

Serious Image Lag Problem

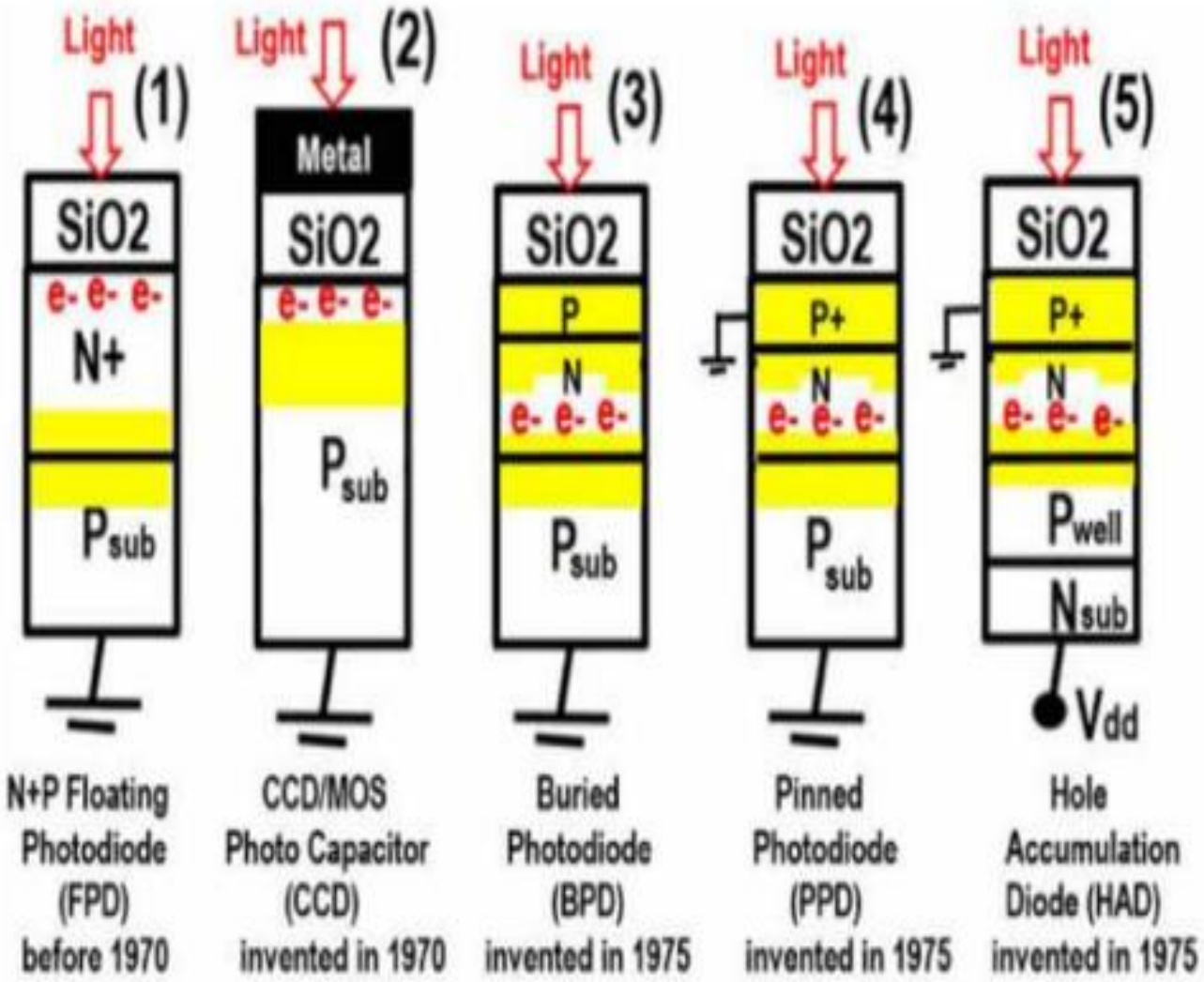
NEC IEDM1982 Paper



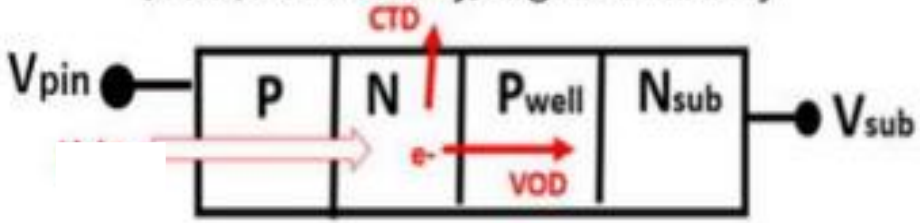


KODAK IEDM1984 Paper

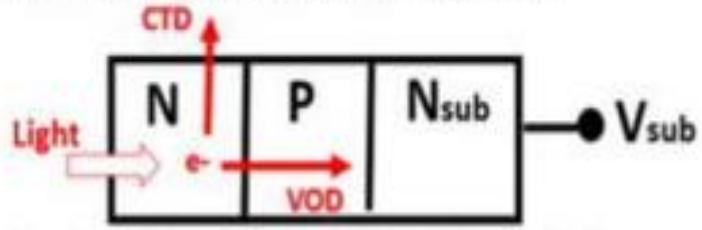
Historical Developments of Five types of Basic Photo Sensors Structures.



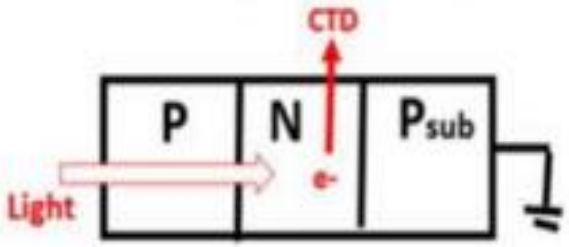
Triple Junction Pinned Photodiode on Substrate
JPA1975-134985 by Hagiwara at Sony



Floating Surface Double Junction Photodiode
JPA1978-1971 by Yamada at Toshiba

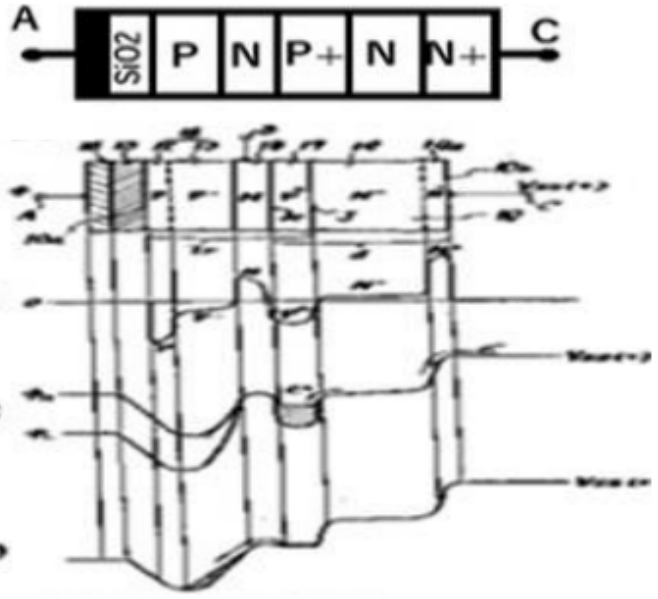


Floating Surface Double Junction Photodiode
JP1980-138026 by Teranishi et al at NEC

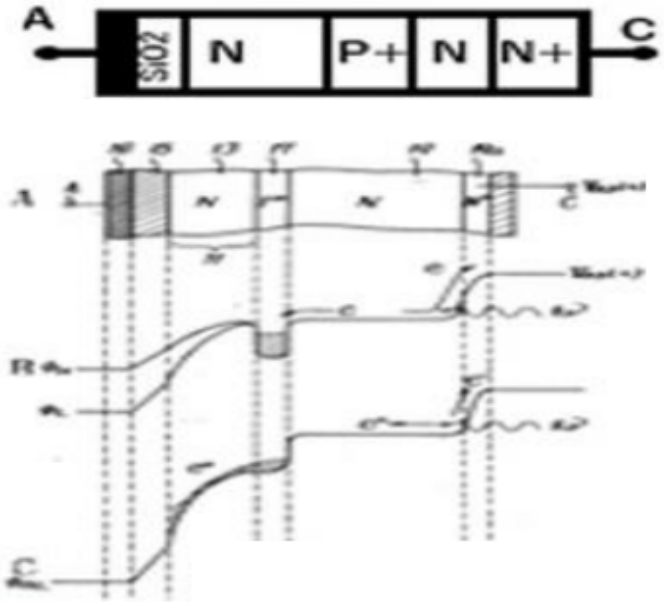


Who invented Pinned Photodiode ?

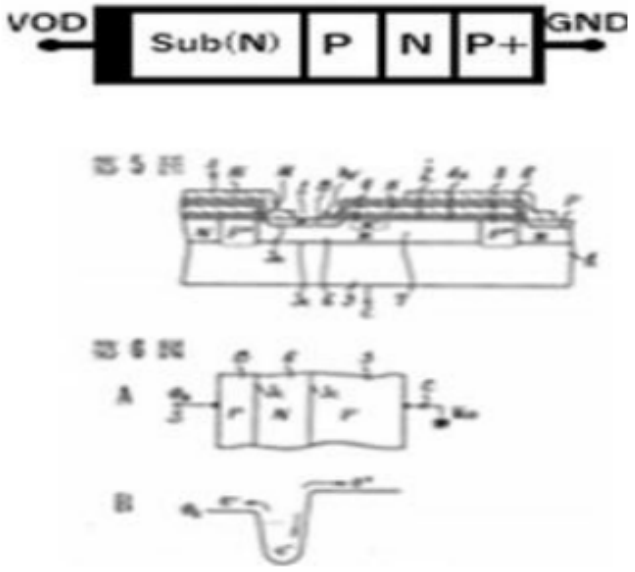
Hagiwara at Sony invented Pinned Photodiode in 1975. The evidence is give by the three Japanese patent applications, JPA1975-127646, JPA1975-127647 and JPA1975-134985. The first Pinned Photodiode was defined in October 23, 1975 as the N+NPNP triple junction(in Fig. 7 of JAP1975-127646) type and the N+NPN double junction type (in Fig. 7 of JAP1975-127647) type photodiodes with the N+ type pinned surface and the P type buried photo charge storage region with the complete charge transfer capability and the no-image-lag feature. The photo charge is transferred and drained to the CCD/MOS type charge storage buffer memory quicky by the strong punch-thru action. The second Pinned Photodiode was defined in November 10, 1975 as the PNP double junction (in Fig. 6 of JAP1975-134985) type photodiode with the vertical overflow drain action also with the complete charge transfer capability and the no-image-lag feature as evidence the empty potential well of the buried photo charge storage, completely depleted of the charge.



JPA1975-127646 Fig. 7



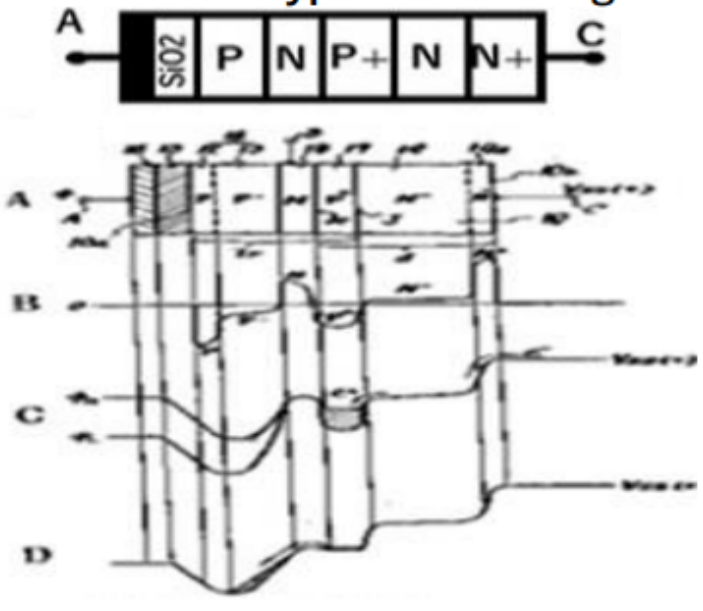
JPA1975-127647 Fig. 7



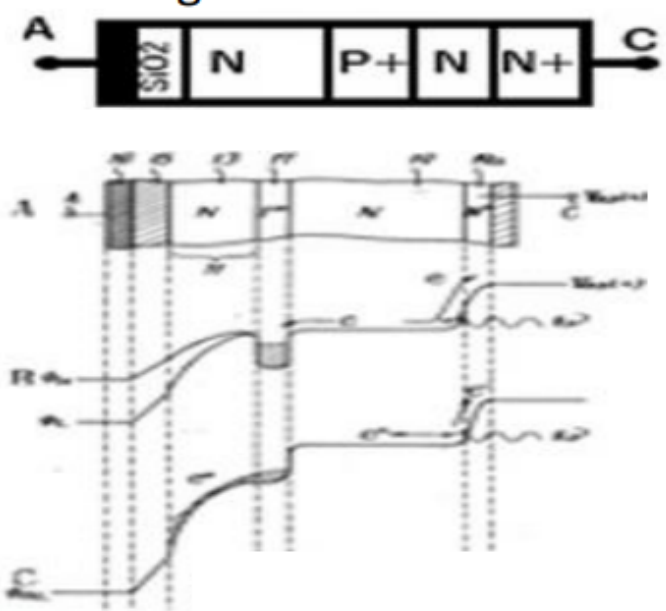
JPA1975-134985 Fig. 6

Who invented Electric Shutter ?

Hagiwara at Sony invented Electric Shutter in October 23, 1975. The evidence is give and explained in Fig. 7 of the Japanese patent application, JPA1975-127646, in which the first Electric Shutter function was defined. The photo charge is transferred and drained to the in-pixel buried channel type vertical overflow drain (VOD) region, which is defined as the buried channel region of the buried channel type CCD/MOS buffer memory capacitor. The three-voltage-level clocking scheme (Clock C and D) of the first Electric Shutter Function mode was defined in Fig. 7 of JPA1975-127646, using the strong punch-thru action mode between the buried P type photo charge storage region and the P-type in-pixel vertical overflow drain (VOD) region. The strong draining gate clock D voltage as shown by creates the very deep potential well in the in-pixel P-type buried vertical overflow drain (VOD) region in case of Fig. 7 of JPA1975-127646 while the strong draining gate clock C voltage creates the very deep potential well in the in-pixel surface N-type inverted region in case of Fig. 7 of JPA1975-127647.



JPA1975-127646 Fig. 7



JPA1975-127647 Fig. 7

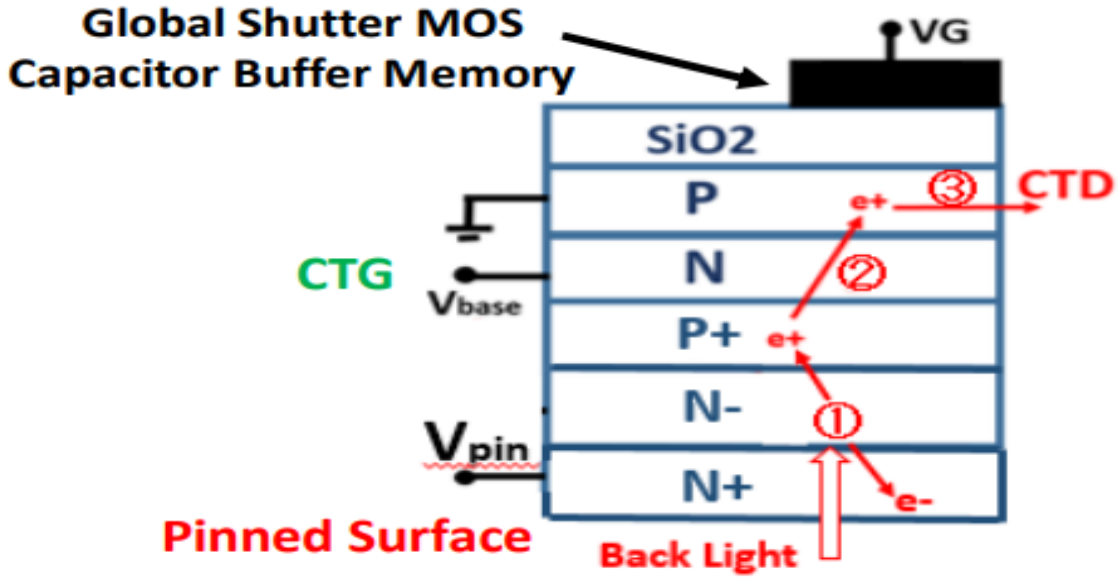
Hagiwara at Sony invented in 1975 the first Electric Shutter Function.

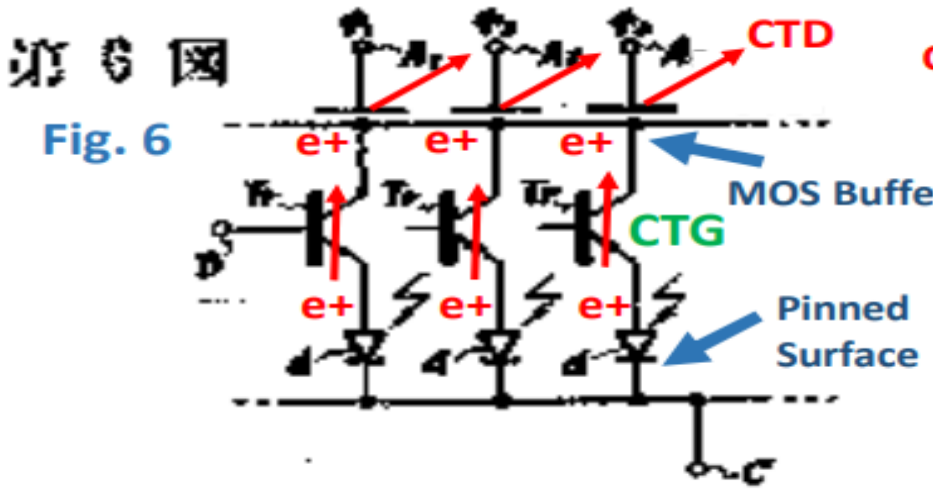
To achieve the complete Electric Shutter function, the surface of the photodiode must be pinned and fixed by the external constant voltage with the zero resistance.

The first Pinned Photodiode was invented by Hagiwara in 1975 to achieve the electric shutter function.

Japanese Patent 1975-127646

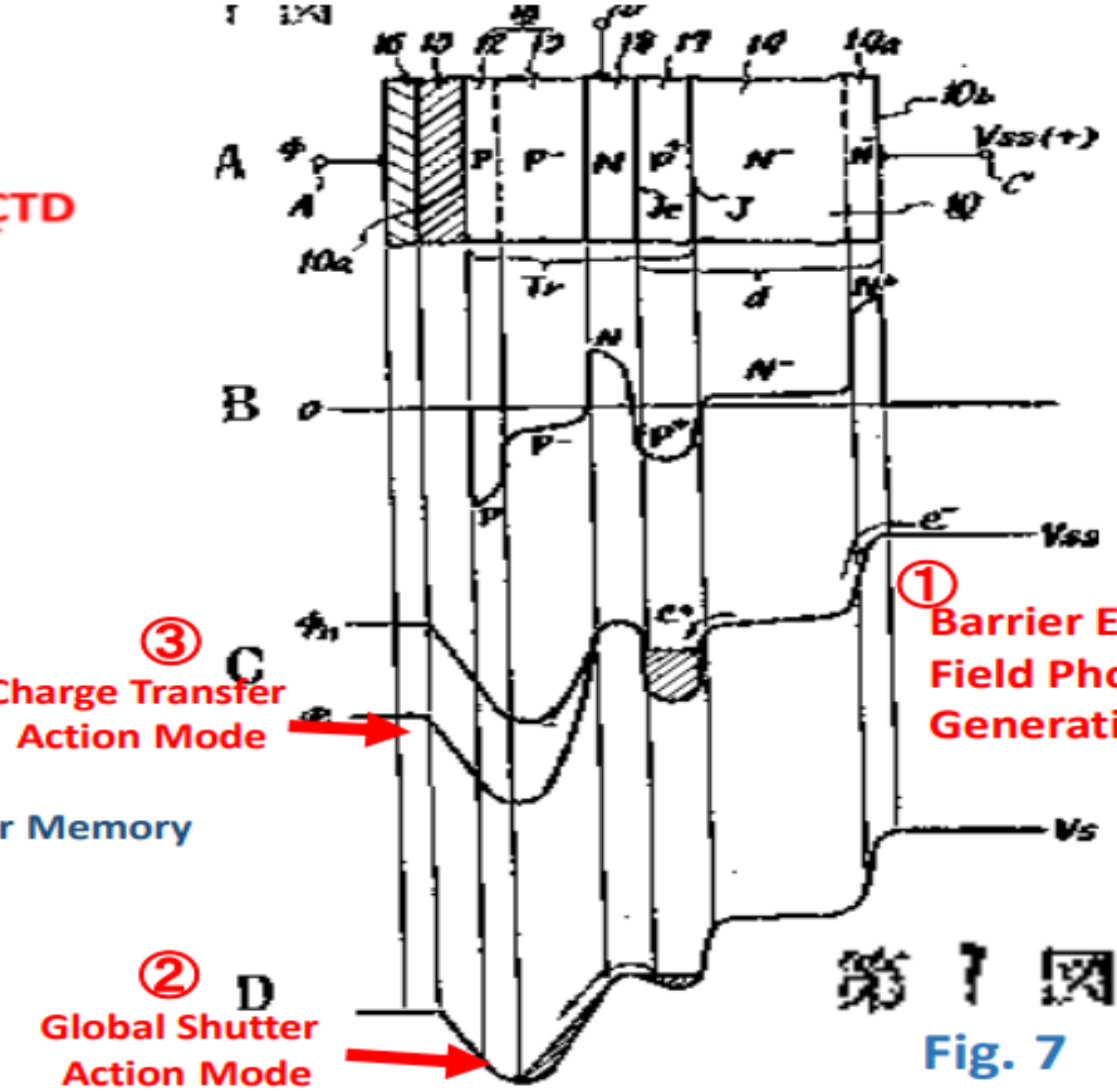
N+NP+NP junction type Buried Pinned Photodiode with Built-in MOS Capacitor Buffer Memory Global Shutter Function and the surface N+N doping slope Barrier Electric Field Photo Pair Generation





第 6 図

Fig. 6

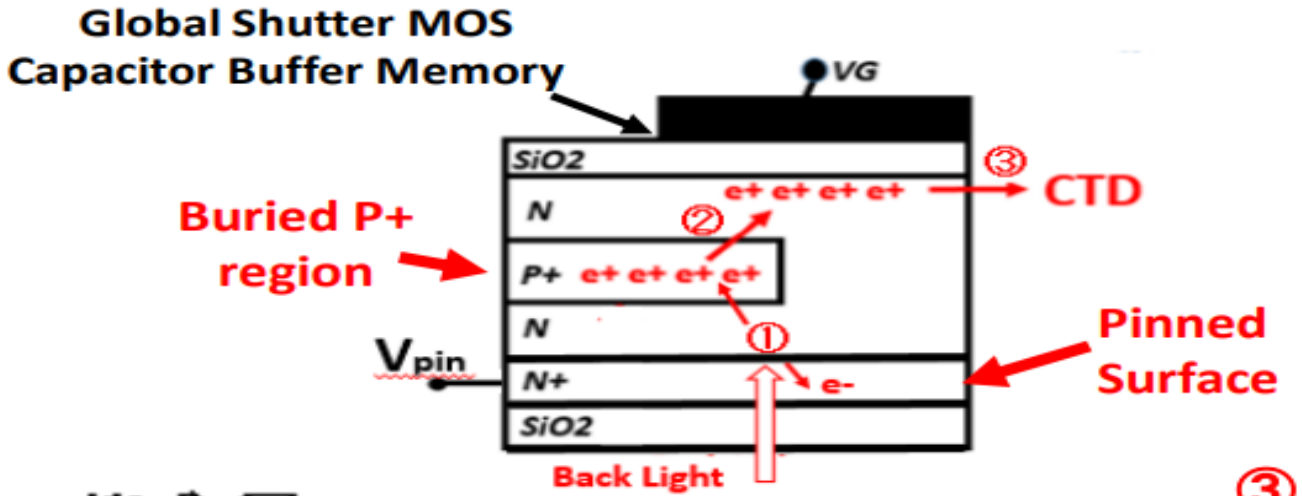


第 7 図

Fig. 7

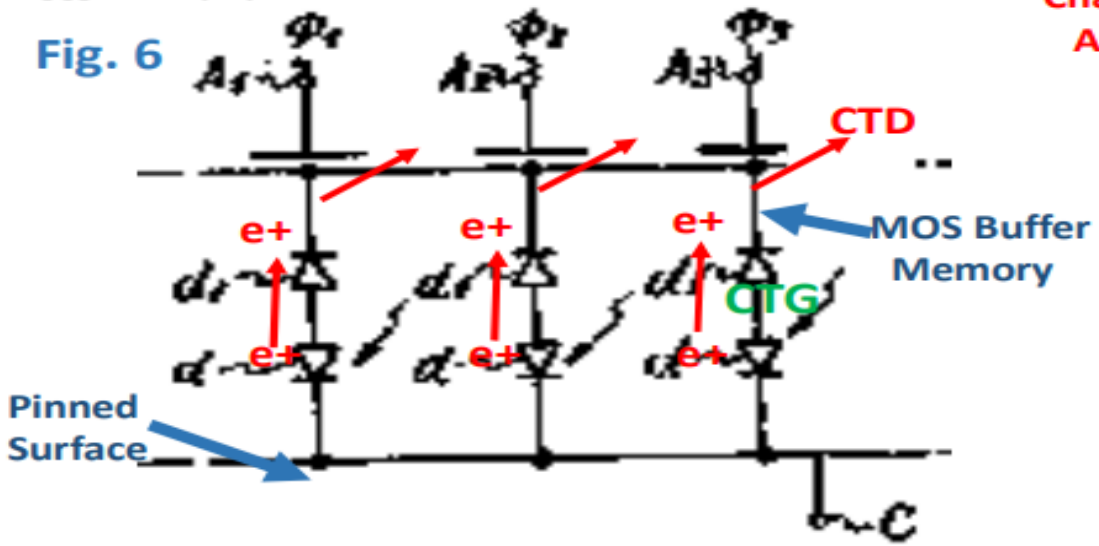
Japanese Patent 1975-127647

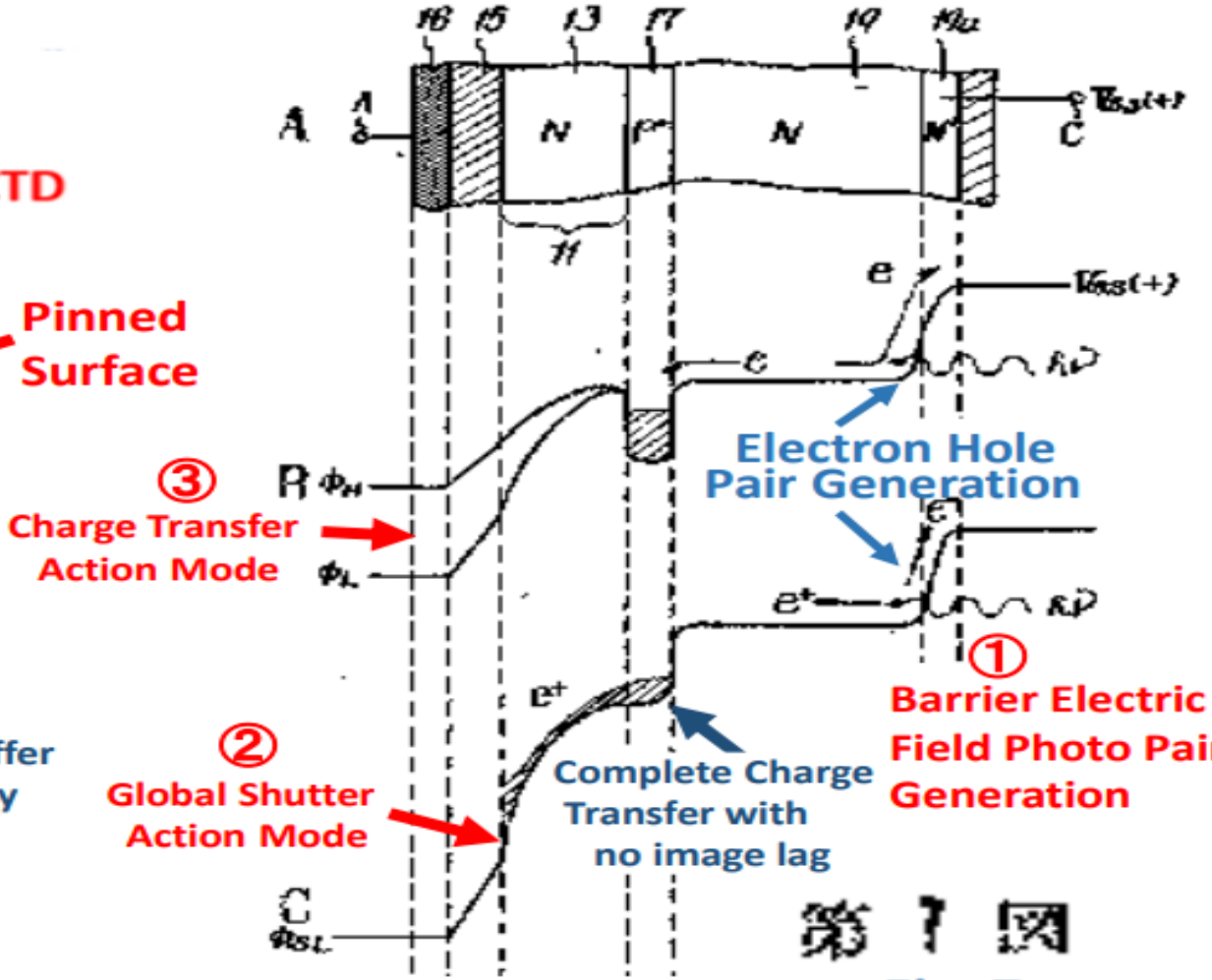
N+NP+N junction Dynamic Photo Transistor type Buried Pinned Photodiode with Built-in MOS Capacitor Buffer Memory Global Shutter Function and the surface N+N doping slope Barrier Electric Filed Photo Pair Generation



第 6 図

Fig. 6





第 7 図

Fig. 7

PNPN junction Transistor type Pinned Photodiode

Visit https://www.j-platpat.inpit.go.jp/ and put the patent number 1975-134985

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

Patent Claim in English Translation

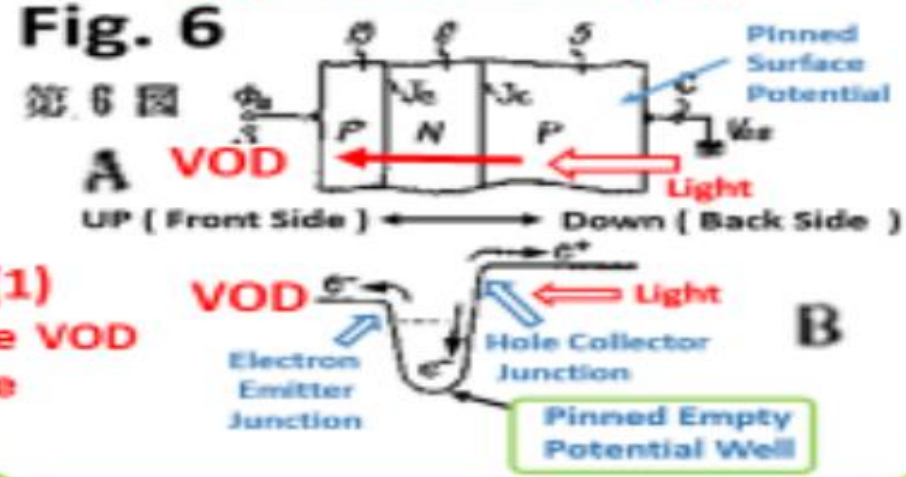
(1) In the semiconductor substrate (Nsub), the first region(P well) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N) is is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N) . And (6) Collector junction (Jc) is formed by the second region (N) and the first region (P well), forming a (PNP) transistor structure, (7) Photo charge is stored in the Base (N) according to illuminated light intensity and transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.

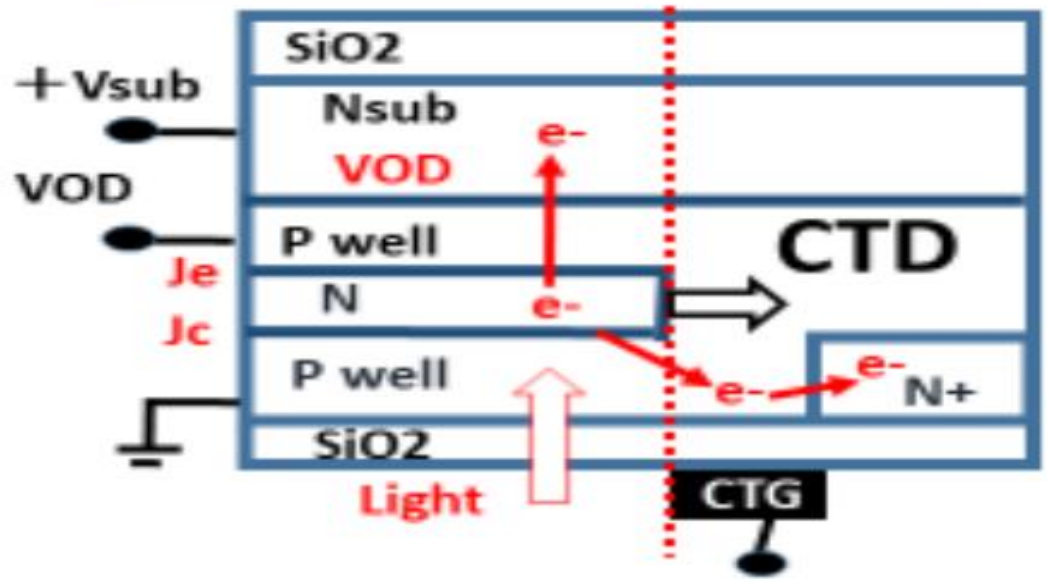
Fig.6 shows that this is also the invention of the in pixel VOD (vertical overflow drain).

Japanese Patent 1975-134985

Hole Accumulation Diode (HAD)

Fig. 6





International Journal of Systems Science and Applied Mathematics
2021; 6(2): 55-76
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ISSN: 2575-5838 (Print); ISSN: 2575-5803 (Online)

Electrostatic and Dynamic Analysis of P+PNP Double Junction Type and P+PNPN Triple Junction Type Pinned Photodiodes

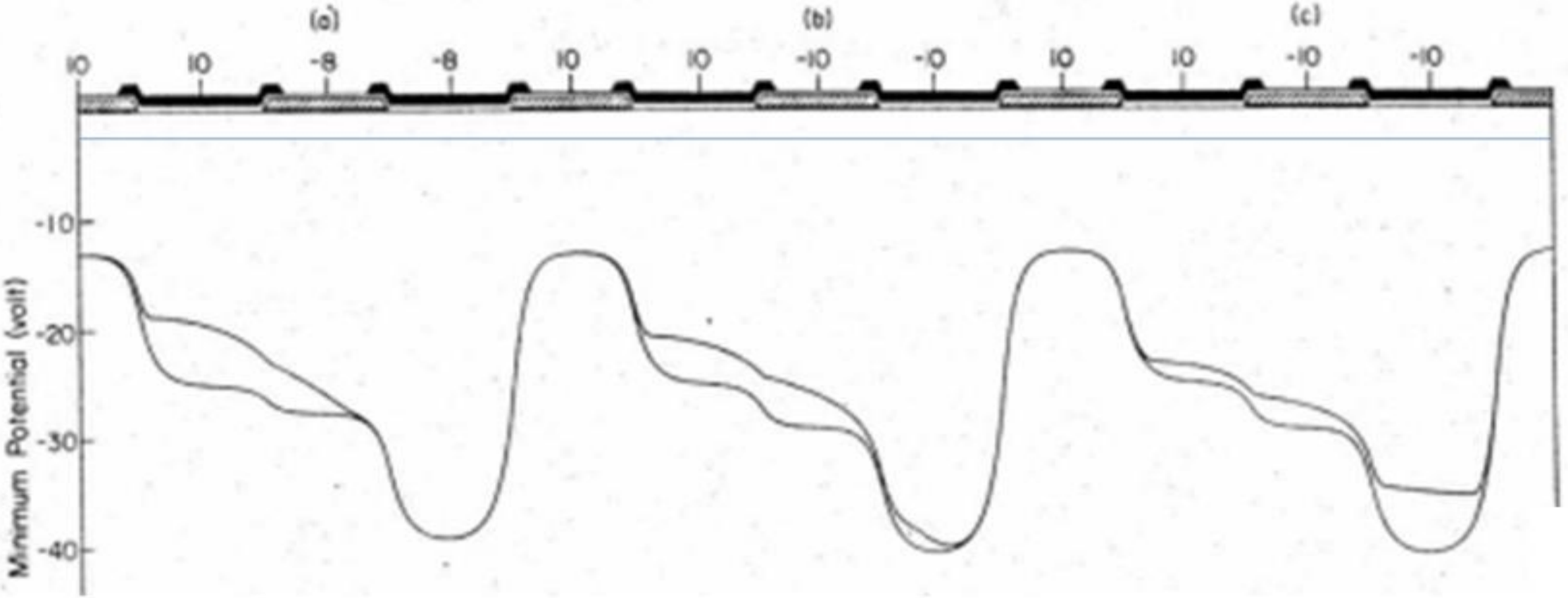
Yoshiaki Hagiwara

Artificial Intelligent Partner System (AIPS), AIP LAB, Atsugi City, Japan

Abstract: This paper explains the device structure and operation of image sensors and solar cells. Both are semiconductor devices operating with the same physical principle of detecting photons. A high efficiency of the photon to electron energy conversion is very much desired in both devices. Image sensors now use a very advanced and scaled down CMOS fabrication process technology to achieve high performance features such as the excellent short wave blue light sensitivity for good color reproduction, the low noise and the no image lag picture quality for filmless and mechanical free action cameras. On the other hand, solar cells are still now built with the primitive floating N+P single junction type photodiode to minimize the fabrication process cost but with very low energy conversion efficiency of about 20%. It is explained in details that the depletion region of the PN junction is not the only place where we can achieve photo electron and hole pair separations effectively. The short-wave blue light has only 1000 Å silicon crystal penetration depth. The pinned surface P+P Gaussian doping profile has a very important role to achieve a better photon to energy conversion efficiency, especially for the short-wave blue light. Electrostatic and dynamic behaviors of Pinned Surface P+PNP Double Junction type Dynamic Photo Transistor and Pinned Surface P+PNPN Triple Junction type Dynamic Photo Thyristor are analyzed in details. Both of them are shown to be expected to have much excellent photon-to-electron energy conversion efficiency.

Keywords: Pinned Buried Photodiode, Double Junction Dynamic Photo Transistor, Triple Junction Dynamic Photo Thyristor, Empty Potential Well, Rotary Shutter, Global Shutter, Surface Barrier Potential, Double Junction Type Solar Cell

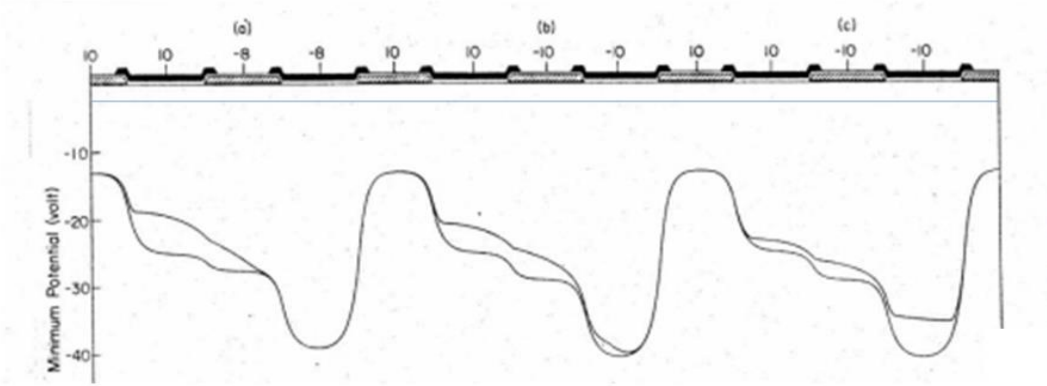
Exact Numerical Computer Simulation of Charge Transfer Action in Buried Channel CCD presented in ISSCC1974 by Yoshiaki Daimon-Hagiwara



for details see the PhD Thesis by Yoshiaki Daimon-Hagiwara on June 1975 from Caltech.

Caltech_1975_PhD_Thesis_Yoshiaki_Daimon_Hagihara.pdf

Exact Numerical Computer Simulation of Charge Transfer Action
in Buried Channel CCD presented in ISSCC1974 by Yoshiaki Daimon-Hagiwara



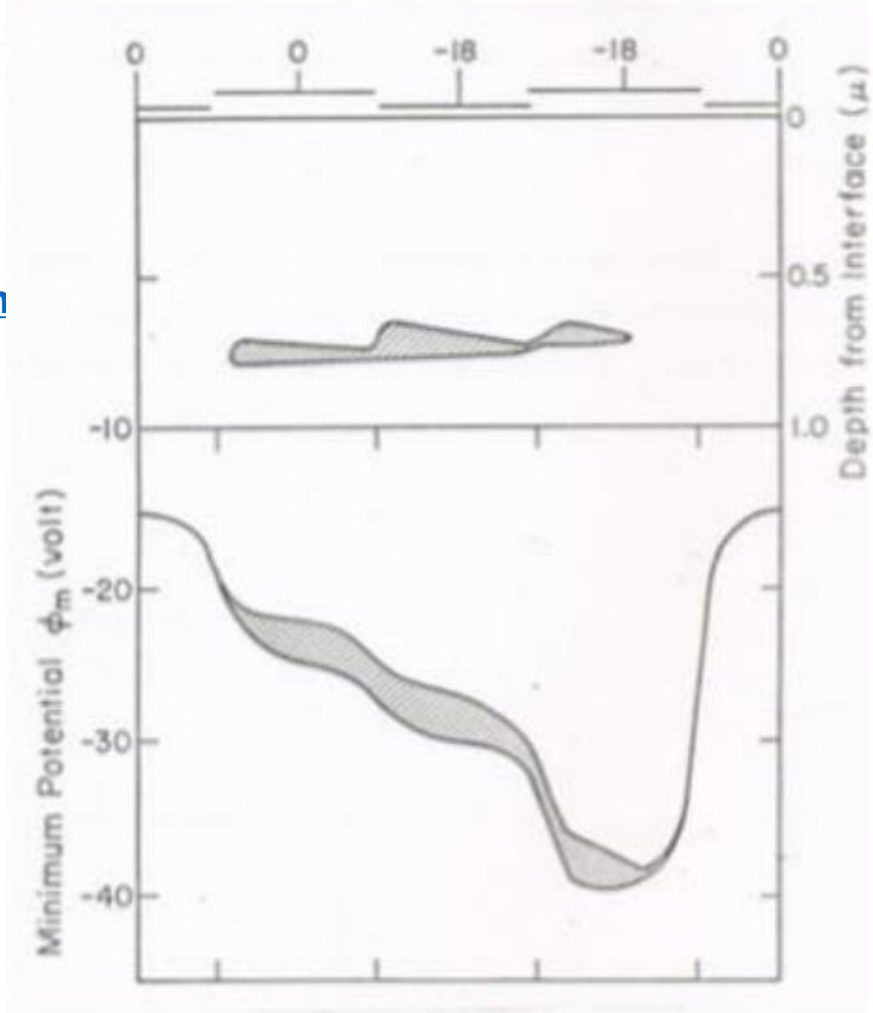
for details see the PhD Thesis by Yoshiaki Daimon-Hagiwara on June 1975 from Caltech.

[Caltech_1975_PhD_Thesis_Yoshiaki_Daimon_Hagih]



Prof. James McCaldin and Hagiwara

My PhD thesis paper
on buried channel CCD
at ISSCC1974, in Philadelphia, USA





Prof. T. C. McGill



Prof. C. A. Mead

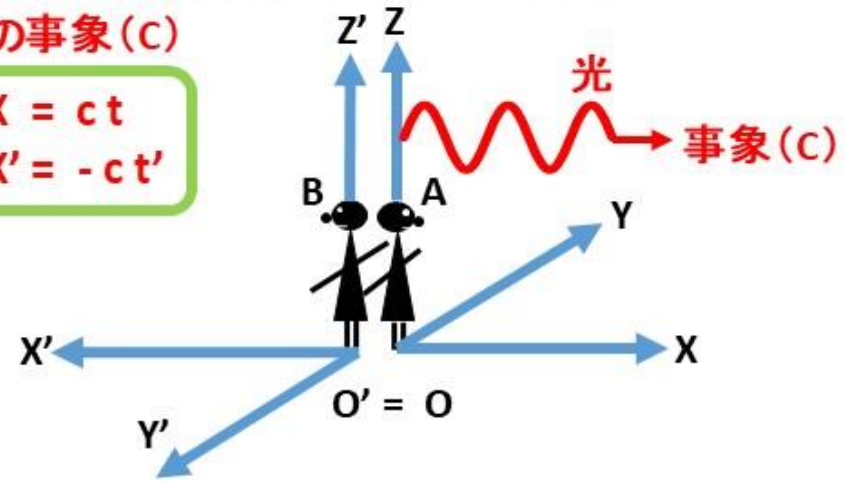
(1)座標系の定義

初期状態 $t = t' = 0$ の時

光の事象(C)

$X = ct$

$X' = -ct'$



座標系の相対性

$X = \alpha X' + \beta t'$
$Y = -Y'$
$Z = Z'$
$t = \gamma X' + \delta t'$

$X' = \alpha X + \beta t$
$Y' = -Y$
$Z' = Z$
$t' = \gamma X + \delta t$

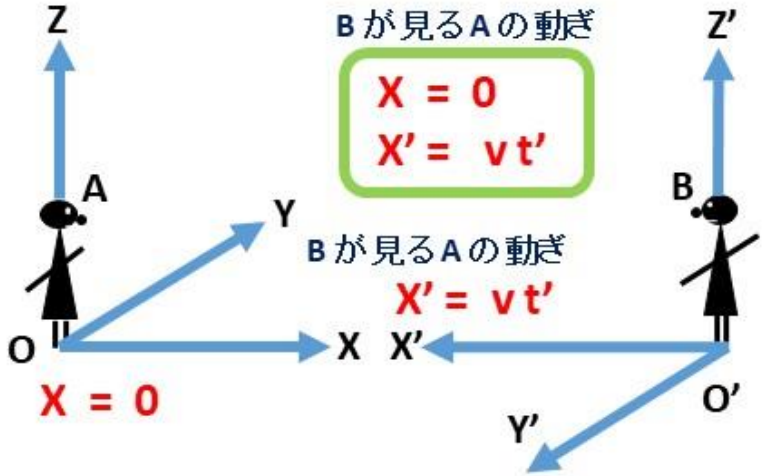
Bが見るAの動き

$X = 0$
$X' = vt'$

Aが見るBの動き

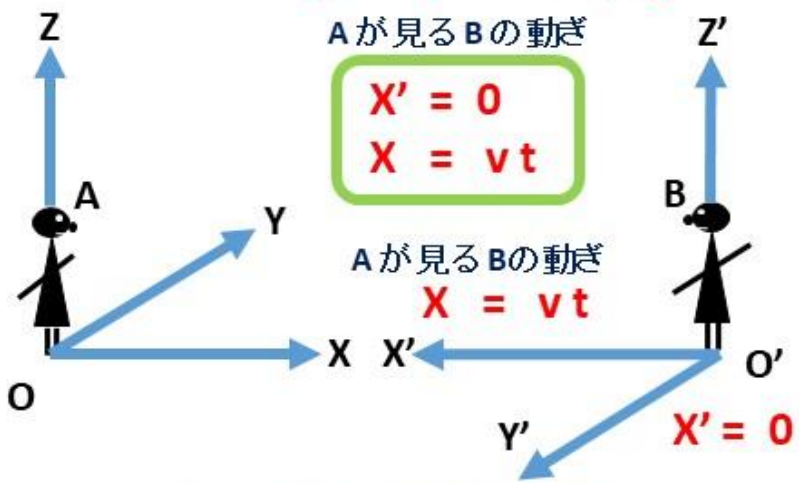
$X = vt$
$X' = 0$

$t > 0$ でかつ、$t' > 0$ の時

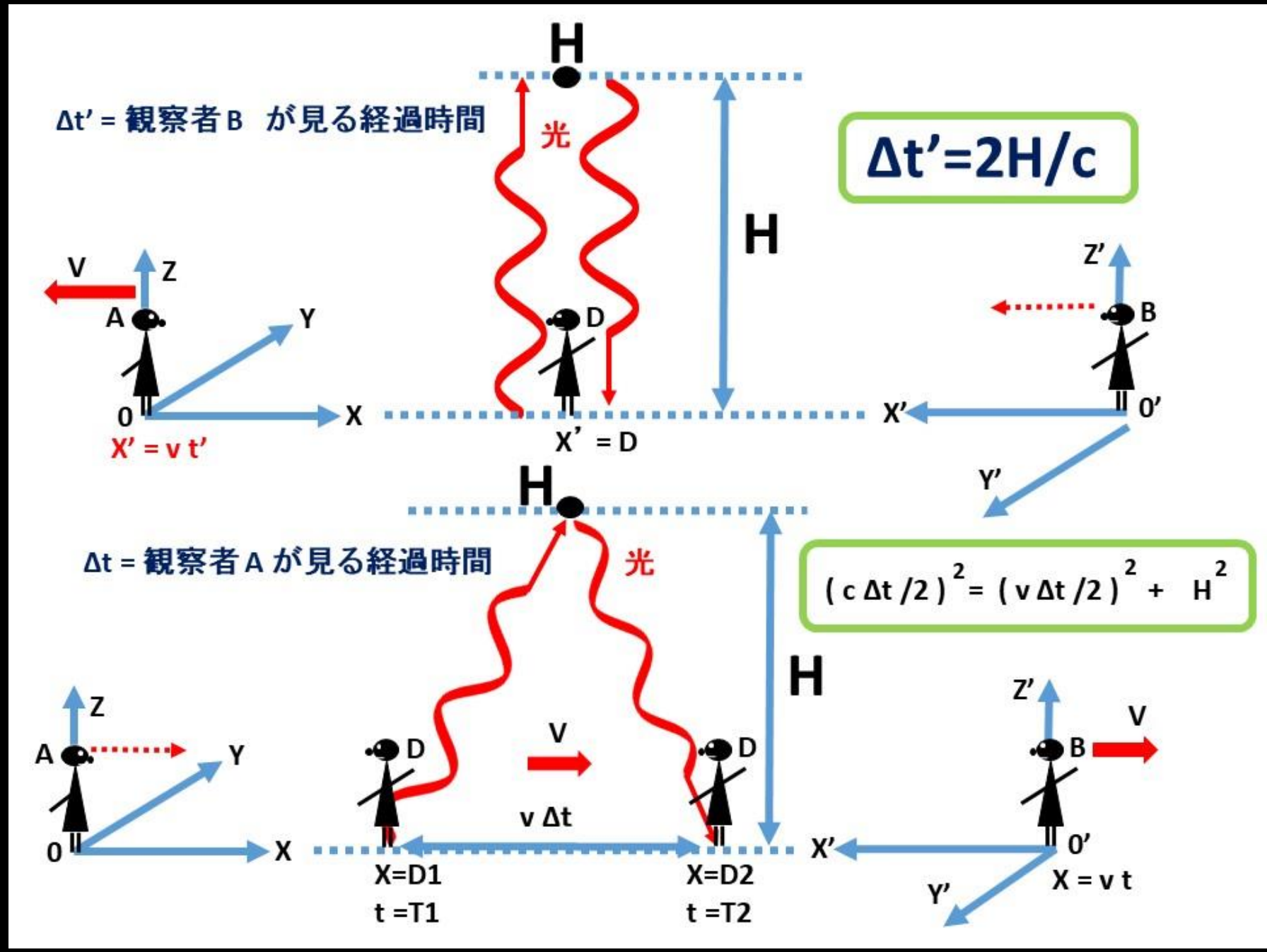


AとBは互いに離れて行く。

$t > 0$ でかつ、$t' > 0$ の時



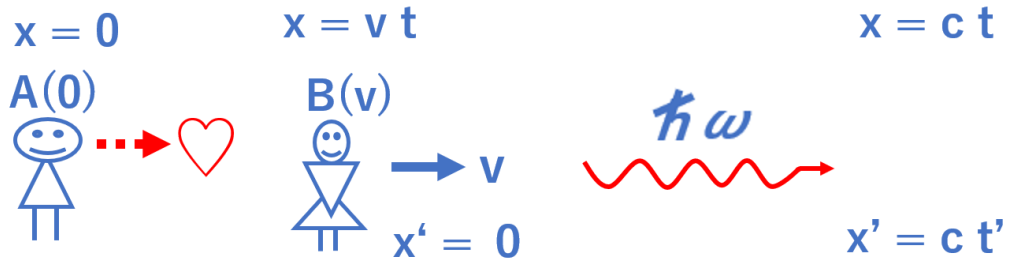
AとBは互いに離れて行く。


H
Δt' = 観察者 B が見る経過時間
光
H
Δt'=2H/c
V
Z
A
Y
0
X
X' = v t'
D
X' = D
Z'
B
X'
0'
Y'
H
Δt = 観察者 A が見る経過時間
光
(c Δt /2) 2 = (v Δt /2) 2 + H 2
H
Z
A
Y
0
X
D
V
v Δt
D
X=D1
t =T1
X=D2
t =T2
X'
Z'
B
V
0'
X = v t
Y'

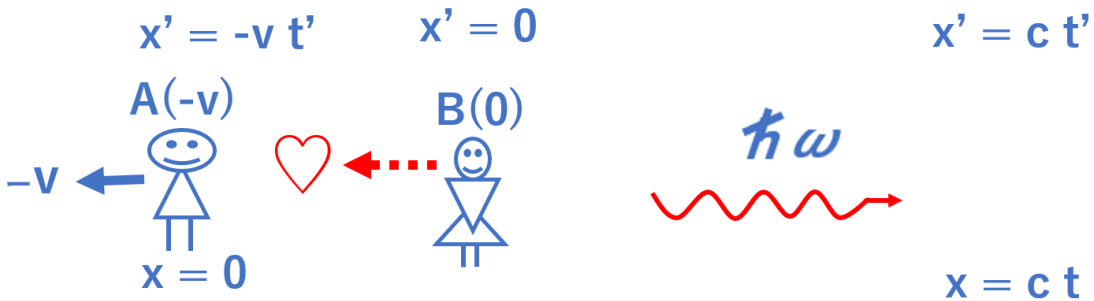
萩原良昭（AIPS）

中学の数学で解ける特殊相対性理論

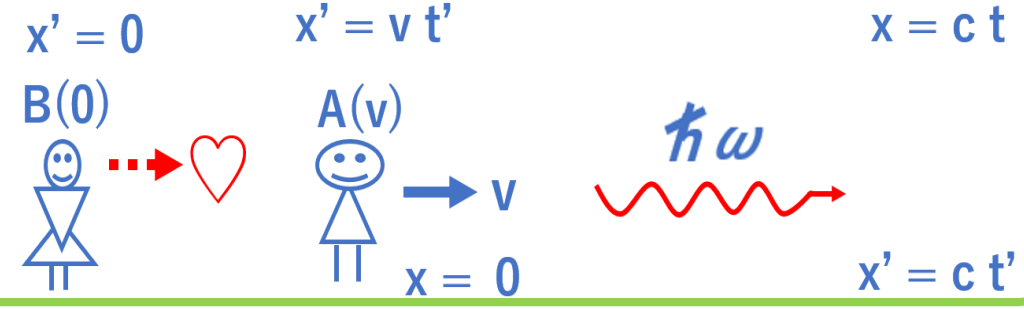
Case(1)



Case(2)



Case(3)



For Case(1) and Case (2) event

(10) $$x' = \beta\,(x - v\,t)$$
$$t' = \beta\,(t - v\,x/c^2)$$

For Case(1) and Case (2) event

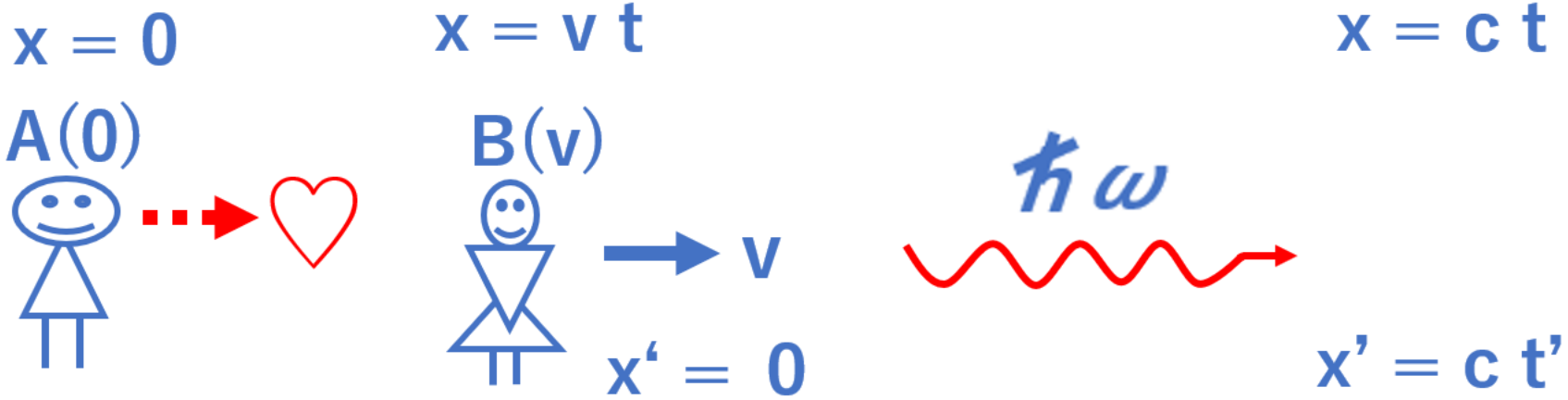
(12) $$x = \beta\,(x' + v\,t')$$
$$t = \beta\,(t' + v\,x'/c^2)$$

For Case(3) event only,
not valid for Case (1) and (2)

(11) $$x' = \beta\,(x + v\,t)$$
$$t' = \beta\,(t + v\,x/c^2)$$

(13) $$\beta = \frac{1}{\sqrt{1 - v^2/c^2}}$$

Case(1)



case A(0)B(v)

(1) $x' = \alpha t + \beta x$, $t' = \gamma t + \delta x$

(2) $0 = \alpha t + \beta v t$, $t' = \gamma t + \delta v t$

(3) $\alpha = -\beta v$

(4) $x' = \beta (x - v t)$, $t' = \gamma t + \delta x$

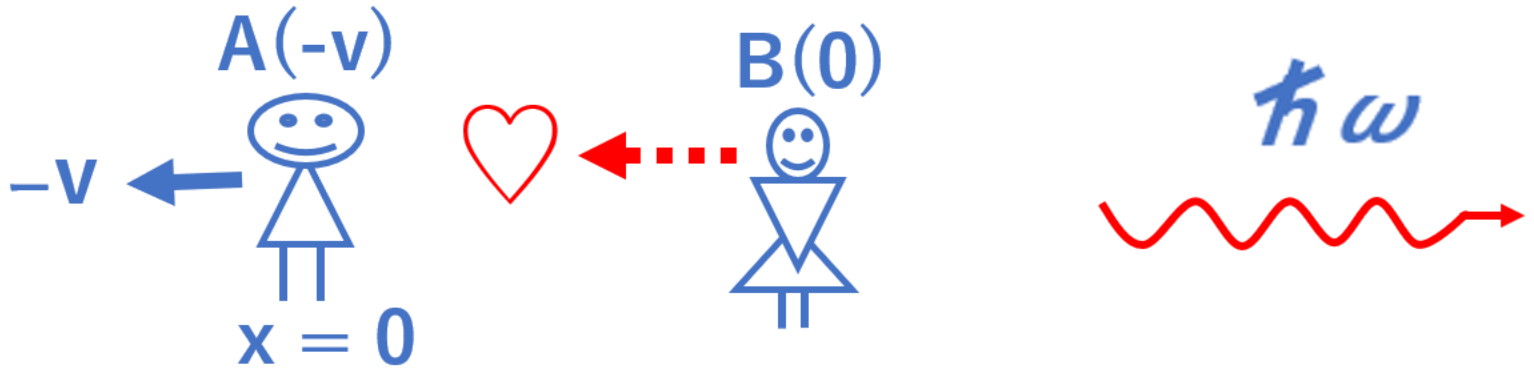
(5) $x = c t$ $x' = c t'$

$c t' = \beta (c t - v t)$, $t' = \gamma t + \delta c t$

(6) $(1 - v/c)\beta = (\gamma + \delta c)$

Case(2)

$x' = -v\,t'$ $\quad x' = 0$ $\quad x' = c\,t'$



(4)

$x' = \beta\,(x - v\,t)$

$t' = \gamma\,t + \delta\,x$

(7) case B(0)A(-v)

$-v\,t' = -v\,\beta\,t$

$t' = \gamma\,t$

(8)

$\gamma = \beta$

(10)

$x' = \beta\,(x - v\,t)$

$t' = \beta\,(t - v\,x/c^2)$

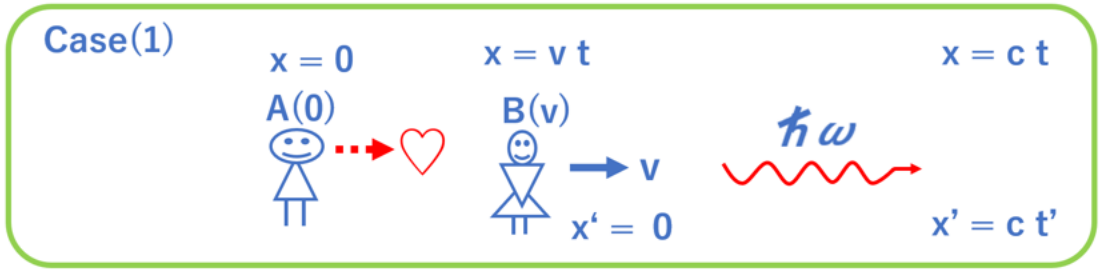
(9)

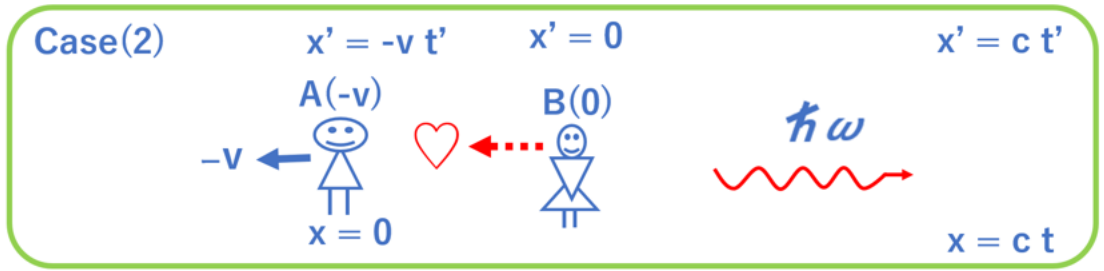
$\delta = -\beta\,v/c^2$

(6)

$(1 - v/c)\,\beta$

$= (\gamma + \delta\,c)$



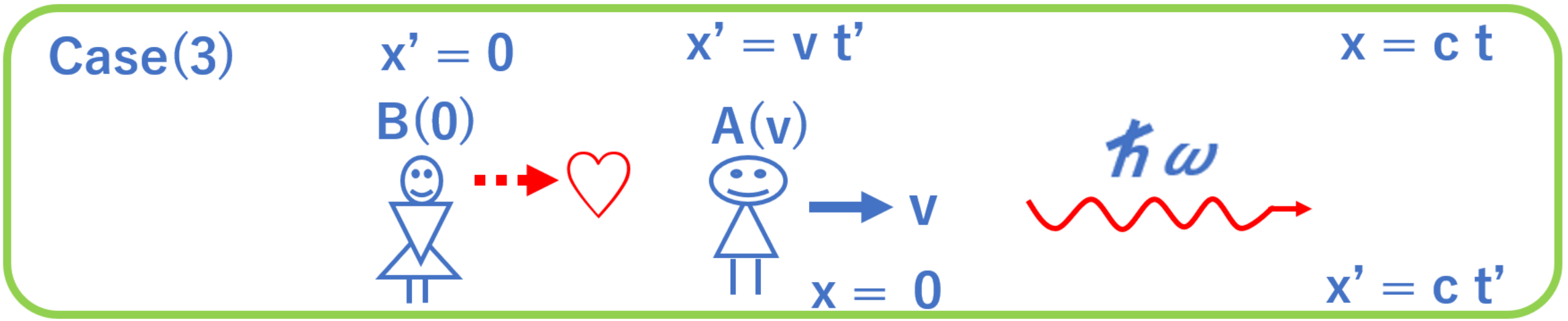


Case(1) and Case (2) describe the same event.

(10) For Case(1) and Case (2) event

$$x' = \beta\,(x - v\,t)$$
$$t' = \beta\,(t - v\,x/c^2)$$

Case (3) is a different event from Case (1) and (2).



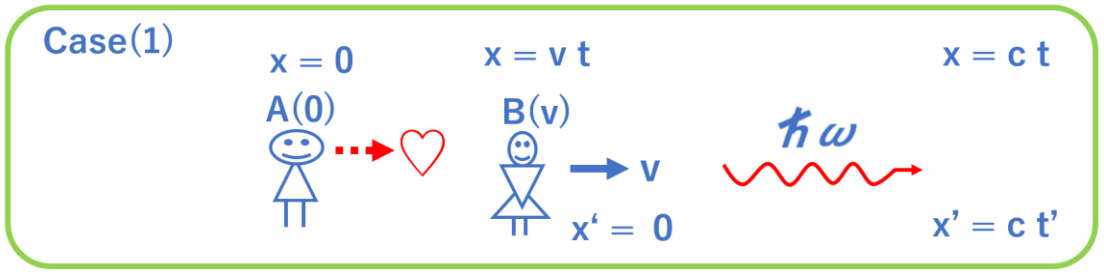
For Case(3)

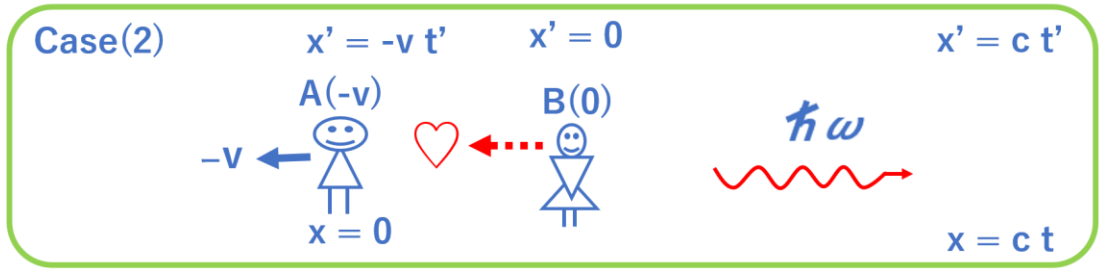
(11)
$$x' = \beta\,(x + v\,t)$$
$$t' = \beta\,(t + v\,x/c^2)$$

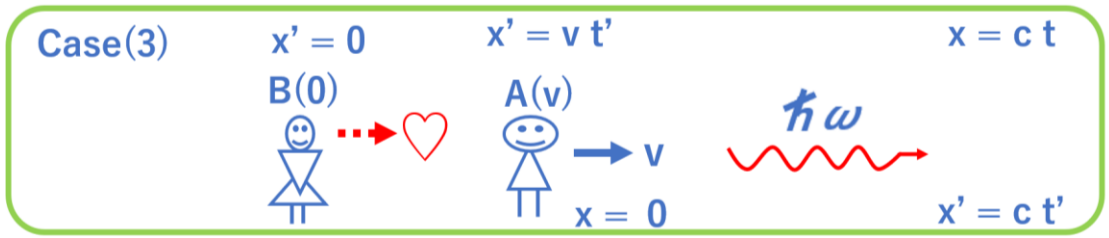
Exchange A and B to get Case(1) event

(12) For Case(1) and Case (2) event

$$x = \beta\,(x' + v\,t')$$
$$t = \beta\,(t' + v\,x'/c^2)$$







Case(1) and Case (2) describe the same event.

(10) For Case(1) and Case (2) event

$$x' = \beta\,(x - v\,t)$$
$$t' = \beta\,(t - v\,x/c^2)$$

Exchange A and B.

(12) For Case(1) and Case (2) event

$$x = \beta\,(x' + v\,t')$$
$$t = \beta\,(t' + v\,x'/c^2)$$

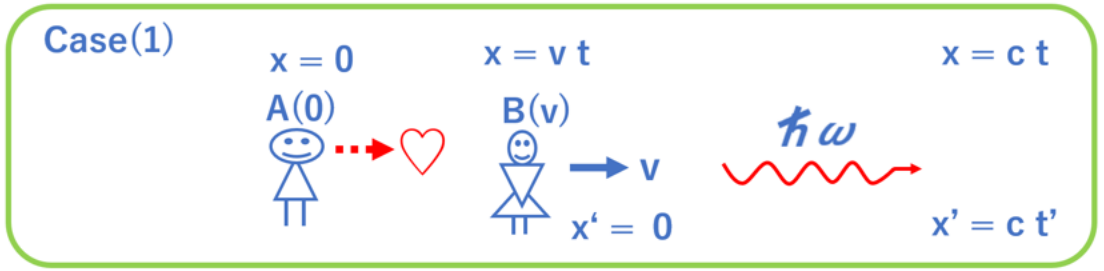
Case (3) is a different event from Case (1) and (2).

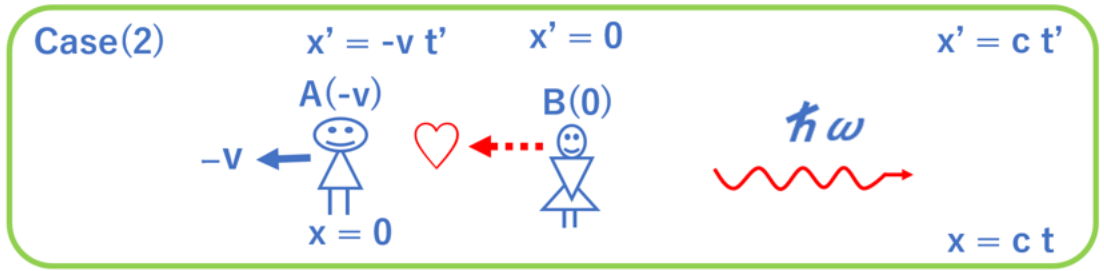
$$x' = \beta\,(\beta\,(x' + v\,t') - v\,\beta\,(t' + v\,x'/c^2)) = \beta^2\,(1 - v^2/c^2)\,x'$$
$$t' = \beta\,(\beta\,(t' + v\,x'/c^2) - v\,\beta\,(x' + v\,t')/c^2) = \beta^2\,(1 - v^2/c^2)\,t'$$

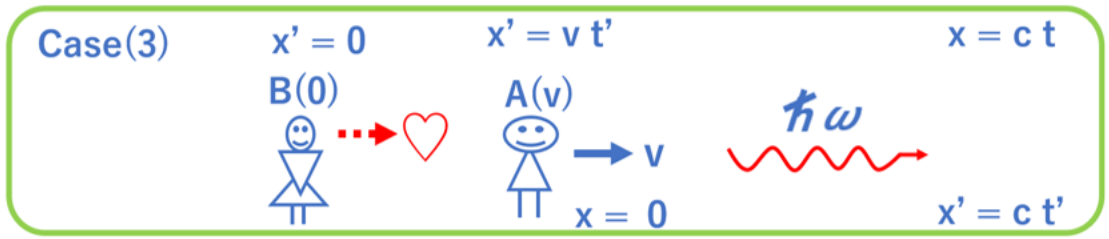
$$\beta^2\,(1 - v^2/c^2) = 1$$

(13)

$$\beta = \frac{1}{\sqrt{1 - v^2/c^2}}$$







(10)

$$x' = \beta (x - v t)$$
$$t' = \beta (t - v x / c^2)$$

(13)

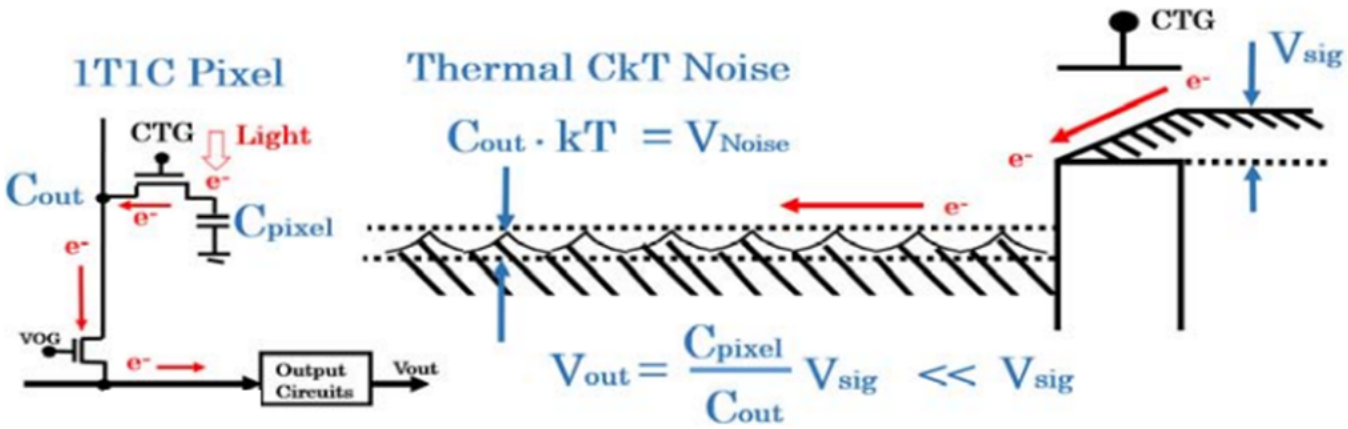
$$\beta = \frac{1}{\sqrt{1 - v^2 / c^2}}$$

True History of Photodiode

(1) Single Junction Type Dynamic Photodiode before 1970

(1) Single 接合型は残像が大問題だった。

わあ、最初から電子と光の総合物理現象や相対性理論の難しい物理学のお話になり、びっくりしたと思いますが怖がらないでください。数学の細かい計算は興味がありチャレンジ精神と意欲がある人が後で挑戦してもらえればそれで十分です。萩原がここで説明したい事は「現在の半導体産業の発展は、はるか１２０年以上前から、多くの科学者と技術者の努力の蓄積とその賜物によるとの事です。



1T1C type MOS Image Sensor with a Large Output Data Line Capacitance.

Arthur H. Compton (1892～1962), while at Washington University at St. Louis found that x-rays increase in wave length when scattered, which he explained in 1923 on the basis of the quantum theory of light.

●人間の心臓は１分間に約６０回鼓動します。これがだいたい１秒という時間単位に近い値です。
●次は光です。光の速度(c)はどこでも同じです。動いている人も、静止している人も一定値(c)を取ります。
　１秒間に進む光が進む距離(約地球をまわりを７周半）を基準にして、距離の単位が定義できます。
●光は速度が一定であるエネルギーの粒子です。光子(photon) と呼びます。光は電磁波でもあります。
　光は粒子の性質をだけでなく、波の性質を持ち、波長(λ)と周波数(f)の間には、 $c = \lambda f$ の関係があります。
●光は周波数(f)に比例するエネルギー量　$E = hf$ を持ちます。比例定数(h)をPlank定数と呼びます。
●光はまた３次元空間ベクトル量の運動量 $(P)_3 = h \cdot (K)_3 = h \cdot (Kx, Ky, Kz)$ を持ちます。
●光はまた４次元時空間 ベクトル量 $(光)_4 = h \cdot (f, Kx, Ky, Kz)$ を持つ４次元時空間粒子でもあります。
●重力のない宇宙空間の真空の中では、光は永遠に Wave Vector $(K)_3$ の定義する方向にまっすぐに進みます。
●宇宙空間にさまよう原子核に光子が遭遇しますと、電子と反電子のペアが生まれる場合があります。
●もとの光子には電荷量(Q)がありませんが生まれた電子は（－q）の電荷を、反電子は（＋q）の電荷を持ちます。
　電荷Qや質量Mや運動量P等には保存則が成立します。電子も反電子も光と同様に４次元時空間素粒子です。
●電子は正（プラス）の質量(+m)とエネルギー量$(+E = +mc^2)$と運動量$(+P)_3 = (+mV)_3$を持ちます。
　反電子は負（マイナス）の質量(－m)とエネルギー量$(-E = -mc^2)$と運動量$(-P)_3 = (-mV)_3$を持ちます。

$(電子)_4 = (E, Px, Py, Pz)$　$(反電子)_4 = (-E, -Px, -Py, -Pz)$　$E_o^2 = E^2 - c\,P^2$　$E = mc^2 = m_o c^2 + KE$

●原子核も光と同様に４次元時空間ベクトル物理量を持ち、原子核と光の相互作用でも保存則が成り立ちます。

$\Delta(原子核の４次元時空間ベクトル物理量の変化分)_4 = (光)_4 + (電子)_4 + (反電子)_4$

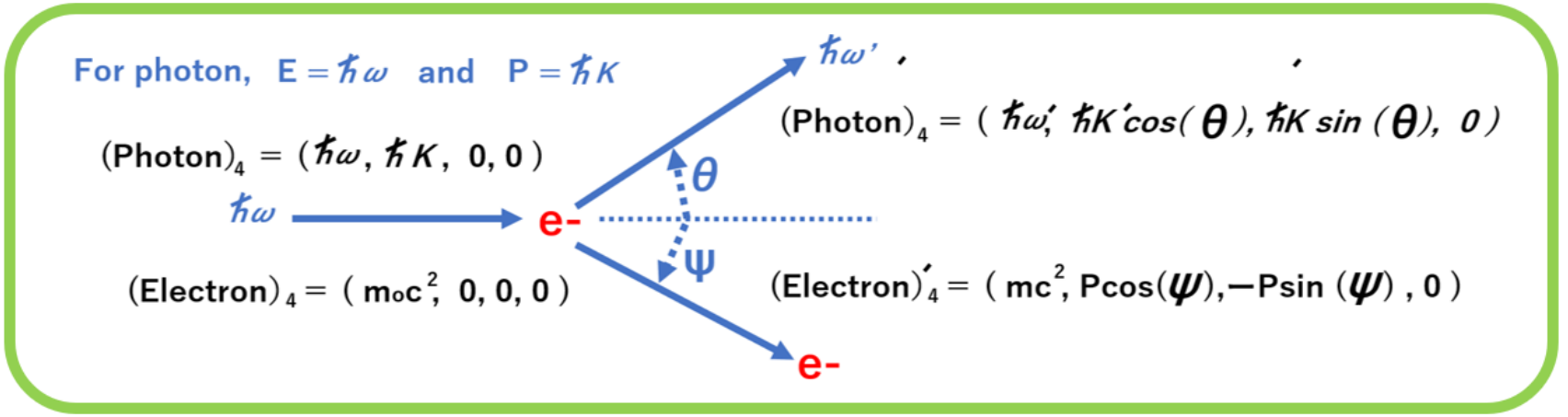
Arthur H. Compton (1892～1962), while at Washington University at St. Louis found that x-rays increase in wave length when scattered, which he explained in 1923 on the basis of the quantum theory of light.

(1) $E_o = m_o c^2$

For photon,

$E = \hbar\omega$ and $P = \hbar K$

$E^2 - c^2 P^2 = 0 \quad \omega = cK$



(2) $KE = \hbar\omega - \hbar\omega' = E - E_o = mc^2 - m_o c^2$

(3) $\omega t - Kx = K(ct - x)$ (4) $\omega = cK = 2\pi c/\lambda$

(5) $c = f\lambda = (2\pi f)(\lambda/2\pi) = \omega/K$

(6) $E^2 - c^2 P^2 = E_o^2$

$$\lambda' - \lambda = \frac{h}{m_o c}\{1 - \cos(\theta)\}$$

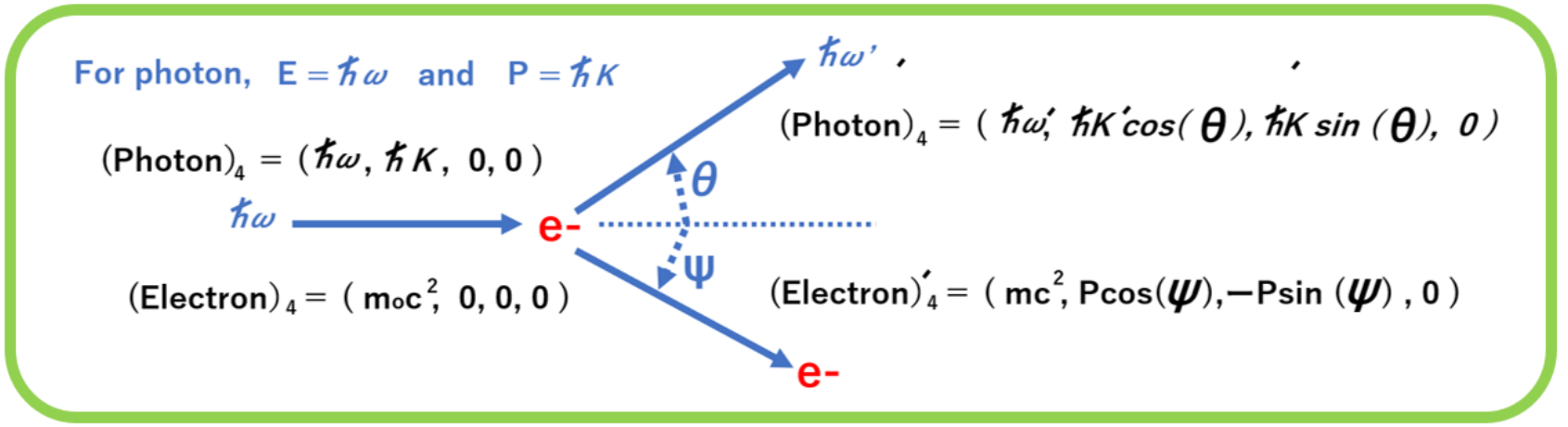
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(2) $KE = \hbar\omega - \hbar\omega' = E - E_o = mc^2 - m_o c^2$

(7) $E^2 = (KE + m_o c^2)^2 = m_o^2 c^4 + P^2 c^2$

(8) $P^2 c^2 = (KE)^2 + 2 m_o c^2 (KE)$

(9) $P^2 c^2 = (\hbar\omega - \hbar\omega')^2 + 2 m_o c^2 (\hbar\omega - \hbar\omega')$

(4) $\omega = cK = 2\pi c / \lambda$

(6) $E^2 - c^2 P^2 = E_o^2 = m_o^2 c^4$

$$\lambda' - \lambda = \frac{h}{m_o c}\{1 - \cos(\theta)\}$$

Arthur H. Compton (1892～1962), while at Washington University at St. Louis found that x-rays increase in wave length when scattered, which he explained in 1923 on the basis of the quantum theory of light.

$(\text{Light})_4 = \hbar \cdot (\omega, Kx, Ky, Kz)$ $\quad (\text{Electron})_4 = (E, Px, Py, Pz)$ $\quad E^2 - c^2P^2 = E_o^2$

(2) $KE = \hbar\omega - \hbar\omega' = E - Eo = mc^2 - m_oc^2 = m_oc^2\left[\dfrac{1}{\sqrt{1 - v^2/c^2}} - 1\right] \sim \dfrac{m_ov^2}{2}$ for $v << c$

(14)
$$\hbar K = \hbar K' \cos(\theta) + P\cos(\psi)$$
$$\hbar K' \sin(\theta) = P\sin(\psi)$$

(9) $P^2c^2 = (\hbar\omega - \hbar\omega')^2 + 2\,m_oc^2(\hbar\omega - \hbar\omega')$

(4) $\omega = cK = 2\pi c/\lambda$

(15) $P^2 = (\hbar K')^2 + (\hbar K)^2 - 2(\hbar K')(\hbar K)\cos(\theta)$ ⇒ $\lambda' - \lambda = \dfrac{h}{m_oC}\{1 - \cos(\theta)\}$

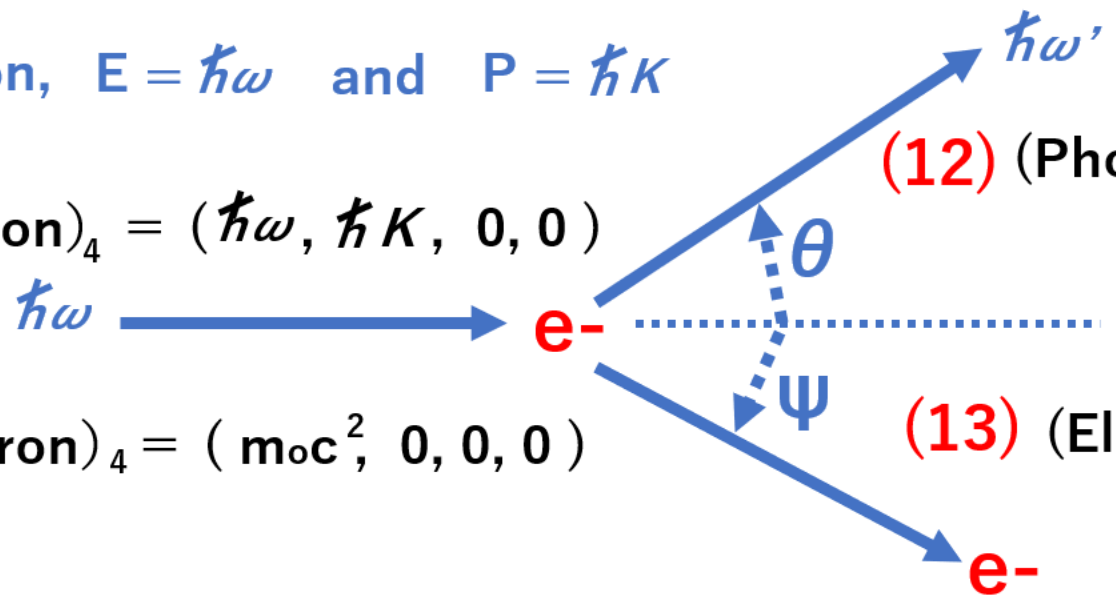
For photon, $E = \hbar\omega$ and $P = \hbar K$

(10) $(\text{Photon})_4 = (\hbar\omega, \hbar K, 0, 0)$

(11) $(\text{Electron})_4 = (m_oc^2, 0, 0, 0)$

(12) $(\text{Photon})'_4 = (\hbar\omega', \hbar K'\cos(\theta), \hbar K'\sin(\theta), 0)$

(13) $(\text{Electron})'_4 = (mc^2, P\cos(\psi), -P\sin(\psi), 0)$



Arthur H. Compton (1892～1962), while at Washington University at St. Louis found that x-rays increase in wave length when scattered, which he explained in 1923 on the basis of the quantum theory of light.

(9) $P^2c^2 = (\hbar\omega - \hbar\omega')^2 + 2\,m_oc^2(\hbar\omega - \hbar\omega')$

(16) $P^2 = (\hbar K - \hbar K')^2 + 2m_oc(\hbar K - \hbar K')$

(15) $P^2 = (\hbar K')^2 + (\hbar K)^2 - 2(\hbar K')(\hbar K)\cos(\theta)$

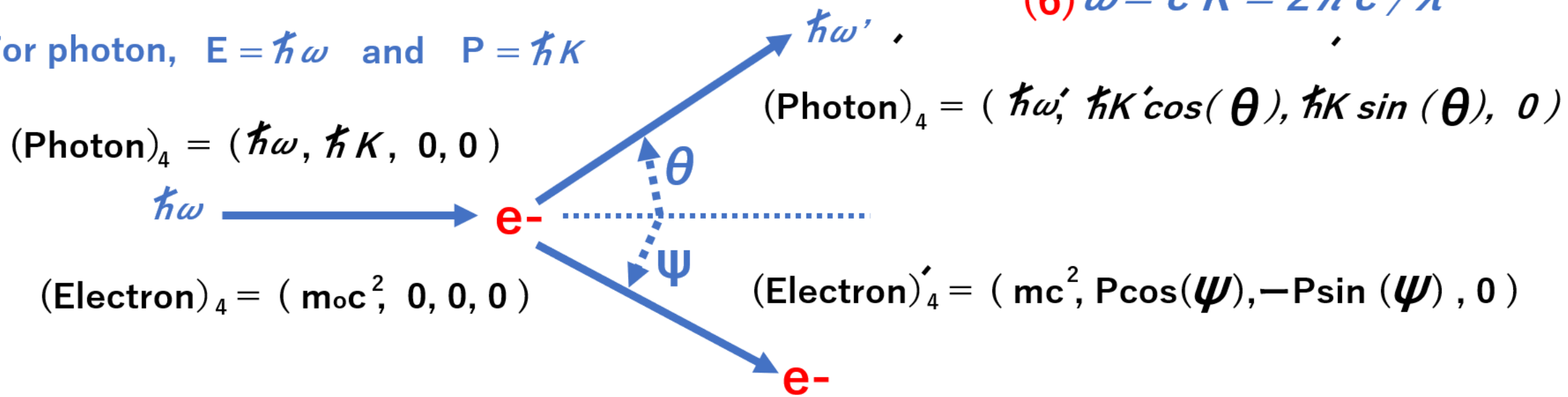
(17) $-2(\hbar K')(\hbar K) + 2m_oc(\hbar K - \hbar K') = -2(\hbar K')(\hbar K)\cos(\theta)$

(18) $m_oc(\hbar K - \hbar K') = (\hbar K')(\hbar K)\{1 - \cos(\theta)\}$

$$\lambda' - \lambda = \frac{h}{m_oc}\{1 - \cos(\theta)\}$$

(6) $\omega = cK = 2\pi c/\lambda$

For photon, $E = \hbar\omega$ and $P = \hbar K$



Arthur H. Compton (1892～1962), while at Washington University at St. Louis found that x-rays increase in wave length when scattered, which he explained in 1923 on the basis of the quantum theory of light.

$$\lambda' - \lambda = \frac{h}{m_o c}\{1 - \cos(\theta)\}$$

地球一周の距離 (外周)はおよそ4万Km

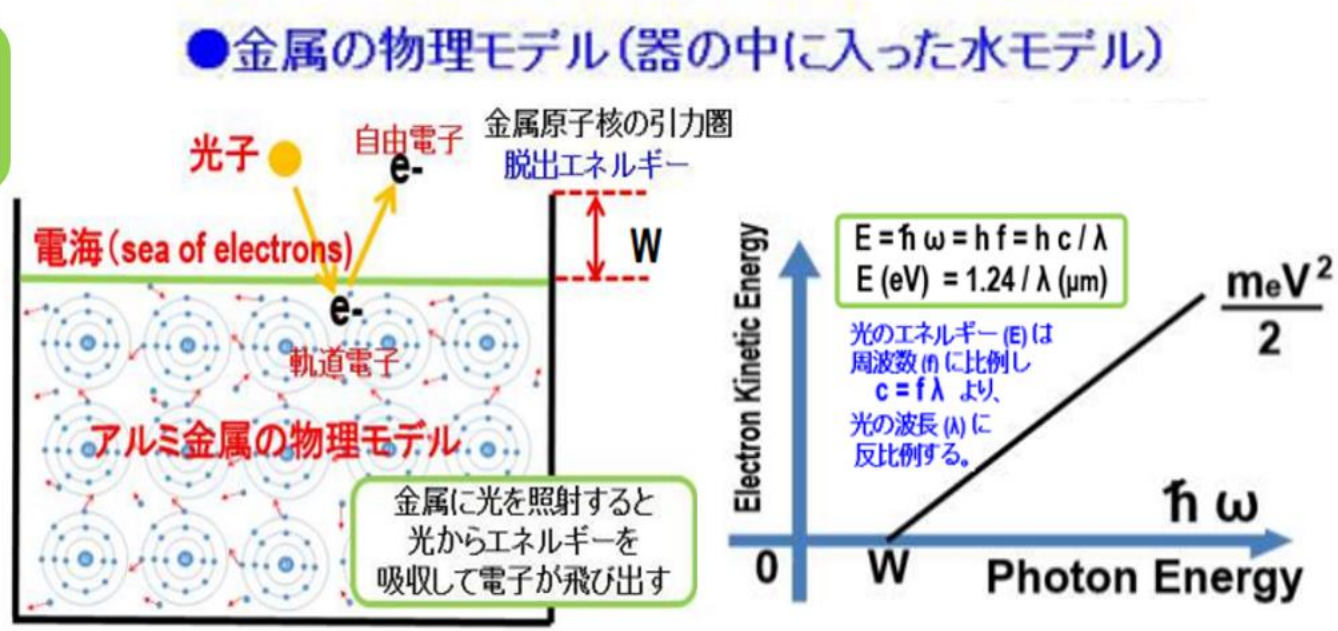
光の速度　$C = 2.99792458 \times 10^{10}$ cm/sec

Plank 定数　$h = 6.62606957 \times 10^{-34}$ Joule・sec

電子の質量　$m_e = 9.10938291 \times 10^{-31}$ kg

Joule = Newton・m = (Kg・m ・sec^{-2})・m

$\frac{h}{m_o c} = 0.02426310241$ Å (10^{-8} cm)



For photon,　$E = \hbar\omega$　and　$P = \hbar K$

$(\text{Photon})_4 = (\hbar\omega, \hbar K, 0, 0)$

$\hbar\omega$ → e- ,　θ

e- ,　ψ

$(\text{Electron})_4 = (m_o c^2, 0, 0, 0)$

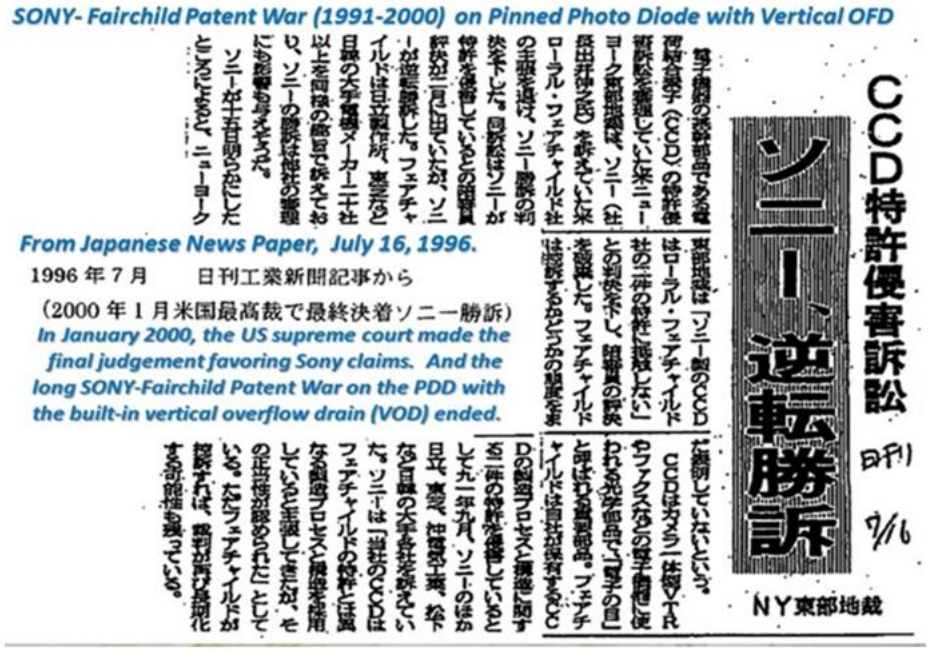
$\hbar\omega'$,

$(\text{Photon})_4 = (\hbar\omega', \hbar K' \cos(\theta), \hbar K \sin(\theta), 0)$

$(\text{Electron})'_4 = (mc^2, P\cos(\psi), -P\sin(\psi), 0)$

e-

SONY- Fairchild Patent War (1991-2000) on Pinned Photo Diode with Vertical OFD



CCD特許侵害訴訟

ソニー、逆転勝訴

NY東部地裁

From Japanese News Paper, July 16, 1996.

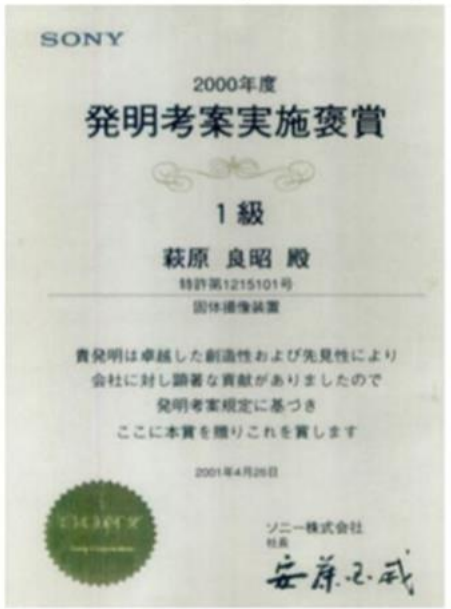
1996 年 7 月　日刊工業新聞記事から

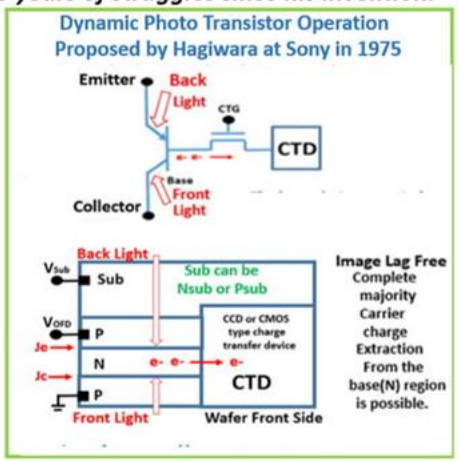
（2000 年 1 月米国最高裁で最終決着ソニー勝訴）

In January 2000, the US supreme court made the final judgement favoring Sony claims. And the long SONY-Fairchild Patent War on the PDD with the built-in vertical overflow drain (VOD) ended.

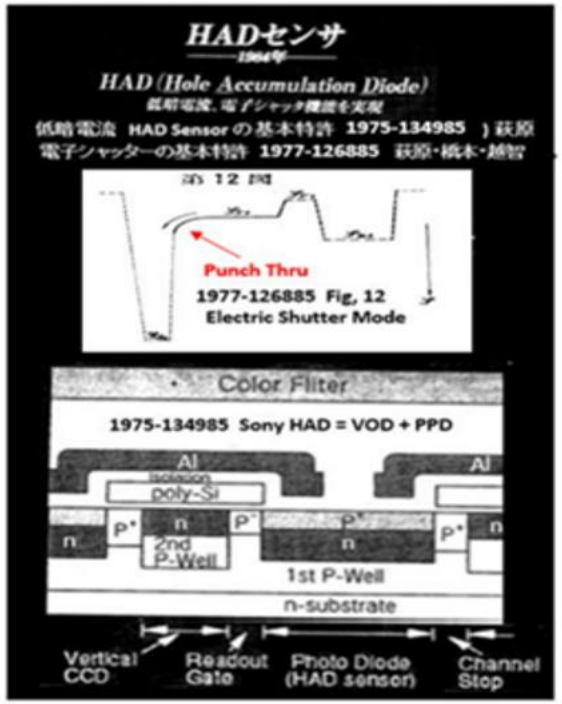
Finally the Sony-Fairchild Patent Wat(1991-2000) ended over the Sony HAD Sensor which is identical to the P+NPNsub junction type Pinned Photodiode with Vertical Overflow Drain, originally invented by Hagiwara at Sony in 1975.

And finally Hagiwara received for his 1975-134985 Japanese Patent officially , the First Patent Award from Mr. Ando, Sony president in April, 2001 after more 26 years of struggles since his invention.





Hagiwara also proposed the thyristor type punch-thru clocking scheme, synchronized with the TV scanning system to achieve the electric shutter.



Electric Shutter Basic Patent Award from Sony President Idei to Yoshiaki Hagiwara for Japanese Patent 1977-126885 by Hagiwara



Four Japanese Patent Applications on Pinned Photodiode with Electric Shutter Function and the in-Pixel Global Shutter MOS/CCD Buffer Memory Function for Modern CMOS Image Sensors.

Japanese Patent Application JPA1975-127646

Japanese Patent Application JPA1975-127647

Japanese Patent Application JPA1975-134985

Japanese Patent Application JPA1977-126885

The first Pinned Photodiode papers in 1977 and 1978 by Hagiwara at Sony

P1977_Narrow_Cahnnel_Transfer_Gate_CCD_SSDM1977_Paper_by_Hagiwara.pdf"

Hagiwara_SSDM1978_Paper_on_Pinned_Buried_Photodiode.pdf

Five Recently Published Papers by Hagiwara(AIPS)

P2019_3DIC2019_Paper_on_3D_Pinned_Photodiode_6_pages.pdf

EDTM2020 Conference Paper_ID_3C4_by_Hagiwara(PDF)

IJSSM2021 e-Journal Paper on Pinned Photodiode.html

ICECET2021_Paper61.pdf

ICECET2021_Paper75.pdf

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Journal of Applied Physics

Detailed Balance Limit of Efficiency of *p-n* Junction Solar Cells

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Submitted: 03 May 1960 • Published Online: 11 June 2004

William Shockley and Hans J. Queisser


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JOURNAL OF APPLIED PHYSICS VOLUME 32, NUMBER 3 MARCH, 1961

Detailed Balance Limit of Efficiency of *p-n* Junction Solar Cells*

WILLIAM SHOCKLEY AND HANS J. QUEISSER
Shockley Transistor, Unit of Clevite Transistor, Palo Alto, California
(Received May 3, 1960; in final form October 31, 1960)

In order to find an upper theoretical limit for the efficiency of *p-n* junction solar energy converters, a limiting efficiency, called the *detailed balance limit* of efficiency, has been calculated for an ideal case in which the only recombination mechanism of hole-electron pairs is radiative as required by the principle of detailed balance. The efficiency is also calculated for the case in which radiative recombination is only a fixed fraction f_c of the total recombination, the rest being nonradiative. Efficiencies at the matched loads have been calculated with band gap and f_c as parameters, the sun and cell being assumed to be blackbodies with temperatures of 6000°K and 300°K, respectively. The maximum efficiency is found to be 30% for an energy gap of 1.1 ev and $f_c=1$. Actual junctions do not obey the predicted current-voltage relationship, and reasons for the difference and its relevance to efficiency are discussed.

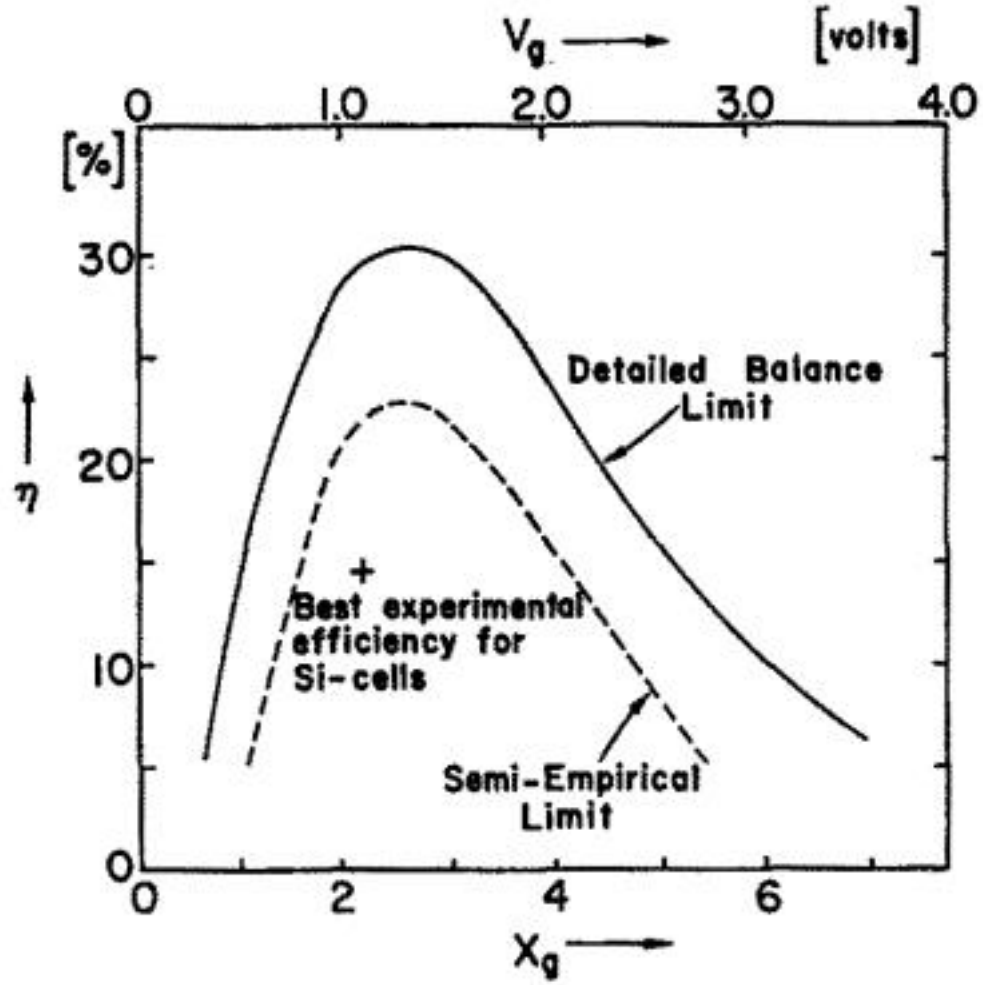
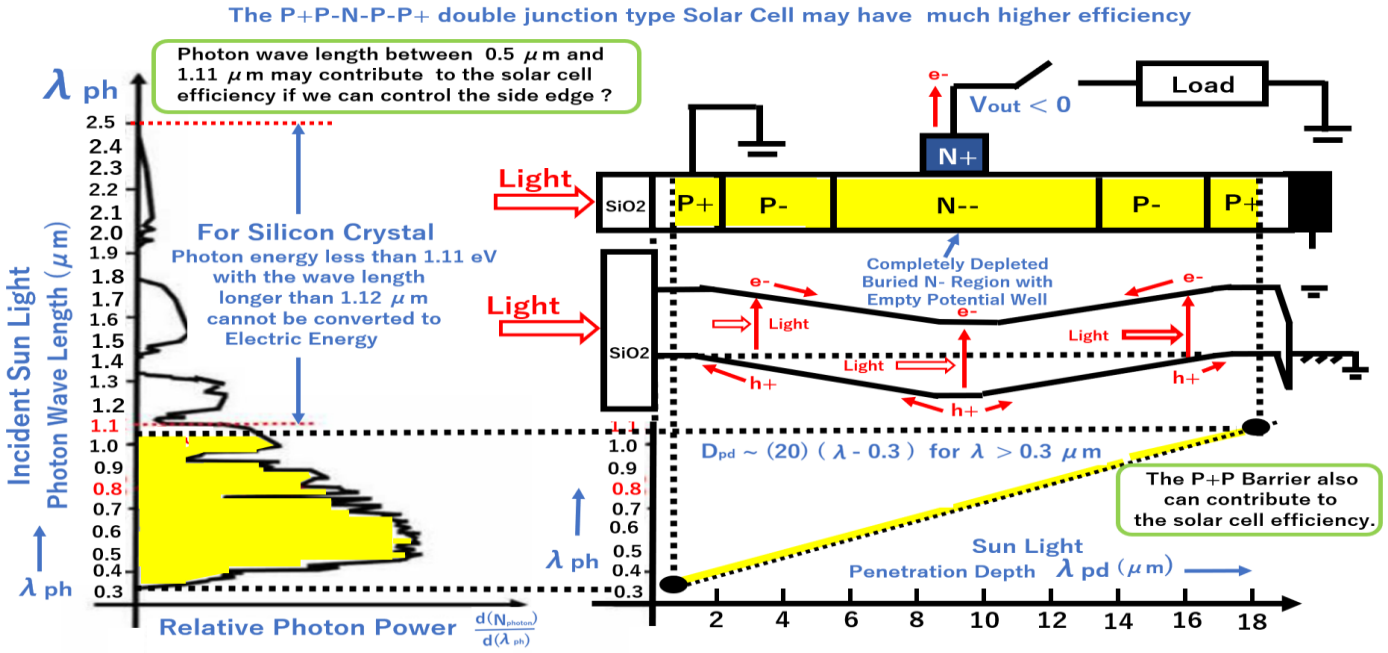
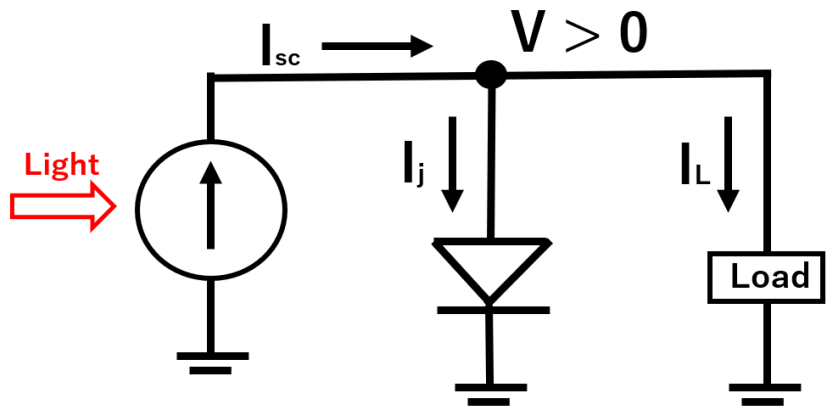


FIG. 1. Comparison of the "semiempirical limit" of efficiency of solar cells with the "detailed balance limit," derived in this paper. + represents the "best experiment efficiency to date" for silicon cells. (See footnote 6.)

P+PNN+接合Diodeの電流(Ij)電圧(V)特性

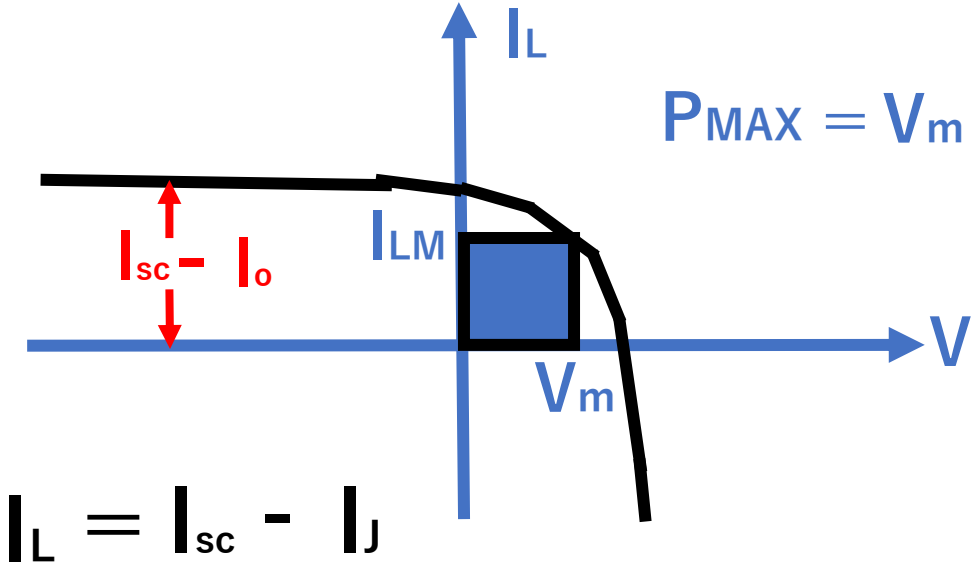




$$(1)\quad I_o = A \exp\left(-\frac{E_G}{kT}\right)$$

$$(2)\quad I_j = (I_o)\left[\exp\left(\frac{V}{kT}\right) - 1\right]$$

$$(3)\quad I_{sc} = I_J + I_L$$



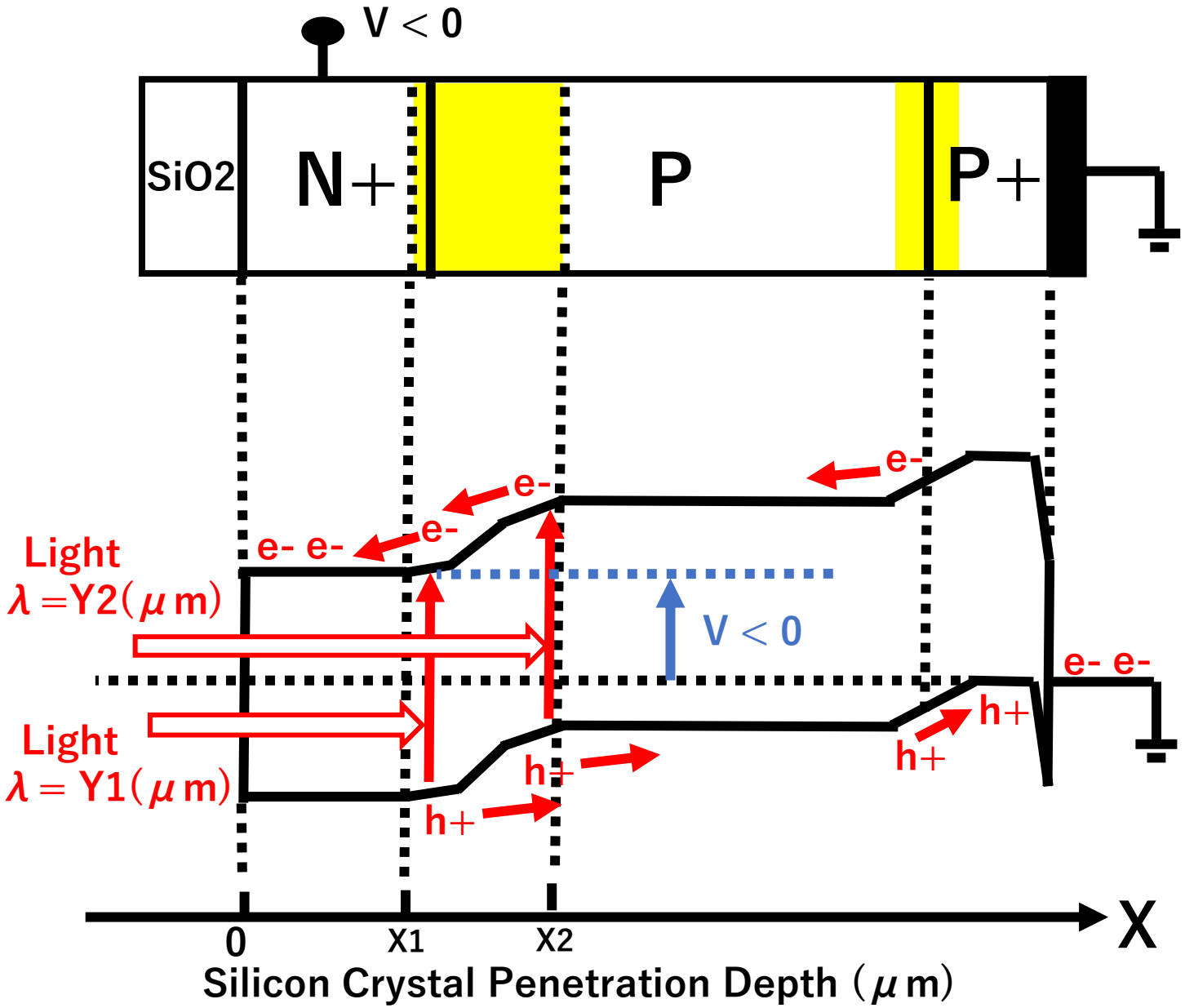
$$P_{MAX} = V_m I_{LM}$$

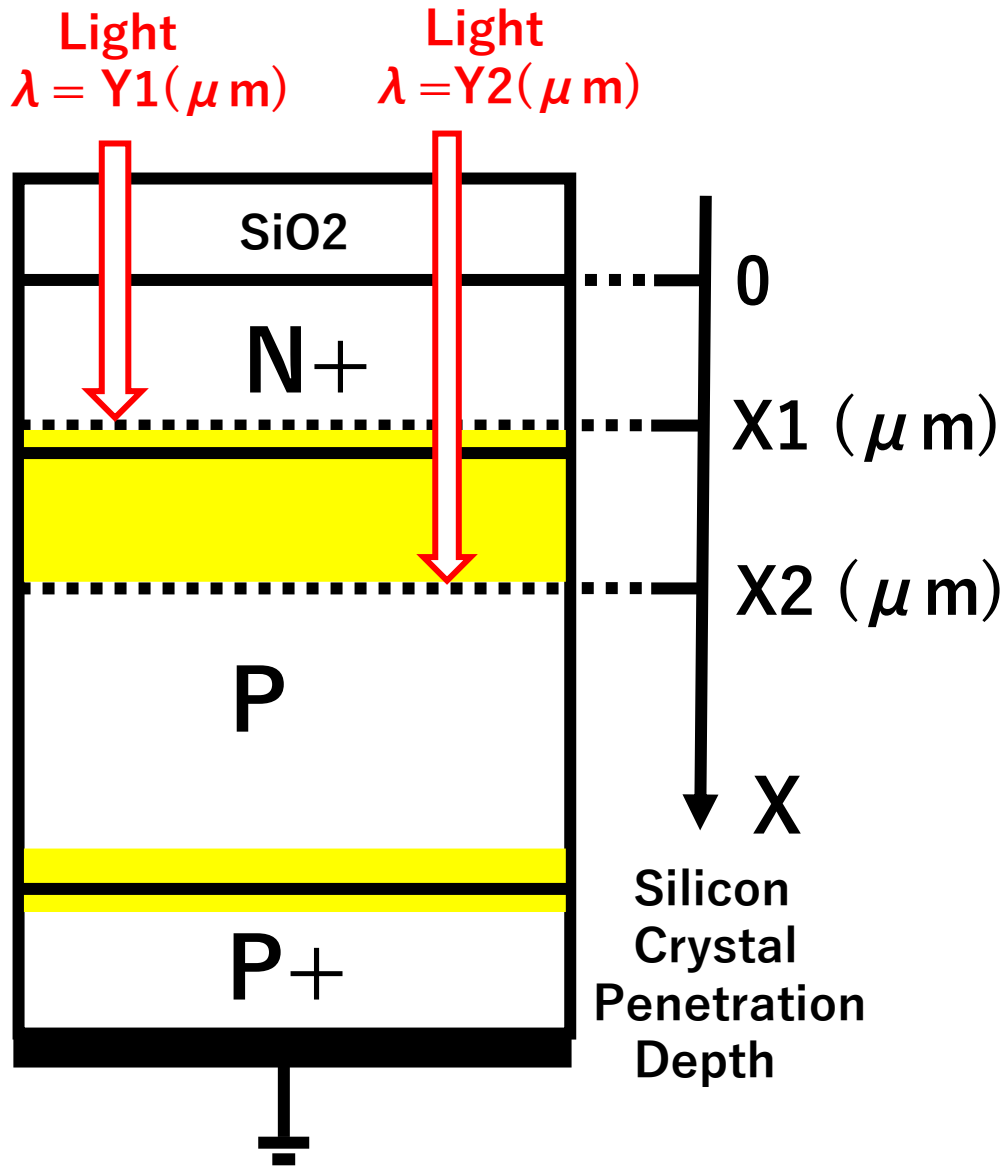
$$I_L = I_{sc} - I_J$$

$$\frac{(V I_L)}{(V I_{sc})} = \frac{\left(\frac{V}{kT}\right)}{1 + \left(\frac{V}{kT}\right) - \exp\left(\frac{-V}{kT}\right)} = (0.5 \sim 1.0)$$

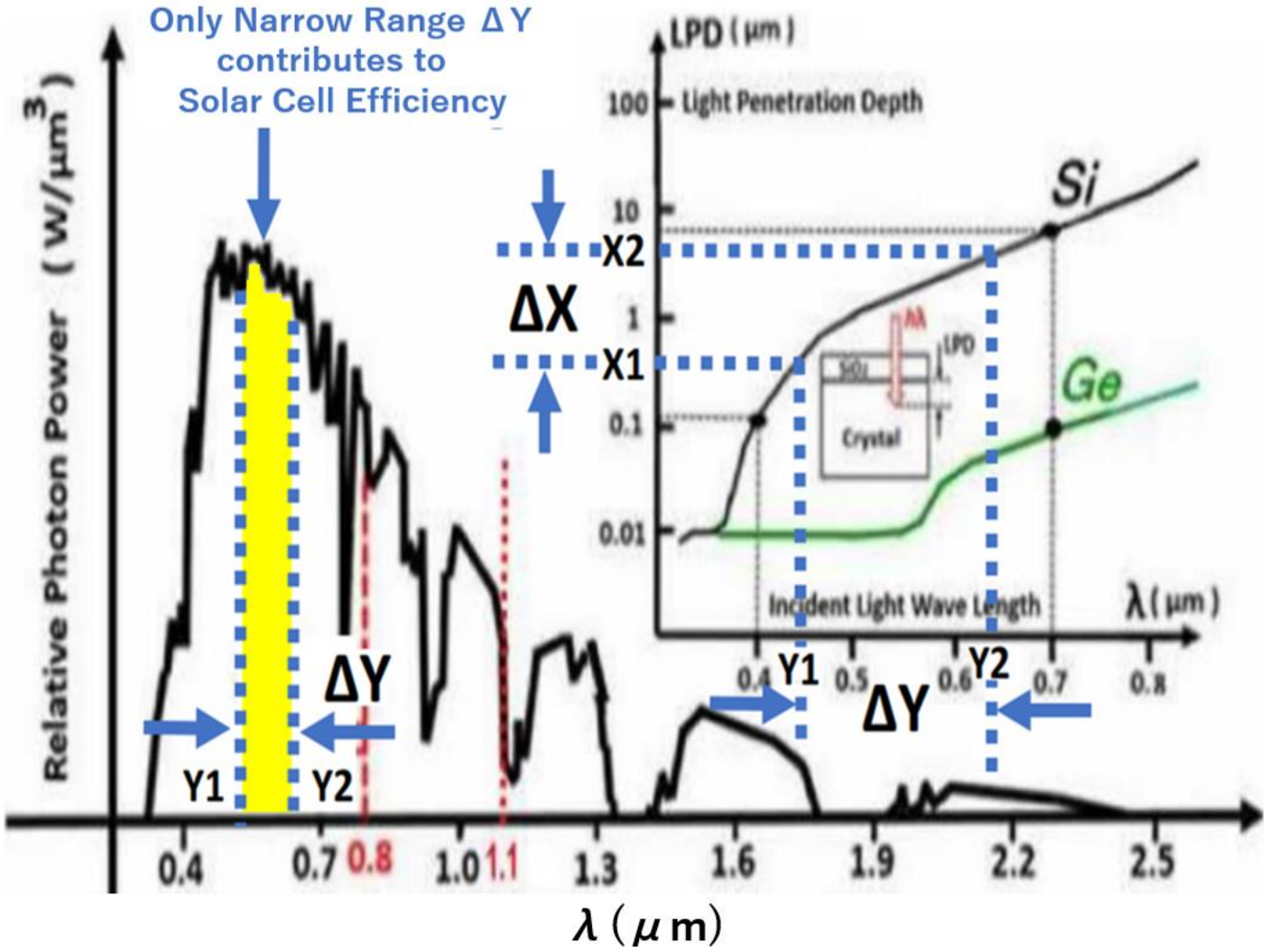
$$d(I_{sc}) = \frac{(hc)}{(\lambda)}\left\{1 - \exp\left(-a D_{pd}(\lambda)\right)\right\}\frac{dN_{ph}}{d\lambda}\, d\lambda$$

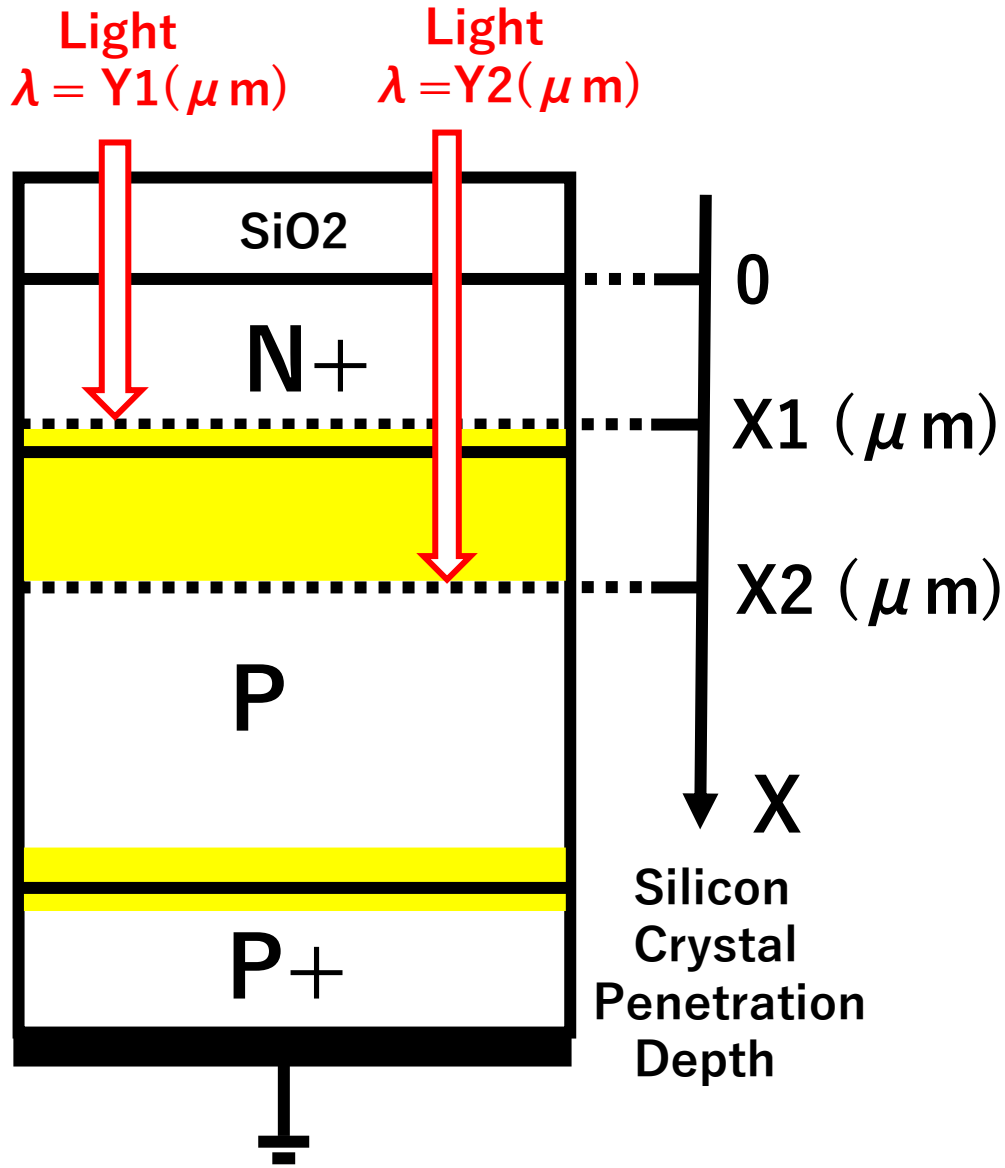
For Single Junction type Solar Cell with the floating N+ surface photo charge storage region, only the wave length between Y1(μm) and Y2(μm) can contribute to the Efficiency.





For Single Junction type Solar Cell with the floating N+ surface photo charge storage region, only the wave length between Y1(μm) and Y2(μm) can contribute to the Efficiency.





太陽電池の変換効率の限界

変換効率は、使用される半導体材料が吸収できる太陽光の波長領域と、PN接合の空乏層領域での吸収量で求まります。シリコン結晶では、波長が 0.29μmから 1.20μm までの太陽光を吸収できます。Single PN 接合型での変換効率の限界理論値は 28% です。実際には20%程度です。その理由は(1)受光面での反射や(2)受光表面再結合や(3)PN接合の空乏層内での結晶欠陥による再結合や(4)裏面再結合などが生じ、光電変換された光電子とホールのペアが再結合し無駄になる為です。

Silicon のBand Gap は　1.1 eV

InP のBand Gap は　1.34 eV

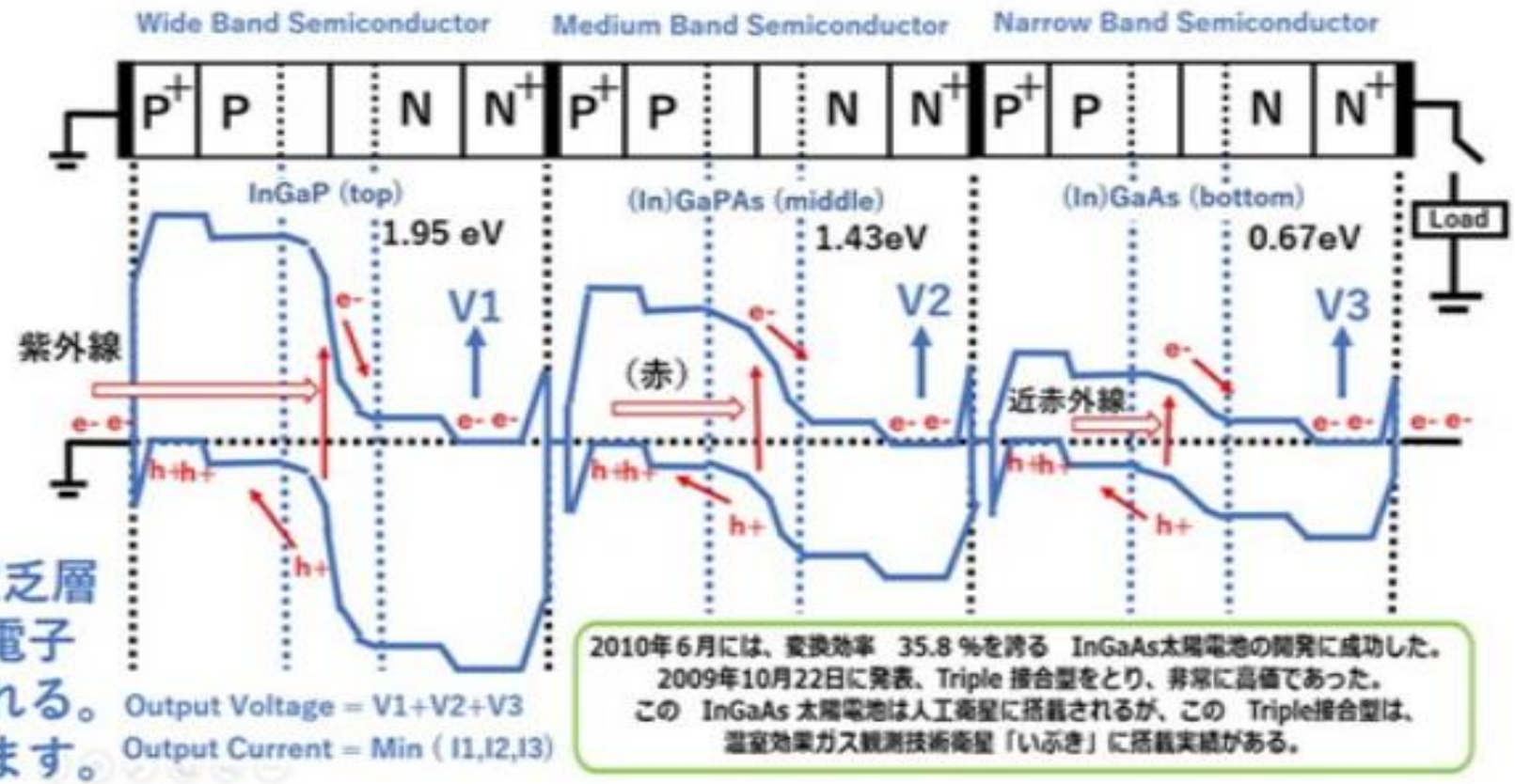
GaAs のBand Gap は　1.42 eV

CdTe のBand Gap は　1.48 eV

GaN のBand Gap は　3.4 eV

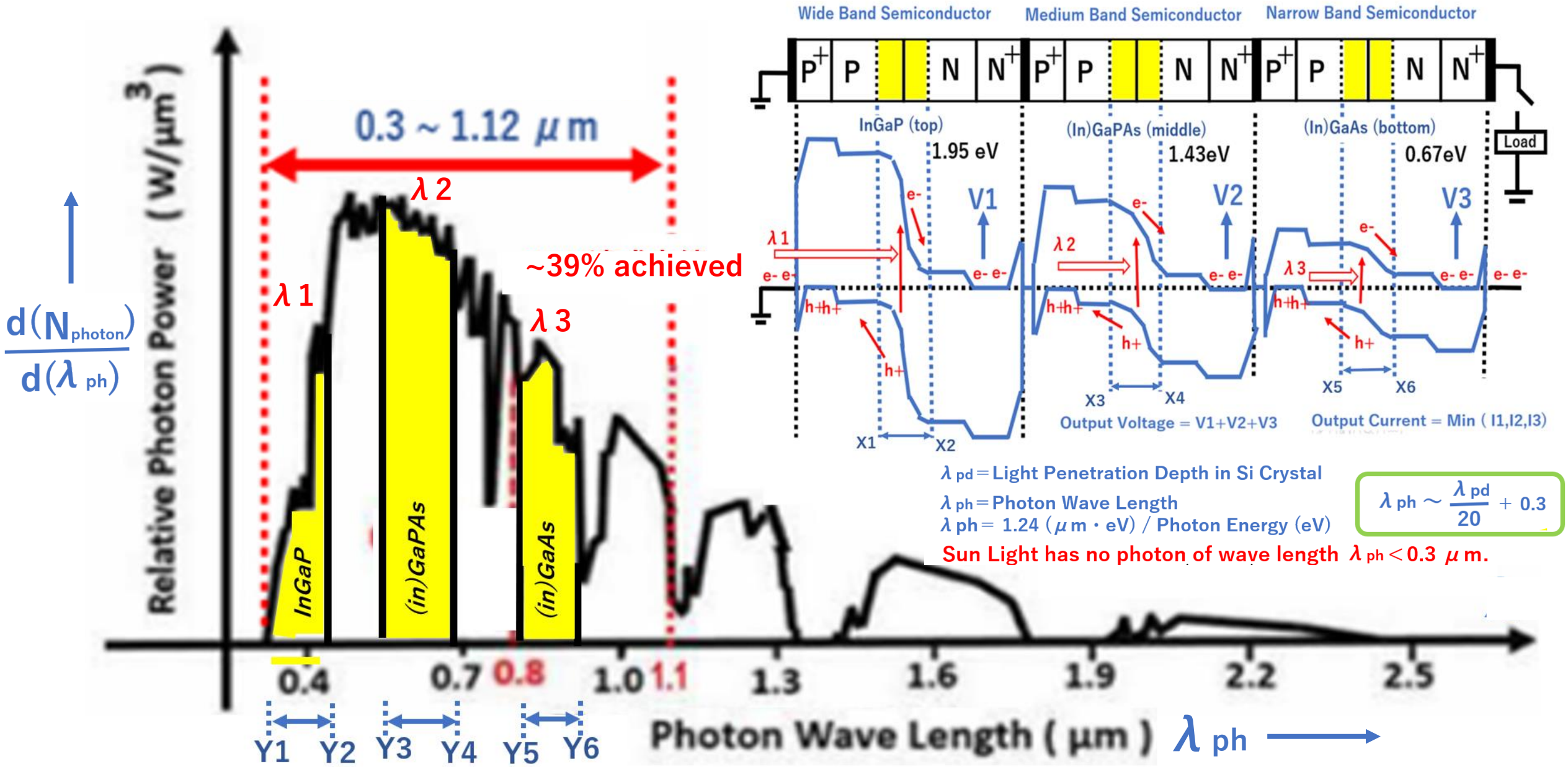
β-Ga_2O_3 のBand Gap は 4.5 eV

バリア電界が存在するPN接合の空乏層領域内でのみ、光電変換による光電子とホールのペアは効率良く分離される。と言う事が、今の常識となっています。



2010年6月には、変換効率　35.8 %を誇る　InGaAs太陽電池の開発に成功した。
2009年10月22日に発表、Triple 接合型をとり、非常に高価であった。
この　InGaAs 太陽電池は人工衛星に搭載されるが、この　Triple接合型は、
温室効果ガス観測技術衛星「いぶき」に搭載実績がある。

Triple Junction Solar Cell with Wide Band Gap Compound Semiconductors achieved ~39% Quantum Efficiency



λ pd = Light Penetration Depth in Si Crystal

λ ph = Photon Wave Length

λ ph = 1.24 (μm・eV) / Photon Energy (eV)

$$\lambda_{ph} \sim \frac{\lambda_{pd}}{20} + 0.3$$

Sun Light has no photon of wave length $\lambda_{ph} < 0.3\ \mu m$.

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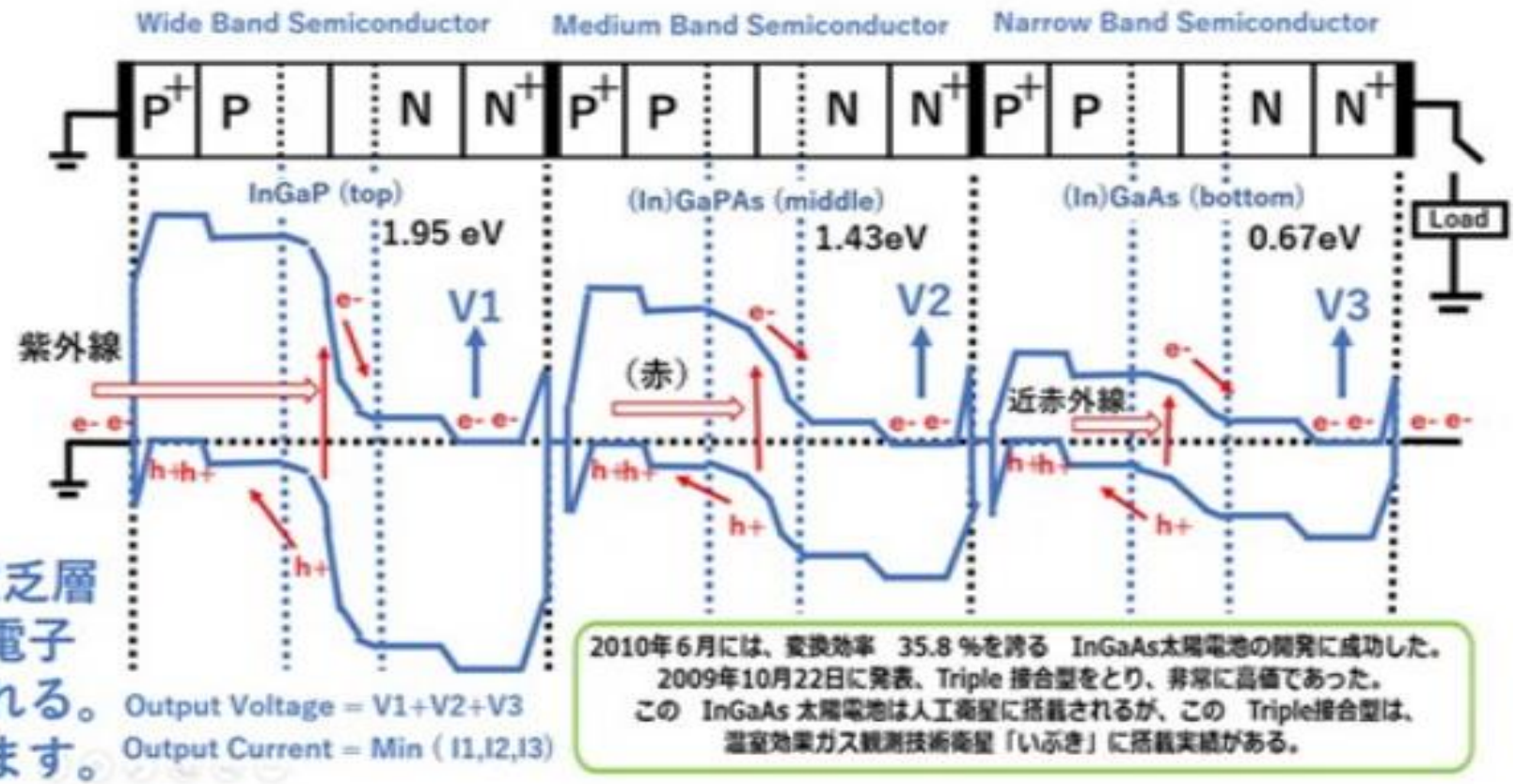
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Invention and Historical Development Efforts of Pinned Photodiode and Electric Shutter

2019



Hagiwara at Sony Kumamoto Tech Center
in 2017, 2019 and 2022.

2001



1. Introduction
2. Patent Wars on Pinned Photodiode
3. Double Junction type Solar Cell
4. Physics of Image Sensor and Solar Cell
5. Conclusion and Summary

1980



1996



Hagiwara also visited Sony Atsugi-Tech Center in July 2020.

Invention and Historical Development Efforts of Pinned Photodiode and Electric Shutter

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Hagiwara at Sony Kumamoto Tech Center
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5. Conclusion and Summary

1980



1996



Hagiwara also visited Sony Atsugi-Tech Center in July 2020.

●技術イノーベーションとは、発明や初期開発努力だけでは実現しません。世の中に役にたつものとして、見えるものとして、具体的に実現されて、はじめて、技術イノーベーションと呼べるものになります。

●企業の社長や責任者が、TVや新聞の報道陣の前で、誇らしげに新しい商品を説明する様子をよく見ます。

製品を開発し商品化を指導した企業の社長や責任者が、その代表者としてではありますが、実際に企業で開発し、生産し、商品化するには、実際には、ひとりでできるわけはありません。実際には、多くの人材とお金と時間を投資する必要が企業にあります。

●そのため、商品化された製品がたいへん素晴らしいもので、世の中に役に立つものであればあるほど、社会に非常に広く貢献した場合であればあるほど、いろいろな業界団体や、社会奉仕財団や、国際学会で企業として、評価され、表彰を受ける場合があります。

その場合、実際に評価され表彰を受ける人は、その企業の責任者や、事業化を推進した責任者、または、開発の責任者です。その成果の代表者として、表彰をもらう場合が多いです。そして、その仕事を実際に一緒に進めた多くの技術開発者、生産立ち上げ者や営業担当や販売担当者とその受賞を一緒に喜び合います。

●なかなか、外部の人間からは、だれが本当に開発を担当し、生産し、商品化を企業内で長い年月をかけて試行錯誤して失敗を繰り返し、それにもあきらめず、がんばり、実行し、その成功に導いたのか、その企業内での細かい開発の歴史の詳細は、実際にはベールに包まれ、見えない場合が多いです。それは、当然であり、しかたのない事です。いつの間にか、若い世代の企業の世代から忘れさられる場合が多いです。

２０２２年９月２０日（火）　ソニー熊本テック訪問記念講演　　萩原良昭（AIPS）

●私でさせも、ものを購入する場合、まず値段とその品質と性能をみます。出願特許とか、だれが苦労して造ったとか、どこの国の生産であるかなどを、まったく確かめる事もなく、私も安くていいものを好んで購入します。

お客様にはあまり、だれが苦労して造ったとか、どこの国の生産であるとかは、まったく問題になりません。

●今、日本で半導体電子産業のあり方、その存在価値、戦略的な価値が日本政府レベルで見直しされ始めました。

半導体電子部品は産業のコメとして、「お米」と同じく、自国で大切に造り、自分たちの食べるお米は最高の品質のお米として育て、おいしく大切に食べる。半導体電子部品も日本の産業のコメとして、大切に自国で育て使うことの重要性を、政府も認識しはじめたと思われます。その覚悟をぜひ実行し通してほいしところです。

●もと日立の専務で、その後、ソニーの出井社長のお誘いを受けて、ソニーの専務して来られた牧本次生さんは２００６年１１月２０日に「一国の盛衰は半導体にあり」という本を出版されました。

●実は、ＩＣの発明は、米国ＴＩ社の　Jack Kilby の1957年7月24日の発明特許である「半導体部品間を接続するために細い金属線でbondingする」というアイデアが始まりか？　それとも、当時 Fairchild 社のRobert Noyce の1959年1月23日の発明特許である「半導体部品間の総合結線を基板に蒸着された薄膜で行う」というアイデアであるのか？　この２件の出願特許が当時長い間、世界の半導体業界では論点になっていました。

●牧本次生さんの著書の中の９６ページには、この「ICの発明者はキルビーかノイズか？」といく課題にふれています。工業調査会出版（ISBN4-7693-6172-6 ￥1900E）、2006年11月20日。

●「一国の盛衰は半導体にあり」 牧本次生 著　の　p.96 掲載の一節、
「ICの発明者はキルビーかノイズか？」からの引用文です。

この後１０年にわたって特許権の帰属をめぐる法廷論争が繰り広げられた。
激しい係争を経た後で、TI社とFairchild社のTopによる会談において、
ICの特許はKilbyとNoyceが共有する形となって決着をみたのである。

Kilby は2000年にノーベル物理賞を受賞したが、その時すでに Noyce は
他界していたため、 Kilby の単独受賞になったものと思われる。

「ICについては Noyce も類似のアイデアを持ち、実現手段も考案していた」
と述べていることから、ノーベル賞についても二人で分かち合いたいという
気持ちがあったのかも知れない。

この発明からわれわれが学ぶことは、半導体における「突然変異」は必ずしも
大勢の人数をかけた研究から生じるものではなく、問題を深く掘り下げる能力
を持つ個人の洞察力が何よりも必要であることを示唆している点だと思う。

工業調査会出版（ISBN4-7693-6172-6 ￥1900E）2006年11月20日出版

●「イノーベーションの成功と失敗」と題して、もとSONYの武田立さんと小樽商科大学の瀬戸篤教授共著で、出版されています。

ISBN978-4-495-38571-2　￥1800E 同文館出版 2015年10月20日。

●戦前戦中から戦後に至る日本型イノーベーションの真実

イノーベーションは、「知恵の創造」「知の具現化」「知の商業化」の３段階を経て完成する。

日本発イノーベーションの歴史に学び、溢れるほどの技術シリーズをもちながらも、新規事業・新製品開発に苦しみすべての産業人に贈る！

●テクノロジー・ベンチャーの誕生とイノーベーションの興隆には、強い相関があることは歴史が証明している。

それゆえに、21世紀日本のイノーベーションを一層活発化させるためには、テクノロジー・ベンチャーの誕生を促すことが最短だと確信している。

これまでの日本の戦後教育においてあまり触れられることのなかったイノーベーション誕生の歴史を追い、イノーベーションが誕生したメカニズムを精密に後追いすることで、これからのイノーベーションを担うテクノロジー・ベンチャーの誕生を加速させたいという志を共有している。

●トランジスタの発明は1947年の暮れとされるがその発端ははるか1936年にまでさかのぼる。当時は電気製品といえば真空管が広く使われていた時代だった。整流特性を持つ二極管と電流増幅特性を持つ三極管が主流だった。二極管に代わり、整流特性を持つ半導体素子（ダイオード）が開発されはじめた時代だった。

そこで当時、米国ベル研究所の研究部長だった M. J. Kerryは、三極真空管に代わる個体スイッチの開発に注目した。そして三極真空管に代わる個体スイッチの開発を当時はまだ２６歳だった W. Shockleyに命じた。不幸にも戦争により中断される事なったが、戦後再び、三極真空管に代わる個体スイッチの開発が W. Shockley チームで継続される事になった。

W. Shockley の部下だった J. Bardeenと W. Brattain は1947年12月に半導体基板（Base端子）に２本の金属針（EmitterとCollector端子）を立てて、三極個体スイッチの組み立てに成功し、その電流増幅特性を確認した。 W. Shockley はその場にいなかったが、その後、半導体デバイス物理の基礎となる、接合型トランジスターの理論を作った。1948年の夏になり、W. Shockley , J. Bardeen, W. Brattain の連名で金属針の接合型トランジスターの発明が一般公開された。1949年にはベル研で成長接続型トランジスターが開発された。

さらに1951年には RCA と WE の両社で 合金型が開発された。その後1952年には RCAからベル研に John Louis Moll が加わり PNP double 接合型トランジスタ動作解析で有用な Ebers-Moll モデルをはじめ PNPN triple 接合型のサイリスタのPunch-thru 動作を利用した高速 Switch 理論を提唱した。その為には表面がピン留めされる事が必要であるが、1975年Sonyに入社した萩原は、このサイリスタ型高速 Switch 特性に注目しこの構造と機能を受光素子に応用し、メカフリーの電子シャッターを発明した。副産物として、これが世界で最初の Pinned Photodiode の発明となった。

●太陽電池もイメージセンサも、ともに、光を効率よく電気エネルギーに変換するという、有用な役割を担う重要な半導体電子デバイス部品です。

２００７年３月に独立行政法人新エネルギー・産業技術総合開発機構の「NEDOBOOKS」編集委員会から、「なぜ、日本が太陽光発電で世界一になれたか」と題して大変わかりやすい、１２７ページの一般社会人向けの技術解説書（非売品）[1] が刊行された。そしてあれから１５年が経過した。

この１５年間で日本の半導体電子デバイス産業は衰退した。生産コスト競争だけでなく、品質でも中国や東南アジア隣国の勤勉さと努力は無視できるものではない。技術革新でも欧米諸国の奇才天才的な、自由闊達な発想に驚きを隠せない。この危機をどう乗り越えるかが日本政府の重要な課題となっている。

技術イノーベーションとは、発明(者)だけでは何も実現できない。アイデアをまず実験検証して存在定理を証明することが必要である。その発明の素性の良さに、確信を持ち自信を持ち、最後まであきらめる事なく、生産技術に磨きをかける努力があってこそ、社会に役に立つ製品を提供することが可能となる。

この１５年間日本の半導体電子デバイス産業が衰退した本当の理由はどこにあったのだろうか。「半導体電子部品は努力すれば安くなる」という信念を今の日本は忘れているのではないかと感じる。生産手順が確立すれば後は電気代だけで生産ロボットが均一な製品を量産できる時代になっている。すべては「いかに安く電気エネルギーを創出するか」にかかっている。

●技術イノーベーションとは、発明や初期開発努力だけでは実現しません。世の中に役にたつものとして、見えるものとして、具体的に実現されて、はじめて、技術イノーベーションと呼べるものになります。

●地球規模での脱炭素社会の実現は人類の永遠のテーマです。

京都地球温暖化防止会議（COP3）が１９９７年１２月に開催されてから２５年になります。

今後さらに人類の共通理念として環境を大切にしていこうという活動がさらに加速される事になるでしょう。

今では太陽光パネルをビルの屋上や住宅の屋根に組み込む事を奨励する事が普通になりました。

太陽電池だけでなく、電気自動車から自動走行車まで、人工知能を組み込んだ、
人間にやさしいシステム(AIPS*)はすべて半導体電子部品の塊です。

今後、半導体電子デバイス産業は「産業のコメ」として国家戦略として非常に重要な存在となります。

資源の乏しい日本にとっては、エネルギー政策と食料政策は永遠の課題です。

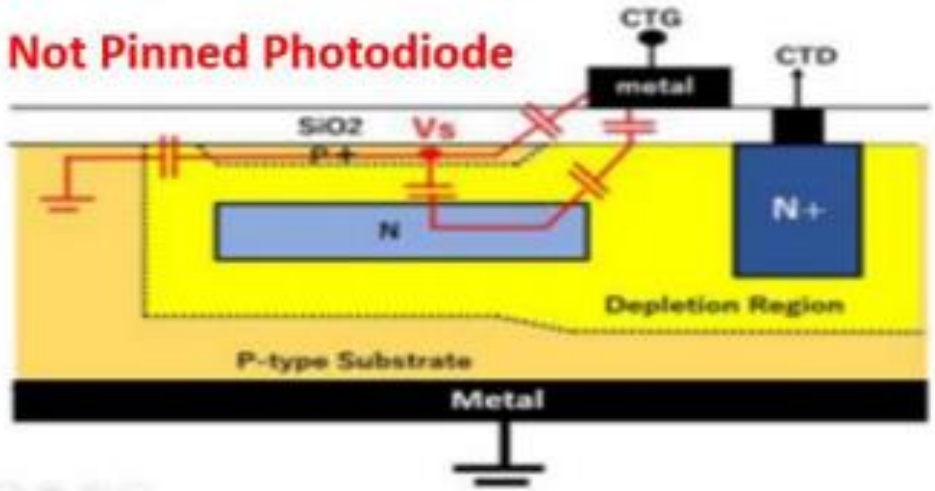
今後、そんな中で半導体電子デバイス産業を支える日本の技術力に期待される事は大きいです。

特に光エネルギーを効率よく電気エネルギーに変換する半導体電子デバイスの基本構造と
動作原理についてわかりやすく説明する事を狙いとしています。

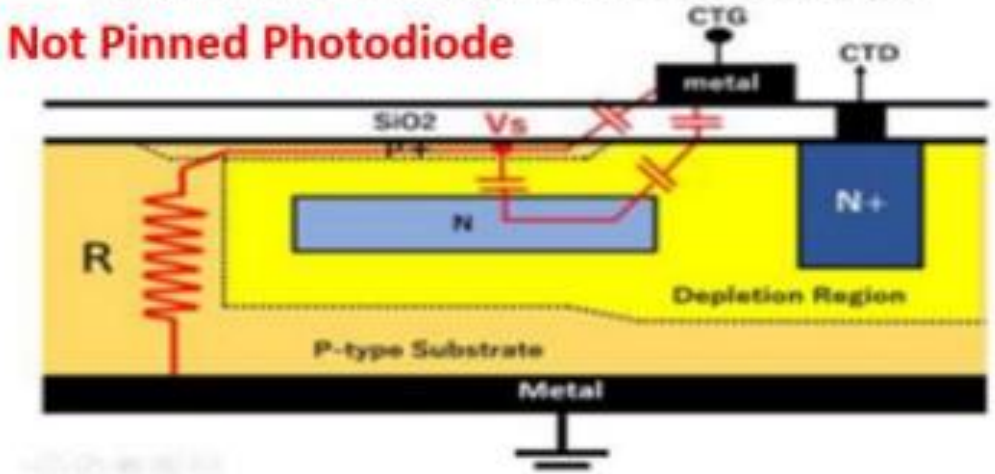
科学技術に関心ある若い世代だけでなく一般社会人の皆様にも半導体電子デバイスの楽しさを
感じていただければ幸いです。

Difference of Floating Surface PNP Buried Photodiode and Pinned Photodiode

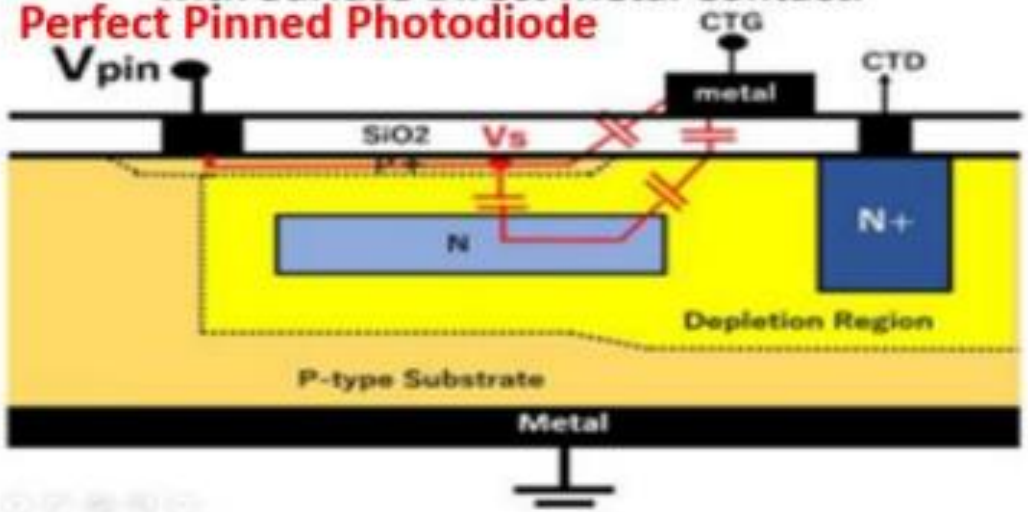
(a) Floating P+ Surface Completely Isolated by the extended depletion region



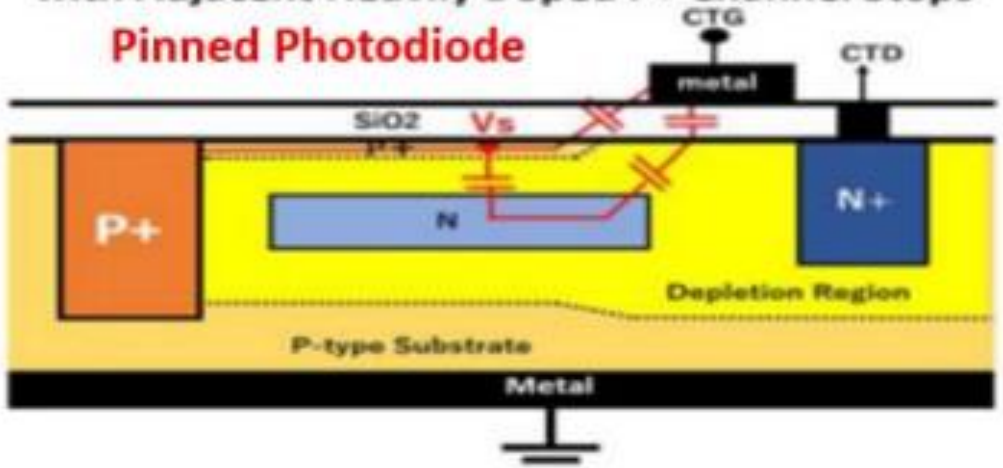
(b) Floating P+ Surface with RC Delay Time of the finite ohmic substrate resistance (R).



(C) Completely Pinned P+ Surface with RC = 0 with Surface Direct Metal Contact.



(D) Completely Pinned P+ Surface with RC~0 with Adjacent Heavily Doped P+ Channel Stops



History of Semiconductor Devices

MOSFETの発明
Al/Al2O3/Cu2S
1926,1928 Lilienfield

Si MOSFETの発明
1960 Kahng

Si CMOSの発明
1963 Wanlass

④ 1T1C 型DRAMの発明
1966 NEC 樗本、一条

1T1C 型DRAM の開発と Scaling 則
1967 IBM Dennard

初の3T1C DRAM 製品
1970 Intel

初の1T1C DRAM 動作実証
1971 GI

1T1C DRAM 用 Sense Amp回路
1972 GI

初の1T1C DRAMの製品化
1975 TI

① Bipolar Transistorの発明
1948年 Schocley et al

Wire Bond 型 集積回路の発明 1958 Kilby at TI

世界初の集積回路 1961 TI

MOS 集積回路 商品化
1963 RCA

TI JAPAN 設立 (TI and SONY)

1970 SONY カラーTV用 Bipolar IC

Mooreの法則(original)
1965 Intel

All MOS Transistor Memory Computer
1970 IBM

初の MPUの商品化
1971 Intel

MOS Scaling 則
1972, 1974 Dennard et al,

② コンデンサー容量メモリー発明
1948年 Norbert Wiener

③ Photo Transistorの 発明
1950年 John Northrop Shive

Bipolar 型電荷転送装置(CTD)
1967年 G.Krause

Bipolar 集積回路商品化
1963 Fairchild

MOS imager with Pixel 3 Tr Active AMP
by Peter Noble in 1966

磁気コア Bubble Memoryの発明
1967年 F.L.J. Sanster

MOS BBD 型電荷転送装置(CTD)
1970年 F.L.J. Sanster

⑤ SCCD 型電荷転送装置(CTD)
1970年 Boyle and Smith

⑥ BCCD 型電荷転送装置(CTD)
1974年 Boyle and Smith

⑦ 1975 Philips PNP Buried Photodiode

⑧ 1975 Sony HAD Sensor
PNPN Pinned Photodiode
with Anti-Blooming VOD

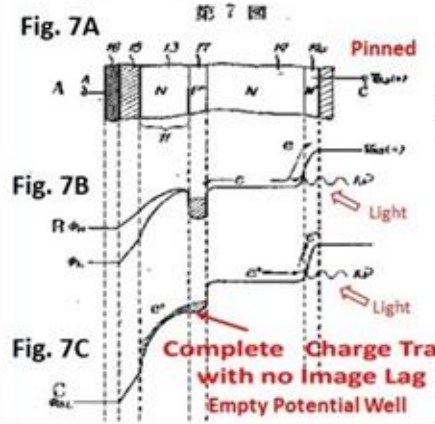
⑨ 1978 Sony PNP Pinned Photodiode
with adjacent P+ channel stops

⑩ NEC Buried Photodiode (= SONY HAD) @IEDM1982
KODAK Pinned Photodiode (= SONY HAD) @IEDM1984
SONY HAD Interline Transfer CCD Imager with VOD
の 商品化で市場制覇 1987 SONY

SONY HAD CMOS Imager 2019
with Back Light Illumination and Global Shutter Function

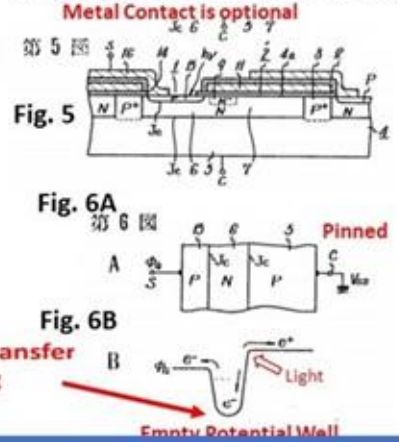
Hagiwara 1975 patents showed Features of No Image Lag , Empty Potential Well and Complete Charge Transfer of the double junction Pinned Buried Photodiodes.

(a) Pinned Photodiode defined in Fig. 7 of JPA1975-127647



(b) Pinned Photodiode defined in Fig. 5 and 6 of JPA1975-134985

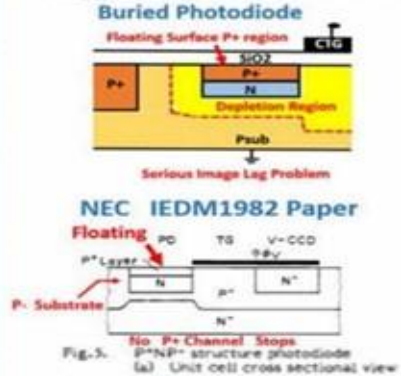
Metal Contact is optional

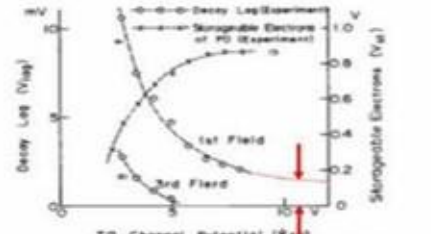


NEC IEDM1982 paper was not Pinned Photodiode by definition.

Difference of Buried Photodiode and Pinned Photodiode

Figure 5 does not have the P+ channel stop nearby.



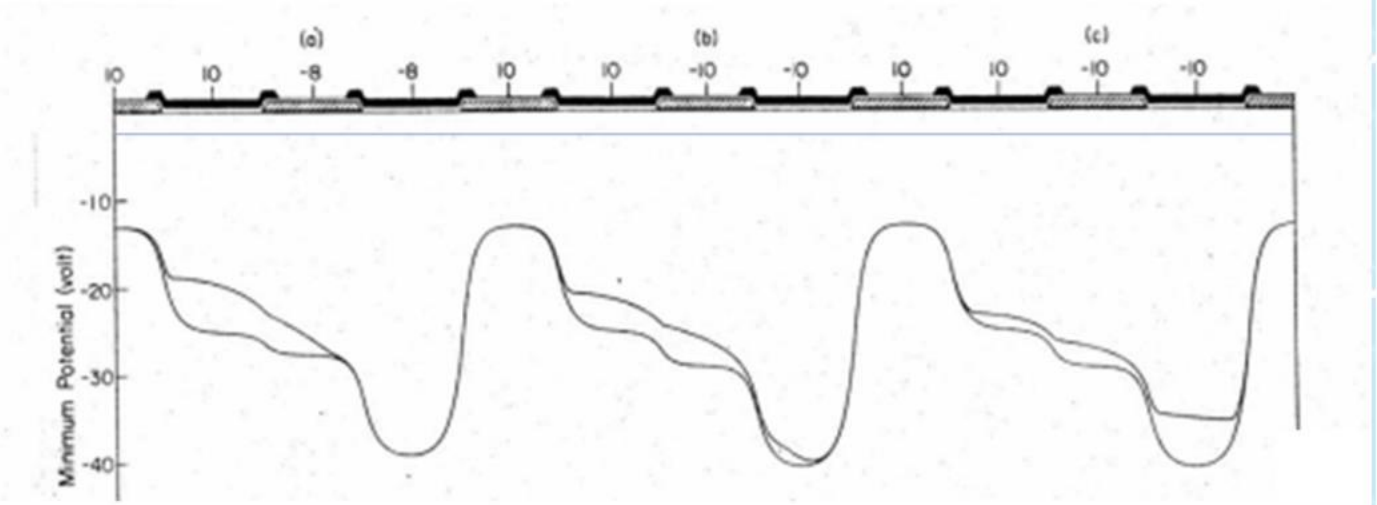


NEC IEDM1982 Paper reported Image Lag

Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 volt.

Caltech_1975_PhD_Thesis_Yoshiaki_Daimon_Hagihara.pdf

Exact Numerical Computer Simulation of Charge Transfer Action in Buried Channel CCD presented in ISSCC1974 by Yoshiaki Daimon-Hagiwara



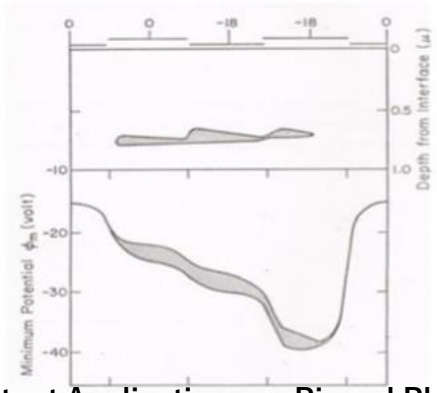
for details see the PhD Thesis by Yoshiaki Daimon-Hagiwara on June 1975 from Caltech.



Charge-Coupled Devices and Applications

Chairman
Lewis M. Terman

My PhD thesis paper on buried channel CCD at ISSCC1974, in Philadelphia, USA





Prof. T. C. McGill



Prof. C. A. Mead

Four Japanese Patent Applications on Pinned Photodiode with Electric Shutter Function and also with the in-Pixel Global Shutter MOS/CCD Buffer Memory for Modern Back Light CMOS Image Sensors. Function

[Japanese Patent Application JPA1975-127646]

[Japanese Patent Application JPA1975-127647]

[Japanese Patent Application JPA1975-134985]

[Japanese Patent Application JPA1977-126885]

The first Pinned Photodiode papers in 1977 and 1978 by Hagiwara at Sony

[P1977_Narrow_Cahnnel_Transfer_Gate_CCD_SSDM1977_Paper_by_Hagiwara.pdf"]

[Hagiwara_SSDM1978_Paper_on_Pinned_Buried_Photodiode.pdf]

Five Recently Published Papers

[ICECET2021_Paper75.pdf]

[ICECET2021_Paper61.pdf]

[IJSSM2021 e-Journal Paper on Pinned Photodiode.html]

[EDTM2020 Conference Paper_ID_3C4_by_Hagiwara(PDF)]

[P2019_3DIC2019_Paper_on_3D_Pinned_Photodiode_6_pages.pdf]



Prof. James McCaldin and Hagiwara

https://pc.watch.impress.co.jp/docs/column/semicon/1220487.html

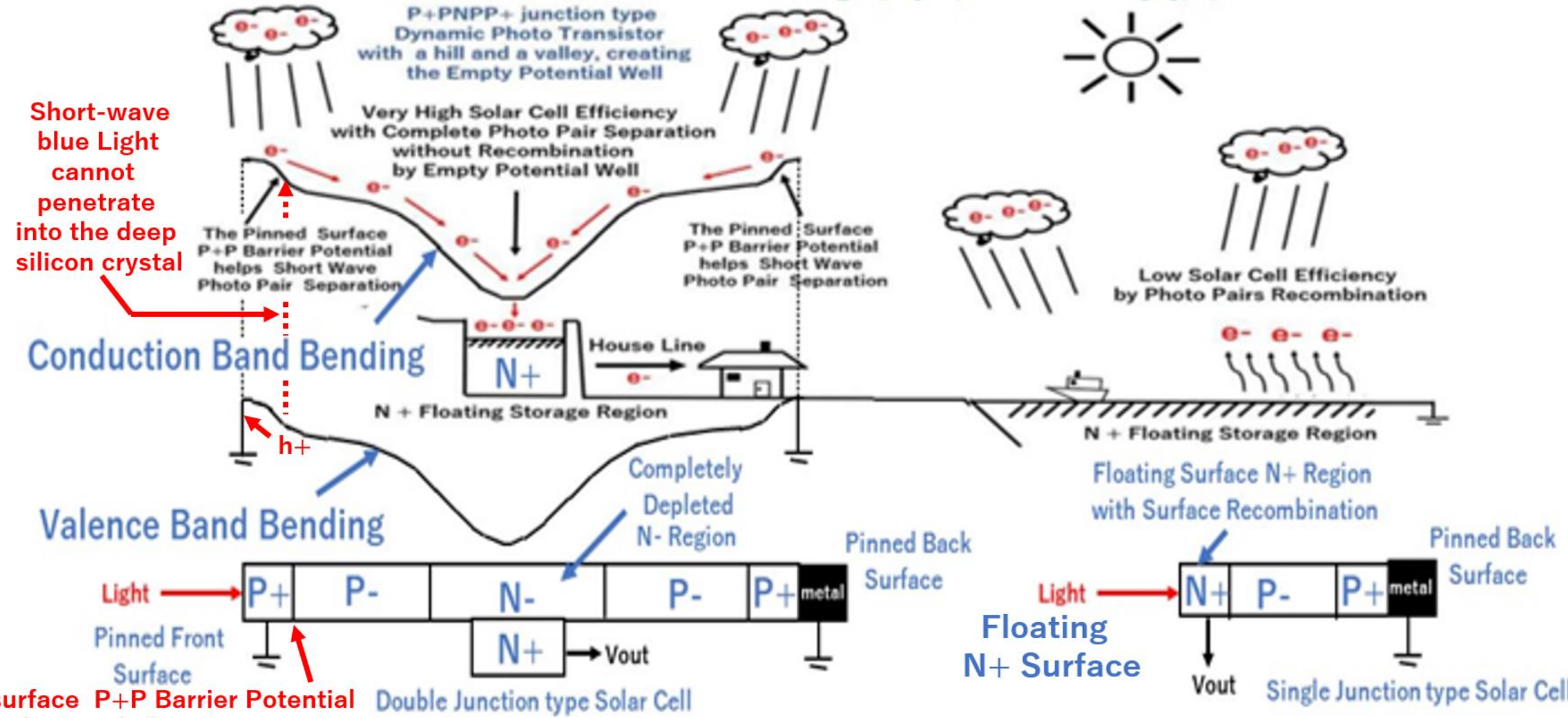
Band Gap of Diamond is ~ 5 eV

パワー半導体の材料とデバイスの特性比較

	シリコン(Si)	炭化珪素(4H-SiC)	窒化ガリウム(GaN)	酸化ガリウム(β-Ga2O3)
高耐圧デバイス	量産中	量産中	開発中	研究段階
中耐圧デバイス	量産中	量産中	量産中	開発段階
デバイスのオン抵抗	やや高い	低い	低い	極めて低い
低周波損失の性能指数(BFOMの相対値)	1	500	900	3000(極めて高い)
絶縁破壊電界(MV/cm)	0.3	2.8	3.5	8(推定値)
熱伝導率(W/(cm・K))	1.5	4.9	2	0.1～0.3(低い)
基板(ウェハ)コスト	極めて低い	高い	極めて高い(GaN基板)	低い(研究段階)
バンドギャップ(eV)	1.1	3.3	3.4	4.8～4.9
縦型デバイス	量産中	量産中	開発中(やや難しい)	開発段階(十分に可能)

True History of Photodiode

The difference of Double and Single junction type Solar Cells



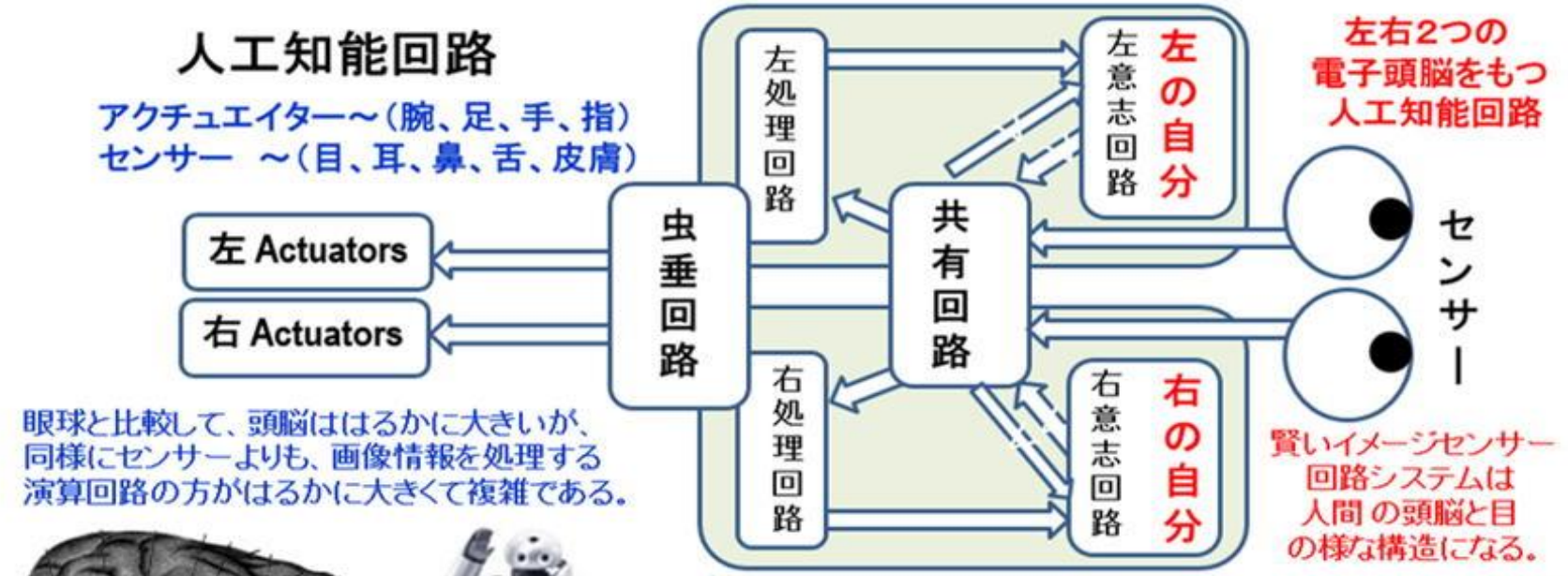
The surface P+P Barrier Potential helps electron-hole pair separations.

AIPSとは？　家庭内監視支援システムへの応用例です。

●イメージセンサー（賢い電子の目）にはいろいろな信号処理用の賢い回路が必要である。

人工知能回路

アクチュエイター～（腕、足、手、指）
センサー　～（目、耳、鼻、舌、皮膚）



眼球と比較して、頭脳ははるかに大きいが、
同様にセンサーよりも、画像情報を処理する
演算回路の方がはるかに大きくて複雑である。

賢いイメージセンサー
回路システムは
人間の頭脳と目
の様な構造になる。



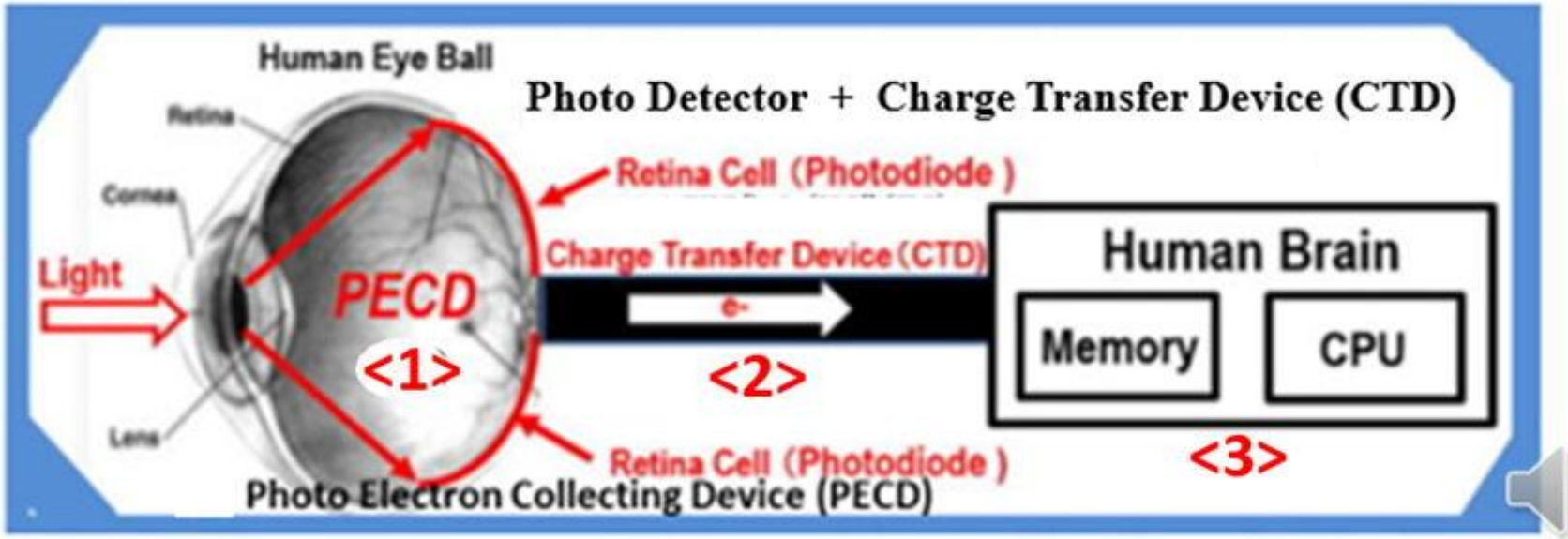
Basic Structure of Image Sensors

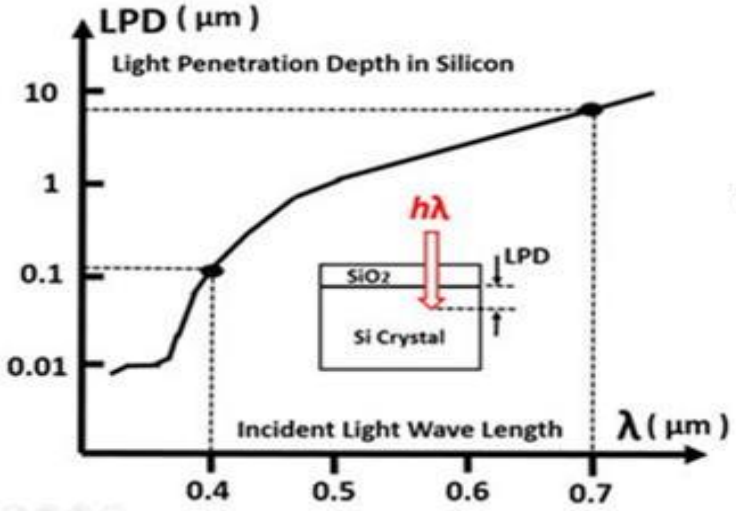
<1> Photo Electron Conversion Device (PECD) functioning as the human eye retina cells.

(A) N+P junction Photodiode with Poor Quantum Efficiency (QE) and Serious Image Lag Problems
(B) P+NP junction Pinned Photodiode with High QE, Low Surface Dark Current, and no Image Lag
(C) P+NPNsub junction Hole Accumulation Diode (HAD) with Vertical Overflow Drain (VOD) function

<2> Charge Transfer Device (CTD) transferring the signal charge to the output circuits.

(A) Original MOS type CTD with Very Serious CkT and Clock Noise Problems.
(B) CCD type CTD with low CkT and Low Clock Noise but with Large Power Problems.
(C) CMOS type CTD with In Pixel Active AMP and Global Shutter Buffer Memory.





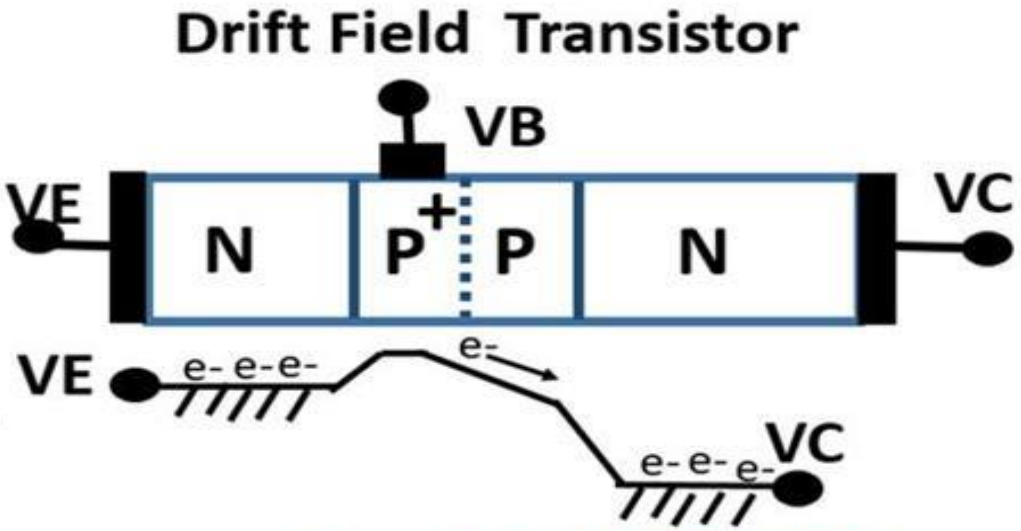


Figure 7 of JAP 1975-127647

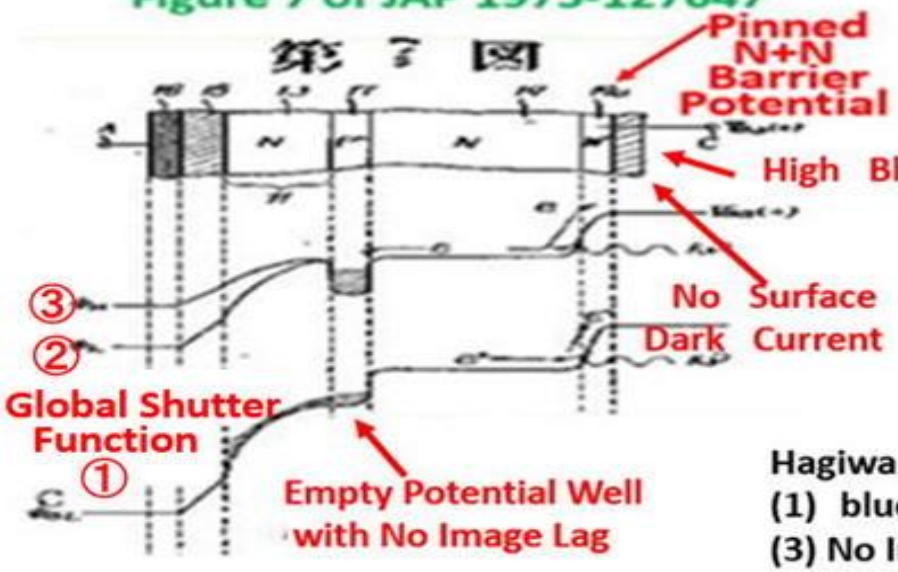


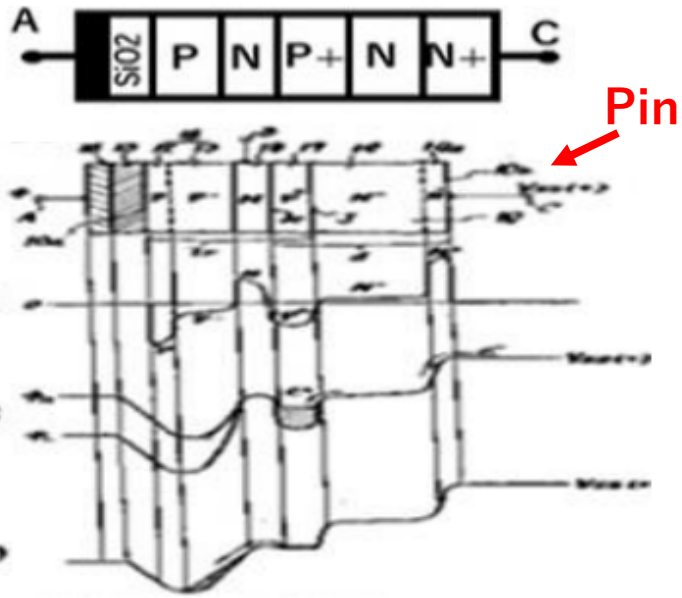
Figure 6 of JAP 1975-134985



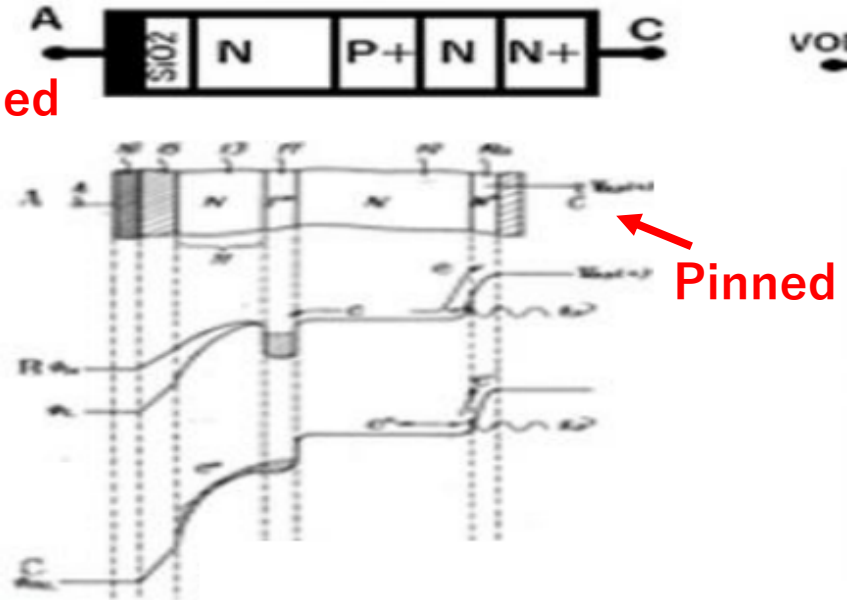
Hagiwara invented PNP junction type PPD in 1975 with
(1) blue light 100% QE, (2) No Surface Dark Current and
(3) No Image Lag, Complete Charge Transfer features.

Who invented Pinned Photodiode ?

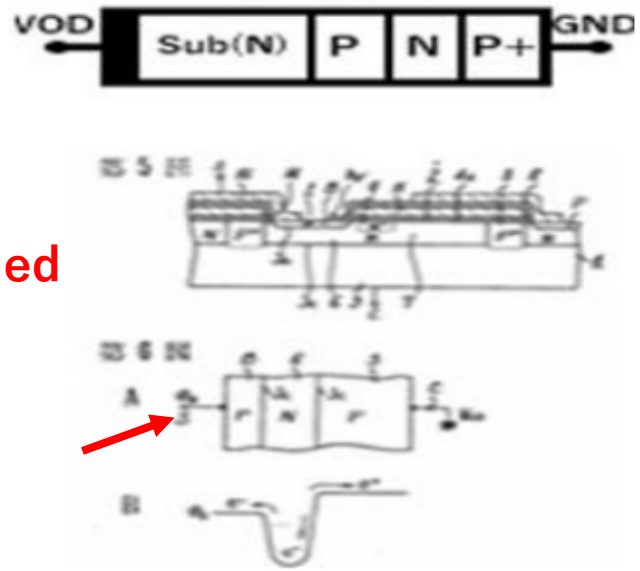
Hagiwara at Sony invented Pinned Photodiode in 1975. The evidence is give by the three Japanese patent applications, JPA1975-127646, JPA1975-127647 and JPA1975-134985. The first Pinned Photodiode was defined in October 23, 1975 as the N+NPNP triple junction(in Fig. 7 of JAP1975-127646) type and the N+NPN double junction type (in Fig. 7 of JAP1975-127647) type photodiodes with the N+ type pinned surface and the P type buried photo charge storage region with the complete charge transfer capability and the no-image-lag feature. The photo charge is transferred and drained to the CCD/MOS type charge storage buffer memory quicky by the strong punch-thru action. The second Pinned Photodiode was defined in November 10, 1975 as the PNP double junction (in Fig. 6 of JAP1975-134985) type photodiode with the vertical overflow drain action also with the complete charge transfer capability and the no-image-lag feature as evidence the empty potential well of the buried photo charge storage, completely depleted of the charge.



JPA1975-127646 Fig. 7



JPA1975-127647 Fig. 7



JPA1975-134985 Fig. 6

Proceedings of the 9th Conference on Solid State Devices, Tokyo, 1977;
Japanese Journal of Applied Physics, Volume 17 (1978) Supplement 17–1, pp. 255–261

Two Phase CCD with Narrow-Channel Transfer Regions

Yoshiaki DAIMON-HAGIWARA

Sony Corporation Research Center Yokohama 240

with no image lag

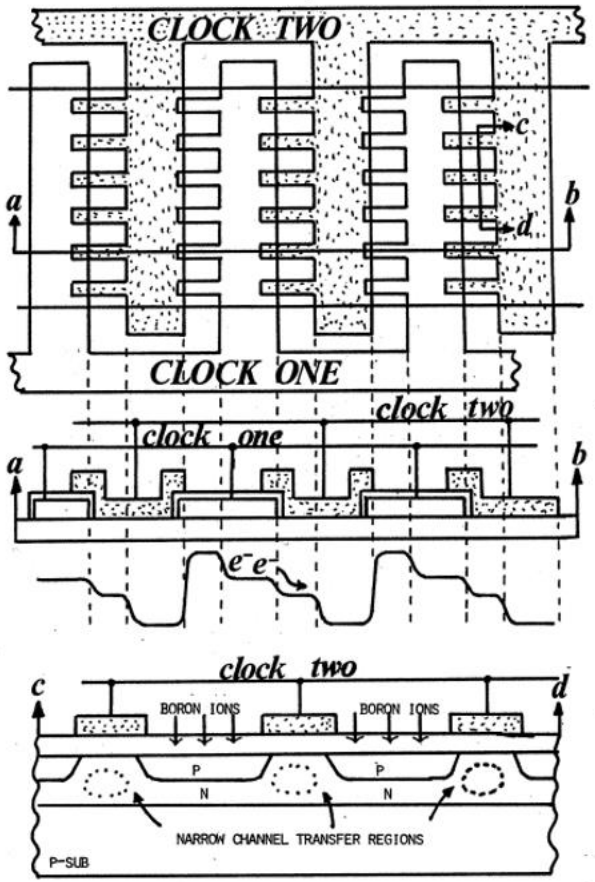


Fig. 1. Top and crosssectional views of the electrode structure for two phase CCD with narrow-channel transfer regions.

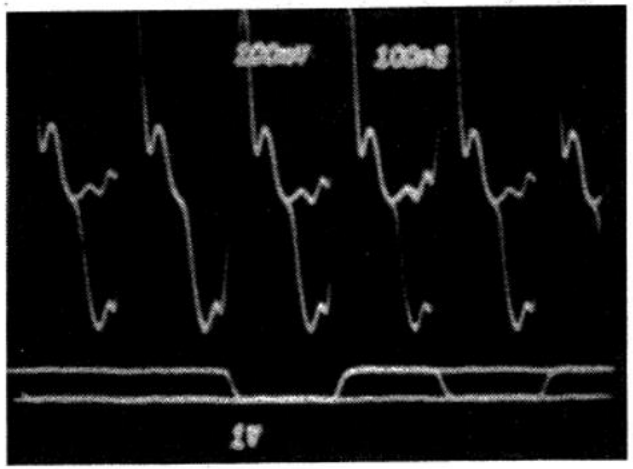


Fig. 4. Input and output wave forms for 242 analo delay line in buried channel version.

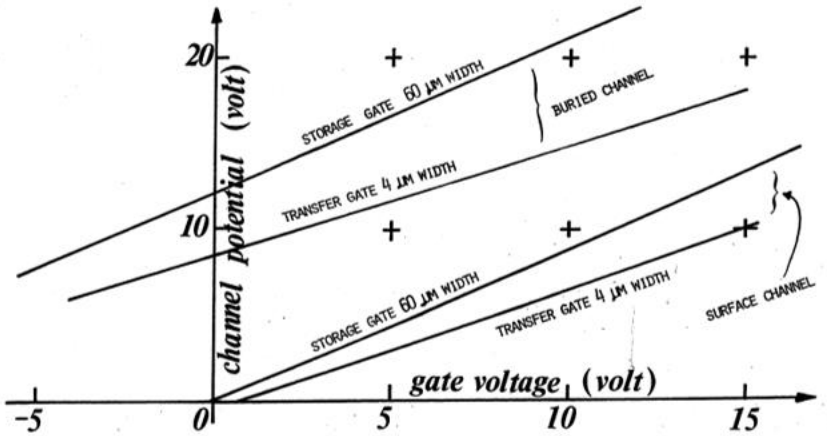


Fig. 2. The actual measured channel potentials plotted against the gate voltage for both surface and buried channel versions.

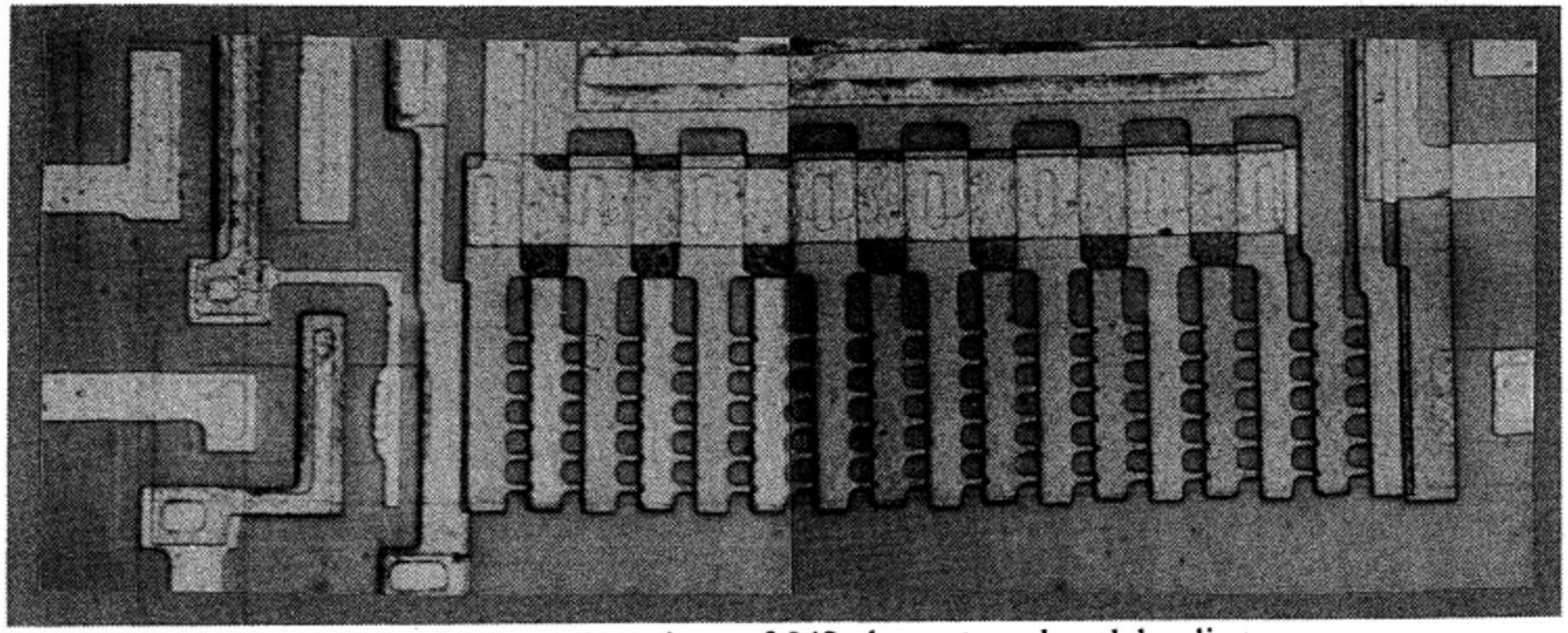


Fig. 3. The end sections of 242 element analog delay line.

Proceedings of the 9th Conference on Solid State Devices, Tokyo, 1977;
Japanese Journal of Applied Physics, Volume 17 (1978) Supplement 17–1, pp. 255–261

Two Phase CCD with Narrow-Channel Transfer Regions

Yoshiaki DAIMON-HAGIWARA

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with no image lag

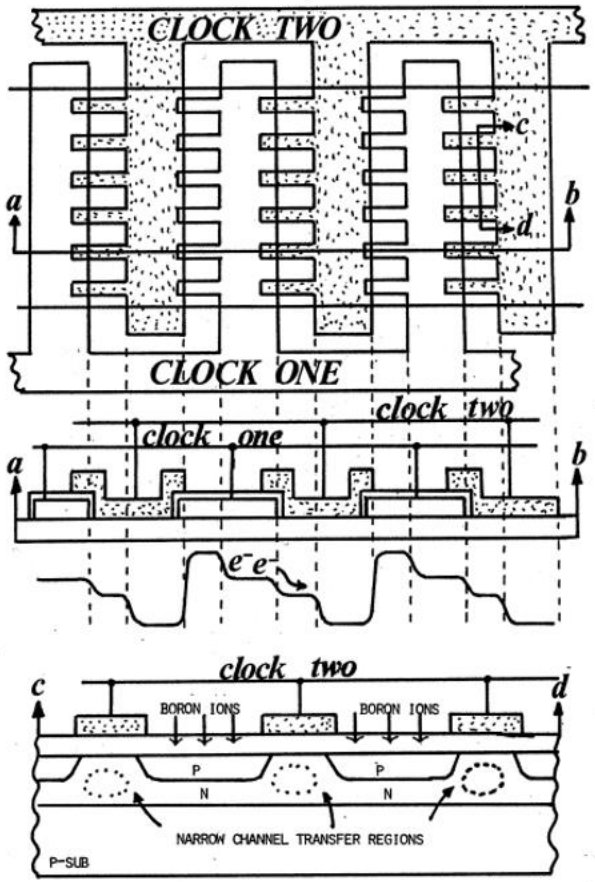


Fig. 1. Top and crosssectional views of the electrode structure for two phase CCD with narrow-channel transfer regions.

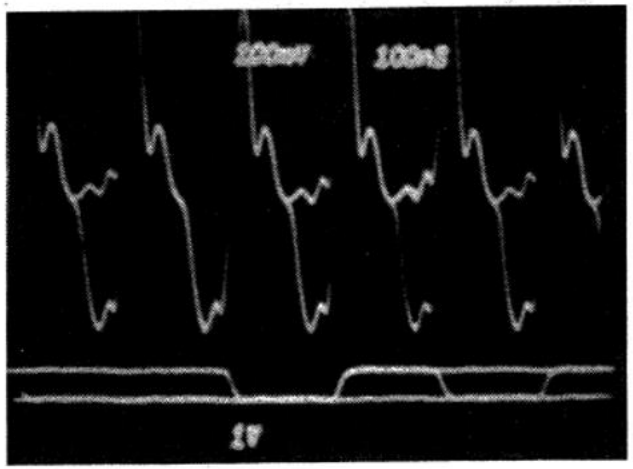


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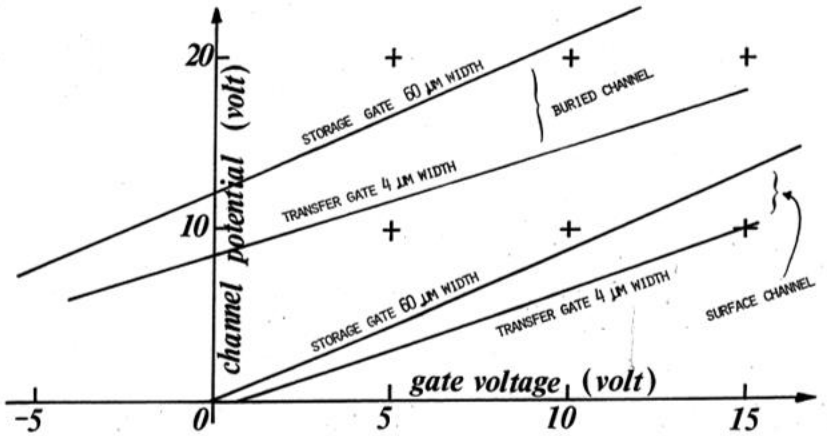


Fig. 2. The actual measured channel potentials plotted against the gate voltage for both surface and buried channel versions.

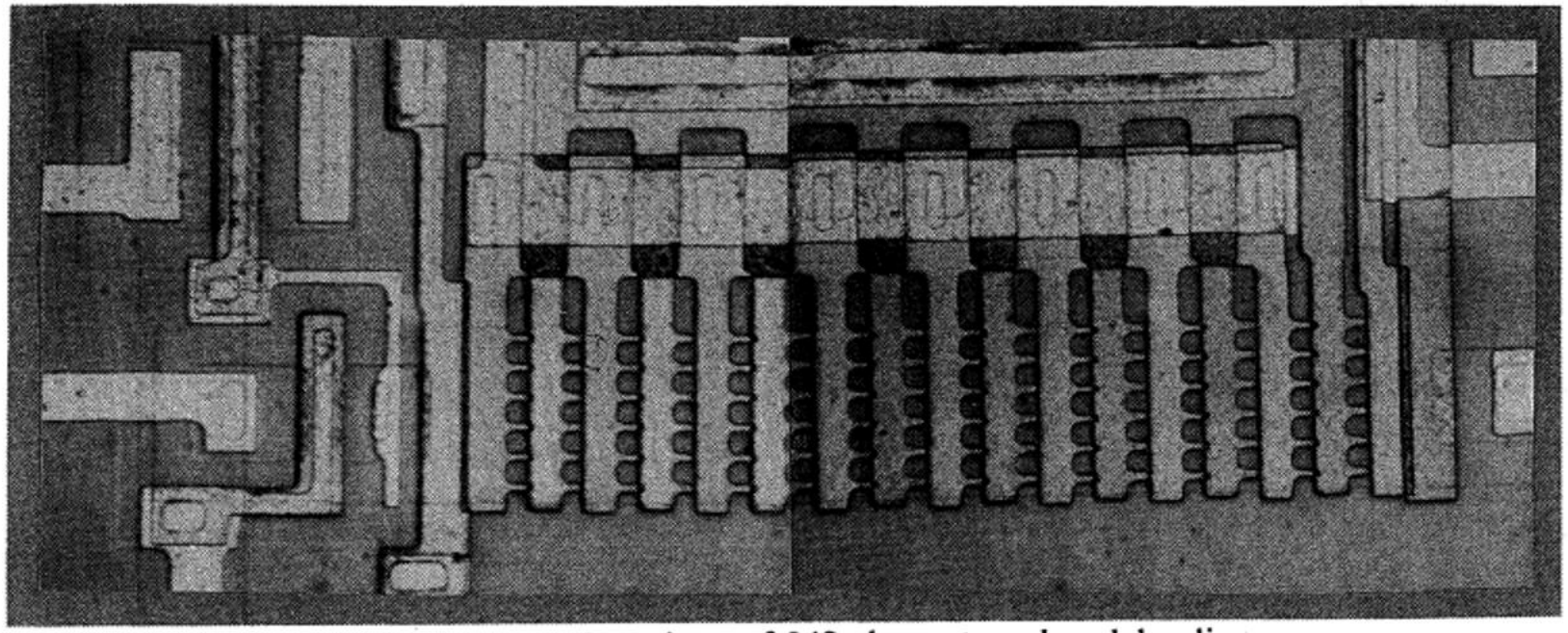


Fig. 3. The end sections of 242 element analog delay line.

Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978;
Japanese Journal of Applied Physics, Volume 18 (1979) Supplement 18-1, pp. 335-340

A 380H × 488V CCD Imager with Narrow Channel Transfer Gates

Yoshiaki Daimon-HAGIWARA, Motoaki ABE† and Chikao OKADA†

Sony Corporation Research Center, Yokohama 240
†Semiconductor Development Division, Yokohama 240

with no image lag

When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of threshold voltage is observed. This narrow-channel effect has been applied successfully in creating an asymmetric potential well under an electrode for two phase CCD operations. The feasibility of this new structure has been confirmed in a 242 element analog delay line and the application is now extended to a 380H × 488V CCD Imager. In the constructed B/W CCD camera,

Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978;
Japanese Journal of Applied Physics, Volume 18 (1979) Supplement 18-1, pp. 335-340

A 380H × 488V CCD Imager with Narrow Channel Transfer Gates

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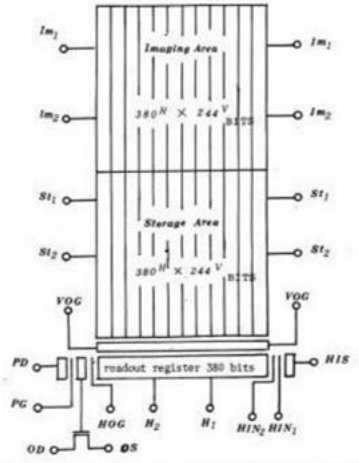


Fig. 1. The block diagram of a 380 H×488 V CCD imager in frame transfer organization.

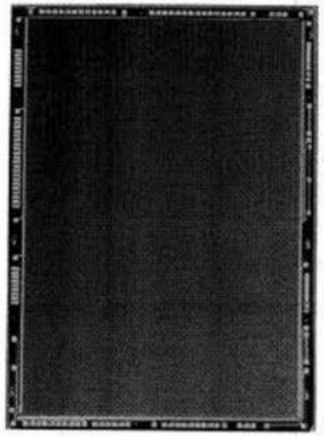


Fig. 3. Photomicrograph of the 380 H×488 V CCD imager. The chip size is 14.6 mm by 10.1 mm.

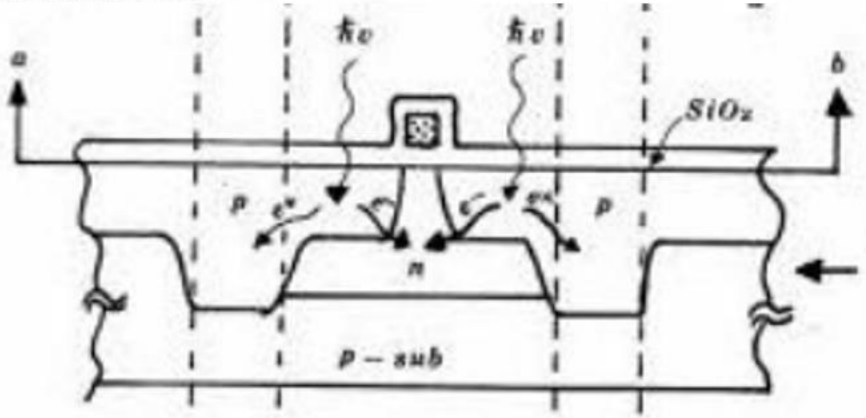


Fig. 2. Top and cross sectional views of the electrode for two phase CCD structure.

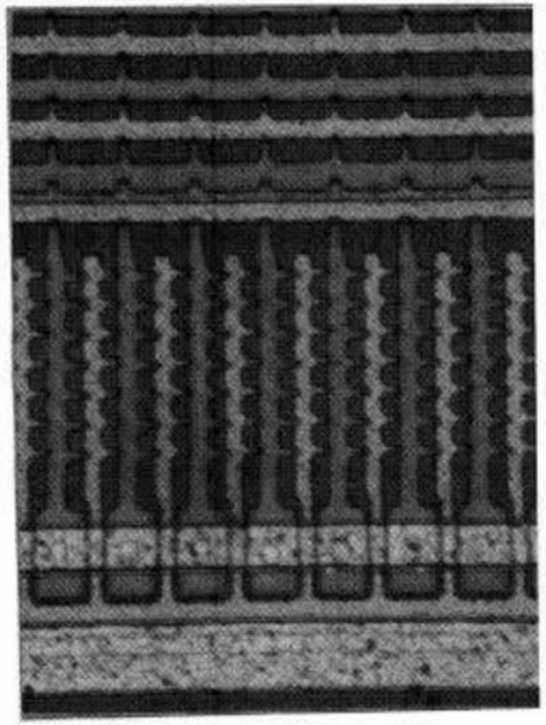


Fig. 5. The horizontal readout register with 14 μm-pitch-per bit electrode structure.

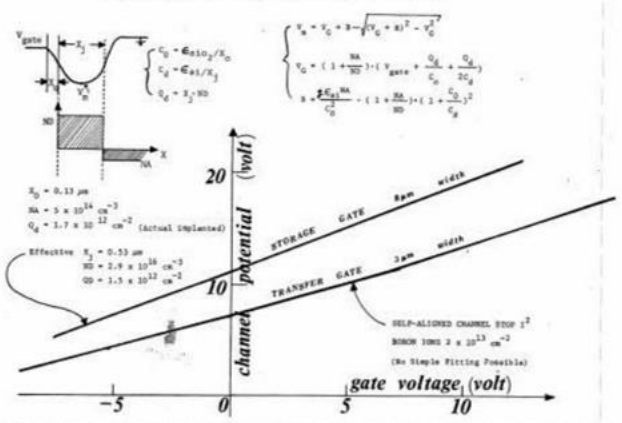


Fig. 9. The actual measured channel potentials plotted against the gate voltage for the buried channel version. The curve fitting with the simple relations by depletion approximation gives the effective values of X_j, ND and QD as seen in the figure.

with no image lag

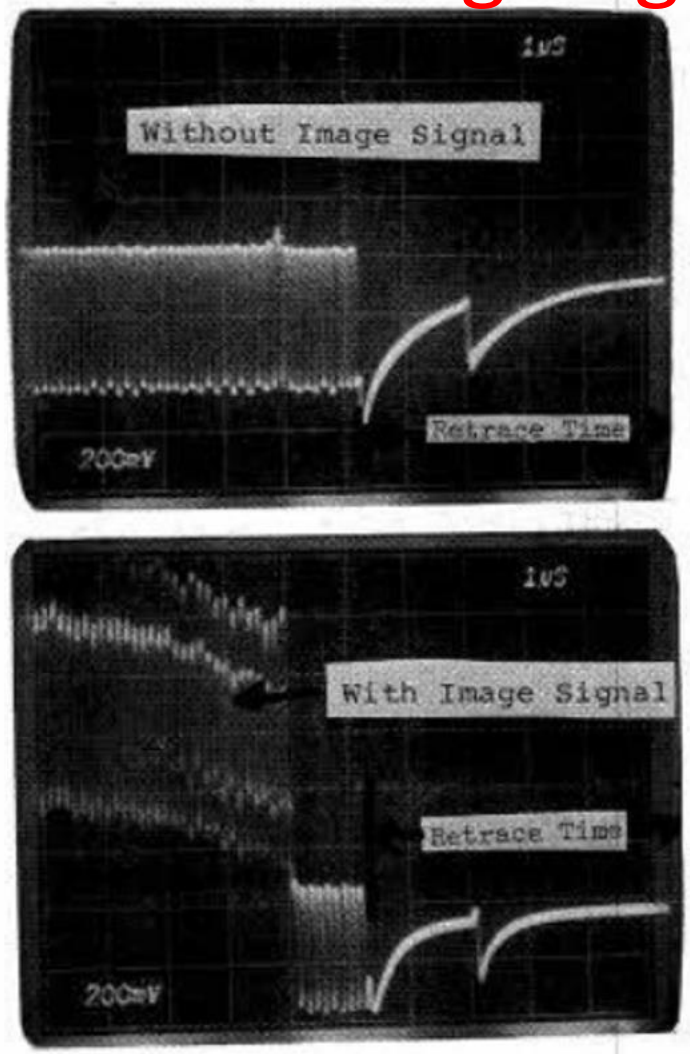


Fig. 12. The output wave forms of the horizontal readout register at the tailing end of a TV picture line, that is, right before the horizontal retrace time. The comparison of the output levels with and without image signal gives the dark current level of the imager.

High-Density and High-Quality Frame Transfer CCD Imager with Very Low Smear, Low Dark Current, and Very High Blue Sensitivity

Yoshiaki Hagiwara, *Member, IEEE*

with no image lag

Abstract—**When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of the threshold voltage is observed. This narrow channel effect has been applied successfully in creating an asymmetric potential well under an electrode for two-phase CCD operation. The feasibility of this structure has been confirmed in a 242-element analog delay line. The application is now extended to a 800 H × 492 V frame transfer-type buried channel CCD imager with 14.31818 MHz frame shift, which results in a very low smear level of 0.01%, which is good enough for low-cost multimedia video camera applications.**

I. Introduction

Since their introduction in the 1970's, CCD sensors have improved dramatically. CCD's, however, have a number of disadvantages in multimedia applications. Ackland emphato the interline-type CCD imager, yet holds a large signal charge packet. The on-chip frame memory can also be used as a buffer memory for various multimedia applications.

On these points, some brief discussions regarding a new frame-transfer CCD structure and their results are reported. The new structure is bipolar-type image sensing element with a p-n-p SUB structure. The structure was originally proposed by the author in 1975 [8]. Some related ideas, hidden in the form of difficult legal wording, and other efforts, disclosed in the form of published papers, will be reviewed and discussed in details to explain the background and originality of the author's proposed structure.

II. Bipolar Image Sensing Element

High-Density and High-Quality Frame Transfer CCD Imager with Very Low Smear, Low Dark Current, and Very High Blue Sensitivity

Yoshiaki Hagiwara, *Member, IEEE*

with no image lag

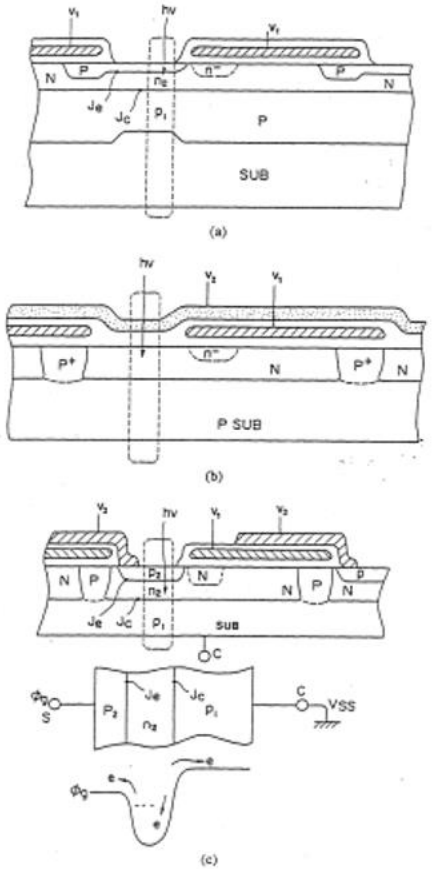


Fig. 1. (a) Basic structure of bipolar junction-type image sensing element now widely adapted in interline transfer CCD imagers. The hatched regions (V_1) covering the top are the polysilicon electrodes for the vertical CCD shift registers. The sensor regions are not covered by the polysilicon electrodes. (b) MOS capacitance-type imaging sensing element quoted in the author's invention of November 10, 1975, and known then as a conventional structure. The top layer (V_2) can be either a thin polysilicon or a transparent sensor electrode. (c) Bipolar junction-type image sensing element with a top wiring lead (V_3). In this case, as a simple example, the first p-region (P_1) is set equal to the silicon substrate.

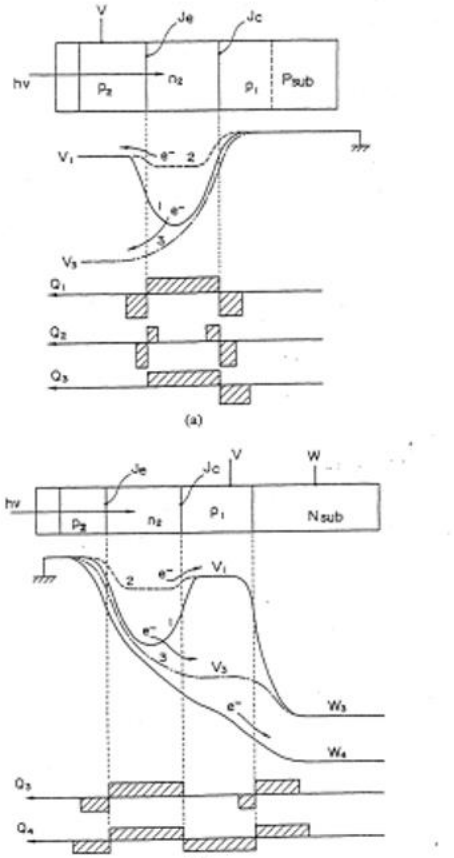


Fig. 2. (a) Operations of bipolar junction-type image sensing element when the substrate is chosen to be the same as the P1 region. Q1, Q2, and Q3 are fixed charges in the depletion regions. (b) Operations of a bipolar junction-type image sensing element when the substrate is different from the P1 region. Q3 and Q4 are fixed charges in the depletion regions, where no mobile carriers are present.

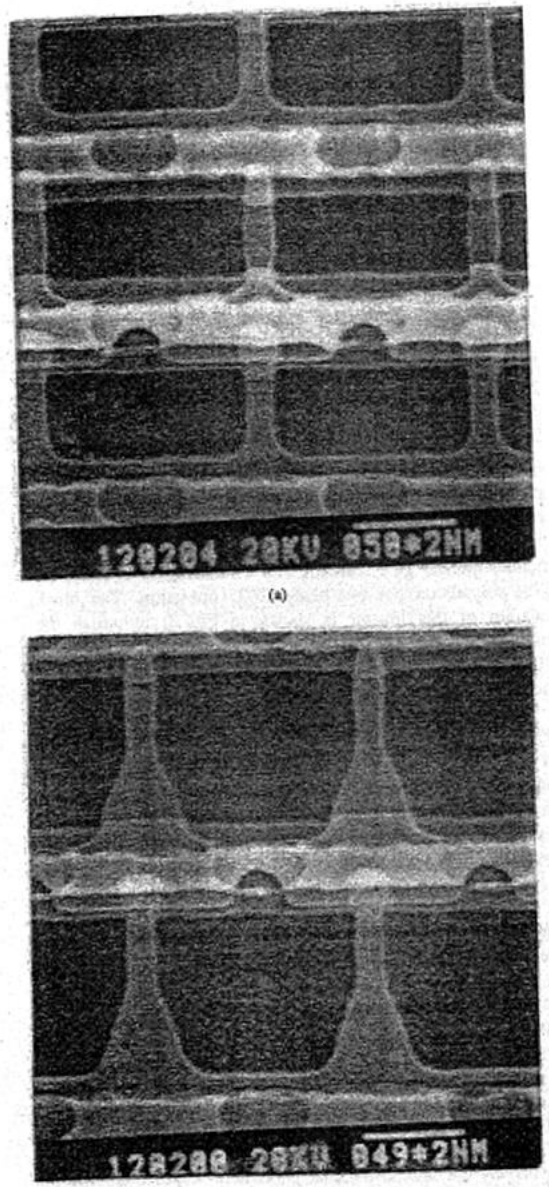


Fig. 4. (a) SEM picture of storage area. Cell size is 11 μm H × 9 μmV. (b) SEM picture of imaging area. Cell size is 11 μm H × 13 μmV.

TABLE II
DEVICE CHARACTERISTICS

Optical Format	2/3 inch
Transfer System	Frame Transfer
Total Number of Pixels	800 H x 492 V
Chip Size	10.0 mm H x 12.5 mm V
Cell Size Imaging Area	11 μm H x 13 μm V
Cell Size Storage Area	11 μm H x 9 μm V
Silicon Substrate	p-type (100) 10-15 ohm-cm
Horizontal Resolution	560 TV lines
Vertical Resolution	350 TV lines
Smear	0.01 %
Noise	10 electrons/pixel
Output Gain	4 μV/e
Lag	Undetectable
Dynamic Range	83 dB
Charge Capacity	200,000 electrons/pixcel
Minimum Illumination (F1.4)	1.6 lux

with no image lag

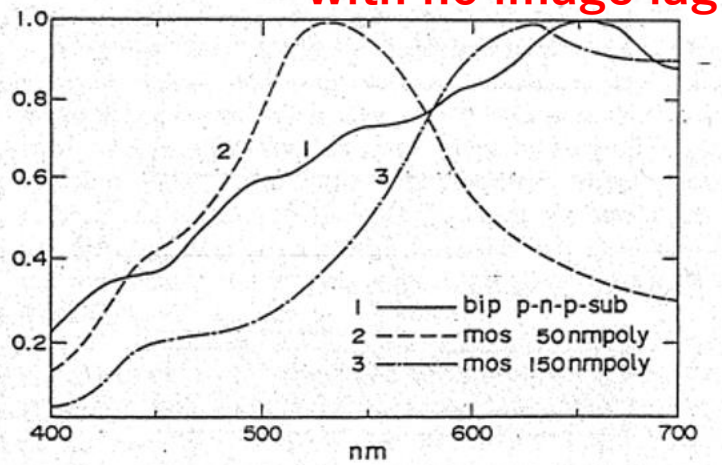
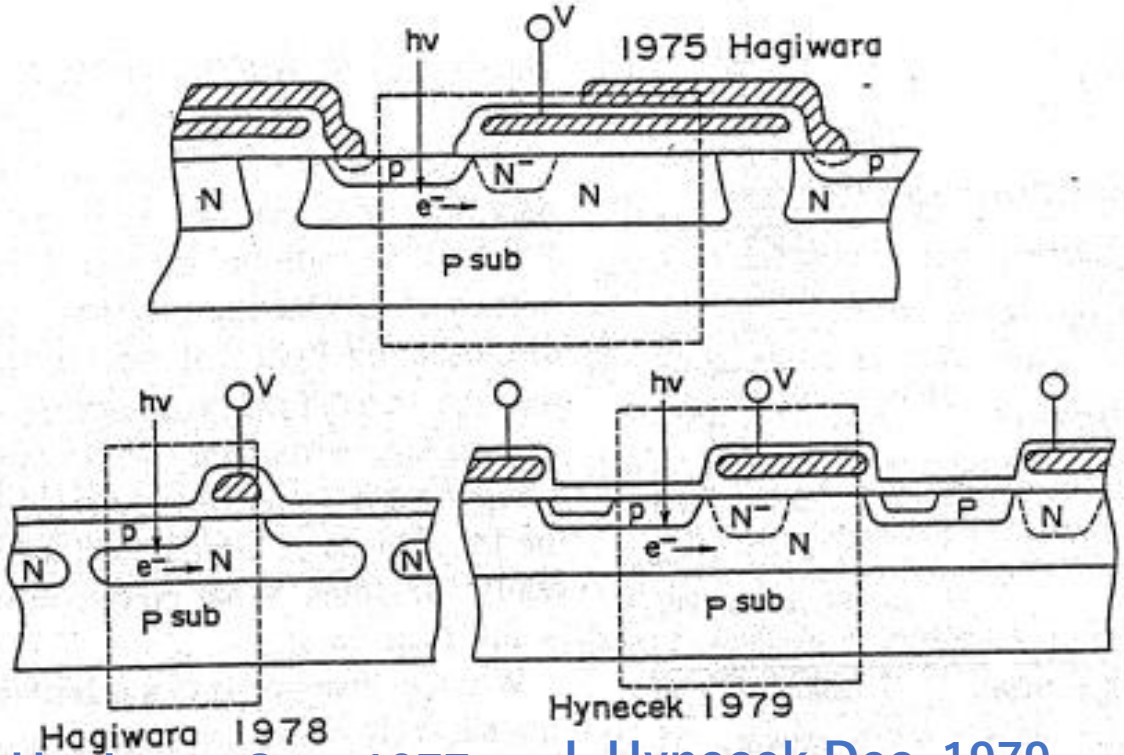


Fig. 7. Relative spectrum response. The relative response of the bipolar-type SiO_2–P2–N1–P1–SUB structure is compared with poly–SiO_2–N2–P(SUB) structures of the polysilicon thickness of 50 and 150 nm.

High-Density and High-Quality Frame Transfer CCD Imager with Very Low Smear, Low Dark Current, and Very High Blue Sensitivity

Yoshiaki Hagiwara, *Member, IEEE*

Y.D. Hagiwara Nov 10, 1975

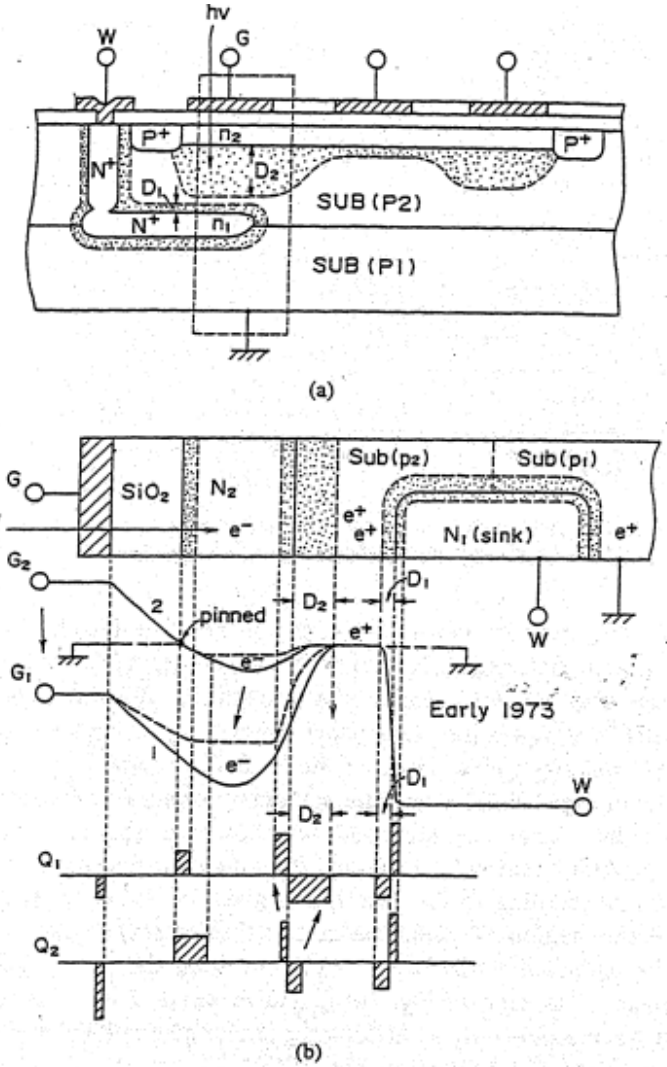


Y.D. Hagiwara Sep, 1977

J. Hynecek Dec, 1979

[16] J. Hynecek, "Virtual phase CCD technology," in *IEEE Proc. IEDM*, Dec. 1979, pp. 611–614.

J.M. Early Dec 3, 1973



[17] J. M. Early, U.S. Patent 3896485, Dec. 3, 1973.

The First Pinned Photodiode was invented by Hagiwara at Sony in 1975 in order to realize the in-pixel electric shutter function. The evidence is given in the Japanese patent application JPA1975-127646, which defined the pinned-surface triple-junction dynamic-thyristor type Pinned Photodiode.

The evidence are given in the Japanese Patent Applications, JPA1975-127646, JPA1975-127646 and JPA1975-134985.

Fig 7 in JPA1975-127646

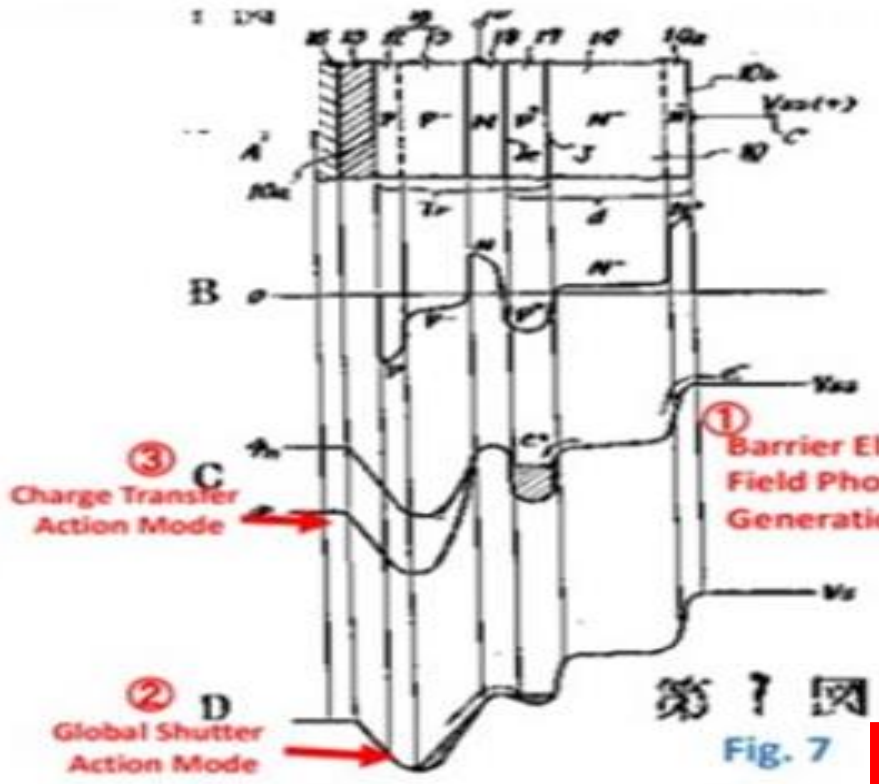


Fig 7 in JPA1975-127647

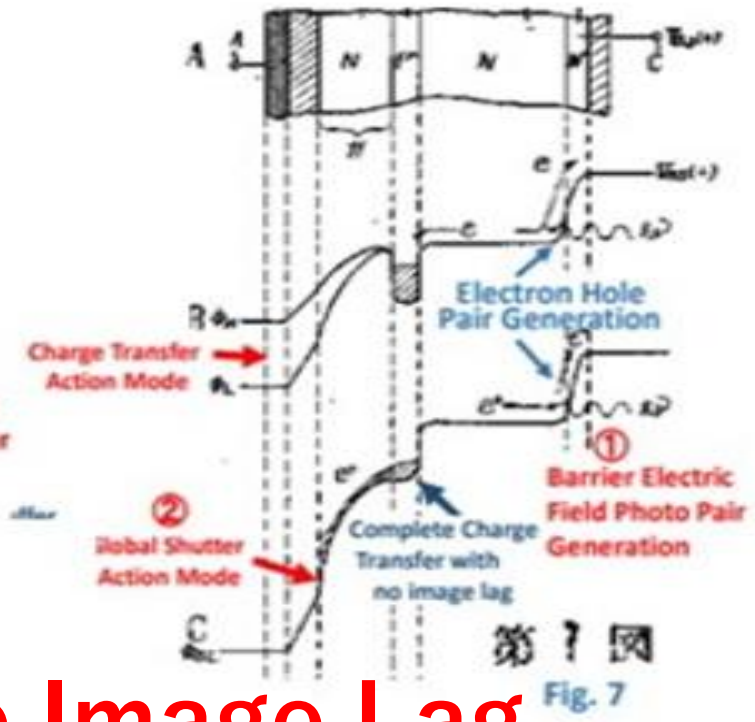
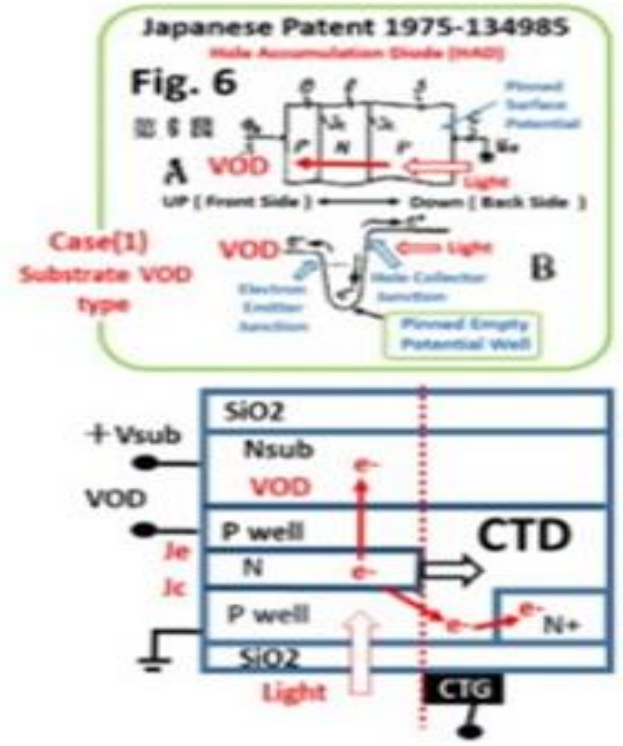


Fig 6 in JPA1975-134985



No Image Lag

PPD with in-pixel VOD function was drawn in Hagiwara Lab Note in Feb 1975.

June 26, 2020

Sony's Representative Inventions Supporting Stacked Multi-Functional CMOS Image Sensors

Sony Corporation

Sony Semiconductor Solutions Corporation

Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

ELECTRICAL ENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

Asked 8 years, 10 months ago Modified 2 years, 8 months ago Viewed 6k times

6

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

Share Cite Follow

edited Aug 16, 2018 at 19:17

answered Sep 21, 2013 at 14:34



placeholder

29.6k ● 10 ● 60 ● 110

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

Hagiwara_in_1975_invented_NEC_1982_Buried_Photodiode_KODAK_1984_Pinned_Photodiode_and_Sony_1987_HAD

The first Pinned Photodiode was developed by Hagiwara Team and reported in Tokyo at the SSDM Conference on Sep 1978. It was in the form of the P+NPsub double junction type photodiode with the pinned P+ surface hole accumulation region, which is pinned and fixed at the P substrate grounded potential by the adjacent heavily doped P+ channel stops.

NEC developed in 1982 also a double junction photodiode and named it as Buried Photodiode.

Kodak also developed in 1984 a double junction photodiode and named it as Pinned Photodiode.

In 1987, Sony produced a triple junction photodiode and named it as Hole Accumulation Diode (HAD) and used it the portable and digital video cameras.

However, they are all similar to the double and triple junction photodiodes invented in 1975 by Hagiwara at Sony. Evidence is given by JPA1975-127646, JPA1975-127647 and JPA1975-134985.

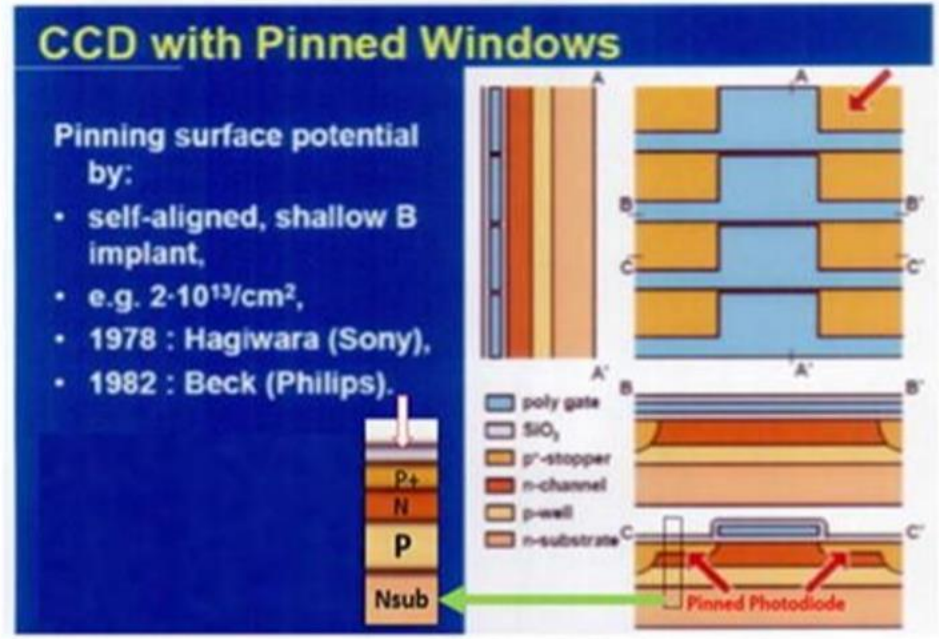
Hagiwara reported the Pinned Windows and Pinning Surface Potential in 1978 based on his 1975 invention of the P+NPNsub junction type Pinned Photo diode.

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO. 12, DECEMBER 2006

The Hole Role in Solid-State Imagers

Albert J. P. Theuwissen, *Fellow, IEEE*

Despite these advantages, notice that parts of the depleted n-type CCD channels are not covered by gate material. In this way, their electrostatic potential is not defined! Such a structure will suffer from serious charge transport issues during its operation, because charge can and will be trapped in local potential pockets. The effect can simply be solved by defining the potential in the open areas through an extension of the p^+-channel stopper. A simple self-aligned p-implant of $2 \cdot 10^{13}/cm^2$ B-ions after the gate construction is sufficient to extend the channel stop area to the gate edge and, consequently, fix the potential in the open areas. The result after this self-aligned implant is shown in Fig. 4. The presence of enough holes plays a crucial role in fixing the potential for the regions normally "beyond control" of the gates. [Is this structure the mother of the PPD or buried diode or hole-accumulation device (HAD)?]



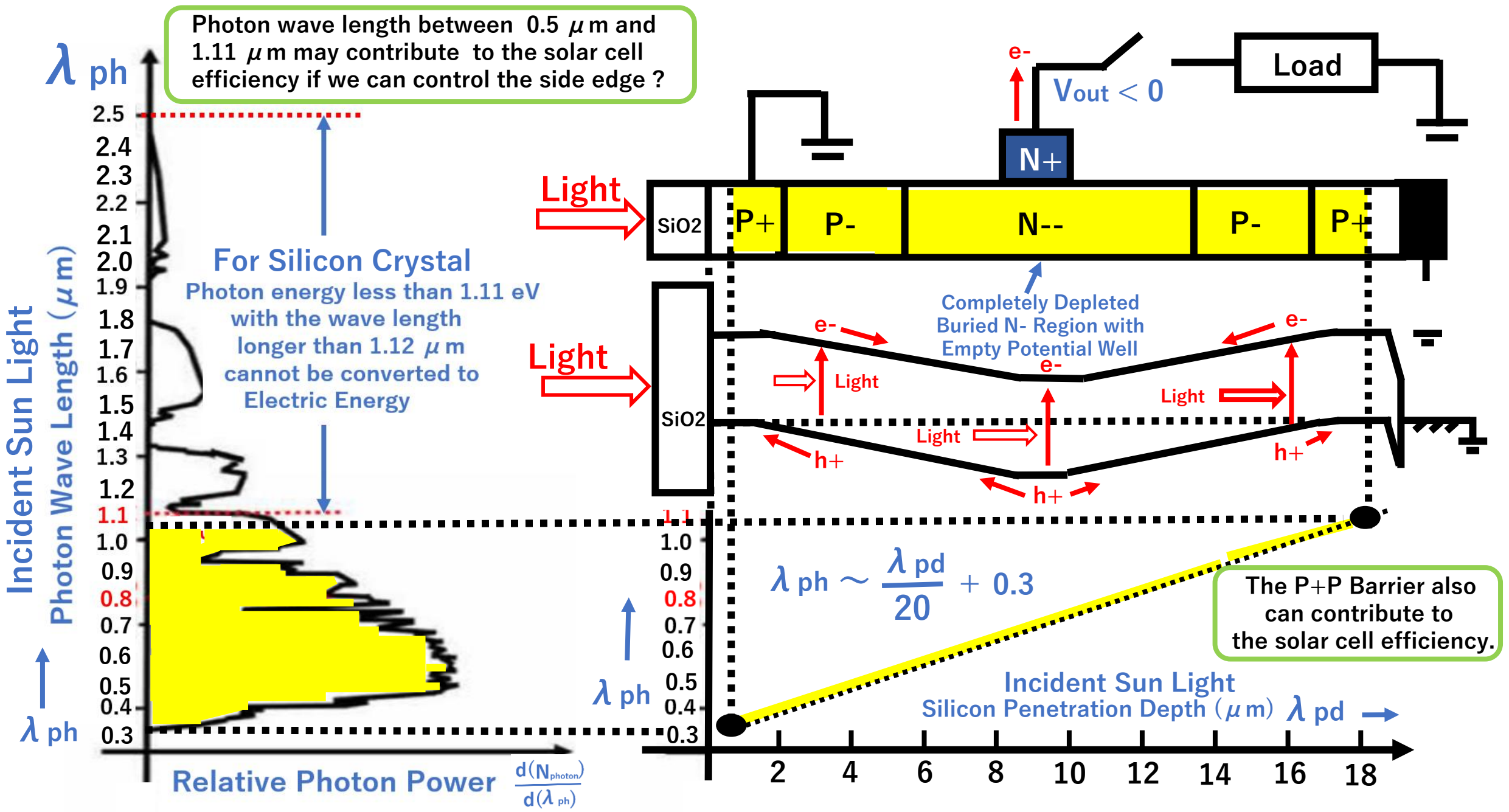
Albert Theuwissen quoted Hagiwara 1978 paper and explained the importance of hole role in image sensors @ Workshop on CMOS Imaging, Duisburg May 16, 2006

Direct Quotation

The presence of enough holes plays a crucial role in fixing the potential for the regions normally "beyond control" of the gates. [Is this structure the mother of the PPD or buried diode or hole-accumulation device (HAD)?]

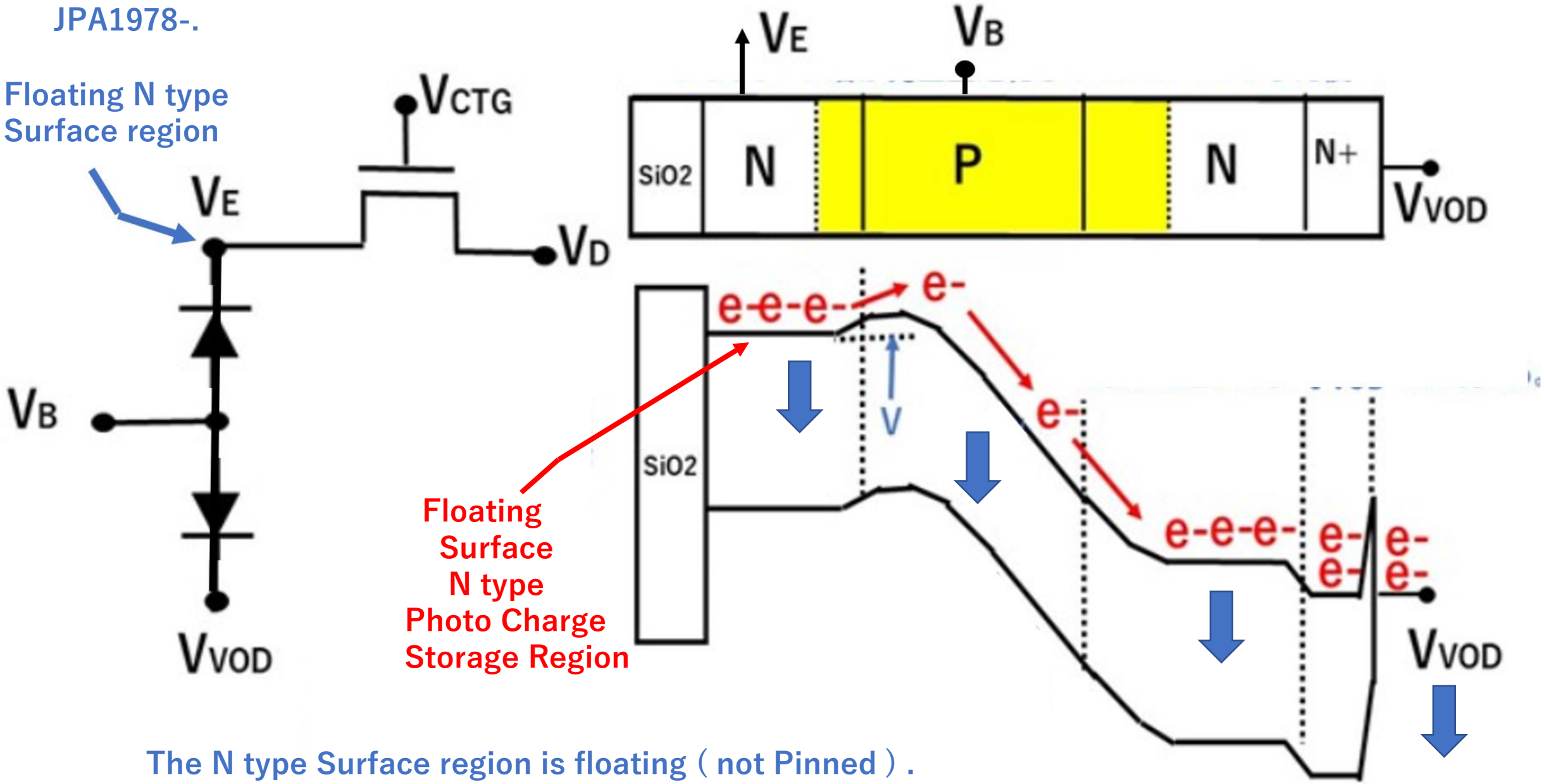
Quoted directly from IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL.53, No.12, DEC 2006

The P+P-N-P-P+ double junction type Solar Cell may have much higher efficiency



JPA1978-.

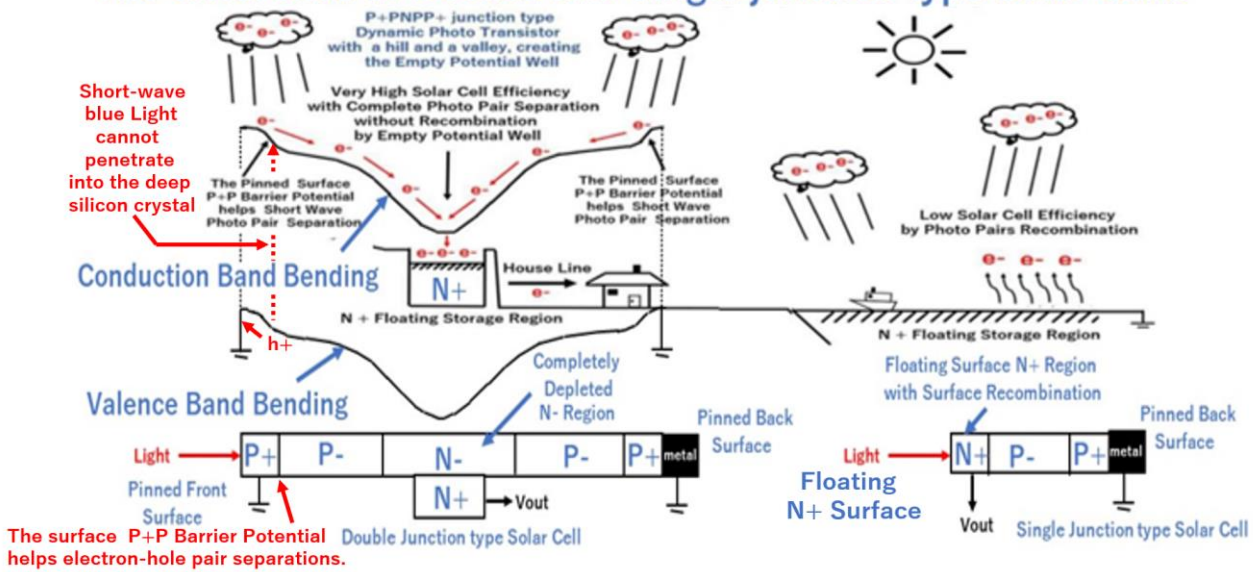
Floating N type
Surface region



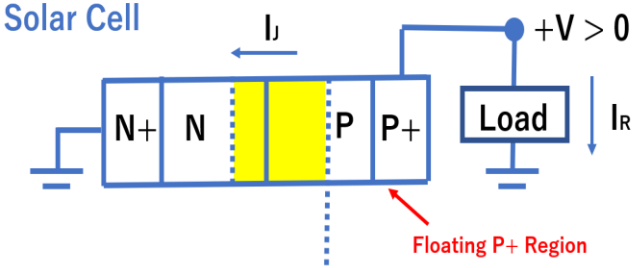
The N type Surface region is floating (not Pinned) .
The anti-blooming VOD does not function well because the N-type surface will also be pulled down as the VOD voltage is pulled down deeper.

True History of Photodiode

The difference of Double and Single junction type Solar Cells

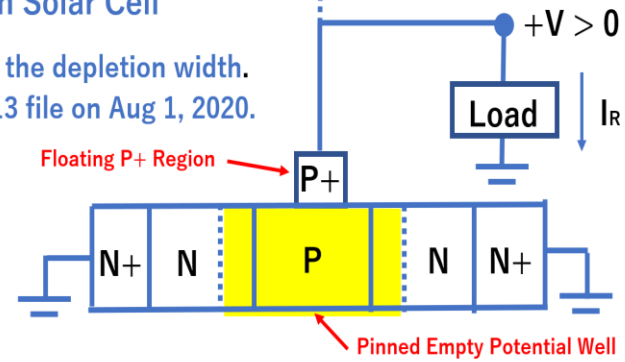


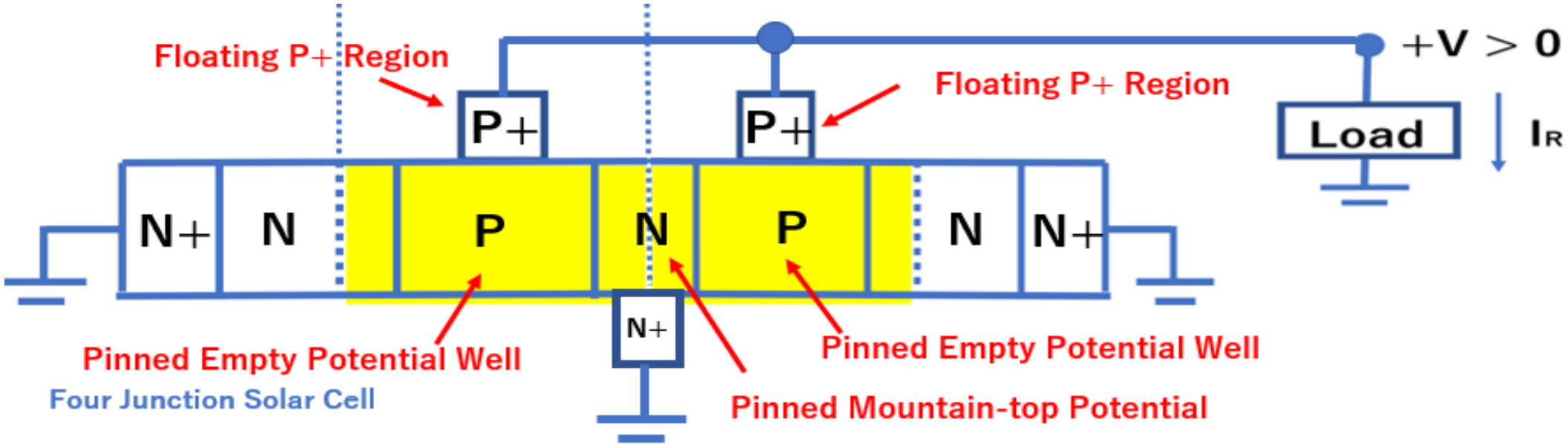
Single Junction Solar Cell



Double Junction Solar Cell

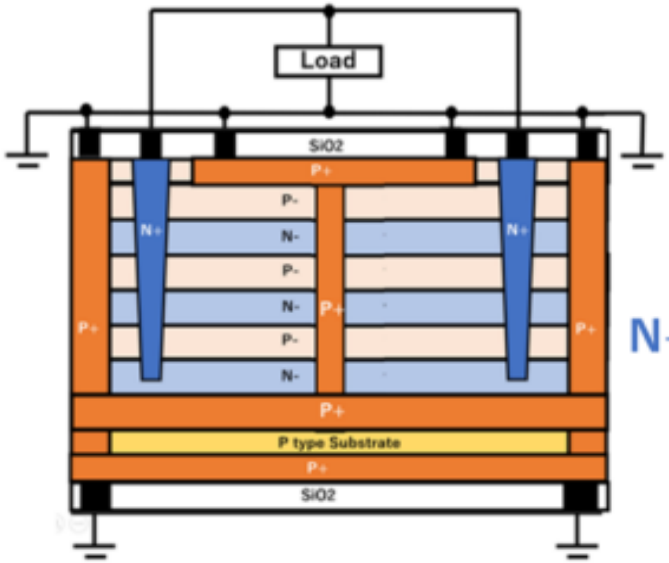
We can double the depletion width.
JPA2020-131313 file on Aug 1, 2020.

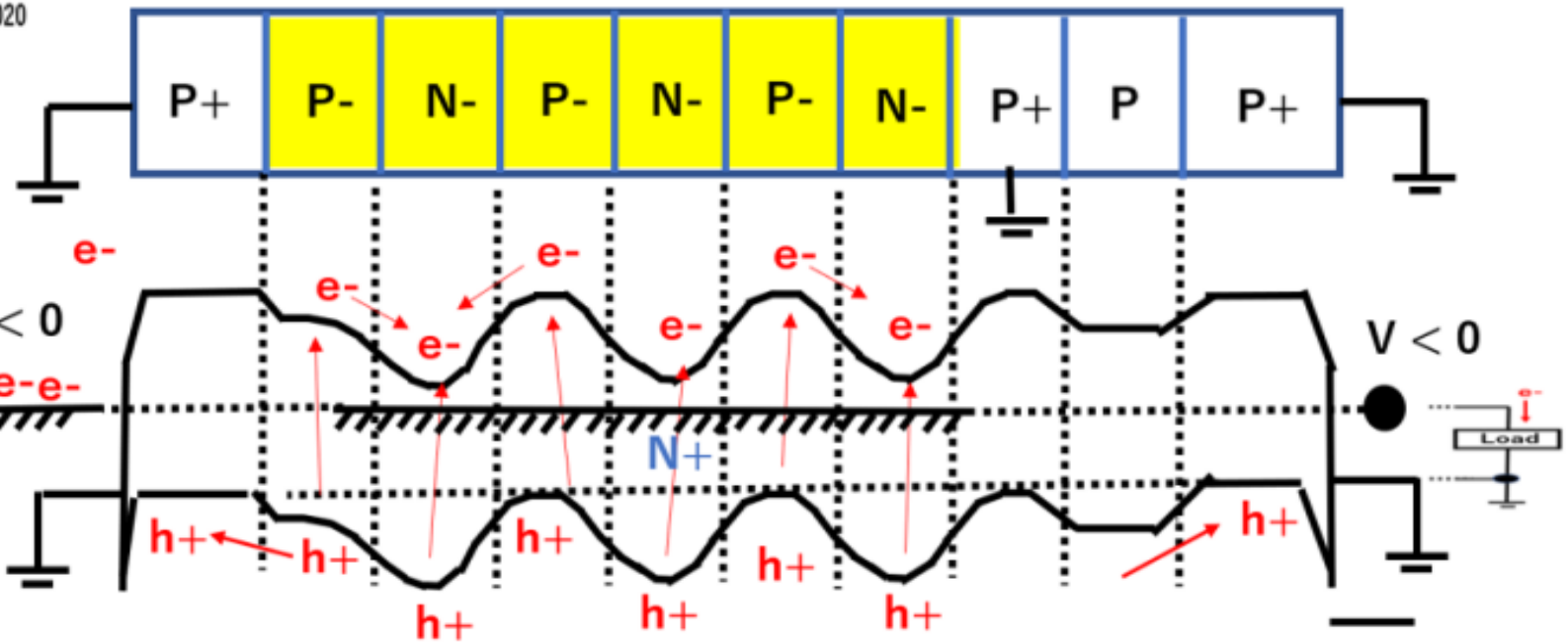


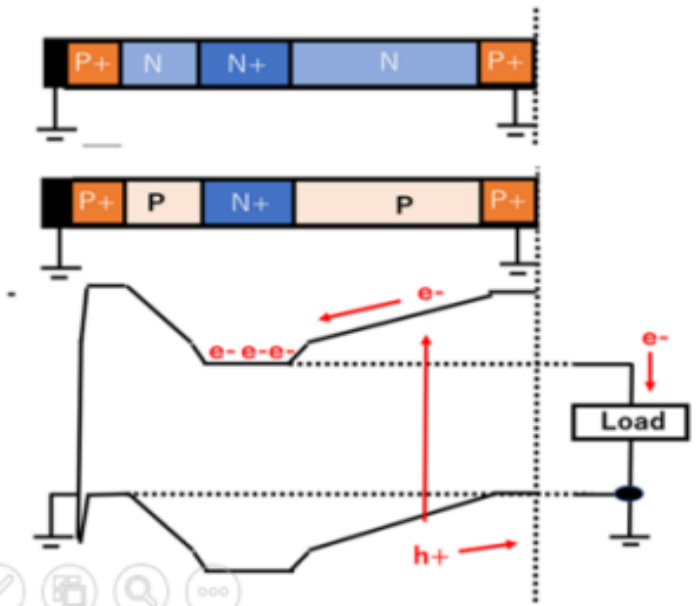


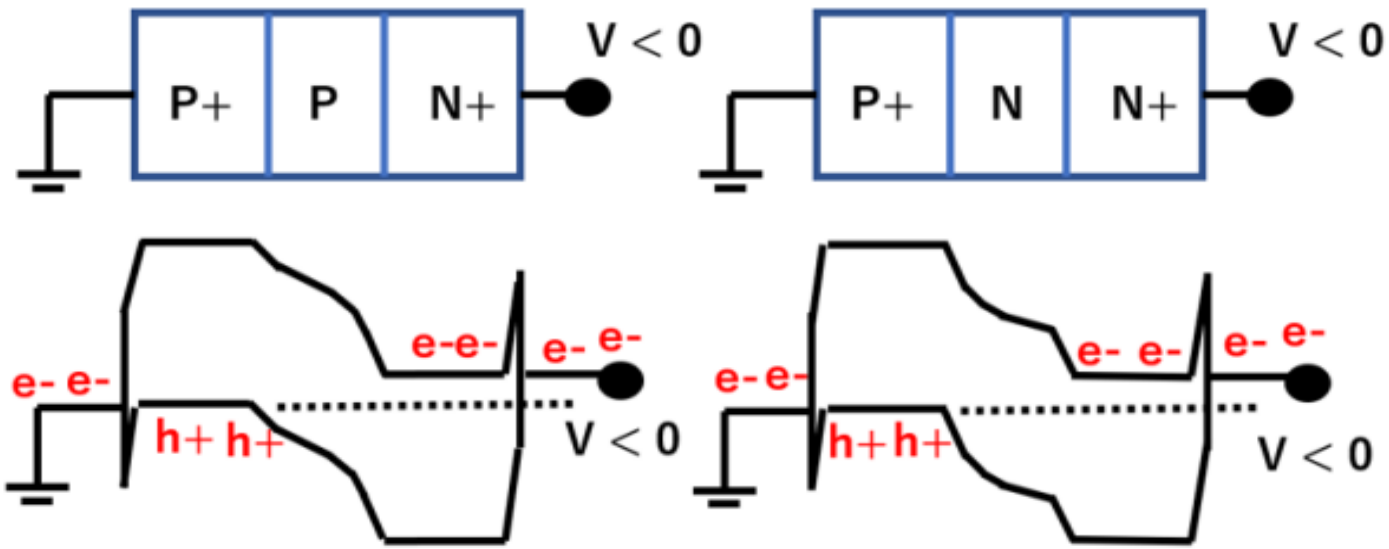
Multi-junction Pinned Photodiode with Completely Depleted of Photo Electron and Hole

Multi-junction Pinned Photodiode type Solar Cell Structure,
based on Double Junction Solar Cell , defined in JPA2020-131313, applied Aug. 1, 2020
by Yoshiaki Hagiwara, Sept 12, 2022



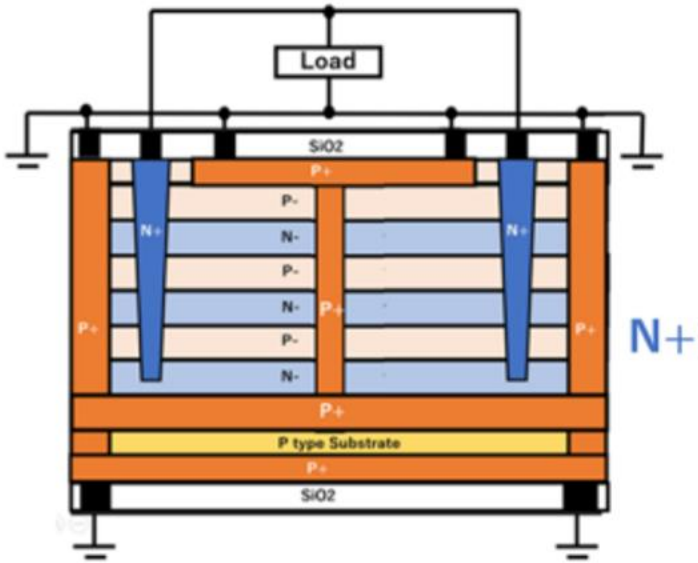


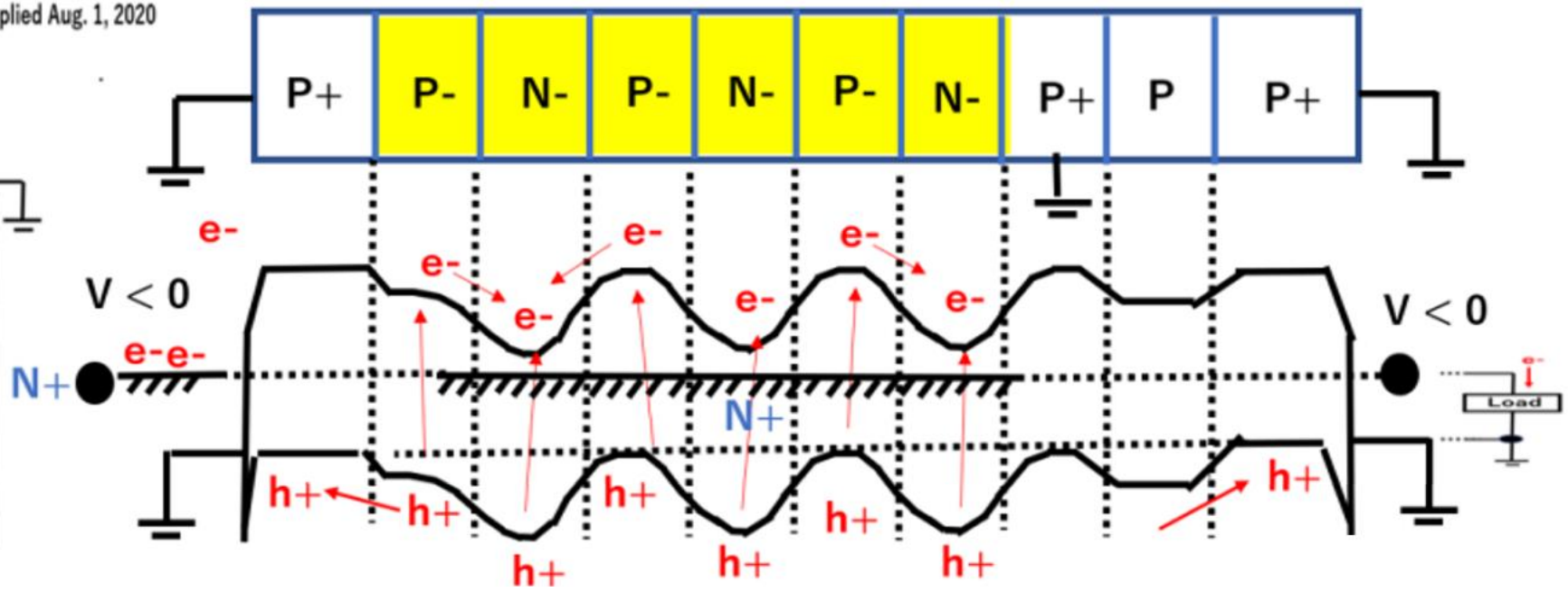


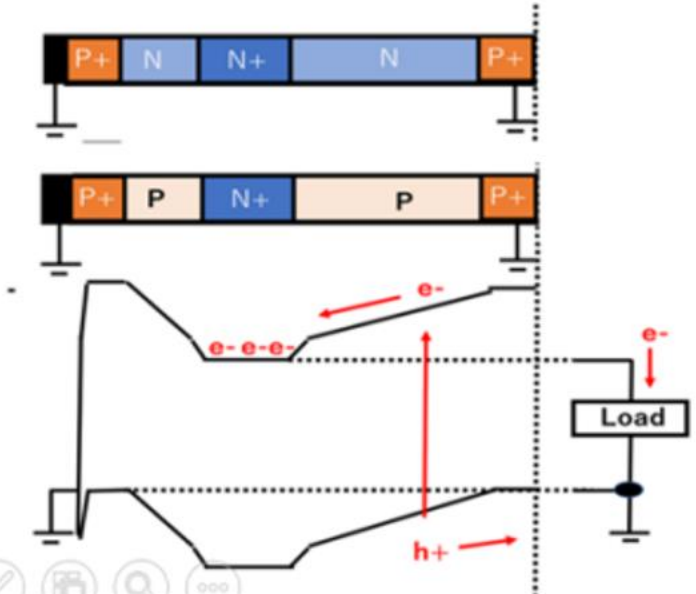


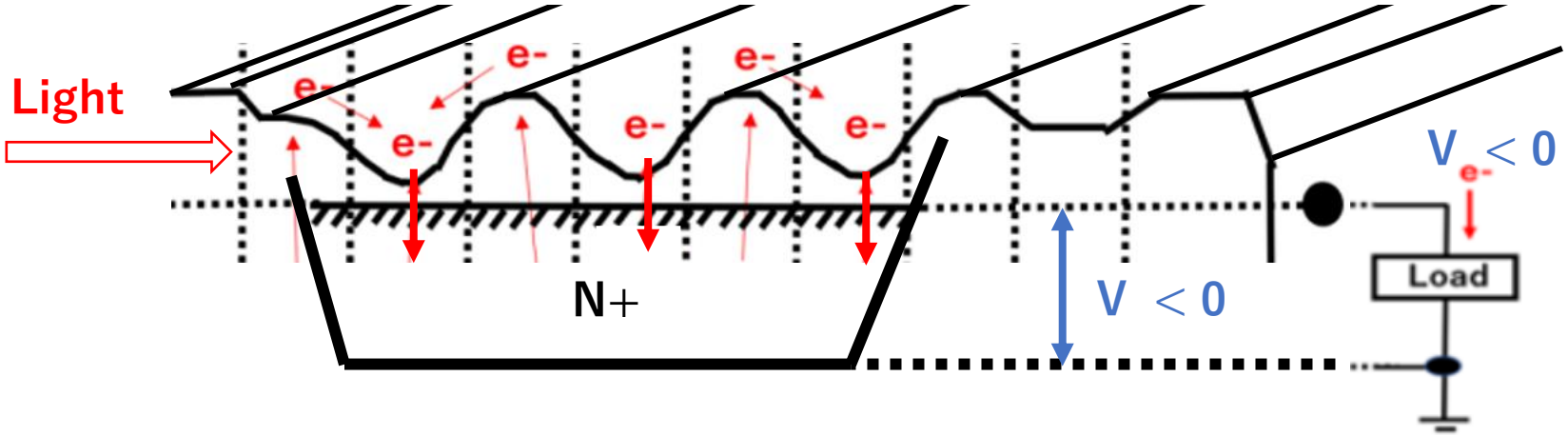
Multi-junction Pinned Photodiode with Completely Depleted of Photo Electron and Hole

Multi-junction Pinned Photodiode type Solar Cell Structure,
based on Double Junction Solar Cell , defined in JPA2020-131313, applied Aug. 1, 2020
by Yoshiaki Hagiwara, Sept 12, 2022









NIKKEI MICRODEVICES 1987年10月号

pp.60～67

ICX022

38万画素に達した固体撮像素子

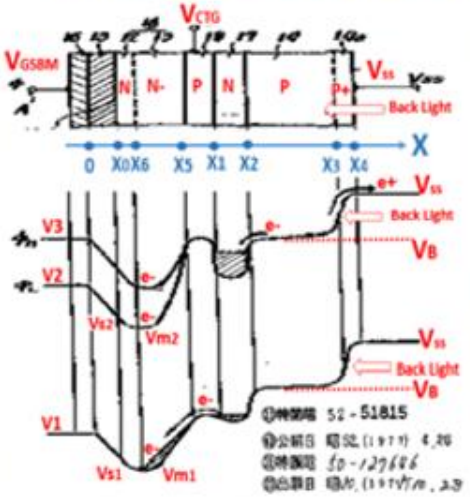
最低照度5 lxの高感度インターライン型CCD

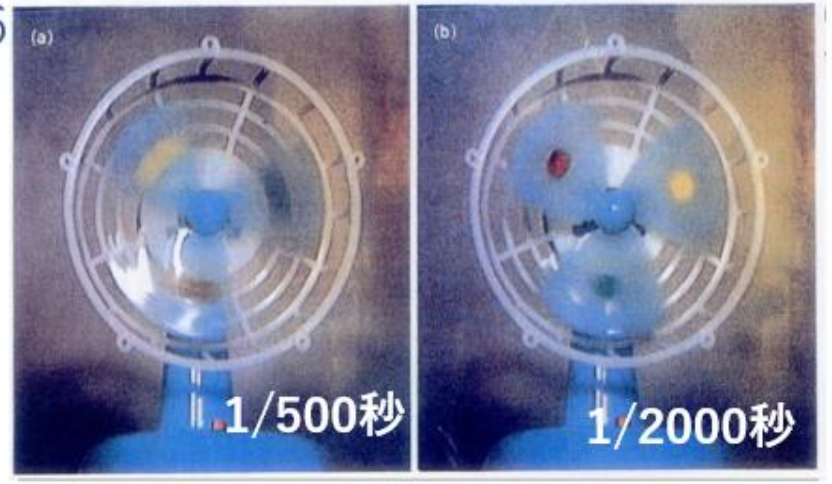
基板に余剰電荷を掃き出し,可変電子シャッタを実現

ソニー 半導体事業本部 CCD 事業部
浜崎 正治
鈴木 智行
賀川 能明
石川 貴久枝
宮田 克郎
ソニー国分セミコンダクタ CCD 製造部
神戸 秀夫

最も一般的な固体撮像素子であるインターライン型 CCD で,
2/3 インチで 38 万と大規模な画素数を持つ素子をソニーが製品化した。
画素面積が小さくなることで減少する信号量を確保するため,
縦型オーバーフロー・ドレインを採用して開口率を上げ,
補色フィルタで光の利用効率を上げた。
さらに界面準位からの暗電流を抑えている。
この結果, 81 dB のダイナミック・レンジが得られた。

JPA1975-127646







JPA1975-127646の図７と同一受光構造である。受光表面はGNDにピン留めされた、P+NPNsub 接合型、 すなわち Triple 接合型の Pinned Photodiode.



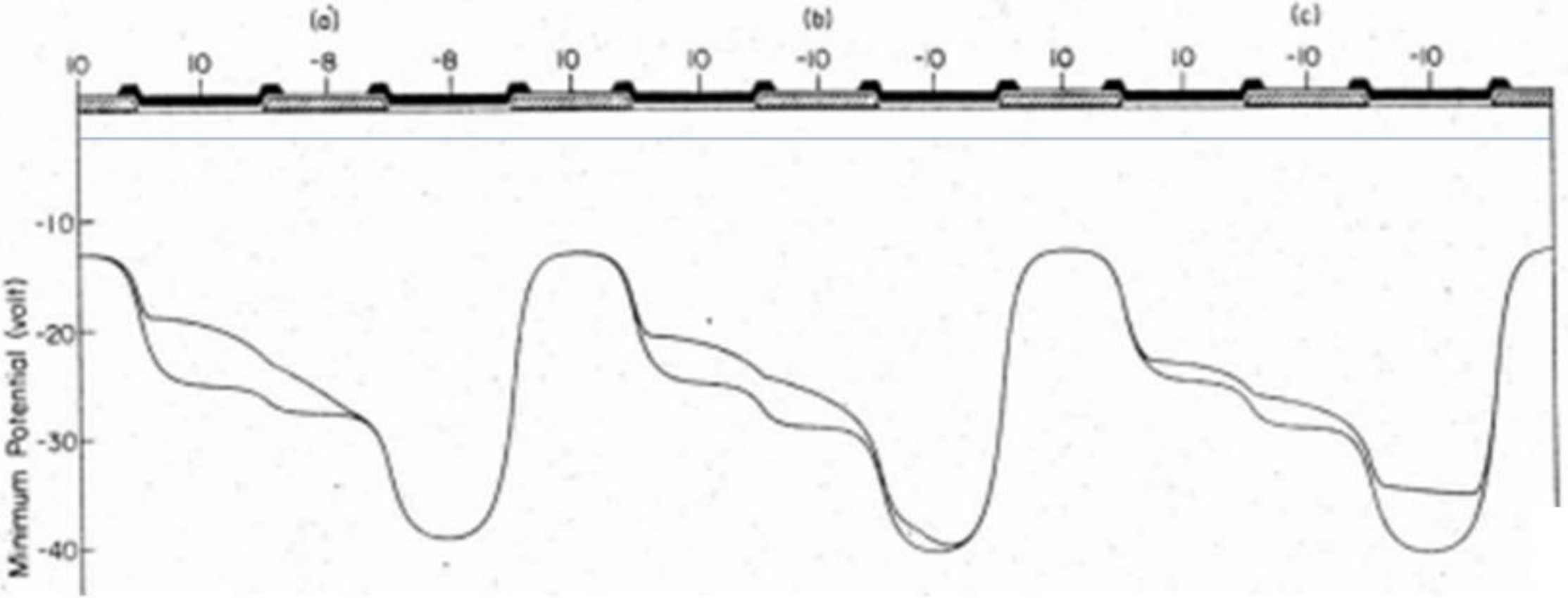
ICX022

電子shutterの動作原理の説明図

図 4

SONYの1987年発表の電子シャッター機能付き Hole Accumulation Diode (HAD) 受光素子構造

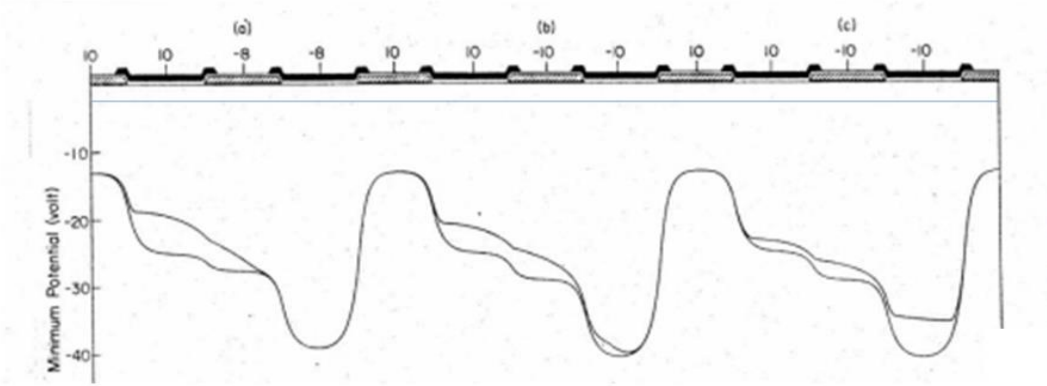
Exact Numerical Computer Simulation of Charge Transfer Action in Buried Channel CCD presented in ISSCC1974 by Yoshiaki Daimon-Hagiwara



for details see the PhD Thesis by Yoshiaki Daimon-Hagiwara on June 1975 from Caltech.

Caltech_1975_PhD_Thesis_Yoshiaki_Daimon_Hagihara.pdf

Exact Numerical Computer Simulation of Charge Transfer Action
in Buried Channel CCD presented in ISSCC1974 by Yoshiaki Daimon-Hagiwara



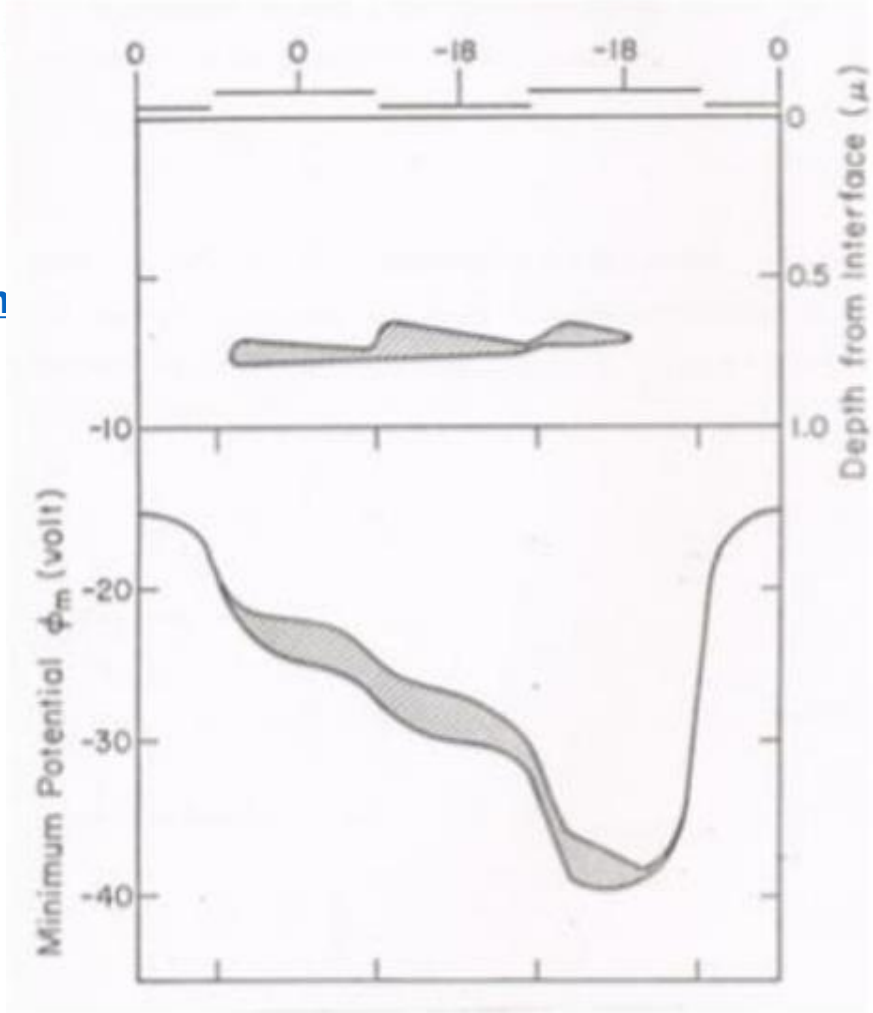
for details see the PhD Thesis by Yoshiaki Daimon-Hagiwara on June 1975 from Caltech.

[Caltech_1975_PhD_Thesis_Yoshiaki_Daimon_Hagih]



Prof. James McCaldin and Hagiwara

My PhD thesis paper
on buried channel CCD
at ISSCC1974, in Philadelphia, USA





Prof. T. C. McGill



Prof. C. A. Mead

True History of Photodiode

(1) Single Junction Type Dynamic Photodiode was used in image sensors before 1970

(2) CCD/MOS type dynamic Photodiode was invented in 1970 with no image lag with the Pinned Gate.

(3) Double Junction type Dynamic Photodiode invented by Philips in June 9, 1975 with RC delay time.

(4) Triple Junction type Dynamic Photodiode with the pinned surface invented by Sony in Oct 23, 1975.



⑪特開昭 51－150288

⑬公開日 昭51.(1976) 12 23

㉑特願昭 51－65705

㉒出願日 昭51.(1976) 6.7

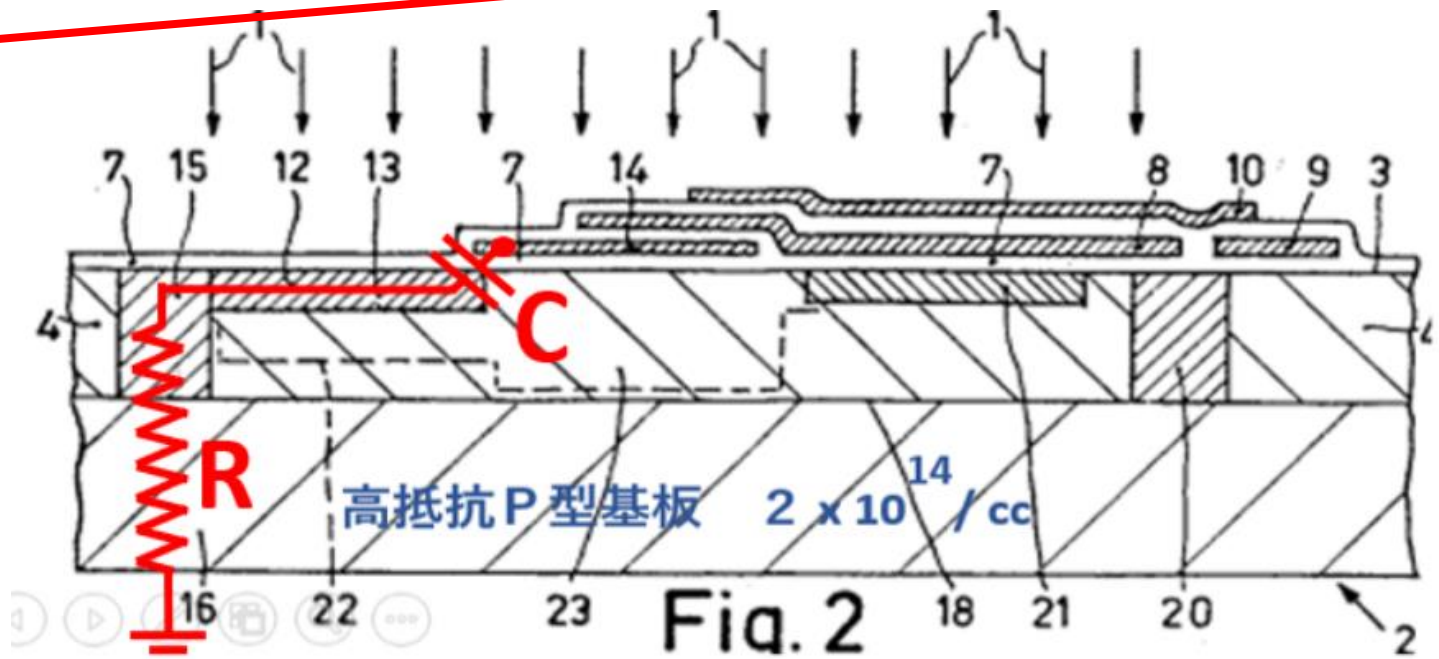


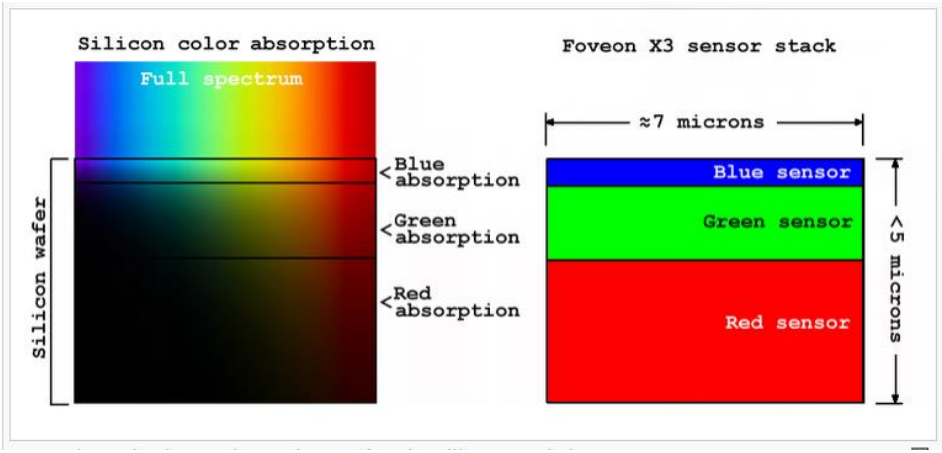
Fig. 2

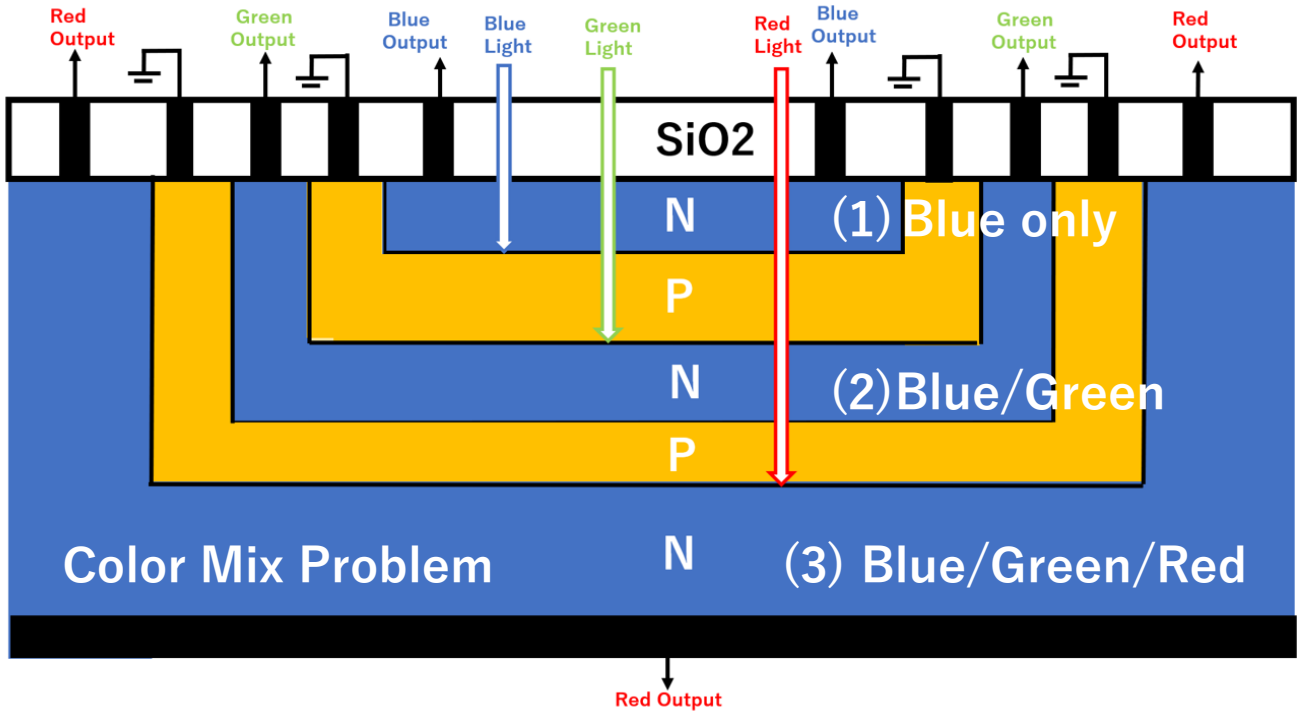
JPA1976-150288(Netherland Patent 7506795, priority June 7, 1975)

https://en.wikipedia.org/wiki/Foveon_X3_sensor

Foveon X3 sensor

From Wikipedia, the free encyclopedia





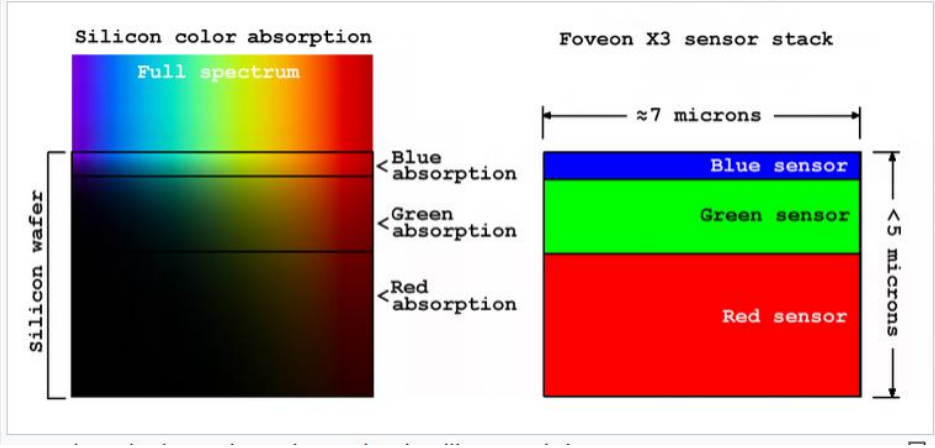
Light gathering and low-light performance

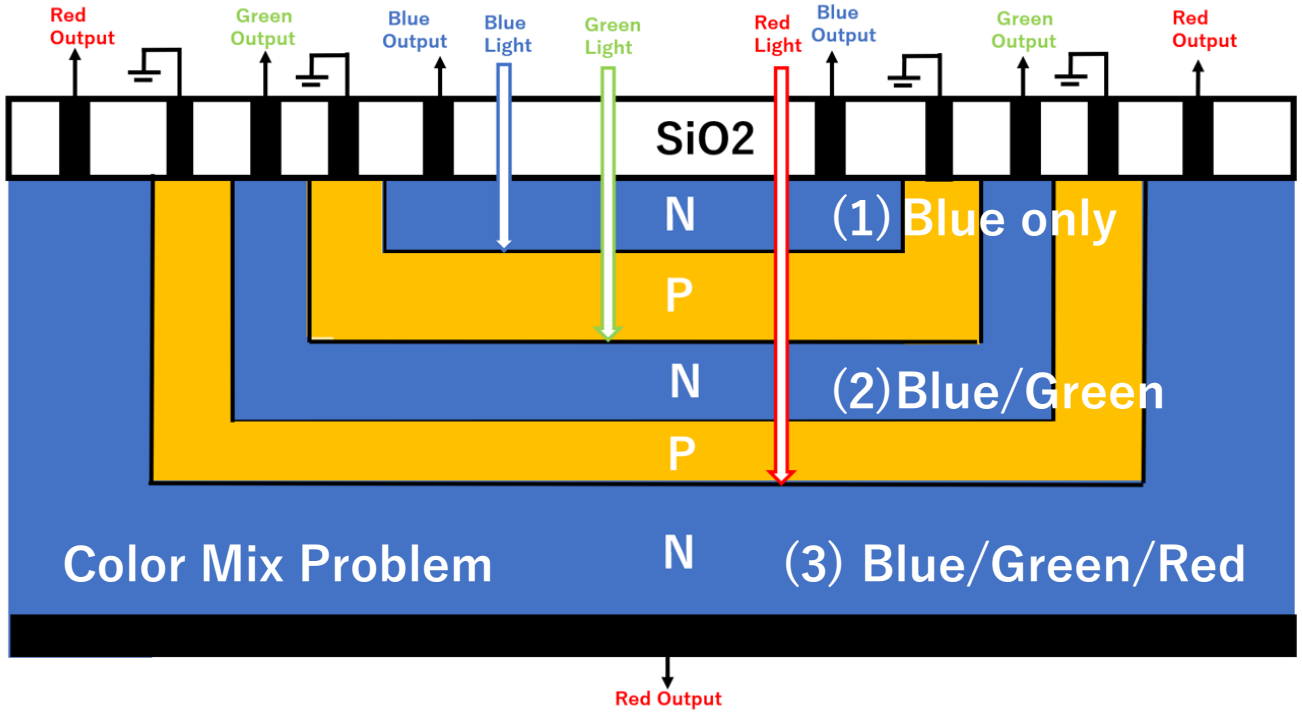
The Foveon X3 photosensor can detect more photons entering the camera than a mosaic sensor, because each of the color filters overlaying each photosite of a mosaic sensor passes only one of the primary colors and absorbs the other two. The absorption of these colors reduces the total amount of light gathered by the sensor and destroys much of the information about the color of the light impinging on each sensor element. Although the Foveon X3 has a greater light-gathering ability, the individual layers do not respond as sharply to the respective colors; thus color-indicating information in the sensor's raw data requires an "aggressive" matrix (i.e., the removal of common-mode signals) to produce color data in a standard color space, which can increase color noise in low-light situations.[15]

https://en.wikipedia.org/wiki/Foveon_X3_sensor

Foveon X3 sensor

From Wikipedia, the free encyclopedia





The **Foveon X3 sensor** is a digital camera image sensor designed by Foveon, Inc., (now part of Sigma Corporation) and manufactured by Dongbu Electronics.[1] It uses an array of photosites that consist of three vertically stacked photodiodes. Each of the three stacked photodiodes has a different spectral sensitivity, allowing it to respond differently to different wavelengths.[2] The signals from the three photodiodes are then processed as additive color data that are transformed to a standard RGB color space.

The X3 sensor technology was first deployed in 2002 in the Sigma SD9 DSLR camera, and subsequently in the SD10, SD14, SD15, SD1 (including SD1 Merrill), the original mirrorless compact Sigma DP1 and Sigma DP2 in 2008 and 2009 respectively, the Sigma dp2 Quattro series from 2014, and the Sigma SD Quattro series from 2016. The development of the Foveon X3 technology is the subject of the 2005 book *The Silicon Eye* by George Gilder.

Japanese Patent JPA 1977-837

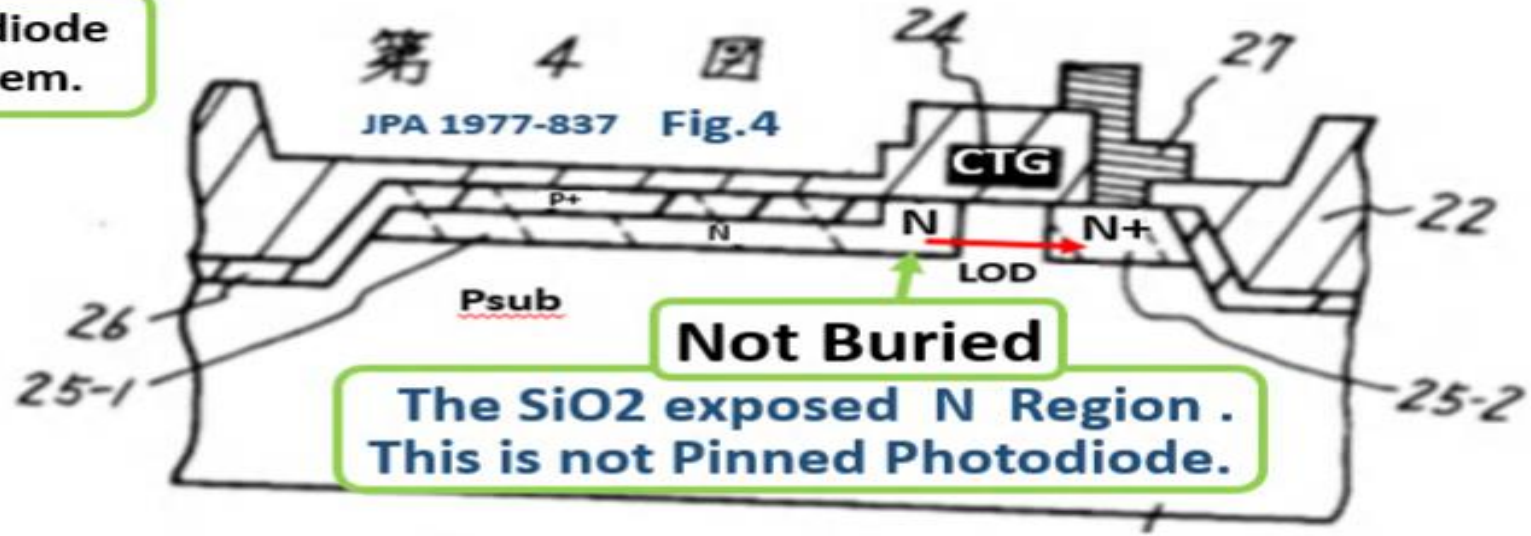
This patent is applied for the lateral overflow drain (LOD) function.
The excess charge is drained to the N+ lateral output drain (LOD).

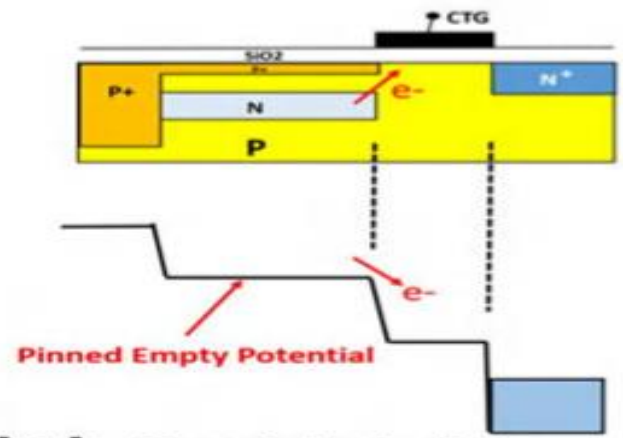
This SiO2 surface exposed photodiode has the serious Image lag problem.

㊵固体撮像装置

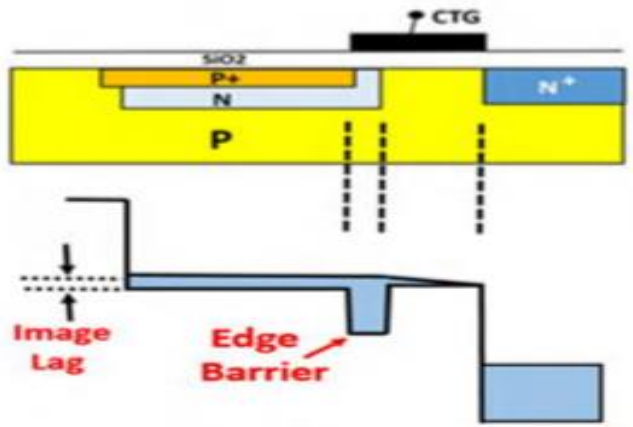
㉑特　　願　昭52—837
㉒出　　願　昭52(1977) 1 月10日
㉗発 明 者　小池紀雄
㊶特許出願公開　昭53—86516

第 4 図
JPA 1977-837 Fig.4

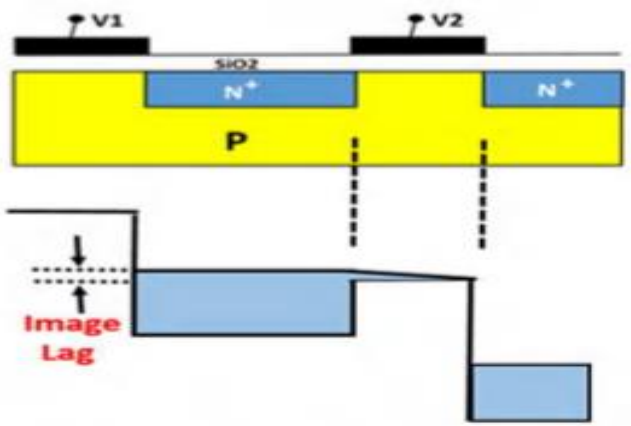




(1) Pinned Photodiode with No Image Lag



(2) Buried Photodiode with BBD Barrier



(3) Bucket Brigade Device (BBD)

JPA1978-1971 by T. Yamada at Toshiba, an invention of the in-pixel anti-blooming using the NPN junction photodiode with the floating N photo charge storage

⑲日本国特許庁(JP)

⑪特許出願公開

⑫公開特許公報(A)

昭54—95116

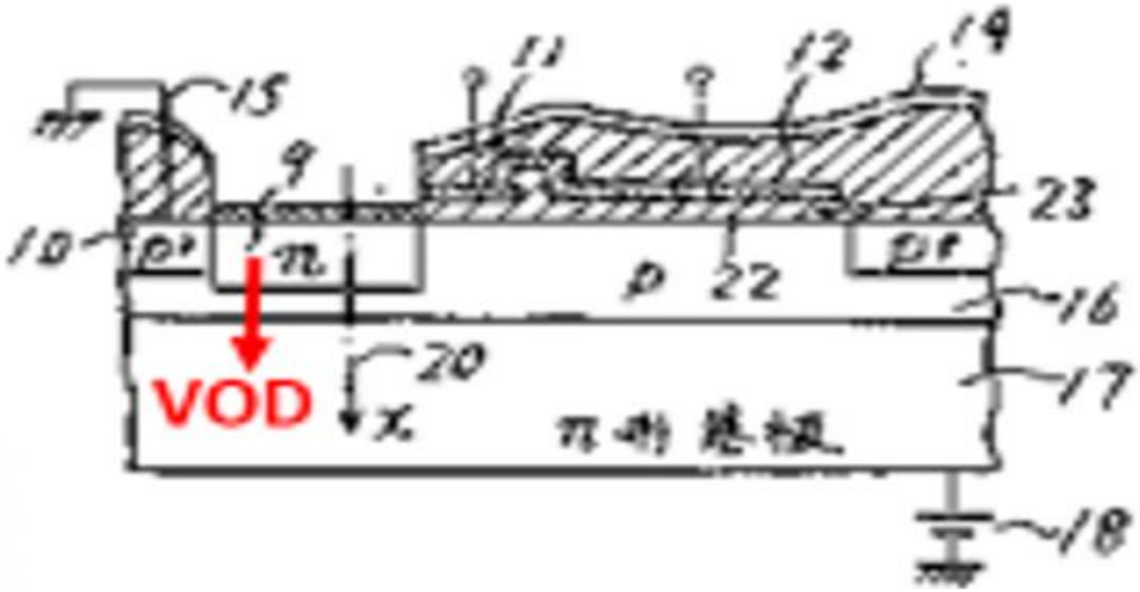
⑤固体撮像装置

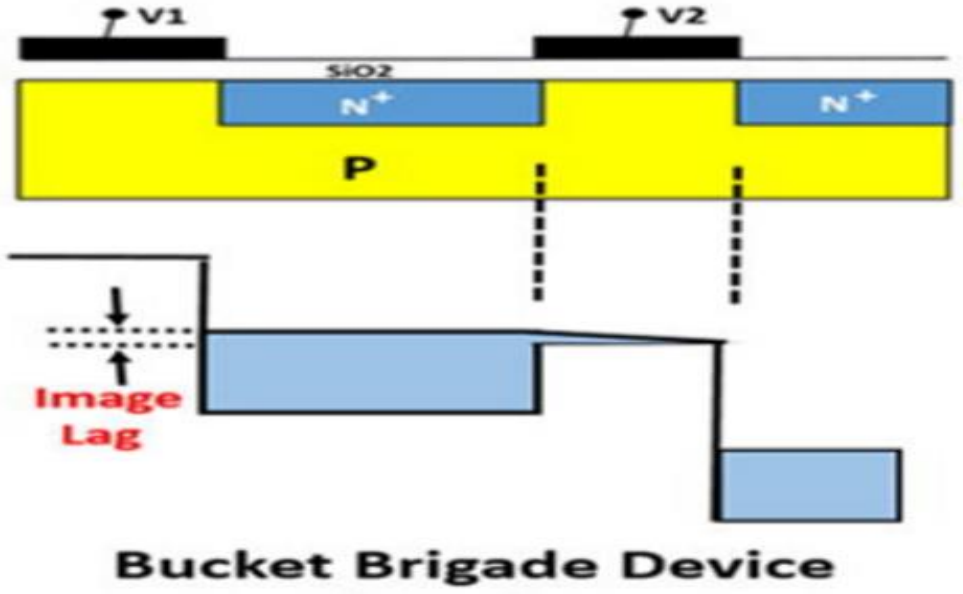
⑳特　　願　昭53—1971

㉒出　　願　昭53(1978)1月13日

㉓発　明　者　山田哲生

⑬公開　昭和54年(1979)7月27日



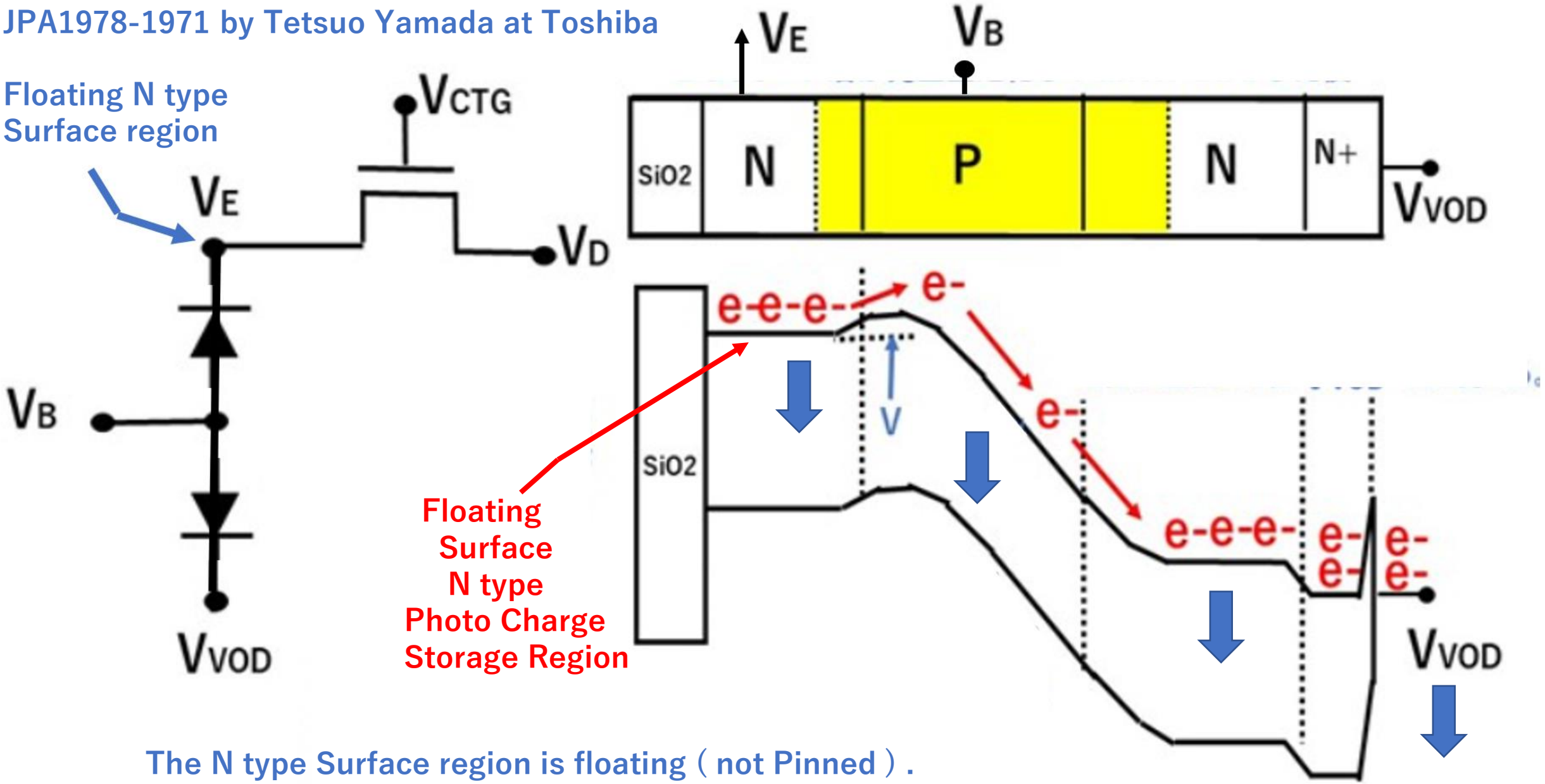


Bucket Brigade Device

This floating surface photodiode operates in the BBD type charge transfer mode with the serious image lag and the truth is that the in-pixel anti-blooming function does not function properly at high frequency.

JPA1978-1971 by Tetsuo Yamada at Toshiba

Floating N type
Surface region



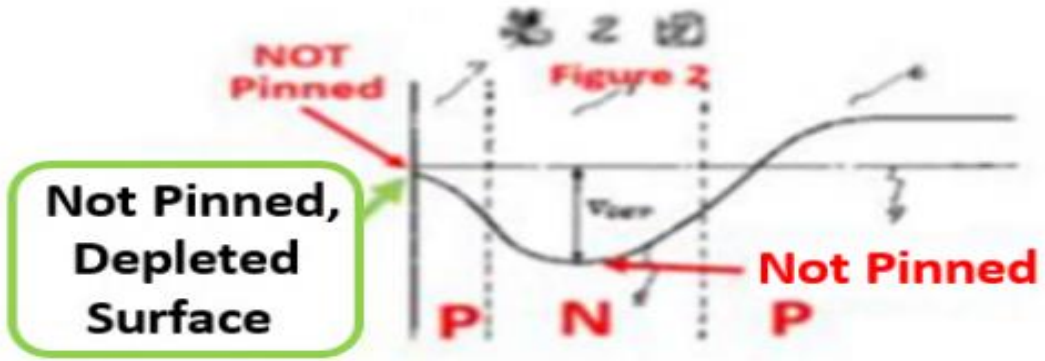
The N type Surface region is floating (not Pinned) .
The anti-blooming VOD does not function well because the N-type surface will also be pulled down as the VOD voltage is pulled down deeper.

JPA1980-138026 by N. Teranishi et al at NEC

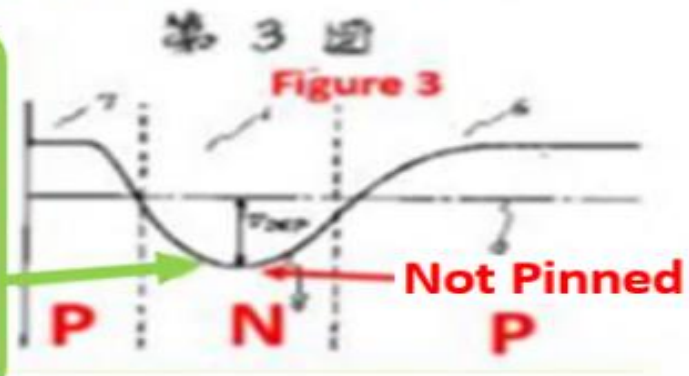
JPA 1980-138026

1980年10月2日出願

⑫特　　願　昭55—138026
⑫出　　願　昭55(1980)10月2日
⑫発　明　者　寺西信一
⑫発　明　者　石原保雄
⑫発　明　者　白木廣光



Not Pinned, Depleted Surface

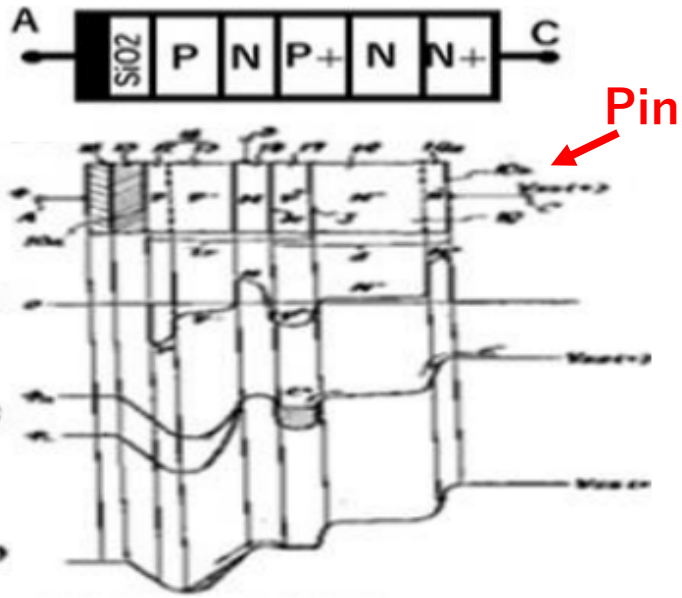


The surface P region is not Pinned. The Buried N region is still floating.

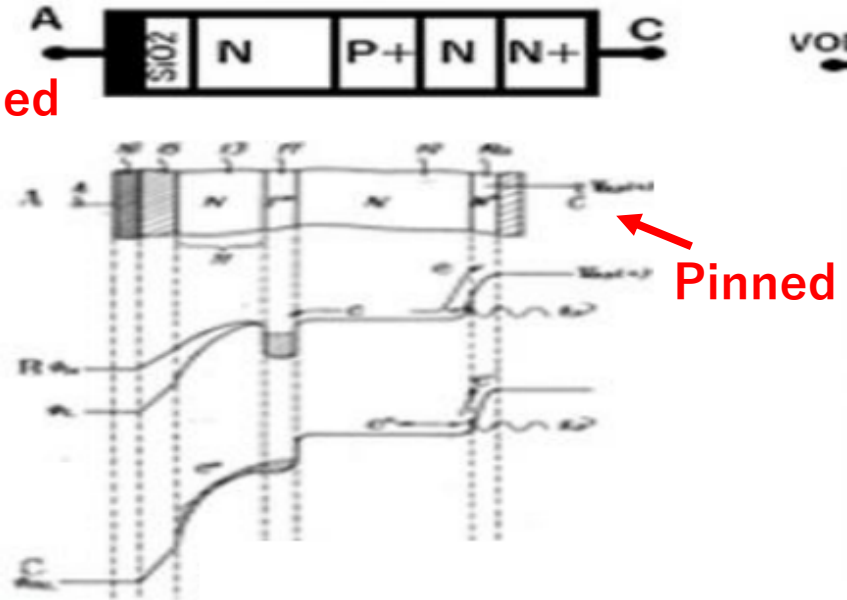
This patent is on the PNP junction type Buried Photodiode but NOT Pinned Photodiode. The surface P region is not pinned and grounded. The surface potential can be of any value depending on the floating buried N region potential, which is actually controlled by the substrate Psub potential which is grounded in this case, but in case of a built-in VOD function P+NPNsub junction photodiode, the P region potential is controlled by the Nsub VOD voltage and can be any value. The surface P region must be pinned by the adjacent P+ channel Stops region or the adjacent metal contact wiring.

Who invented Pinned Photodiode ?

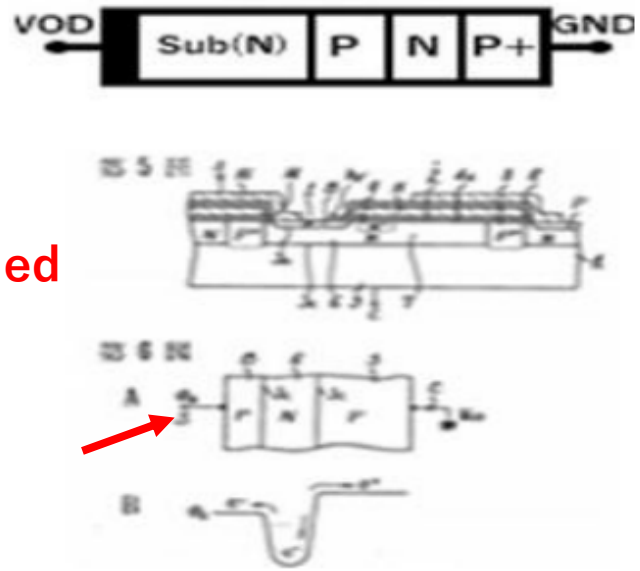
Hagiwara at Sony invented Pinned Photodiode in 1975. The evidence is give by the three Japanese patent applications, JPA1975-127646, JPA1975-127647 and JPA1975-134985. The first Pinned Photodiode was defined in October 23, 1975 as the N+NPNP triple junction(in Fig. 7 of JAP1975-127646) type and the N+NPN double junction type (in Fig. 7 of JAP1975-127647) type photodiodes with the N+ type pinned surface and the P type buried photo charge storage region with the complete charge transfer capability and the no-image-lag feature. The photo charge is transferred and drained to the CCD/MOS type charge storage buffer memory quicky by the strong punch-thru action. The second Pinned Photodiode was defined in November 10, 1975 as the PNP double junction (in Fig. 6 of JAP1975-134985) type photodiode with the vertical overflow drain action also with the complete charge transfer capability and the no-image-lag feature as evidence the empty potential well of the buried photo charge storage, completely depleted of the charge.



JPA1975-127646 Fig. 7



JPA1975-127647 Fig. 7



JPA1975-134985 Fig. 6

Proceedings of the 9th Conference on Solid State Devices, Tokyo, 1977;
Japanese Journal of Applied Physics, Volume 17 (1978) Supplement 17–1, pp. 255–261

Two Phase CCD with Narrow-Channel Transfer Regions

Yoshiaki DAIMON-HAGIWARA

Sony Corporation Research Center Yokohama 240

with no image lag

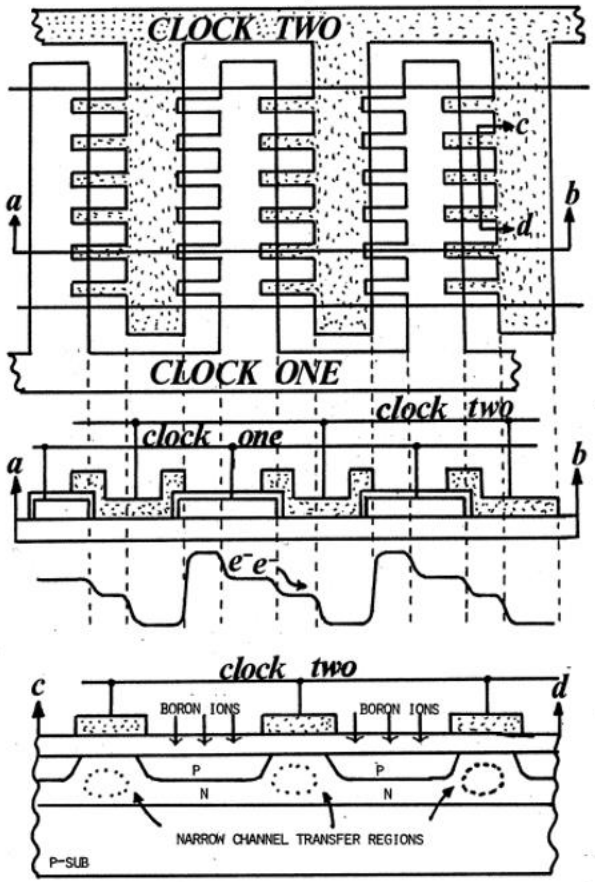


Fig. 1. Top and crosssectional views of the electrode structure for two phase CCD with narrow-channel transfer regions.

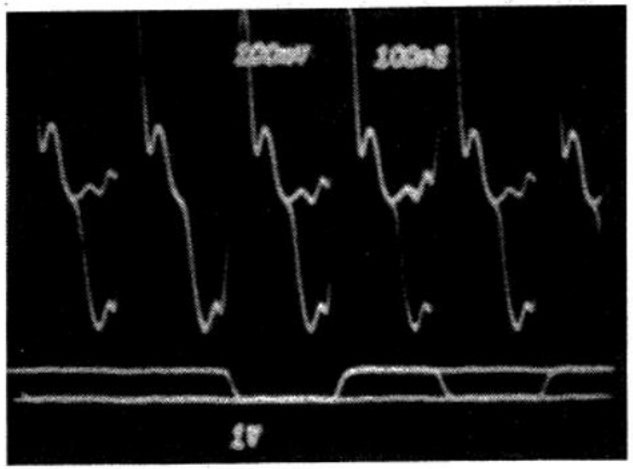


Fig. 4. Input and output wave forms for 242 analo delay line in buried channel version.

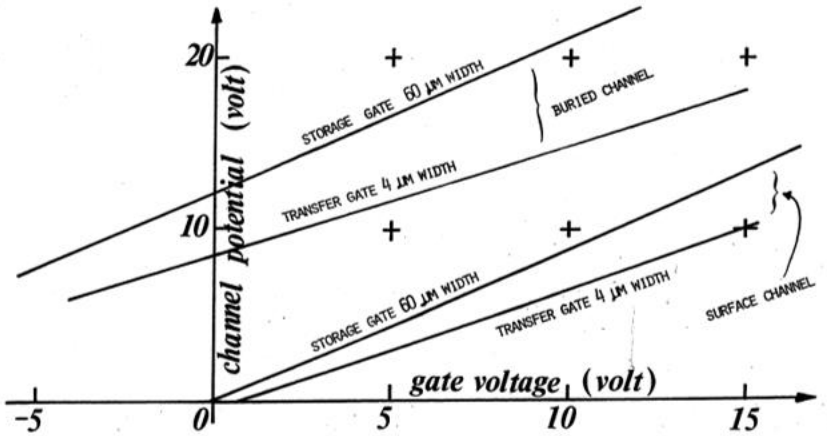


Fig. 2. The actual measured channel potentials plotted against the gate voltage for both surface and buried channel versions.

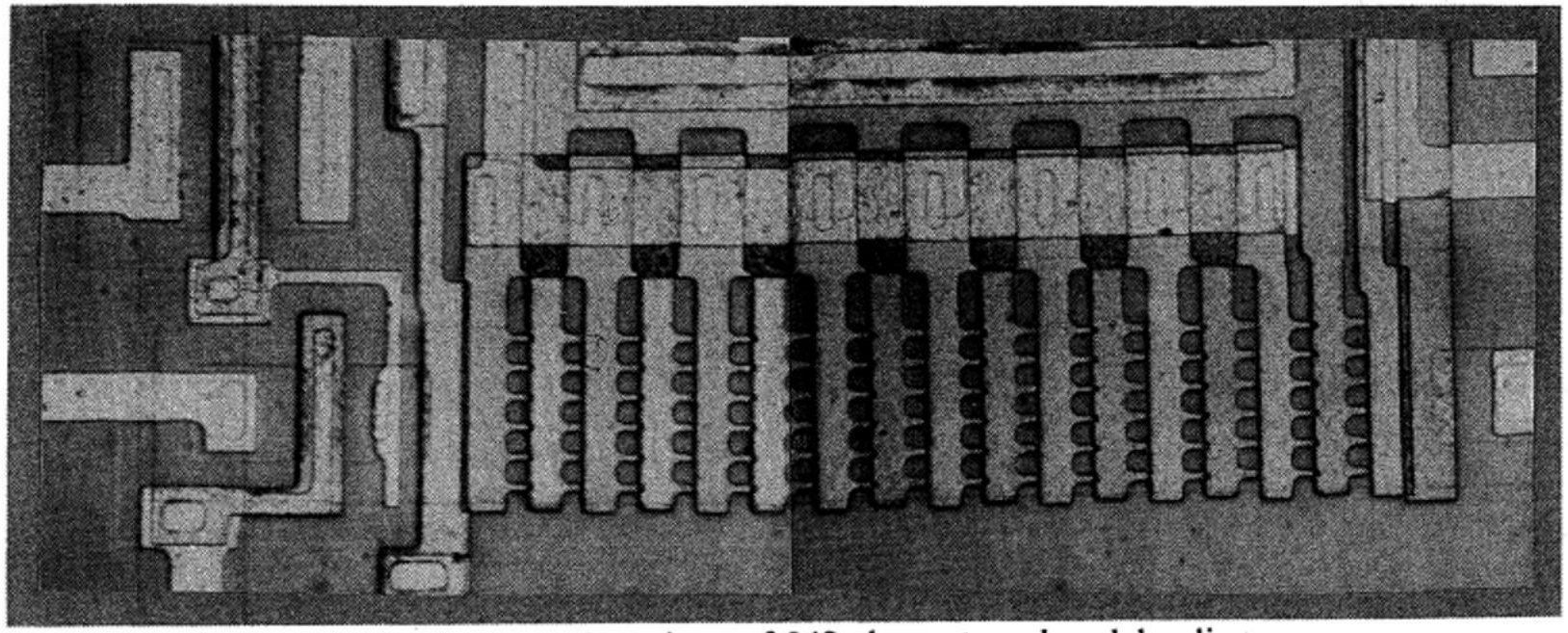
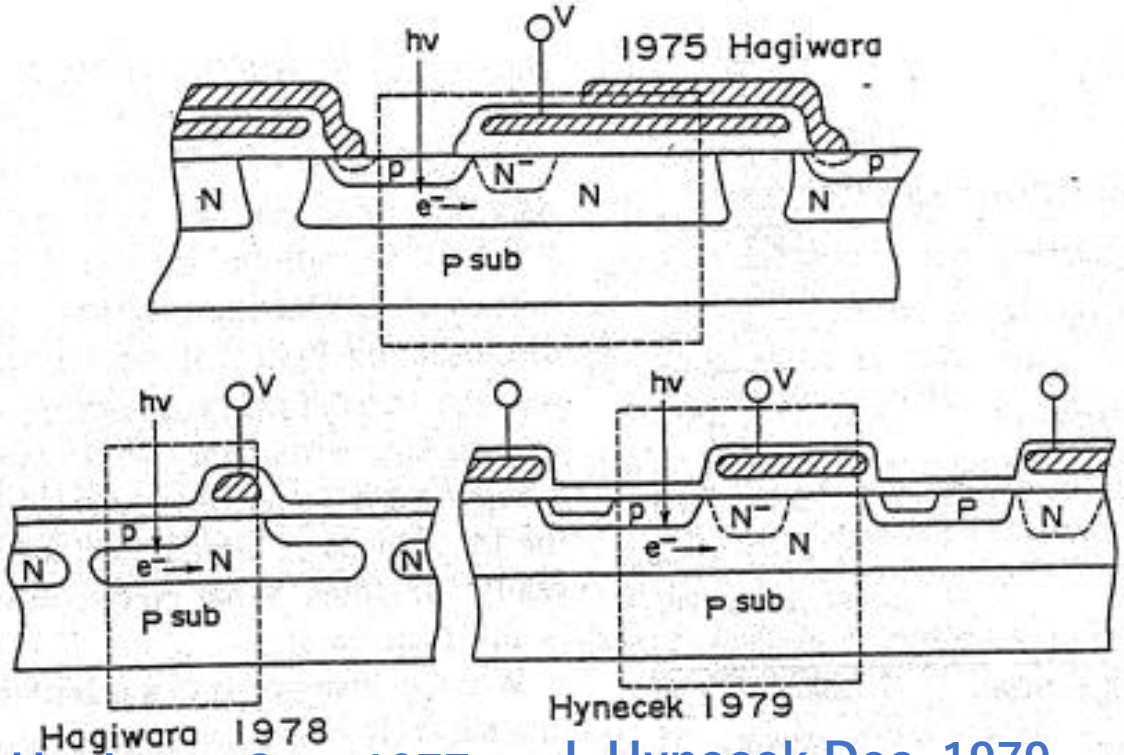


Fig. 3. The end sections of 242 element analog delay line.

High-Density and High-Quality Frame Transfer CCD Imager with Very Low Smear, Low Dark Current, and Very High Blue Sensitivity

Yoshiaki Hagiwara, *Member, IEEE*

Y.D. Hagiwara Nov 10, 1975

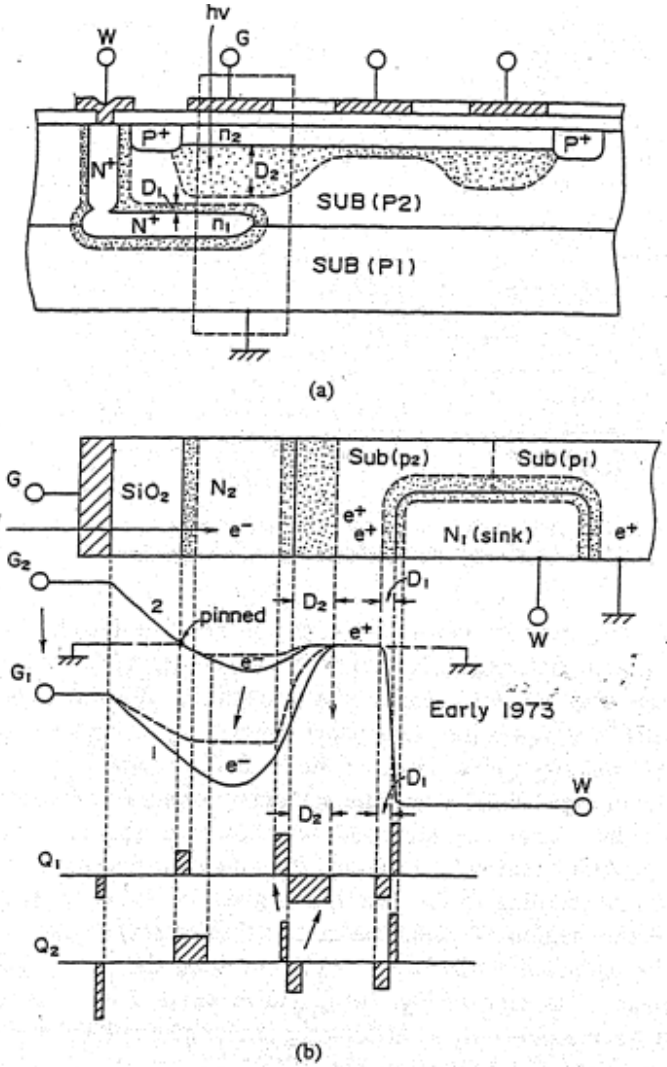


Y.D. Hagiwara Sep, 1977

J. Hynecek Dec, 1979

[16] J. Hynecek, "Virtual phase CCD technology," in *IEEE Proc. IEDM*, Dec. 1979, pp. 611–614.

J.M. Early Dec 3, 1973



[17] J. M. Early, U.S. Patent 3896485, Dec. 3, 1973.

Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978;
Japanese Journal of Applied Physics, Volume 18 (1979) Supplement 18-1, pp. 335-340

A 380H × 488V CCD Imager with Narrow Channel Transfer Gates

Yoshiaki Daimon-HAGIWARA, Motoaki ABE† and Chikao OKADA†

Sony Corporation Research Center, Yokohama 240
†Semiconductor Development Division, Yokohama 240

with no image lag

When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of threshold voltage is observed. This narrow-channel effect has been applied successfully in creating an asymmetric potential well under an electrode for two phase CCD operations. The feasibility of this new structure has been confirmed in a 242 element analog delay line and the application is now extended to a 380H × 488V CCD Imager. In the constructed B/W CCD camera,

Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978;
Japanese Journal of Applied Physics, Volume 18 (1979) Supplement 18-1, pp. 335-340

A 380H × 488V CCD Imager with Narrow Channel Transfer Gates

Yoshiaki Daimon-HAGIWARA, Motoaki ABE† and Chikao OKADA

Sony Corporation Research Center, Yokohama 240
†Semiconductor Development Division, Yokohama 240

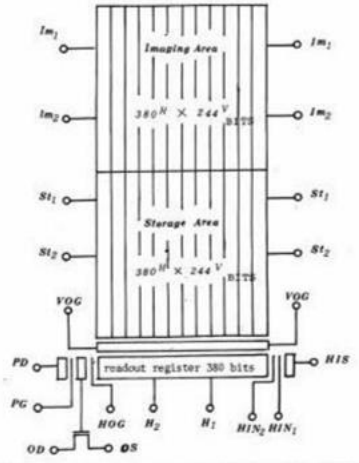


Fig. 1. The block diagram of a 380 H×488 V CCD imager in frame transfer organization.

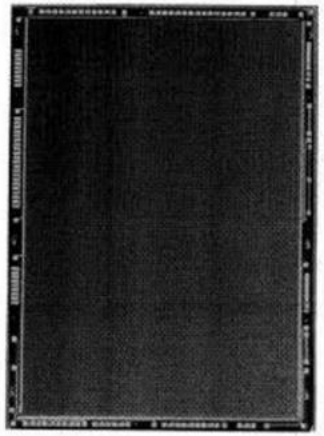


Fig. 3. Photomicrograph of the 380 H×488 V CCD imager. The chip size is 14.6 mm by 10.1 mm.

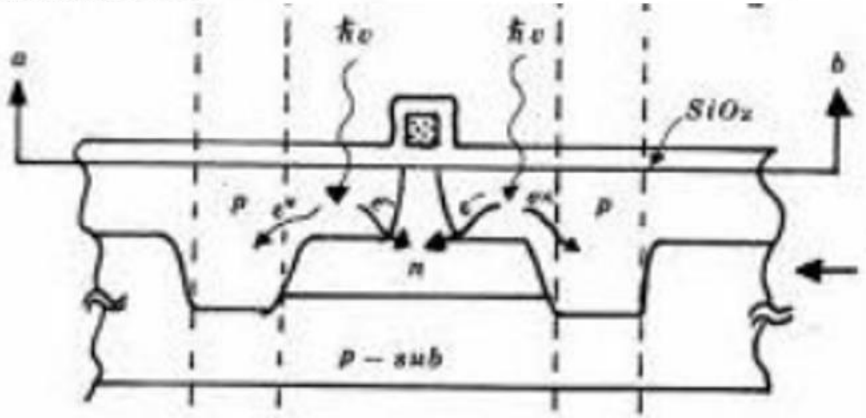


Fig. 2. Top and cross sectional views of the electrode for two phase CCD structure.

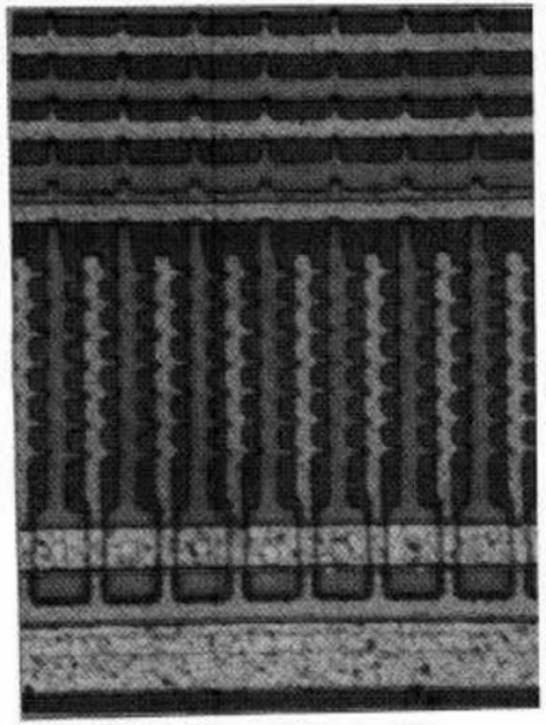


Fig. 5. The horizontal readout register with 14 μm-pitch-per bit electrode structure.

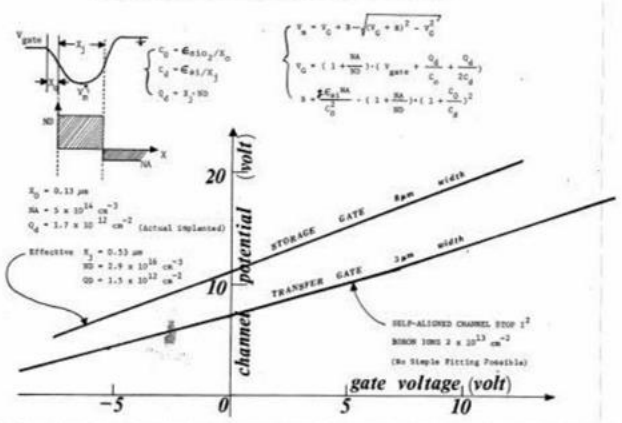


Fig. 9. The actual measured channel potentials plotted against the gate voltage for the buried channel version. The curve fitting with the simple relations by depletion approximation gives the effective values of X_j, ND and QD as seen in the figure.

with no image lag

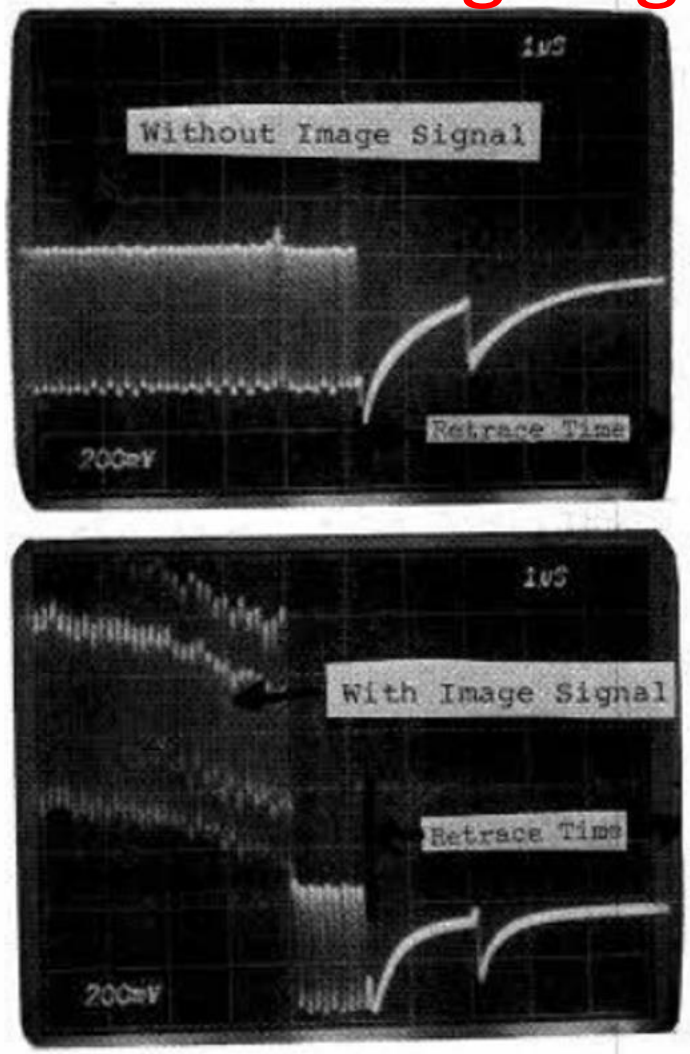
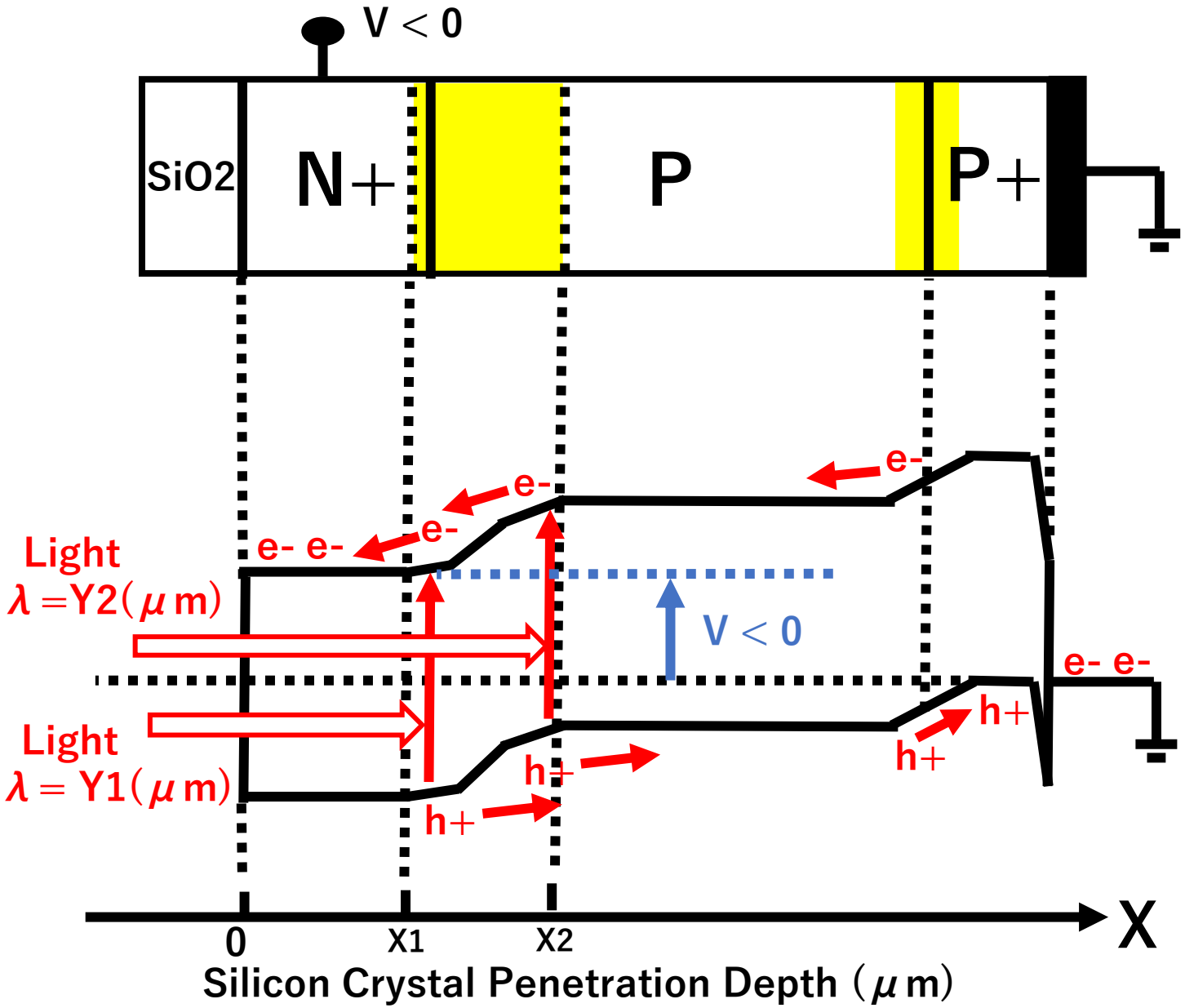
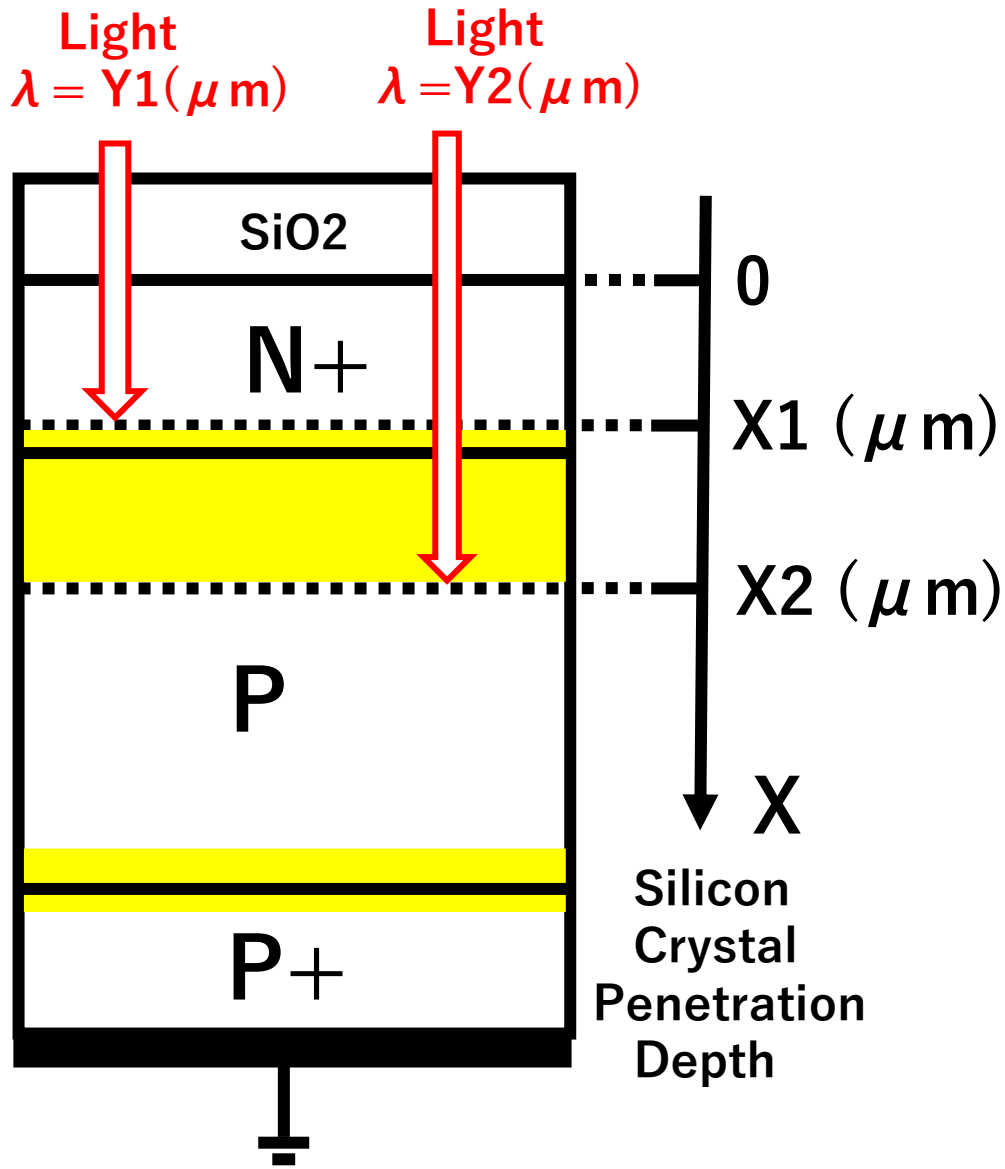


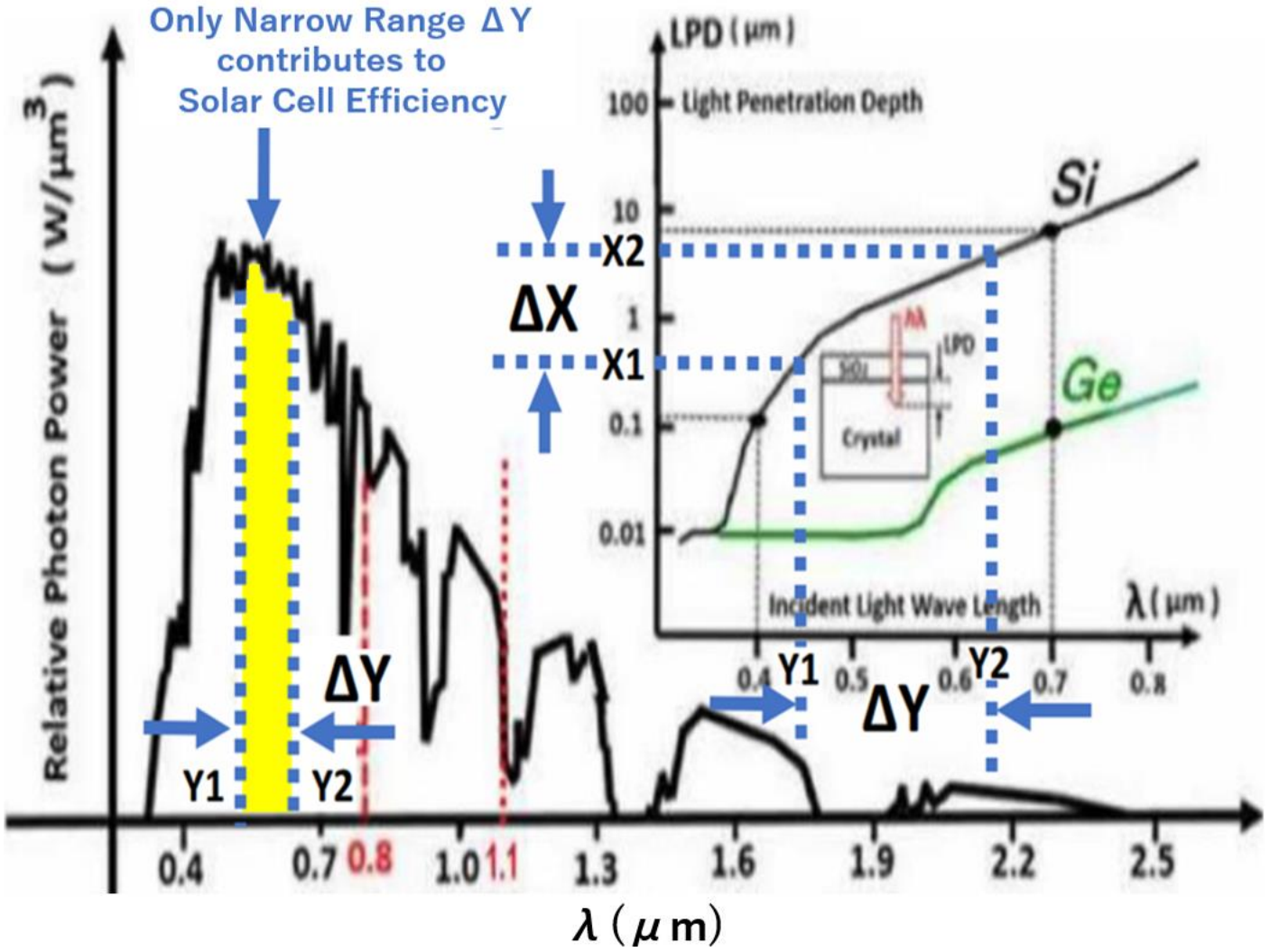
Fig. 12. The output wave forms of the horizontal readout register at the tailing end of a TV picture line, that is, right before the horizontal retrace time. The comparison of the output levels with and without image signal gives the dark current level of the imager.

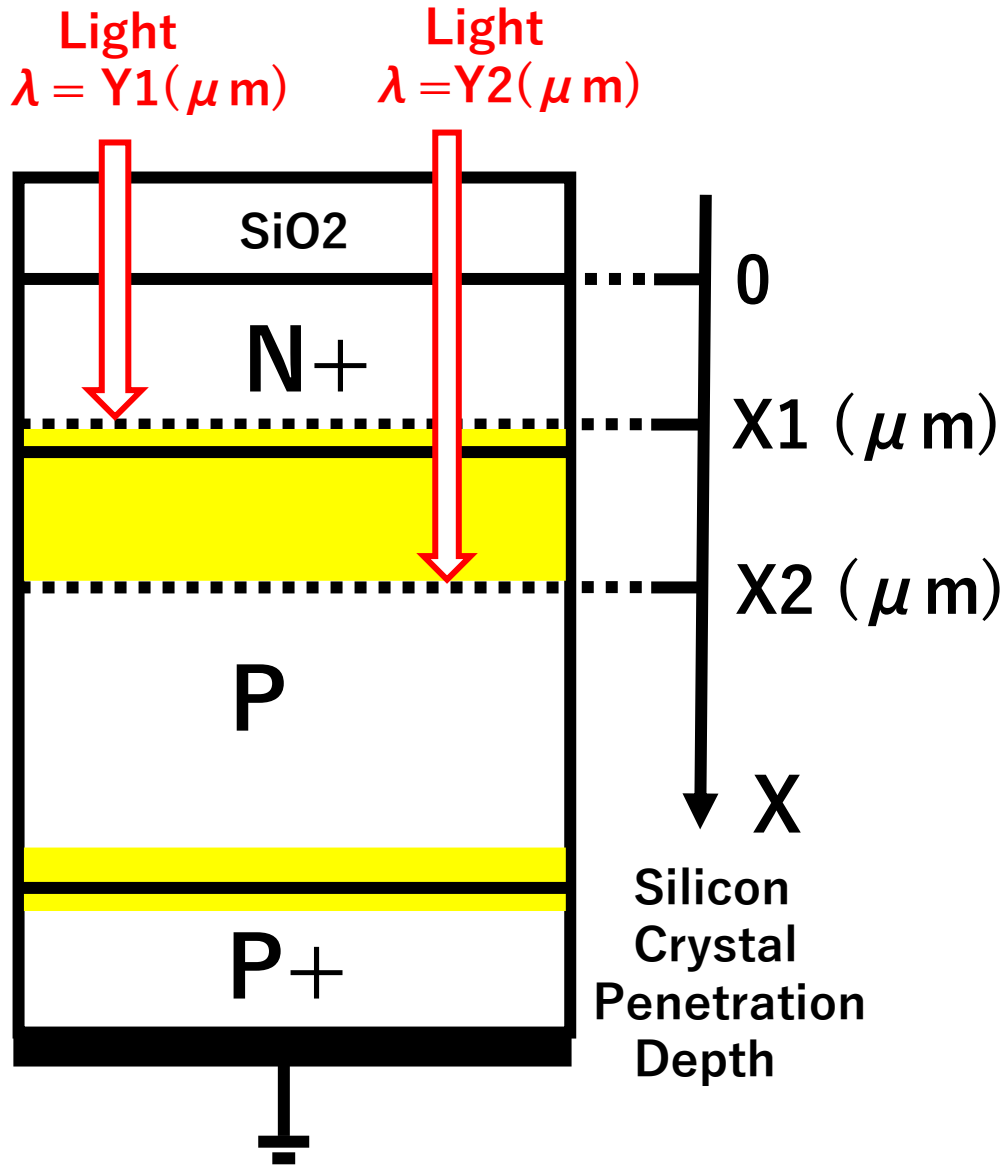
For Single Junction type Solar Cell with the floating N+ surface photo charge storage region, only the wave length between Y1(μm) and Y2(μm) can contribute to the Efficiency.





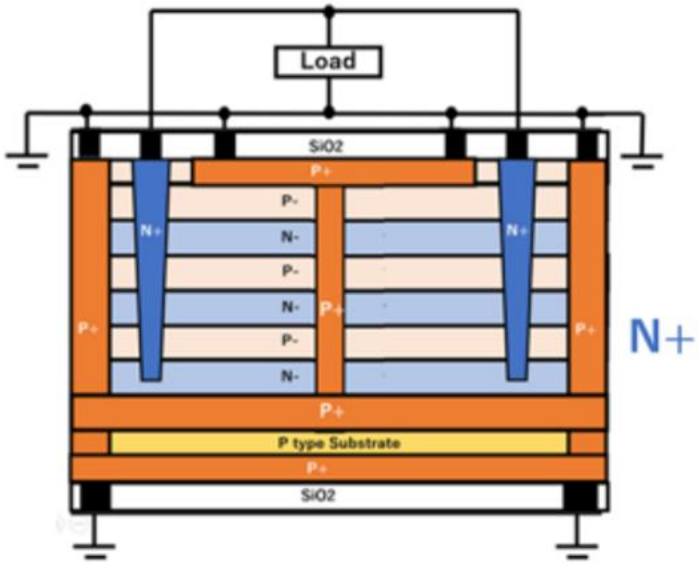
For Single Junction type Solar Cell with the floating N+ surface photo charge storage region, only the wave length between Y1(μm) and Y2(μm) can contribute to the Efficiency.

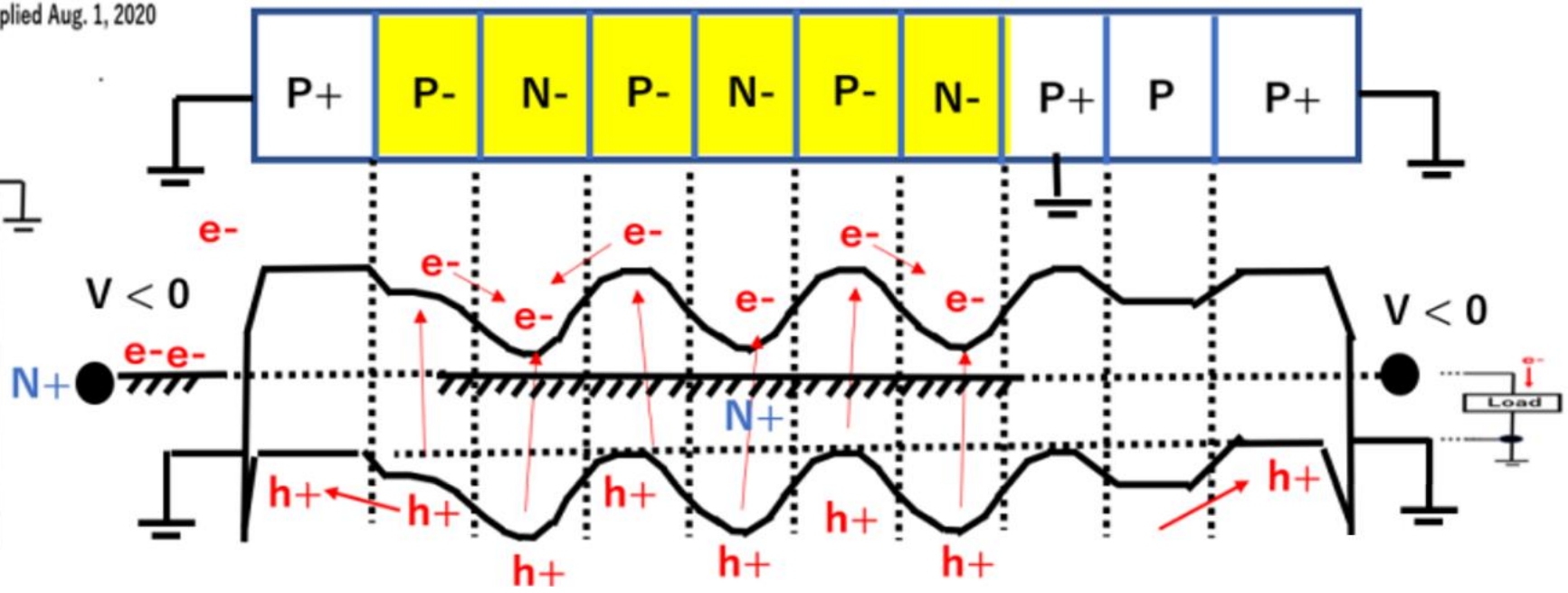


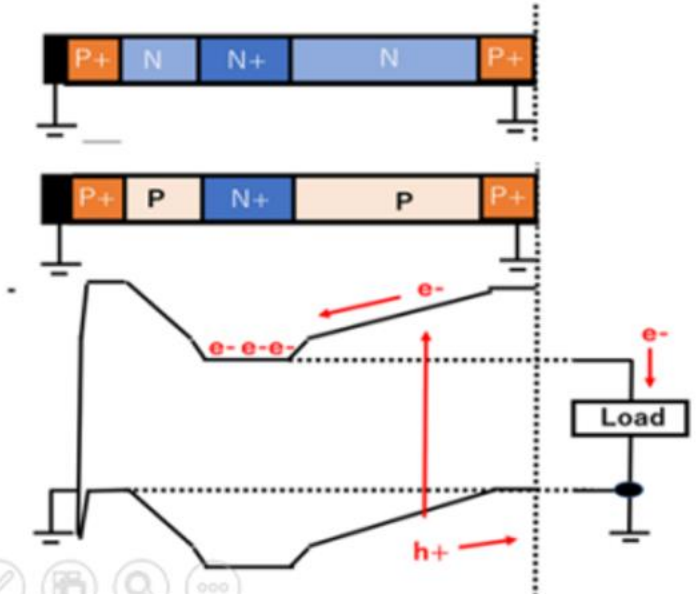


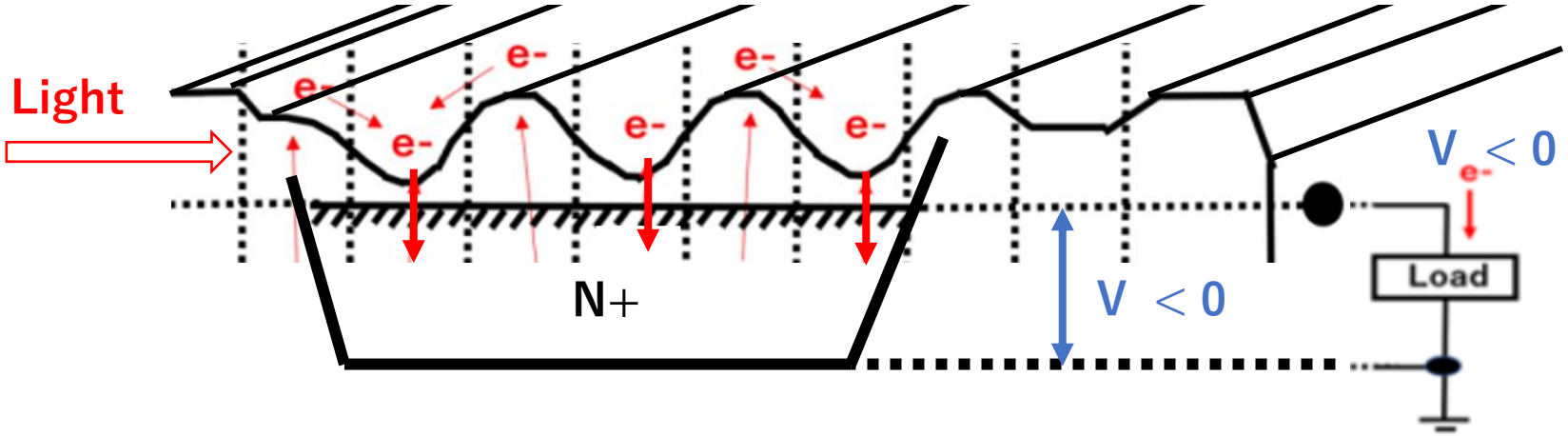
Multi-junction Pinned Photodiode with Completely Depleted of Photo Electron and Hole

Multi-junction Pinned Photodiode type Solar Cell Structure,
based on Double Junction Solar Cell , defined in JPA2020-131313, applied Aug. 1, 2020
by Yoshiaki Hagiwara, Sept 12, 2022



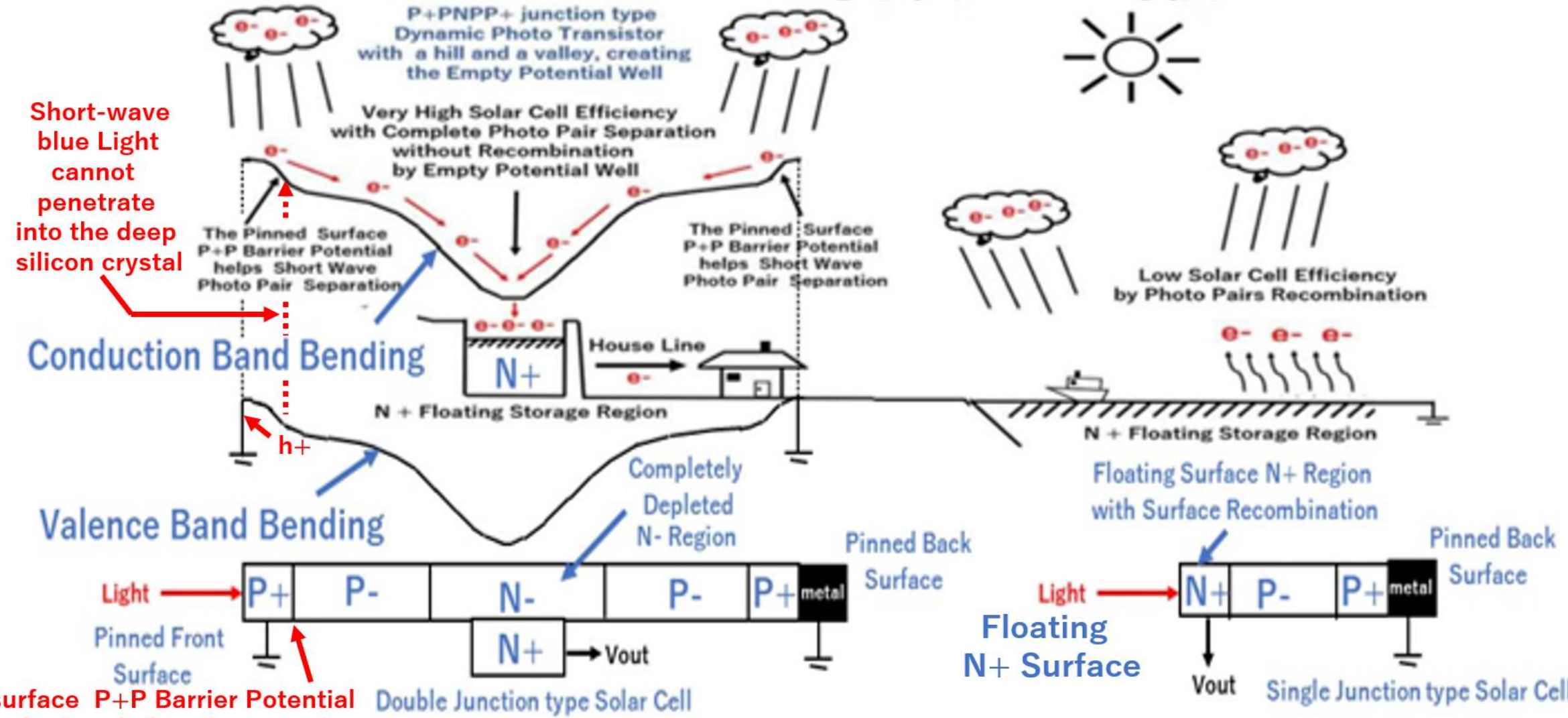






True History of Photodiode

The difference of Double and Single junction type Solar Cells



The surface P+P Barrier Potential helps electron-hole pair separations.






Artificial Intelligence in Robot Vision



Mighty ATOM / ASTRO BOY © Osamu Tezuka



WALL·E © 2008 The Walt Disney Studios

Hello, my name is Yoshiaki Hagiwara. I am also called simply as Yoshi, and as Yoshiaki Daimon and also as Yoshiaki Daimon-Hagihara. I believe that I am the true inventor of the digital camera with the mechanical shutter function capability, which is completely filmless and free from mechanical parts. I worked at Sony from 1975 till 2008. My friends in Sony developed the digital camera in 1987. Sony is now enjoying image sensor business. Image sensors are very important to realize Artificial Intelligent AI robots and self-driving cars.



Evidence that Yoshiaki Hagiwara is the inventor of Pinned Buried Photodiode with in-pixel overflow Drain (VOD) function is given by the three basic Japanese Patent Applications, JPA1975-127646, JPA1975-127647 and JPA1975-134985.

Hagiwara also invented the in in-pixel Overflow Drain (OFD) Punch-thru Clocking Scheme to realize the completely-mechanical-part-free Electrical Shutter for digital cameras, opening a way to realize our modern digital TV world.

Evidence that Yoshiaki Hagiwara is the inventor of Electrical Shutter is given by the basic Japanese Patent Applications, JPA1977-126885.

The first Double Junction Pinned Buried Photodiode was developed by Hagiwara team at Sony in 1978. The first Triple Junction Pinned Buried Photodiode with Electrical Shutter function was developed by Hamazaki team at Sony in 1987.

Thank you very much !

http://www.aiplab.com hagiwara.yoshiaki@aiplab.com

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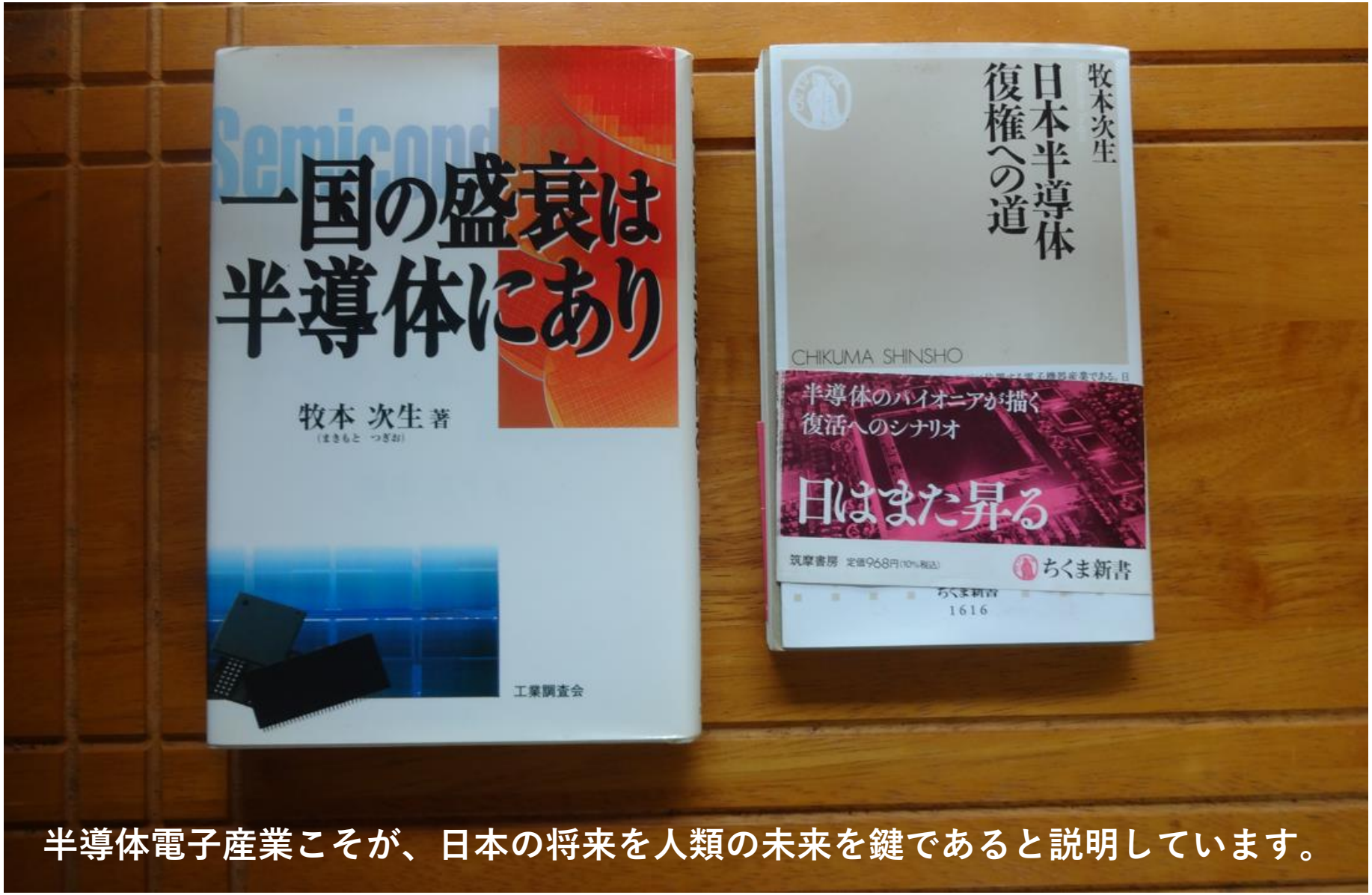
講演に関する参考図書



日本の未来エネルギの鍵である太陽電池への熱い思いと期待を述べています。

もと三洋電機の社長　桑野幸徳様からいただきた本です。

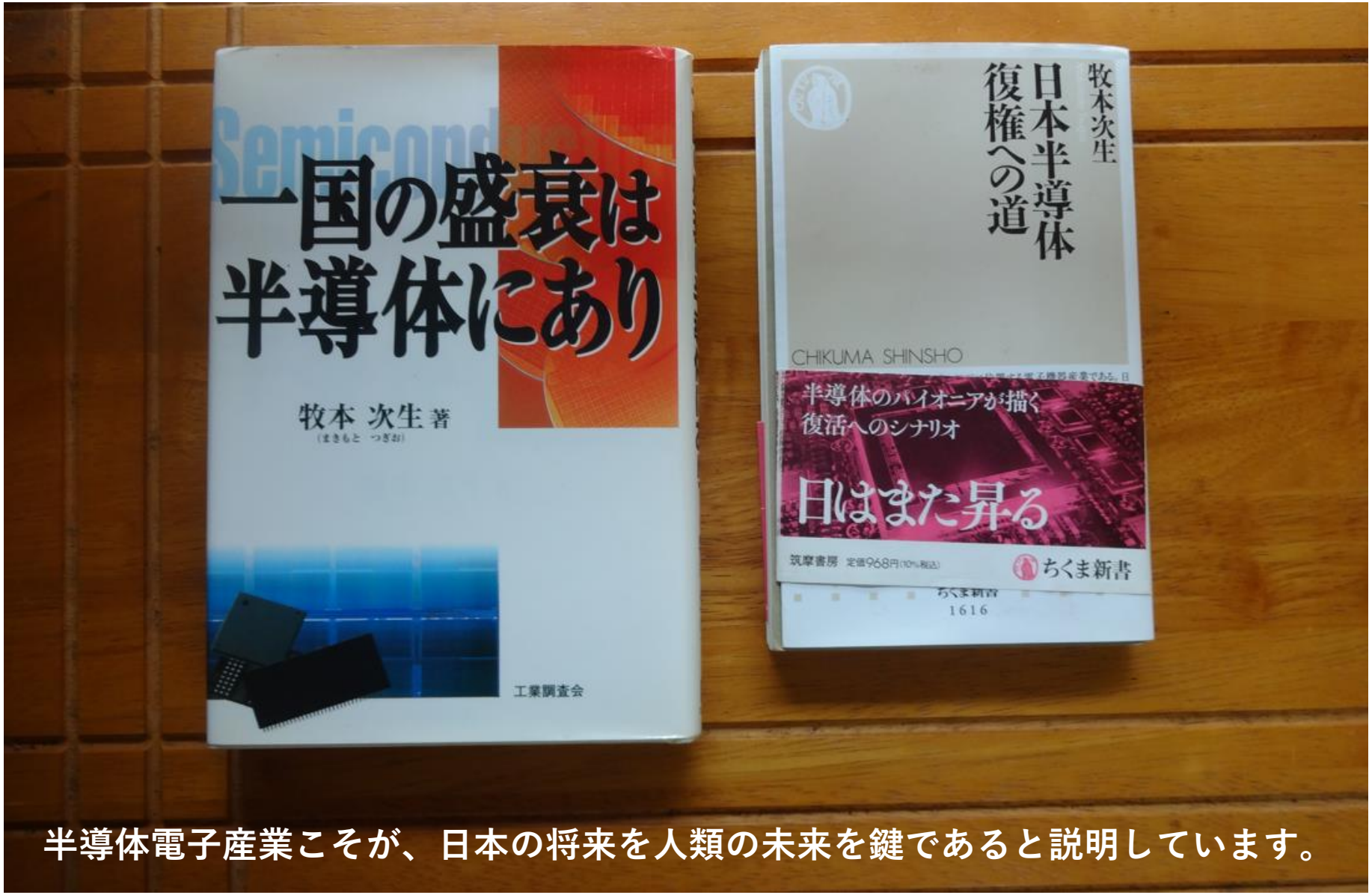
講演に関する参考図書



半導体電子産業こそが、日本の将来を人類の未来を鍵であると説明しています。

もと日立とSONYの専務の牧本次生様からいただいた本です。

講演に関する参考図書



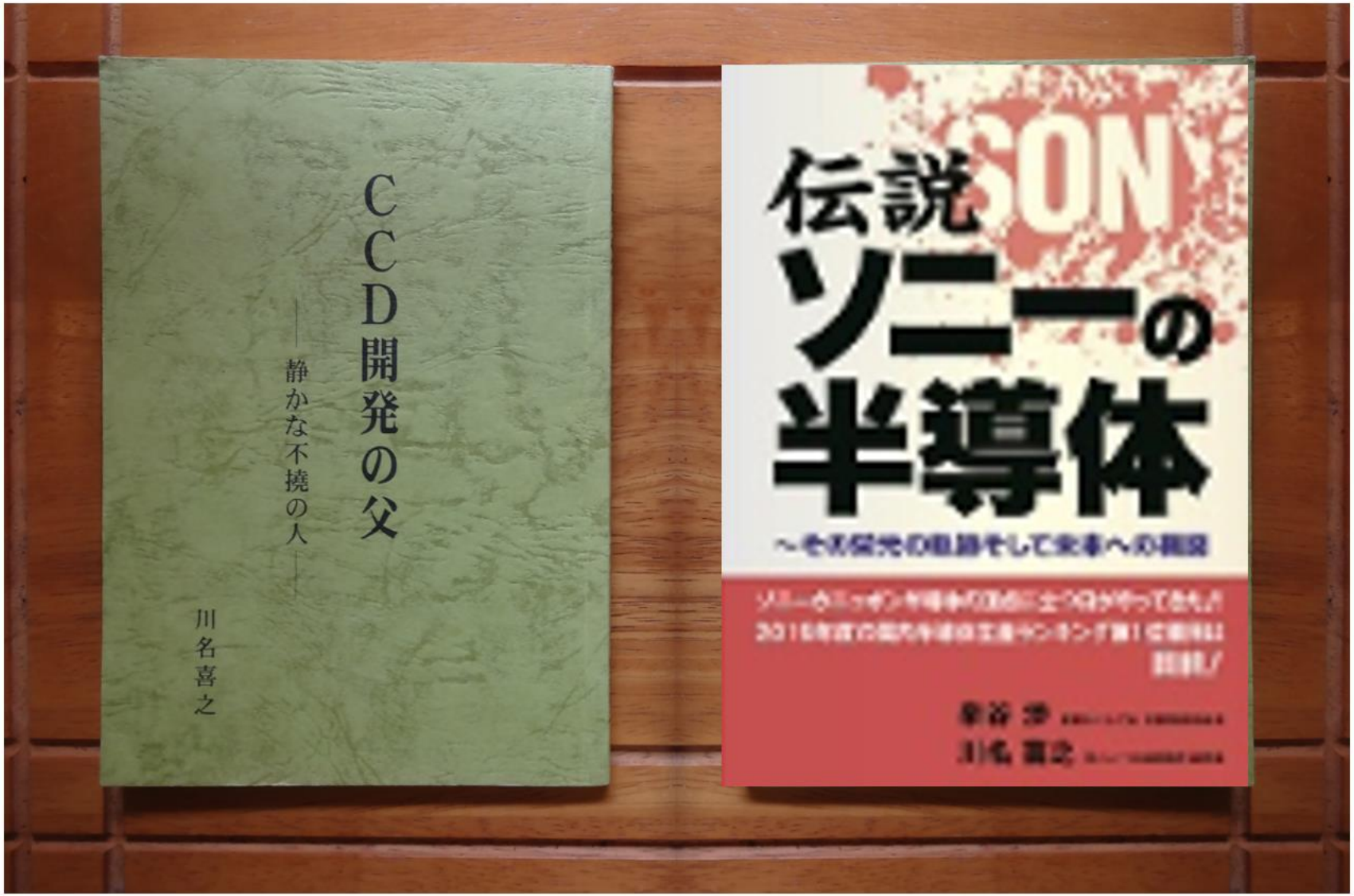
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講演に関する参考図書

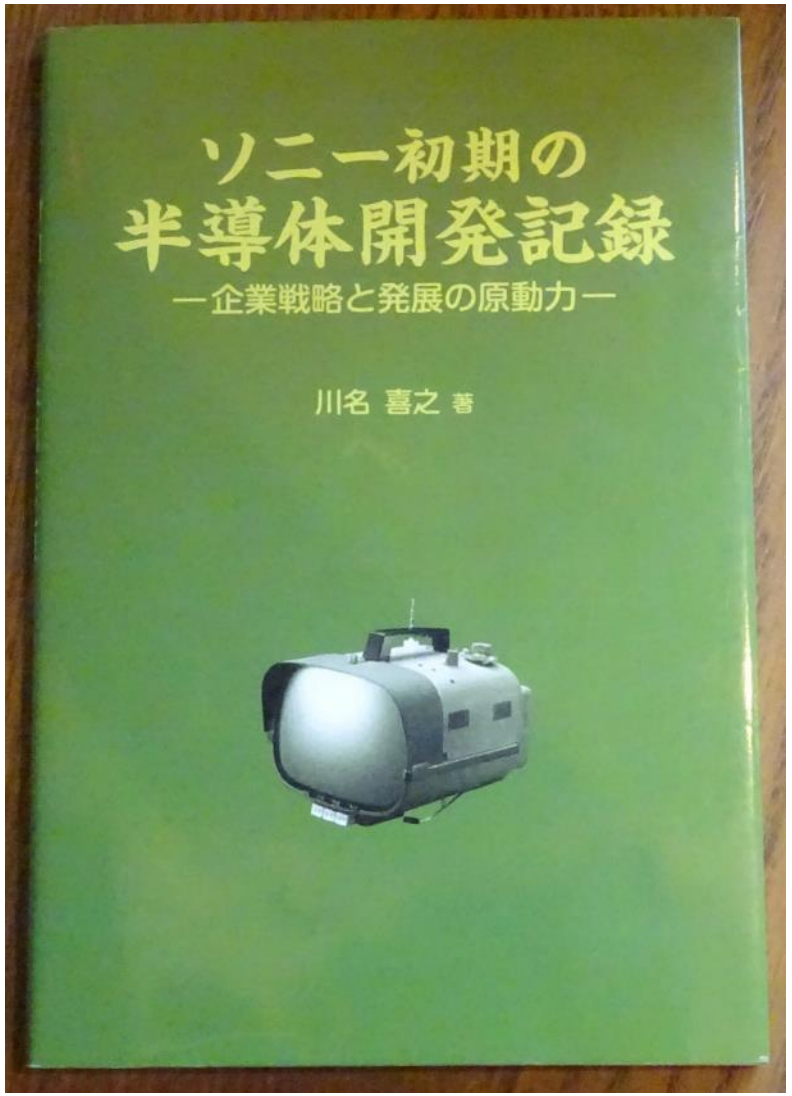
「CCD開発の父」
川名喜之著（非売品）

「伝説ソニーの半導体」
その栄光の軌跡そして未来への構図
泉谷渉、川名喜之著　産業タイムズ社



講演に関する参考図書

「ソニー初期の半導体開発記録」　企業戦略と発展の原動力
　川名　喜之　著　　美研プリンティング株式会社　（非売品）





Sonyの半導体の過去を振り返って、その強さと、源泉と、
今後に向けて、一緒に考えてみましょう♡

●SONYの半導体がどうして昔は、日本一なのか？
●どうして　Bipolar Transistorで世界一だったのか？

講演に関する参考図書

「イノベーションの成功と失敗」　武田　立、瀬戸篤著、
同文舘出版　ISBN978-4-495-38571-2　単行本 – 2015/10/24



戦前戦中から戦後に至る　日本型イノベーションの真実

三知一体論

イノベーションにおいて技術革新のみが重要視されるが、成功
させるためには「知 の創造」「知 の具現化」「知 の商業化」の３つが不可欠である。SONY の知恵袋がイノベーションの真実を語る。

**車には運転手が必要だし、
エンジンがあっても、
車輪がないと前には進まない。**



萩原さん、ご一読いただいたようなので、趣旨はご理解いただきましたが、一言でいえば、
　井深さんがよく言ってた、「1-10-100の法則」をかみ砕いたもので、「イノベーション」は「発明」ではなく、「事業化すること」であり、「発明はカンタンだが『商業化』できてナンボのモノ」ということに尽きます。

講演に関する参考図書

人工知能パートナーシステム（AIPS)を支える「デジタル回路の世界」
萩原良昭著　青山社　ISBN978-4-88359-339-2

https://www.seizansha.co.jp/ISBN/ISBN978-4-88359-339-2.html



人工知能パートナーシステム(AIPS)を支える
デジタル回路の世界

IEEE Life Fellow, Ph.D.

萩原　良昭　著

ISBN978-4-88359-339-2　B5判　上製　475頁
定価(本体9,000円＋税)

未来の人間社会には人工知能パートナーシステム(AIPS)とも言える人間にやさしい支援システムが出現すると期待している。AIPS搭載の自動走行車や老人介護システム、人間型歩行ロボットやロボット・ハウスなどである。そこで本書では、そのAIPSを支える「デジタル回路の世界」と題し、ハードとソフトの両面で、人とコンピュータをつなぐデジタル技術について紹介している。図や絵をたくさん用意して、基礎からやさしく解説している。

Invention and Historical Development Efforts of Pinned Photodiode and Electric Shutter

2019



Hagiwara at Sony Kumamoto Tech Center
in 2017, 2019 and 2022.

2001



1. Introduction
2. Patent Wars on Pinned Photodiode
3. Double Junction type Solar Cell
4. Physics of Image Sensor and Solar Cell
5. Conclusion and Summary

1980



1996



Thank you very much !

Hagiwara also visited Sony Atsugi-Tech Center in July 2020.



Thank you very much !