The evidence and supporting comments that Yoshiaki Hagiwara is the true inventor of Pinned Photodiode

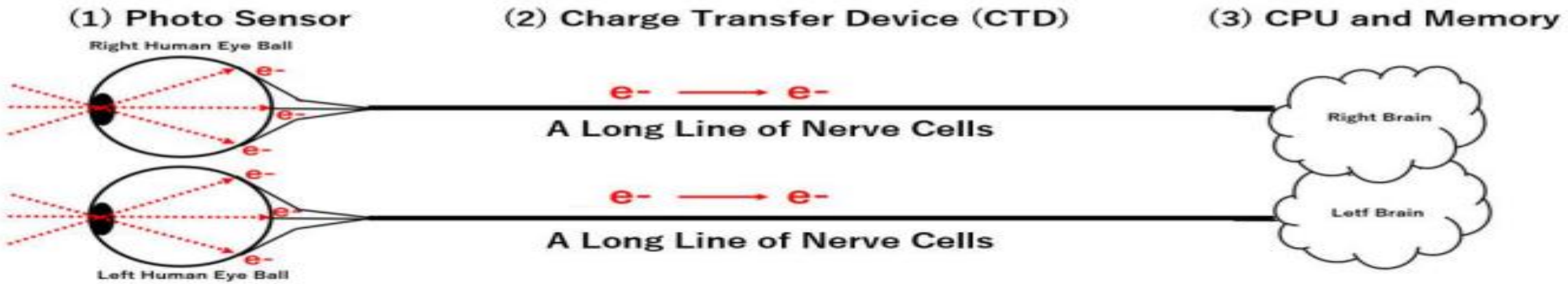
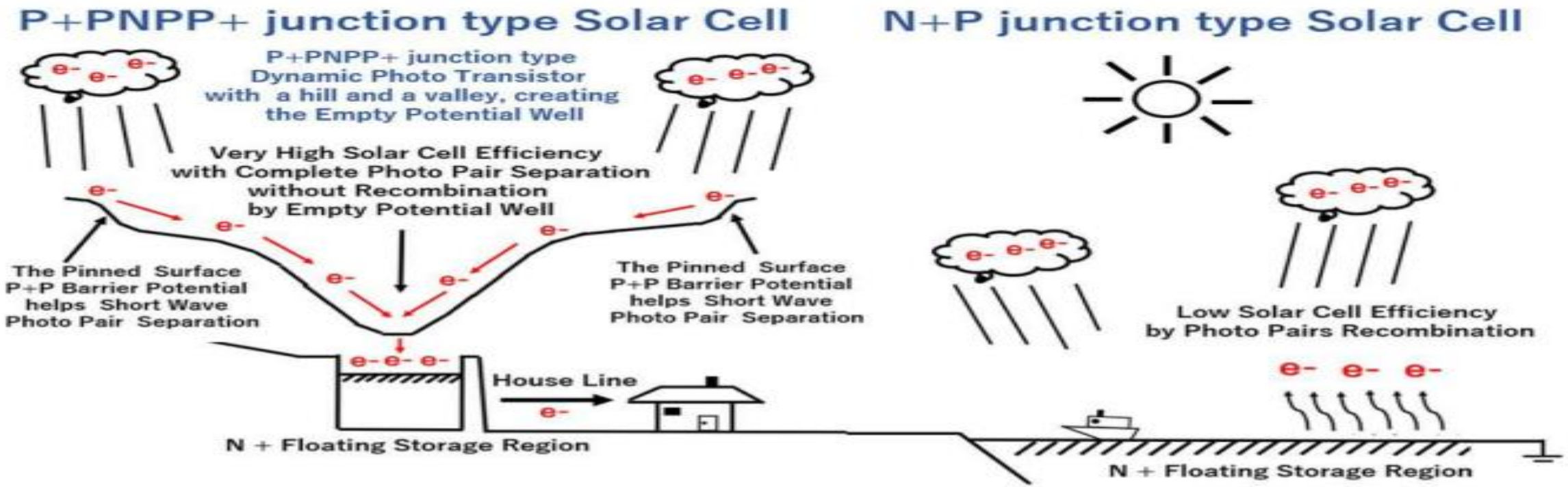


Figure 1. Artificial Intelligent (AI) Image Sensor Structure with Three Basic Parts.



The evidence and supporting comments that Yoshiaki Hagiwara is the true inventor of Pinned Photodiode

- **http://www.aiplab.com/Evidence_that_Hagiwara_at_Sony_is_the_inventor_of_Pinned_Photodiode.html**

which has the link to the following documentations to explain the invention and development efforts by Yoshiaki Hagiwara at Sony

- https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

- **https://harvestimaging.com/pubdocs/089_2005_dec_IEDM_hole_role.pdf**

[Is this structure the mother of the PPD or buried diode or hole-accumulation device (HAD)?]

- **https://www.sony.com/en/SonyInfo/News/notice/20200626/**

Difference between Buried Photodiode and Pinned Photodiode

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

This is a commonly misunderstood misused set of terminologies.

First off these are not PIN Photodiodes - which stands for P - Intrinsic- N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though.

Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space.

You can get surface state pinning from the dangling Si/SiO2 bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The Si/SiO2 surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface.

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

ELECTRICALENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

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A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO. 12, DECEMBER 2006

The Hole Role in Solid-State Imagers

Albert J. P. Theuwissen, *Fellow, IEEE*

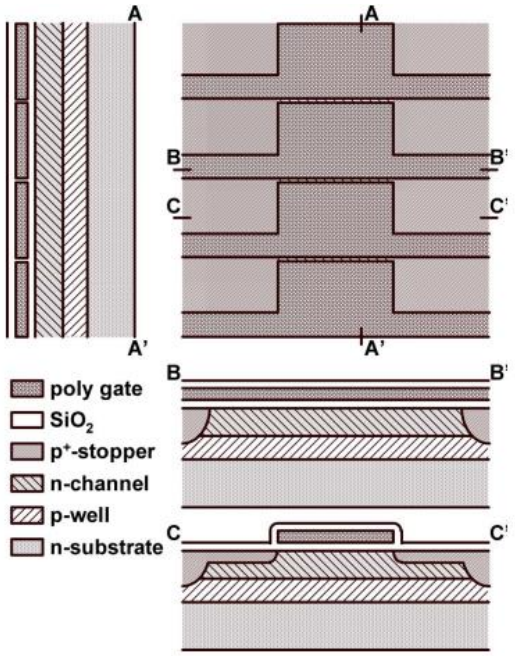

Fig. 4. Same structures are given as shown in Fig. 3, but with an additional self-aligned p^+-implant to extend the stopper region.

[3] G. Beck, M. Collet, J. van Gils, A. Klinkhamer, H. Peek, W. Ruis, J. van Santen, T. Smit, and G. Vandormael, "High density frame transfer image sensor," in *Proc. 14th Conf. Solid-State Devices*, Tokyo, Japan, 1982, pp. 109–112.

[8] Y. Hagiwara, M. Abe, and C. Okada, "A 380H × 488V CCD imager with narrow channel transfer gates," in *Proc. 10th Conf. Solid-State Devices*, Tokyo, Japan, 1978, pp. 335–340.

A relatively old technique to create a two-phase clocking system [8] and/or to increase the blue sensitivity of the imager [3] can be found in the so-called light windows cut in the polysilicon gates. The result is shown in Fig. 3. The open areas

Despite these advantages, notice that parts of the depleted n-type CCD channels are not covered by gate material. In this way, their electrostatic potential is not defined! Such a structure will suffer from serious charge transport issues during its operation, because charge can and will be trapped in local potential pockets. The effect can simply be solved by defining the potential in the open areas through an extension of the p^+-channel stopper. A simple self-aligned p-implant of $2 \cdot 10^{13}/\text{cm}^2$ B-ions after the gate construction is sufficient to extend the channel stop area to the gate edge and, consequently, fix the potential in the open areas. The result after this self-aligned implant is shown in Fig. 4. The presence of enough holes plays a crucial role in fixing the potential for the regions normally "beyond control" of the gates. [Is this structure the mother of the PPD or buried diode or hole-accumulation device (HAD)?]

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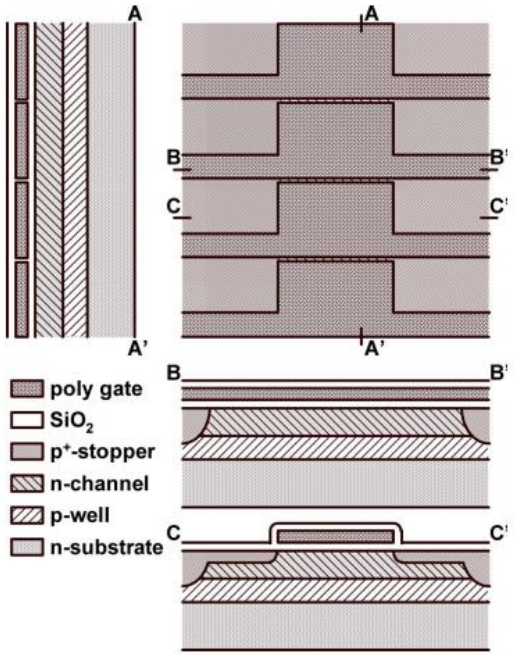

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Proceeding of the 10th Conference on Solid State Devices, Tokyo, 1978;
Japanese Journal of Applied Physics, Volume 18 (1979) Supplement 18-1, pp.335-340

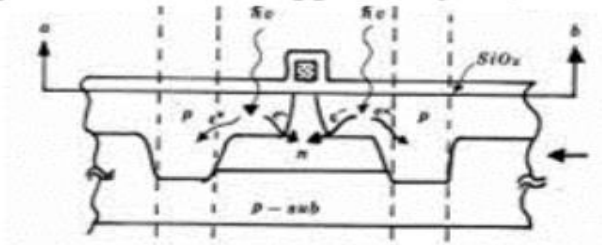

Fig.3 Cross sectional view of the Narrow Channel Transfer Electrode with the SiO2 exposed Pinned Window and the Pinned Photodiode P+ surface.

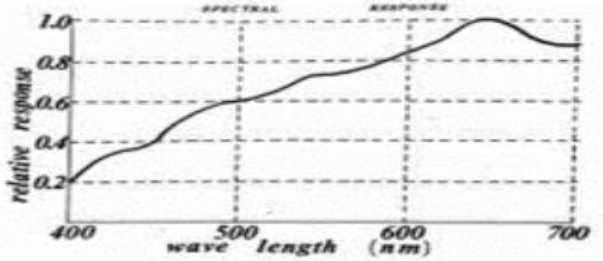

Fig.13 Spectral Response of the Pinned Photodiode with Pinned SiO2 Window and Pinned Surface.

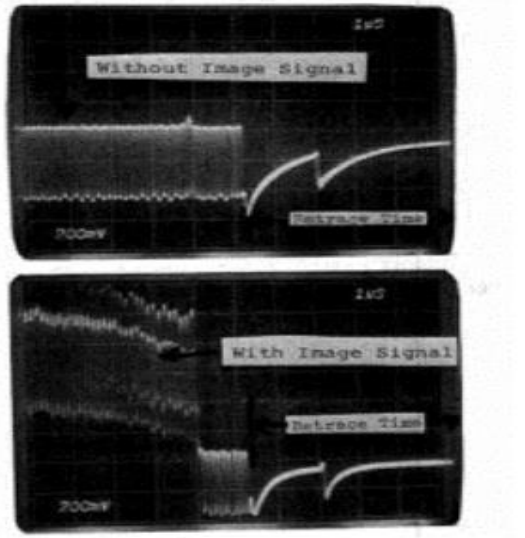

Fig.12 Comparison of the Pinned Photodiode image sensor with and without image signal gives the very low dark current level at retrace time.

A simple self-aligned p-implant of $2 \cdot 10^{13}/\text{cm}^2$ B-ions after the gate construction is sufficient to extend the channel stop area to the gate edge and, consequently, fix the potential in the open areas. The result after this self-aligned implant is shown in Fig. 4. The presence of enough holes plays a crucial role in fixing the potential for the regions normally "beyond control" of the gates. [Is this structure the mother of the PPD or buried diode or hole-accumulation device (HAD)?]

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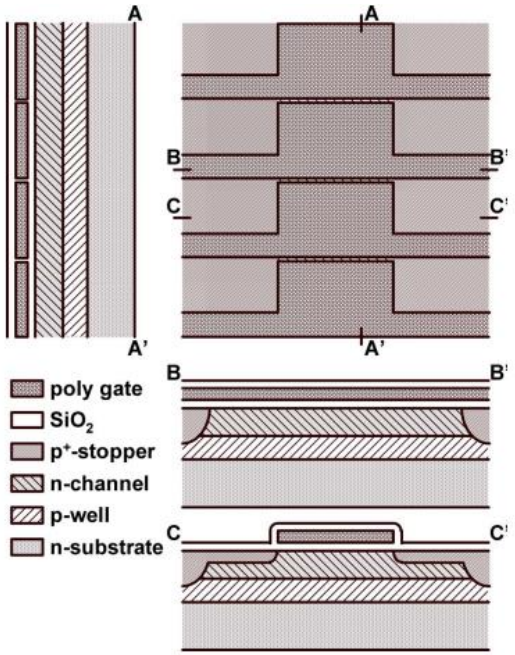

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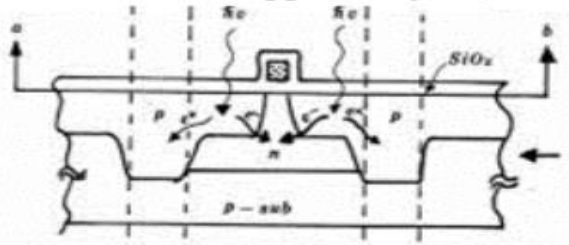

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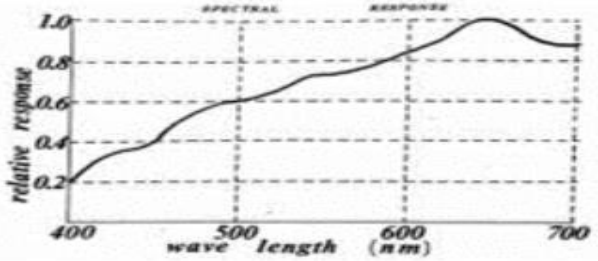

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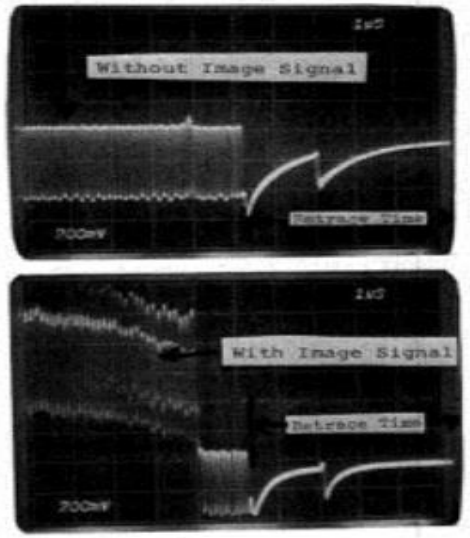

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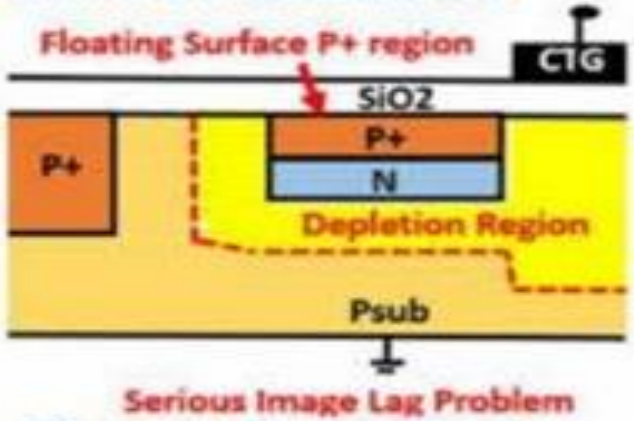
using the polysilicon patterning as an ion implantation mask, boron ions with the dose level of 2×10^{13} cm^{-2} are implanted into the silicon substrate throughout the exposed portions of the thermally grown oxide. This step provides self-aligned channel stops which surround the narrow-channel transfer part of each electrode. The gate oxide thickness is 130 nm throughout the device. Phosphorus doped polysilicon with the sheet resistivity of 50–70 ohm/M and the thickness of 500 nm is used for the gate electrode structure.

The feasibility of the narrow transfer channel CCD structure is confirmed by the realization of 380H × 488V CCD Imager with frame transfer organization. The transfer efficiency of the vertical and horizontal shift registers are more than 99.995%. And high image resolution of 280 TV lines/p.h. (Horizontal) and 350 TV lines/p.h. (Vertical) have been obtained. The typical dark current level is less than 3% of the maximum signal level at the room temperature of 20°C. It is expected that this inherently SiO_2 exposed structure has high enough quantum efficiency at 450 nm wavelength and functions as a color imager with high sensitivity and resolution.

A long P+ Surface Stripe also has a serious RC delay.

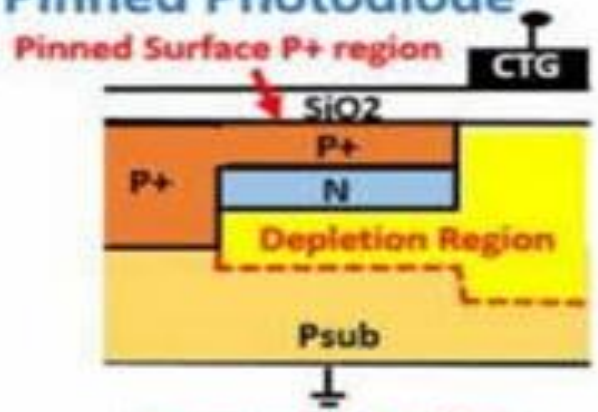
Pinned Photodiode Must Have the Grounded P+ Channel Stops Nearby.

Buried Photodiode



Serious Image Lag Problem

Pinned Photodiode



No Image Lag Problem

The resistivity ρ of the P+ hole accumulation layer is given by

$$\rho = R * W * d / L$$

In the 2/3 inch optical lens system, we have the optical image size of 8.8 mm (H) x 6.6 mm (V) which was a common size in 1980s. Hence, we then have L = 6.6 mm = 6600 μm

The short wave blue light cannot penetrate more than d = 0.2 μm into the silicon crystal in depth. Hagiwara reported in SSDM1978 paper $Qd = 2 \times 10^{13} cm^{-2}$ which gives $Nd = Qd/d = 1 \times 10^{18} cm^{-3}$

For $Nd = 1 \times 10^{18} cm^{-3}$, we have ρ = 0.04 ohm cm = 400 ohm μm

$$RC = \{ L\rho / (W*d) \} \{ \varepsilon W*L / Xo \} = \varepsilon \rho L^2 / (d\, Xo)$$

We have ε = 216 e/volt μm for silicon oxide and $e = 1.6 \times 10^{-19}$ Coulomb

$$RC = (216)(1.6 \times 10^{-19})(400)(6600)(6600) / (0.2)/(0.1) \text{ sec}$$

RC = 30.1 μsec while one frame is 1/60 sec = 16.7 msec and the Vertical CCD register clock period is 16.7/500 = 33.4 μsec

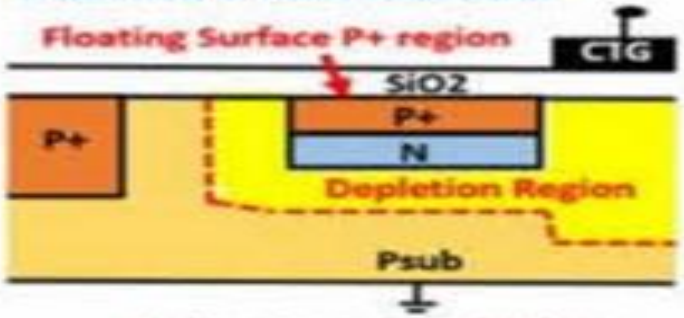
Hence RC delay time may not be ignored and surface P+ may be floating ?

NEC IEDM1982 paper was not Pinned Photodiode by definition.

Difference of Buried Photodiode and Pinned Photodiode

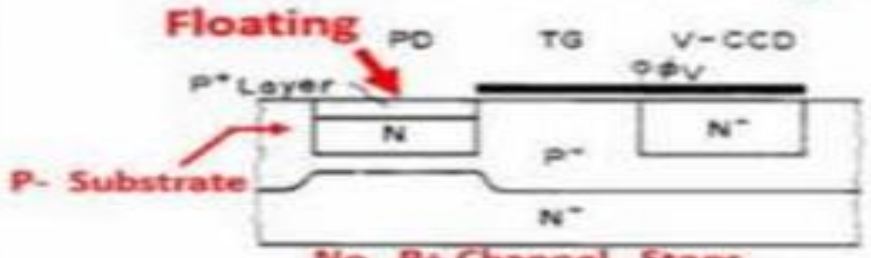
Figure 5 does not have the P+ channel stop nearby.

Buried Photodiode



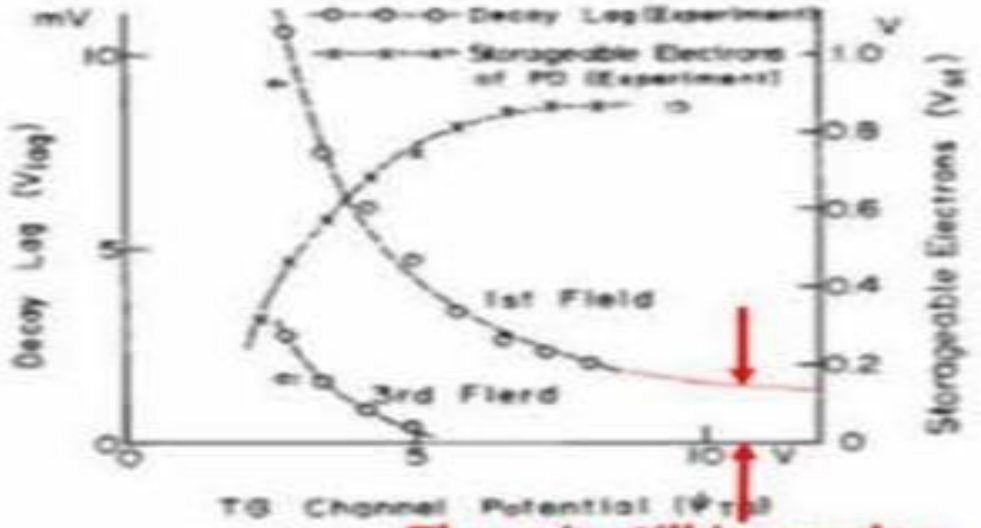
Serious Image Lag Problem

NEC IEDM1982 Paper



No P+ Channel Stops

Fig.5. P+NP- structure photodiode
(a) Unit cell cross sectional view



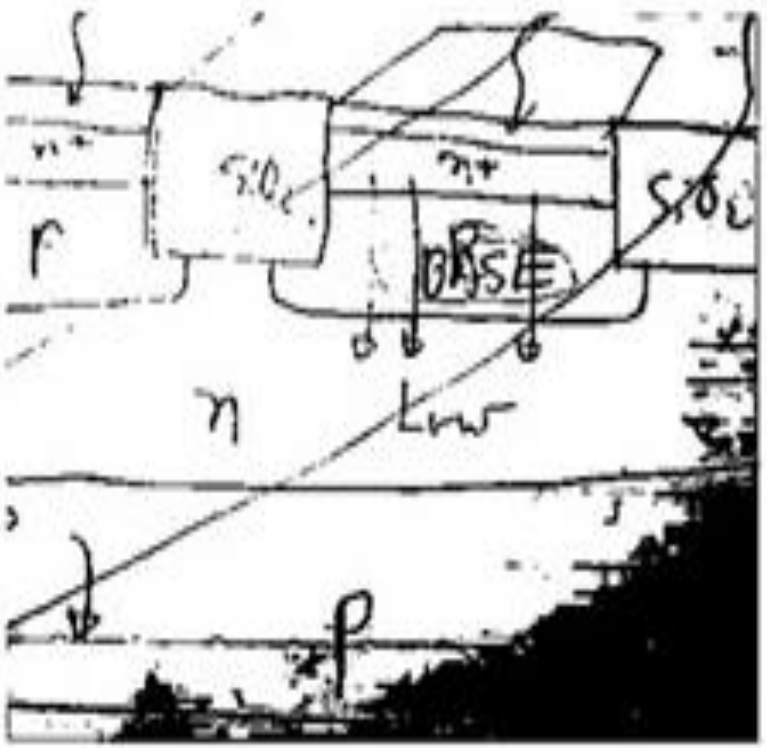
There is still image lag
at the CTD gate voltage more than 10 volt.

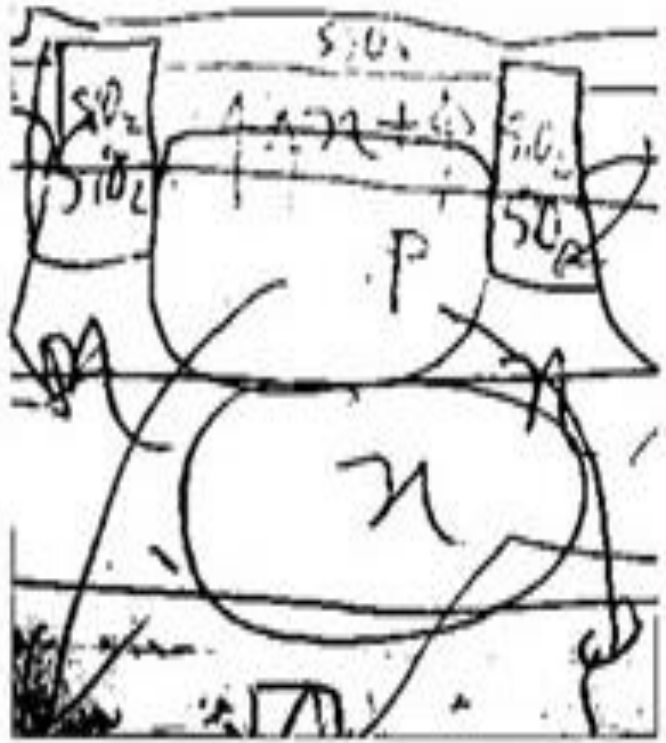
Fig.6. Storageable electrons vs. transfer gate channel potential, and decay lag vs. transfer gate channel potential in the P+NP- structure photodiode

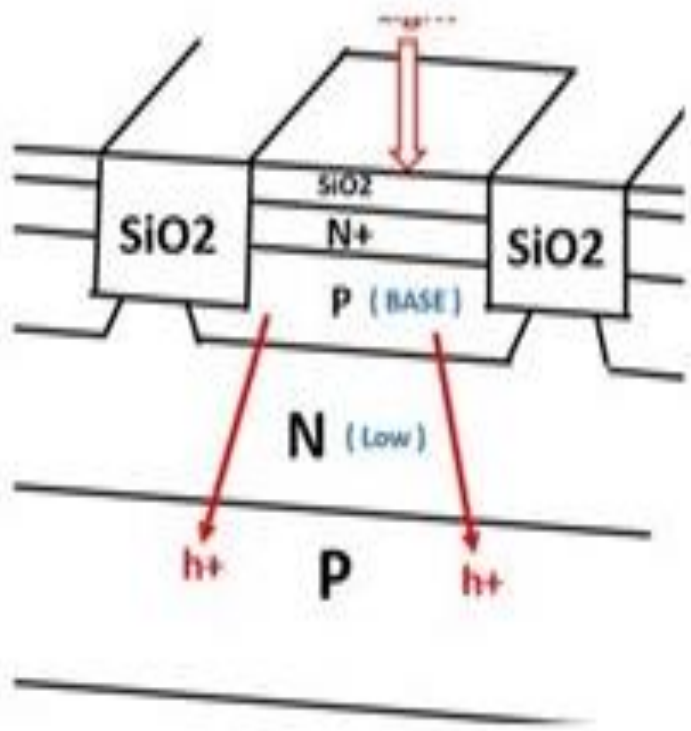
NEC IEDM1982 Paper reported Image Lag

Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 volt.

Hagiwara Note at Sony in March, 1975





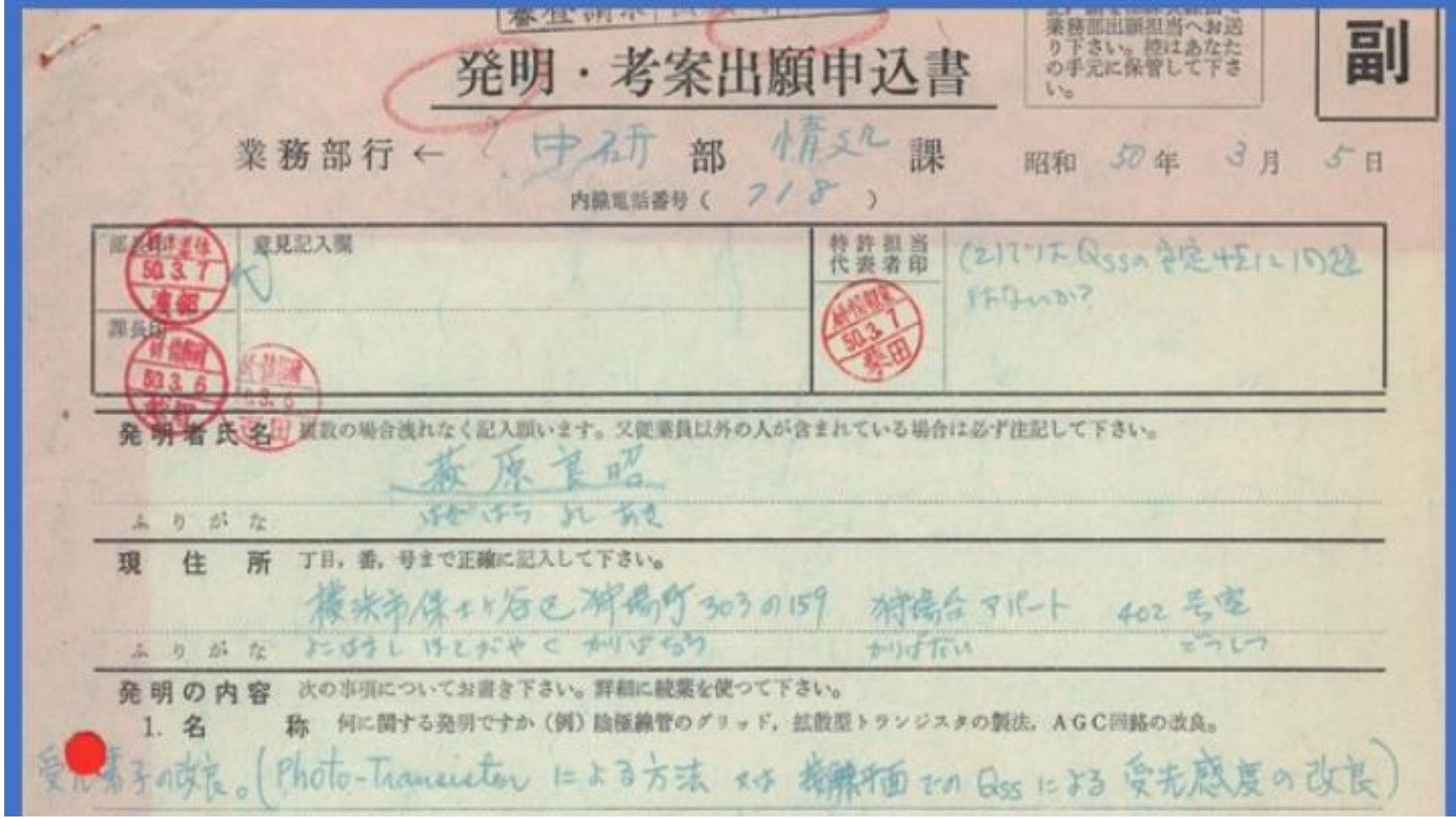


The evidence that Hagiwara at Sony is the inventor of Hole Accumulation Diode (HAD) is given here.
The evidence that Hagiwara at Sony is the inventor of Buried Photodiode (BPD) is also given here.
The evidence that Hagiwara at Sony is the inventor of Pinned Photodiode (PPD) is also given here.
See also Japanese Patent Applications JPA 1975-127646, JPA 1975-127647 and JPA 1975-134985

Who Invented Pinned Photodiode ?

(1) Hagiwara at Sony invented Pinned Photodiode on March 5, 1975.

The evidence is given below by the patent application sheet 1/3 .



発明・考案出願申込書

副

業務部行 ← 中研 部 情処 課　昭和 50 年 3 月 5 日

内線電話番号（ 718 ）

意見記入欄

特許担当代表者印

発明者氏名　萩原良昭

ふりがな　はぎわら よしあき

現住所　丁目，番，号まで正確に記入して下さい。

横浜市保土ヶ谷区神戸町303の159　神保台マンション　402 号室

ふりがな　よこはましほどがやくかんばるちょう　かんばるだい　よつしつ

発明の内容　次の事項についてお書き下さい。詳細に説明を使って下さい。

1. 名　称　何に関する発明ですか（例）陰極線管のグリッド，拡散型トランジスタの製法，AGC回路の改良。

受光素子の改良。(Photo-Transistor による方法 及び 光導体面での Qss による受光感度の改良)

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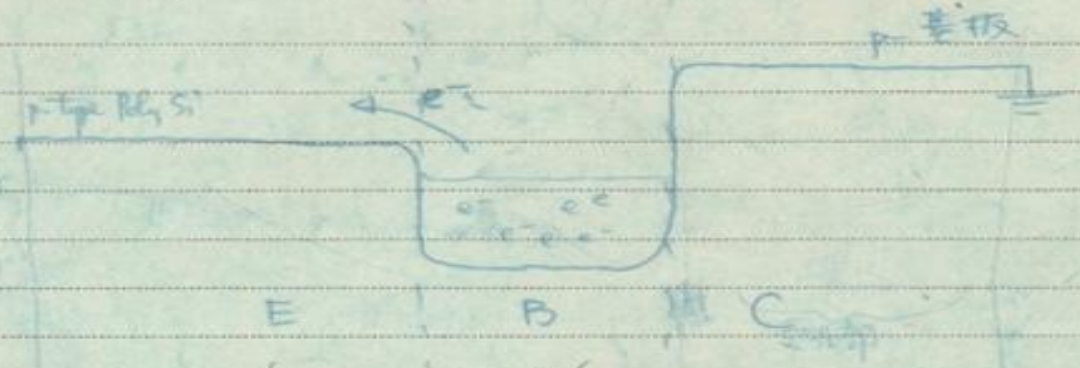
発明の詳細な説明 あなたの発明についてグラフ，図面，回路図などを用いて詳細に説明して下さい。特に 3 要旨 4 実施例 5 効果 などについてお書き下さい。グラフ，図面を別に書く場合は発明考案申込用図表を使用して下さい。

Type ① で述べた Photo-transistor では、Base で受光するわけであるが、
参考にその静電プロテクトを下図に示す。



光電化した電荷量が Overflow する時は E-B 間が On になり、
電荷が Emitter に Drain される。

副

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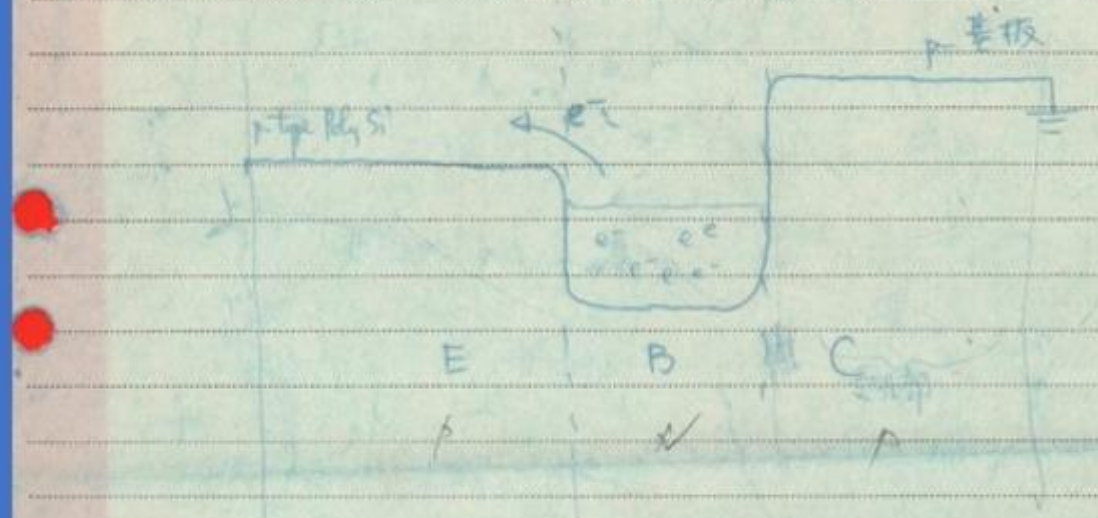

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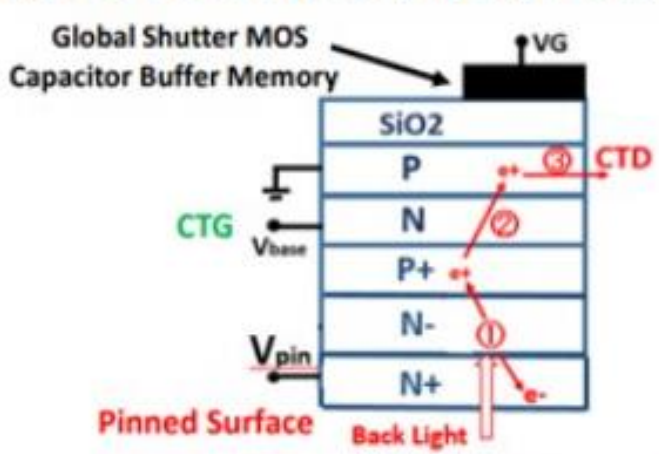
(2) Hagiwara applied JPA 1975-127646 on October 13, 1975 .

Japanese Patent 1975-127646

N+NP+NP junction type Buried Pinned Photodiode
with Built-in MOS Capacitor Buffer Memory Global Shutter Function
and the surface N+N doping slope Barrier Electric Field Photo Pair Generation



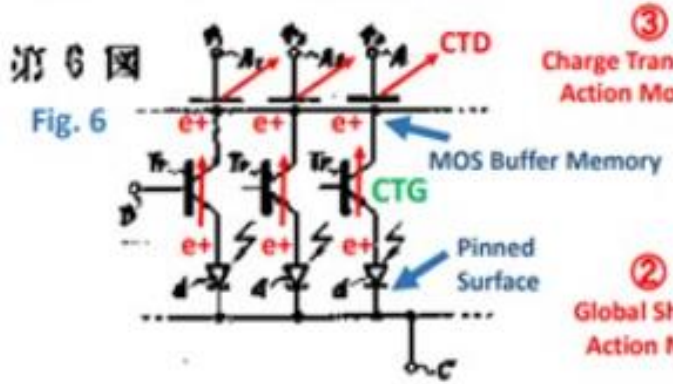


Fig. 6

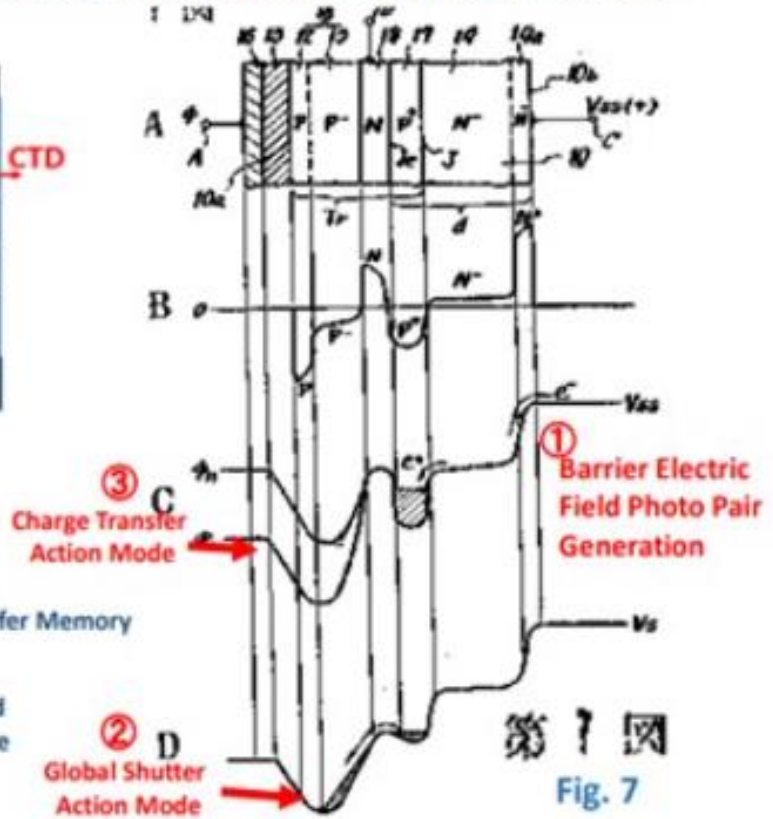


Fig. 7

This shows the original invention of the N+N-P+NP+P triple junction type Pinned Buried Photodiode, which was invented by Hagiwara at Sony on October 13, 1975.

The charge transfer MOS gate can also act as the temporary buffer memory for Global Shutter Operation needed for the modern CMOS image sensors.

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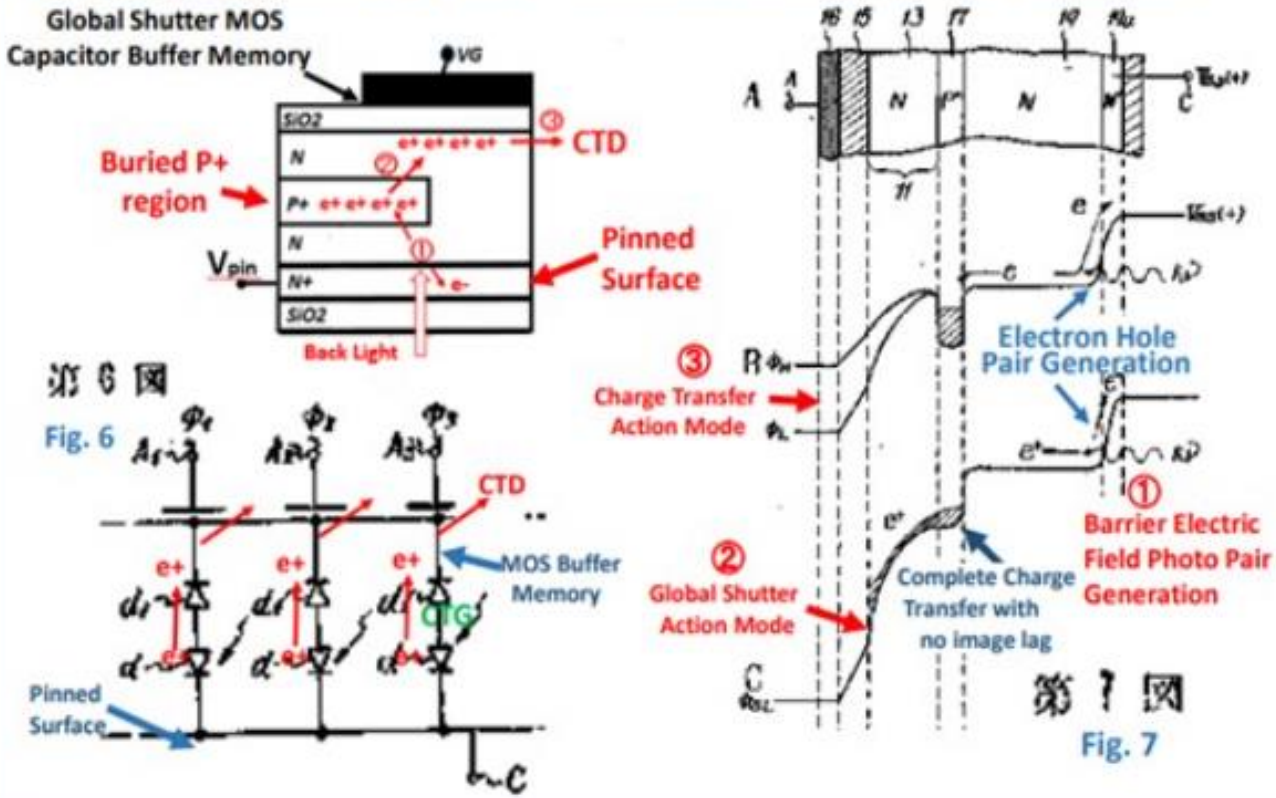

Hagiwara at Sony invented Pinned Photodiode with Backlight Illumination Mode and Global Shutter Function

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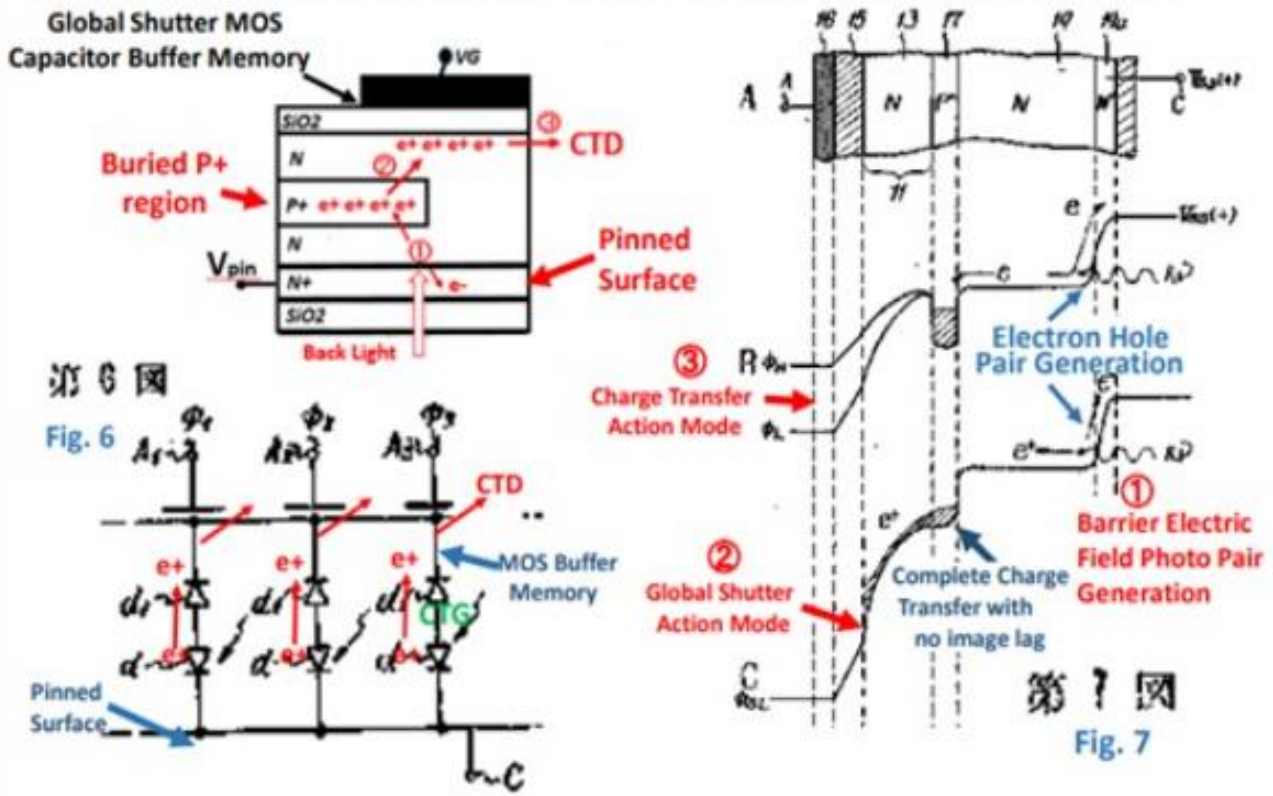
and the surface N+N doping slope Barrier Electric Filed Photo Pair Generation



Hagiwara at Sony invented Pinned Photodiode with Backlight Illumination Mode and Global Shutter Function

This shows the original invention of the PNP double junction type Pinned Buried Photodiode, which was invented by Hagiwara at Sony on November 13, 1975. The charge transfer MOS gate can also act as the temporary buffer memory for Global Shutter Operation needed for the modern CMOS image sensors.

(4) Hagiwara applied JPA 1975-134985 on November 10, 1975 .

Hagiwara at Sony invented Pinned Photodiode with VOD function.

PNPN junction Transistor type Pinned Photodiode

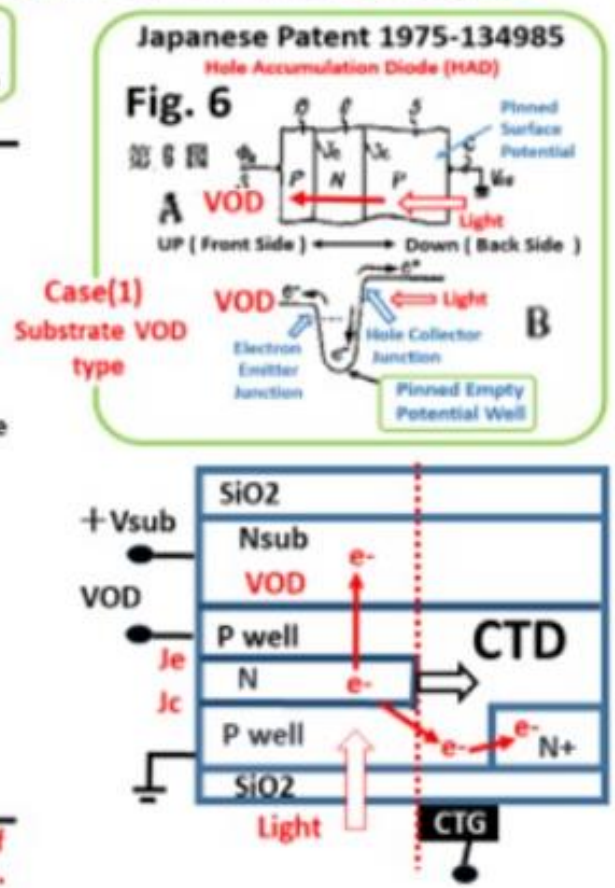
Visit https://www.j-platpat.inpit.go.jp/ and put the patent number 1975-134985

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

Patent Claim in English Translation

(1) In the semiconductor substrate (Nsub), the first region(P well) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N) is is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N) . And (6) Collector junction (Jc) is formed by the second region (N) and the first region (P well), forming a (PNP) transistor structure, (7) Photo charge is stored in the Base (N) according to illuminated light intensity and transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.

Fig.6 shows that this is also the invention of the in pixel VOD (vertical overflow drain).



This shows the original invention of the PNP double junction type Pinned Buried Photodiode with the in-pixel vertical overflow Drain (VOD) structure, which was invented by Hagiwara at Sony on November 10, 1975.

(5) Hagiwara applied JPA 1977-126885 on September 29, 1977 .

Hagiwara at Sony invented also the Electric Shutter Function with the complete image lag free feature by the punch-thru mode.

JPA 1977-126885

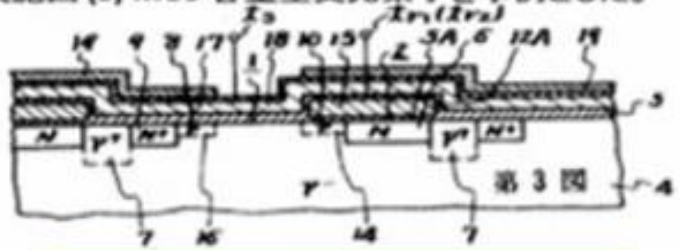
⑩公開特許公報 (A) 昭54—51318
⑪特 願 昭52—126885
⑫出 願 昭52(1977) 9 月29日
⑪出 願 人 ソニー株式会社
⑫発 明 者 荻原良昭
⑫発 明 者 越智成之
同 橋本武夫

発明の名称 固体撮像装置

特許請求の範囲

インターライントランスファ方式による固体撮像装置において、各センサー部のセンサー電極と、上記各センサー部に対応して設けられるオーバーフロー制御部の制御電極とが電気的に共通に構成されると共に、該電気的共通の電極への共通電圧に応じて上記センサー部とオーバーフロー制御部の各ミニマムポテンシャルの差が変化するようになされ、上記各センサー部と、シフトレジスタ部との間のゲート部のゲート電極と、上記シフトレジスタの1のクロック相が与えられる電極とが電気的に共通に構成され、上記ゲート部のミニマムポテンシャルが高められた状態で、オーバーフロー制御を行つてガンマ補正を行うことを特徴とする固体撮像装置。

実施図 (3) MOS 容量型受光素子を事例とした。

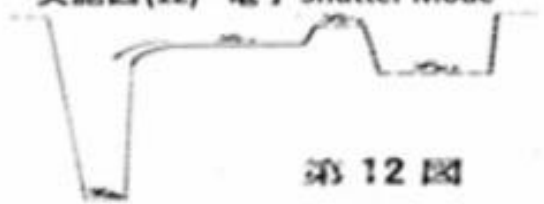


第 3 図

実施図 (9) ガンマ補正 Mode

第 9 図

実施図 (12) 電子 Shutter Mode



第 12 図

VOD 電極端子の電圧を極端に深くして Punch thru を利用して残像のない状態を実現し、電子 shutter 機能を可能にした。

This shows the original invention of the clocking scheme to control the in-pixel overflow drain (OFD) externally to achieve the electric shutter function, which is also applied for the triple junction type Pinned Photodiode with the built-in VOD structure (JPA 1975-134985), originally invented by Hagiwara at Sony on Nov. 10, in 1975.

https://www.sony.com/en/SonyInfo/News/notice/20200626/

Sony's Representative Inventions Supporting Stacked Multi-Functional CMOS Image Sensors

Sony Corporation
Sony Semiconductor Solutions Corporation

Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

The evidence and supporting comments that Yoshiaki Hagiwara is the true inventor of Pinned Photodiode

- **http://www.aiplab.com/Evidence_that_Hagiwara_at_Sony_is_the_inventor_of_Pinned_Photodiode.html**

which has the link to the following documentations to explain the invention and development efforts by Yoshiaki Hagiwara at Sony

- https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

> A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

- **https://harvestimaging.com/pubdocs/089_2005_dec_IEDM_hole_role.pdf**

[Is this structure the mother of the PPD or buried diode or hole-accumulation device (HAD)?]

- **https://www.sony.com/en/SonyInfo/News/notice/20200626/**