Yoshiaki Hagiwara at Sony invented Pinned Buried Photodiode in 1975.

NEC used in 1982 Buried Photodiode and KODAK used Pinned Photodiode in the interline transfer CCD image sensors but they did not invent Pinned Buried Photodiode.

The evidence is given here and explained that, in 1975 at Sony, Yoshiaki Hagiwara invented Pinned Buried Photodiode with the in-pixel Vertical Overflow Drain (VOD) capability. Hagiwara also developed and reported the details of Pinned Buried Photodiode in his SSDM1978 paper.

It is also shown here that there is a big difference between the Pinned Surface Buried Photodiode with Complete Charge Transfer Capability and the Floating Surface Buried Photodiode with the serious Image lag problem.

The presence of the adjacent P+ heavily doped channel stops is important to pin the surface P+ hole accumulation region to realize Complete Charge Transfer capability and achieve the important and desired no-image-lag action picture quality.

The conventional PNP static photo transistor already had the pinned emitter and the pinned collector with the buried base region. The features of the Pinned Surface and Buried Storage Region are not new things. We had them since the early 1950s.

The most important feature of the Pinned Buried Photodiode is the excellent short-wave blue-light sensitivity achieved by the photo electron-hole pair separation in the surface barrier electric field formed by a clever P+P Surface Gaussian Double Doping-engineering proposed by Hagiwara in his 1975 patents.

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

1975-85

Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

~ Discrete Semiconductor/Others ~

In 1975, Sony proposed using a PNP transistor as the photodetector [3]. By providing a P+ layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated to improve the light sensitivity greatly. It was a basic proposal for a pinned photodiode with a P+ layer on the surface of the light receiving part.

Next, proposals were made separately by Hitachi and Sony to use the P+ layer as the substrate potential. In 1977, Hitachi presented a structure in which the high-concentration surface P+ layer is connected to a P-type substrate (well) and pinned it to the same potential as the substrate to increase the charge storage capacity and widen the dynamic range of the photodiode [4]. In 1978, Sony announced an FT (Frame Transfer) -CCD image sensor, using the photodiode with the same structure [5]. Sony succeeded for the first time in the world in prototyping a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor that developed this technology, in 1981 [6].

Photodiodes are used for photodetectors of image sensors. In 1987, Sony developed a 2 / 3-inch, 380,000-pixel CCD image sensor using a new type of photodetector, now called a Pinned Photodiode (Sony named it HAD: Hole Accumulation Diode) [1], and installed it in the 8mm VTR integrated video camera "CCD-V90". In the 1990s, the era of passport size video cameras demands compact CCD image sensors with large numbers of pixels (1/2 inch or smaller with 400,000 pixels or more).

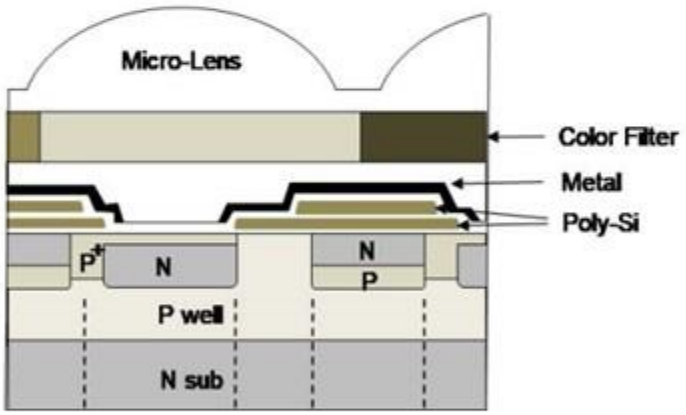


Fig-1 Cross-sectional structure of the IT-CCD image sensor (surface irradiation type)

References:

【1】M. Hamasaki, T. Suzuki, Y. Kagawa, K. Ishikawa, K. Miyata and H. Kambe, "An IT-CCD imager with electronically variable shutter speed" , Technical Report of The Institute of Image Information and Television Engineers. vol. 12, no. 12, pp. 31-36, (1988)

【3】Y. Hagiwara, Japanese Patent JP1975—134985

【4】N. Koike, I. Takemoto. Japanese Patent JP1977—837

【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

【6】I. Kajino, M. Shimada, Y. Nakada, Y. Hirata and Y. Hagiwara, "Single Chip Color Camera Using Narrow channel CCD Imager with Over Flow Drain"、Technical Report of The Institute of Image Information and Television Engineers、vol. 5, no. 29, pp. 32-3S, (1981)

The Photodiode of JP1977-837 is Not Pinned Photodiode !

https://www.sony.com/en/SonyInfo/News/notice/20200626/

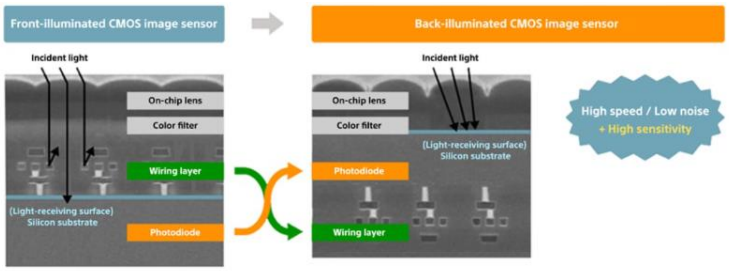
In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP **junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD.**

Sony's Representative Inventions Supporting Stacked Multi-Functional CMOS Image Sensors

Sony Corporation
Sony Semiconductor Solutions Corporation

Taku Umebayashi, an employee of Sony, was awarded the Purple Ribbon Medal in the 2020 Spring Conferment of Medals of Honor. The Purple Ribbon Medals honor influential characters with their outstanding achievement in inventions and discoveries in the field of science and technology, and in the academic, sports, and arts and cultural fields. The medal was awarded to Mr. Umebayashi in appreciation to his achievement in the development of stacked multi-functional CMOS image sensors. His achievement in research and development had already received the Prime Minister Award of the National Commendation for Invention in 2016, and also with recommendation from the Japan Institute of Invention and Innovation ("JIII"), he received the Awards for Science and Technology (Development Category) of the Commendation for Science and Technology by the Minister of Education, Culture, Sports, Science and Technology in 2018. JIII had also recommended Mr. Umebayashi for the Purple Ribbon Medals.

Provided below are explanations of stacked multi-functional CMOS image sensors and Sony's notable inventions which support them.



Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

3. Future Outlook

Stacked CMOS image sensors have made it possible to add completely new functions to CMOS image sensors themselves and have contributed to the dramatic expansion of the image sensor market. As a result, it has promoted domestic investment in equipment for mass production of image sensors and has invigorated the Japanese semiconductor industry.

In the coming era of IoT and AI technology, stacked multi-functional CMOS image sensors will play a large role as a platform for imaging devices that support a new era, and many products equipped with this technology are expected to make our lives richer and more convenient, and to make great contributions to the development and improvement of social infrastructure.

Theuwissen quoted Hagiwara SSDM1978 paper in his IEDM2005 paper and said, “Is this structure the mother of pinned-photodiode or buried diode or hole-accumulation device ?”.

Theuwissen apparently did not know the details of Hagiwara 1975 patents, JPA1975-127646, JPA1975-127647 and JPA1975-134985 on the original Pinned Buried Photodiode with the vertical overflow drain (VOD) function which is identical to the triple junction PNPN dynamic photo thyristor that Sony named the hole accmulation diode (HAD) in 1987.

However, Theuwissen quoted the Hagiwara SSDM1978 paper in his IEDM2005 paper and said, “Is this structure the mother of pinned-photodiode or buried diode or hole-accumulation device ?”.

Yes, this structure is the Pinned Buried and Hole-Accmulation Device that Hagiwara invented in 1975 and develped in 1978.

Albert J.P. Theuwissen, Jan T.J. Bosiers, Edwin Roks, “ The Hole Role “, an invited paper at IEDM2005, Washington DC, Techn. Dig. , 2005.

But in the case that parts of the depleted n-type CCD channels are not covered by gate material, their surface potential is undefined ! Such a structure will suffer from charge transport issues during operation, because charge can be trapped in local potential pockets. The effect can be solved by defining the potential in the open areas through an extension of the p^+ channel stopper. A simple self-aligned implant of $2x10^{13}$ /cm^2 boron ions is sufficient to extend the channel stop areas to the gate edge and consequently fix the potential in the open areas [2]. The result after this self-aligned implant is shown in Figure 3. The presence of enough holes plays a crucial role in fixing the potential for the regions “beyond control” of the gates. (Is this structure the mother of the pinned-photodiode or buried diode or hole-accumulation device ?)

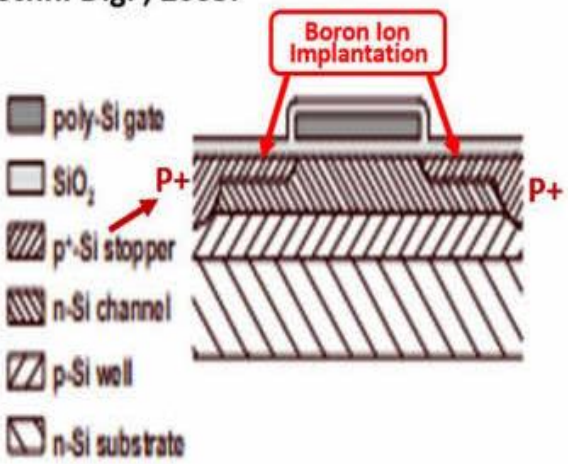
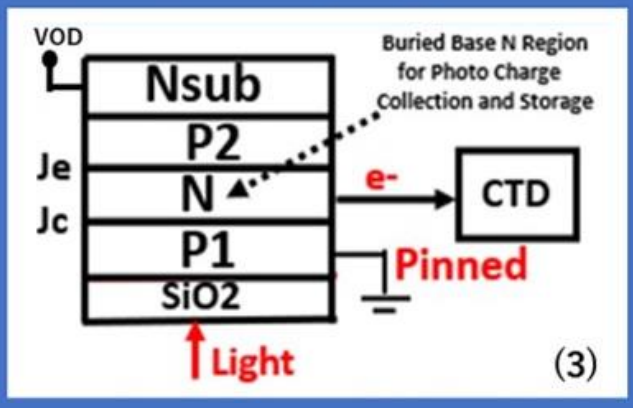


Figure 3. Cross section of a buried-channel CCD on n-Si substrate including light windows and pinned interface potential in the non-covered CCD channels (the cross section is made perpendicular to the CCD channel).

[2] Y. Daimon-Hagiwara et.al., Proc. 10th Conf. on Solid-State Devices, Tokyo, 1978, pp.335-340.

Sony Pinned Buried Photodiode in 1975 with the in-Pixel VOD function and Complete Charge Transfer, Excellent Blue Light Sensitivity and No-Image-Lag Features.

JPA 1975-134985 by Hagiwara in 1975



Original Patent Claims of JPA1975-134985 in Japanese

特許請求の範囲

半導体基体に、第1導電型の第1半導体領域と、之の上に形成された第2導電型の第2半導体領域とが形成されて光感知部と之よりの電荷を転送する電荷転送部とが上記半導体基体の主面に沿う如く配置されて成る固体撮像装置に於いて、上記光感知部の上記第2半導体領域に整流性接合が形成され、該接合をエミッタ接合とし、上記第1及び第2半導体領域間の接合をコレクタ接合とするトランジスタを形成し、該トランジスタのベースとなる上記第2半導体領域に光学像に応じた電荷を蓄積し、ここに蓄積された電荷を上記転送部に移行させて、その転送を行うようにしたことを特徴とする固体撮像装置。

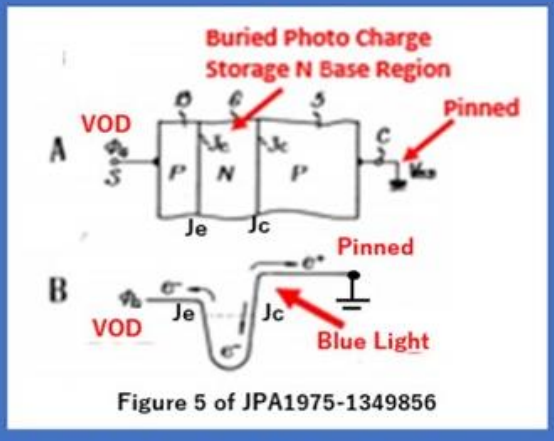
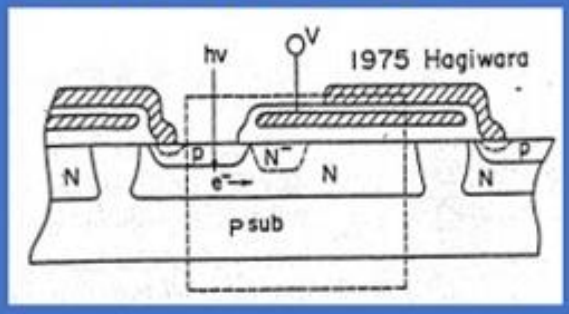


Figure 5 of JPA1975-1349856

English Translation

In a semiconductor substrate (Nsub) the first region (P1) is formed. Then the second region (N) is formed upon it forming the collector junction (Jc). Then on the second region (N), the emitter Junction (Je) is formed. The photo charge is stored in the base region (N) and then transferred to the adjacent charge transfer device (CTD).

(E) Hagiwara 1975 Patent JPA1975-134985



No Image Lag

(A) Toshiba VOD 1978 Patent JPA1978-1971

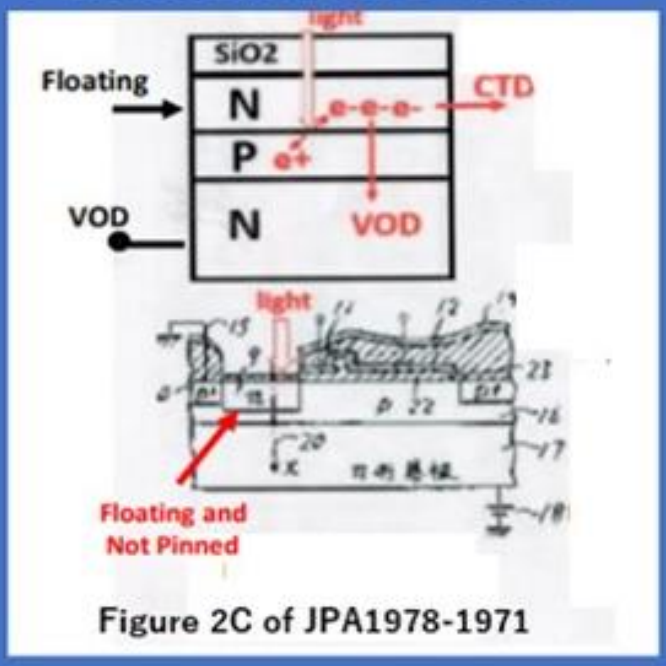


Figure 2C of JPA1978-1971

Toshiba proposed NPN double junction photodiode in 1978 which has a floating surface N type charge storage region. Since the surface N region is floating, this photodiode has the serious image lag and cannot be used for the electrical shutter application since this photodiode does not have the complete charge transfer capability.

Serious Image Lag

(B) NEC Buried Photodiode Patent JPA1980-138026

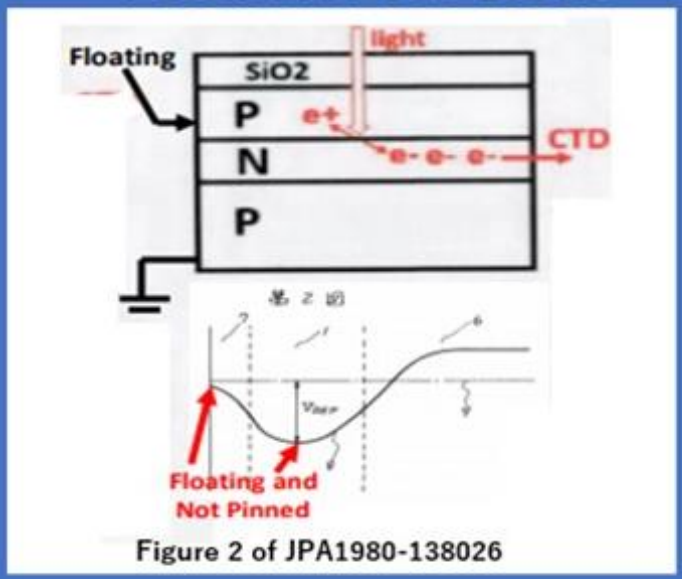


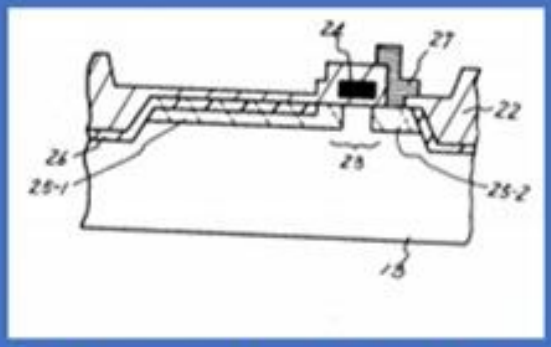
Figure 2 of JPA1980-138026

NEC proposed PNP double junction photodiode in 1980 which has a floating surface P type hole accumulation region. If the surface was pinned, the Fig. 2 shown in the NEC patent could not be possible. NEC claimed that as long as the buried N region is completely drained of photo charge, no-Image-lag feature is possible. But unless the surface is pinned, the N buried region becomes floating and NOT pinned. Hence the complete charge transfer becomes NOT possible and this NEC Buried photodiode suffers the serious image lag problem.

Serious Image Lag

(C) Hitachi OFD 1977

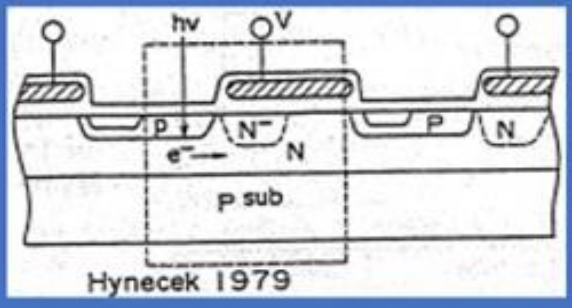
Patent JPA1977-837



Serious Image Lag

LOCOS is used for the device Isolation. Sony did not use LOCOS for imagers. To avoid the thermal oxidation stress, Sony used the high energy ion implantation technology, instead. This Hitachi photodiode of the N charge storage region is not a completely buried photodiode. It has a barrier causing the incomplete charge transfer and the serious image Lag Problem. This is not Pinned Buried Photodiode.

(D) Hynecek 1979

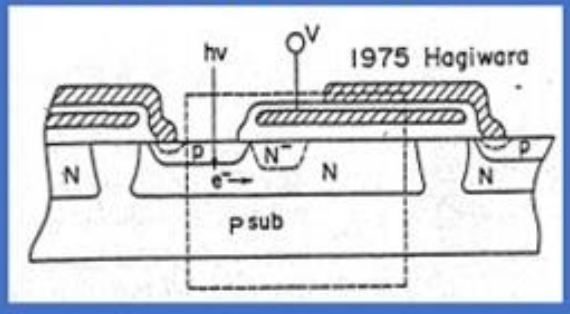


No Image Lag

Hynecek in 1979 proposed the virtual Phase Charge Transfer device with the Pinned Buried Photodiode structure. This device has the complete charge transfer capability and has no serious Image lag problem.

(E) Hagiwara 1975

Patent JPA1975-134985



No Image Lag

Hagiwara in 1975 also proposed the Virtual Phase Charge Transfer Device with the Pinned Buried Photodiode structure. This device has the complete charge transfer capability and has no serious Image lag problem. Note that Hynecek 1979 device is idential to this Hagiwara 1975 device.

ELECTRICALENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

This is a commonly misunderstood misused set of terminologies.

First off these are not PIN Photodiodes - which stands for P - Intrinsic- N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though.

Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space.

You can get surface state pinning from the dangling Si/SiO2 bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The Si/SiO2 surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface.

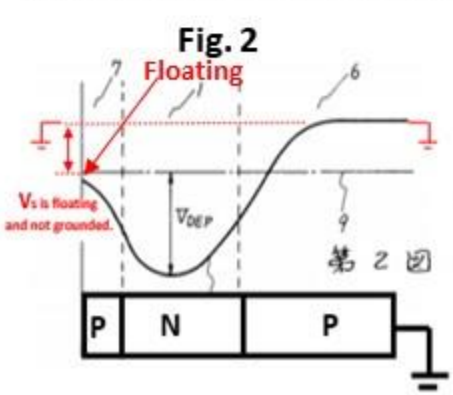
A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

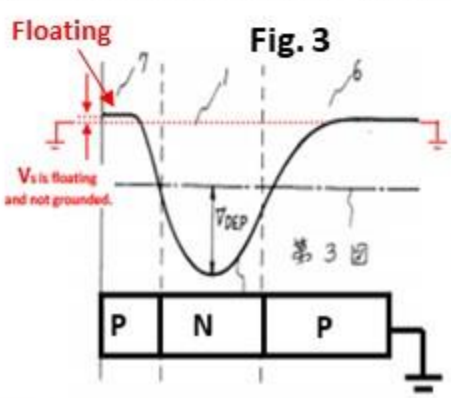
A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

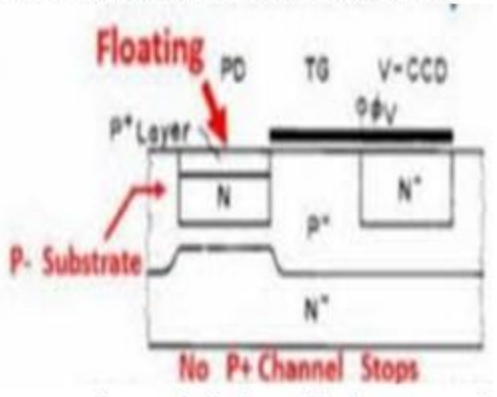
"The first Pinned Photodiode was invented by Hagiwara at Sony."
"It has long been incorrectly attributed to Teranish and to Fossum."

Teranishi at NEC Patent filed Japanese Patent Application JPA 1980-138026 on Buried Photodiode with Fig. 2 and Fig.3 shown below. Observe that the surface potential in Fig.2 is not pinned. It has an undesired surface electric field which induces the serious surface dark current noise problem. Observe also that the surface potential in Fig.2 is not pinned to the substrate ground potential. This is NOT Pinned Photodiode.



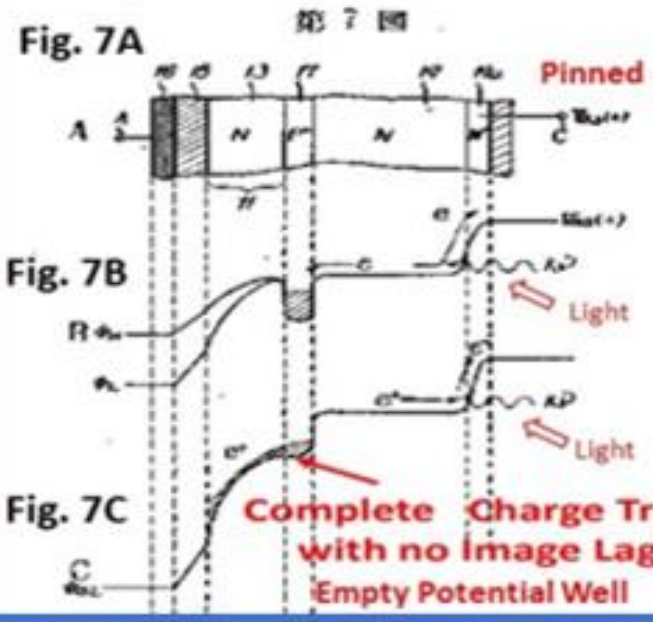


The surface P region is NOT pinned. See Fig.2 of JPA1980-138026

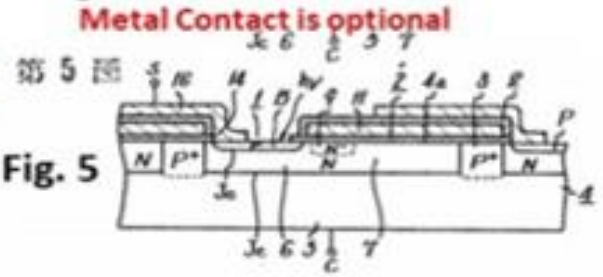


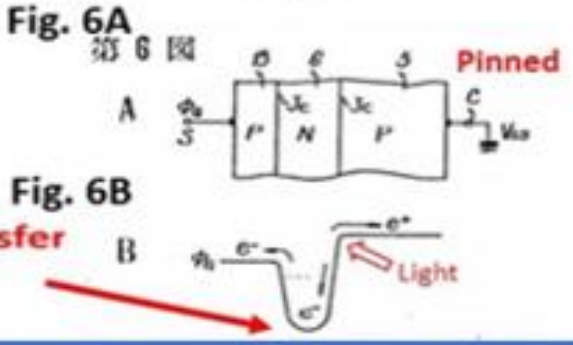
The Buried Photodiode reported in NEC IEDM1982 Paper

(a) Pinned Photodiode defined in Fig. 7 of JPA1975-127647



(b) Pinned Photodiode defined in Fig. 5 and 6 of JPA1975-134985





Hagiwara 1975 patents showed Features of No Image Lag , Empty Potential Well and Complete Charge Transfer of the double junction Pinned Buried Photodiodes.

Fossum 2014 misleading paper invited the serioous misunderstandigs.

This Fossum 2014 paper did not quote Hagiwara 1975 patents completely and with a limited knowledge, made misleading and false comments not based on truth

Indeed, Hagiwara invented PPD with VOD and the virtual charge transfer in 1975

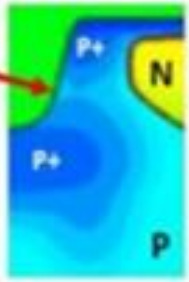
Sony HAD (PPD+VOD) does not use LOCOS

A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Not True and Doubtful ?

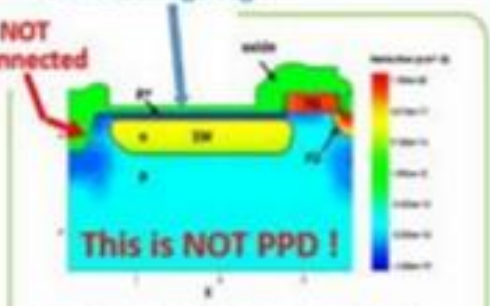
Not True and Doubtful ?

The surface P+ layer is NOT connected to the LOCOS P+ layer. The surface P+ layer may be floating and this photodiode may have serious image lag.



Serious Image Lag ?

NOT connected



Hagiwara in 1975 invented PPD with VOD and the virtual charge transfer.

Study the Japanese Patents 1975-127646, 1975-127647 and 1975-134985.

Pinned Photodiode invented by Hagiwara in 1975 can be used to improve the Solar Cell Efficiency

(a) Pinned Photodiode defined in Fig. 7 of JPA1975-127647

Fig. 7A

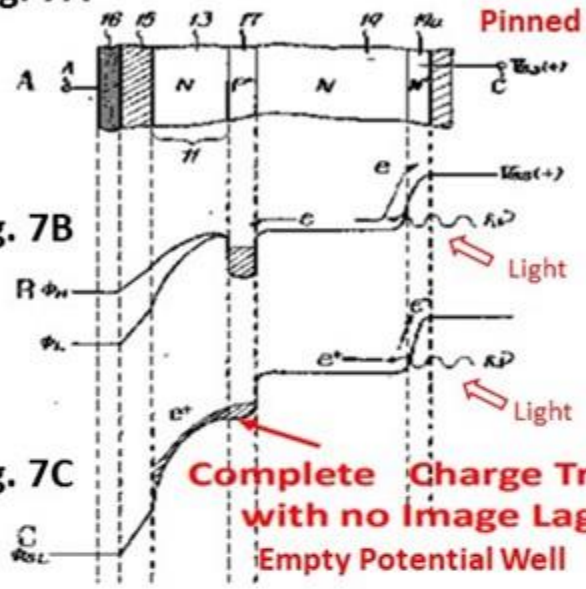


Fig. 7B

Fig. 7C

Complete Charge Transfer with no Image Lag

Empty Potential Well

(b) Pinned Photodiode defined in Fig. 5 and 6 of JPA1975-134985

Metal Contact is optional

Fig. 5

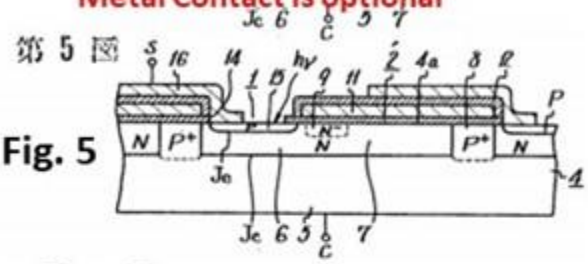


Fig. 6A

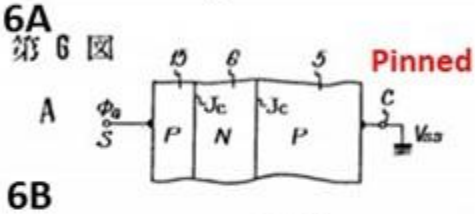
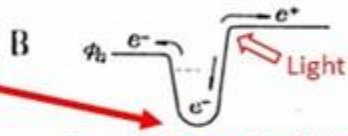
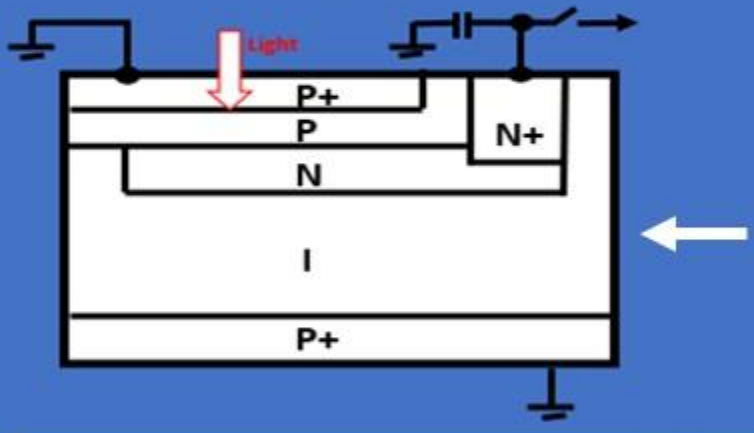


Fig. 6B



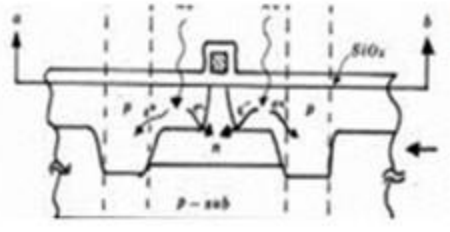
Empty Potential Well

(c) Pinned Buried PIN Photodiode type Image Sensors and Solar Cells (Hagiwara JPA2020-131313)

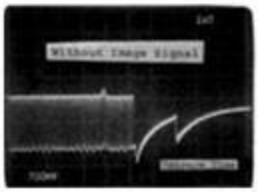


P+ P Pinned Surface Hole Accumulation Region (P), Charge Collecting Buried N region always completely depleted, and Intrinsic Semiconductor Region (I) on the P+ heavily doped region for GND Ohmic contact.

(d) SSDM1978 paper on the PNP junction type Pinned Photodiode with the Pinned P+ surface connected to the adjacent P+ channel stops



Low Dark Current



Complete Charge Transfer
No Image Lag

Proceeding of the 10th Conference on Solid State Devices, Tokyo, 1978:
Japanese Journal of Applied Physics, Volume 18 (1979) Supplement 18-1, pp.335-340