This is a private communication between Albert and Yoshi. Albert is a distinguished expert on the image sensor society. Yoshi asked an expert opinion. An expert must have in public the responsibility of what he says

****

Albert supports that

Yoshi had the Pinned Photodiode idea

before Teranish 1980 Patent.

****

FROM: hagiwara [mailto:hagiwara-yoshiaki@aiplab.com]

SENT: Tuesday, July 10, 2018 3:19 PM

TO: 'a.theuwissen'

SUBJECT: RE: NEC-SONY Patent War

****

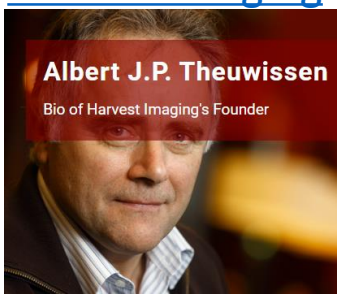
> Hi, Albert,
>
> how are you ?
> I am very mad at Fossum's 2014 paper
> which I found just a few weeks ago.
>I am now 70 years and completely retired..
>Fossum did not quote the very important
> Pain's work at JPL CalTech
>on theGlobal Shutter CMOS image sensor ...
>
> Yoshi

****

On Tue, 10 Jul 2018 18:24:23 +0900, hagiwara wrote:

> Albert,
>
> I am sorry my previous e-mail title was in Japanese,
> copying to many unrelated people.
> But they are also my friends.
> I am re-sending with more information
> on the Pain's paper.
> You know, I was also a visiting professor
> at CalTech during 1998 to 1999
> and frequently visiting Pain's Lab at JPL,
> CalTech during the period.
> I remember Pain and his team really hated
> Fossum at that time.
> I recall they called Fossum a thief.
> Kind regards
>
> Yoshi

Harvest Imaging



This is a private communication between Albert and Yoshi. Albert is a distinguished expert on the image sensor society. Yoshi asked an expert opinion. An expert must have in public the responsibility of what he says

****

From: albert theuwissen

Sent: Tuesday, July 10, 2018 6:55 PM

To: hagiwara-yoshiaki@aiplab.com

Re: How are you ? from Yoshi of Sony(Hagiwara180710)

****

Dear Yoshi,

Good to hear from you, although it is not all good news
you are sending to me.

Can you tell me the reference of the Pain paper ?

When and where was it published ?

Very interesting information !!

At the time Fossum started to write the overview paper
about the PPD, he asked me to become a co-author
and to help him out with the paper.

After some doubt I declined his invitation,
because I do know that the discussion
about the inventor of the PPD is very sensitive,

and I do agree with you that the structure
you developed is indeed a PPD,
maybe not called that way at that time and
also invented for some other purpose.

But it still remains a PPD !

At Philips, in the late '70s a very similar structure
was implemented in the CCDs, this was before
I joined Philips in 1983.

So yes, there were several p+/n-/p- structures
known by the time that Teranishi issued his patent.

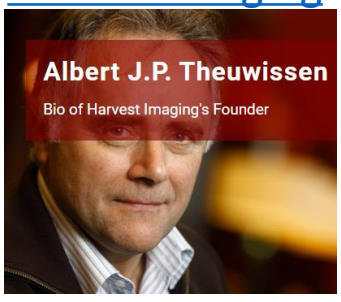
I fully agree to that.

Looking forward to hear from you,

Regards,

Albert.

Harvest Imaging



Evidence that Yoshiaki Hagiwara at Sony in 1975 invented Pinned Buried Photodiode with the complete charge transfer capability of the no-image-lag feature and the Anti-blooming Vertical Overflow Drain (VOD) in order to realize the completely-mechanical-parts-free electrical Shutter. Hagiwara invented Electrical Shutter.

Japanese Patent Application JPA1975-127646

Japanese Patent Application JPA1975-127647

Japanese Patent Application JPA1975-134985

Japanese Patent Application JPA1977-126885

P1977_Narrow_Cahnnel_Transfer_Gate_CCD_SSDM1977_Paper_by_Hagiwara.pdf"

Hagiwara_SSDM1978_Paper_on_Pinned_Buried_Photodiode.pdf

an invited Talk at CCD'79 Conference

"ADVANCES in CCD Imager " Technical Digest of IEEE International Conference

IEEE1996_Review_Paper_on_Sony_1980_One_Chip_FT_CCD_Image_Sensor with_Pinned_Buried_Photodiode

an invited ESSCIRC2001 Plenary Talk,

"Micro-Electronics for Home Entertainment"

IEEE IEDM2004 Conference Short Course

Turorial Short Cource on Image Sesnors by Yoshiaki Hagiwara.pdf

an invited ESSCIRC2008 Plenary Talk,

"SOI Design in Cell Processor and Beyond"

Invited Plenary Panel Talk at ISSCCC2013 on Feb. 2013 on Image Sensors

"Multichip CMOS Image Sensor Structure for Flash Image Acquisition"

"Simulation and Device Characterization of the P+PN+P Junction Type Pinned Photodiode and Schottky Barrier Photodiode"

"Electrostatic and Dynamic Analysis of P+PNP Double Junction Type

P2021_ICECET2021_Paper61_on_Pinned_Buried_PIN_Photodiode_Type_Solar_Cell.pdf

P2021_ICECET2021_Paper75_on_Invention_and_Historical_Development_Efforts_of_Pinned_Burie_Photodiode.pdf

A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, *Fellow, IEEE*, and Donald B. Hondongwa, *Student Member, IEEE*

***Abstract*—The pinned photodiode is the primary photodetector structure used in most CCD and CMOS image sensors. This paper reviews the development, physics, and technology of the pinned photodiode.**

***Index Terms*—C... pixel image s... (PPD), pixel...**

The photocurrent depends on the wavelength-dependent photon flux $\phi(\lambda)$ incident on the semiconductor and the wavelength-dependent quantum efficiency $\eta(\lambda)$ which accounts for optical reflection, absorption and carrier collection:

(2)

The PNP device defined as Pinned Photodiode by Fossum has the surface P+ region is floating with RC delay, actually causing the serious image lag. This is a misleading and a fake paper. Fossum did not explain the important detailed efforts and achievements of Peter Noble reported in the paper,

[6] P. J. W. Noble, "Self-scanned silicon image detector arrays," IEEE Trans. Electron Devices, vol. 15, no. 4, pp. 202–209, Apr. 1968.
on the active photo sensor with the built-in source-follower type in-pixel current amplifier circuit, a very important element for modern CMOS image sensors.

Fossum made many misleading and fake comments on Hagiwara 1975 Japanese patent and SSDM1978 paper.

[24] Y. Hagiwara, Japanese Patent App 50-134985, 1975.
[25] Y. Hagiwara, "High-density and high-quality frame transfer CCD imager with very low smear, low dark current and very high blue sensitivity," *IEEE Trans. Electron Devices*, vol. 43, no. 12, pp. 2122–2130, Dec. 1996.
[26] Y. Hagiwara, "Microelectronics for home entertainment," in *Proc. ESSCIRC*, Sep. 2001, pp. 153–161.
[27] Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488 V CCD imager with narrow channel transfer gates," *Japanese J. Appl. Phys.*, vol. 18, supplement 18–1, pp. 335–340, 1979.

Fossum failed to quote the first Pinned Photodiode patent application JPA1975-127646 and JPA1975-127647 by Hagiwara at Sony on Oct 13, 1975 for the first time in the world.

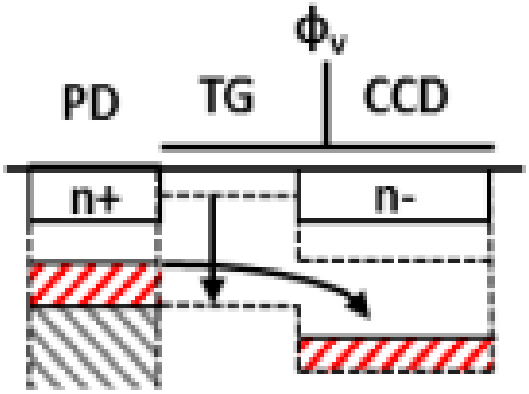


Fig. 1. Signal charge transfer from ILT CCD n+p photodetector.

integrated in the photodetector. The shift register part of the pixel was covered with a metal (or silicide) light shield to eliminate smear. The ILT CCD architecture was more suitable for consumer video application due to reduced smear and more compact chip design than the full-frame CCD. The rapid growth of the consumer electronics video camera market accelerated the improvement of ILT CCD image quality and many advancements [illegible] 1980's. To furt[illegible] a frame-inter[illegible] quently de[illegible] in 1981 [illegible] to that of[illegible]

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Second[illegible] nated, ca[illegible] may cont[illegible] frames. Th[illegible] in CCD vide[illegible] lag is related to [illegible] be substantial.

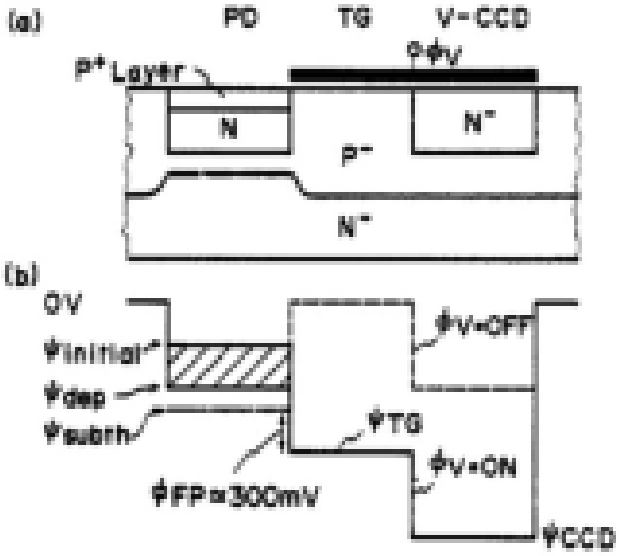

Fig. 2. Complete charge transfer from a pinned photodiode. (a) structure including VOD (b) potential well diagram (from Teranishi et al., 1982).

Third, blue light [illegible] absorption length in silicon may be absorbed in [illegible] region and the photohole may [illegible] junction and be [illegible] in the blue [illegible] devel- [illegible] of the [illegible] ways [illegible] cking [illegible] [14]. [illegible] patent [illegible] hed a [illegible] es in [illegible] hase" [illegible] layer [illegible] ential [illegible] more [illegible] built- [illegible] ozen" [illegible] turing [illegible] itivity [illegible] it had [illegible] urrent [illegible] ted as [illegible] mance [illegible] low- [illegible] EC is [illegible] ig. 2. [illegible] signal [illegible] CCD. [illegible] p layer [illegible] depleted [illegible] e. Since it is [illegible] suppressed. In the

This device is not Pinned Photodiode.
The surface P+ is flaoting with RC delay
without adjacent P+ channel stops

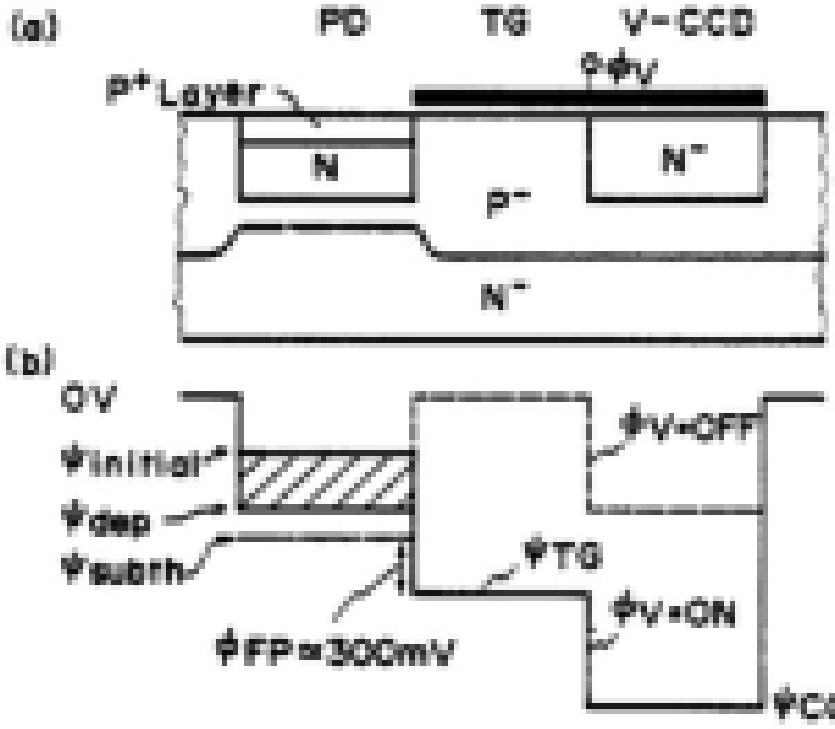

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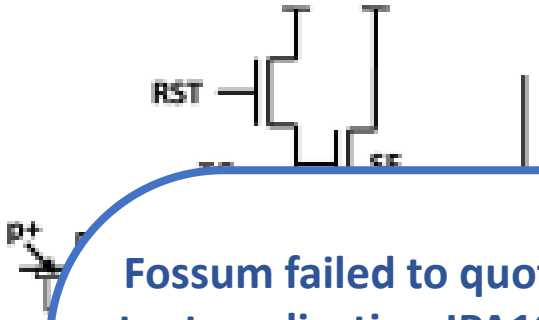
Fig. 2. Complete charge transfer from a pinned photodiode. (a) structure including VOD (b) potential well diagram (from Teranishi et al., 1982).



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In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a pnp vertical structure was disclosed, among several structures [24]. The top p layer was connected by metal to a bias used to control full-well capacity and the n-type base layer was proposed for carrier storage.

Yes, this is the original definition of the PNP junction type Pinned Photodiode.

The external voltage can also be grounded to get the full-charge storage capacity and also the completely Empty Potential Well at the reset time at the start of the photo-charge integration time.

NEC paper was published. However, the "narrow-gate" CCD with an open *p*-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

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C. Other

The PPD
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inventions were solving different problems with essentially the same device structure and operating principles.

In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a *pnp* vertical structure was disclosed, among several structures [24]. The top *p* layer was connected by metal to a bias used to control full-well capacity and the *n*-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1986, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called "Hole Accumulation Diode," or HAD structure [25]. However, the 1975 application did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the

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complete intrapixel charge transfer from the photodiode is not performed. Sometimes "partially pinned photodiodes" [37] were used in 3T CMOS APS devices.)

Shared readout refers to the connection of multiple pixel FDs to a single source-follower output and reset gate [38], [39]. In this case components of the "normal" 4T APS pixel are now spread across 2 or 4 pixels, making the average transistor count per pixel 2.5T, 1.75T, or 1.5T depending on the degree of sharing and other circuit economies. Readout circuit sharing allows either improvement in fill factor or pixel density.

Conceptually, thinning for backside illumination (BSI) originated with silicon targets for vidicon tubes [40]. Backside illumination of CCDs – that is, illuminating the device from the side opposite the "front" side with metal wiring and transistors – was first reported by Shorties et al. [41], [42] and used primarily in scientific and defense applications [see e.g., [43], [44]. Extension of this concept to CMOS image sensors was suggested early [30] and the first patent application on a BSI

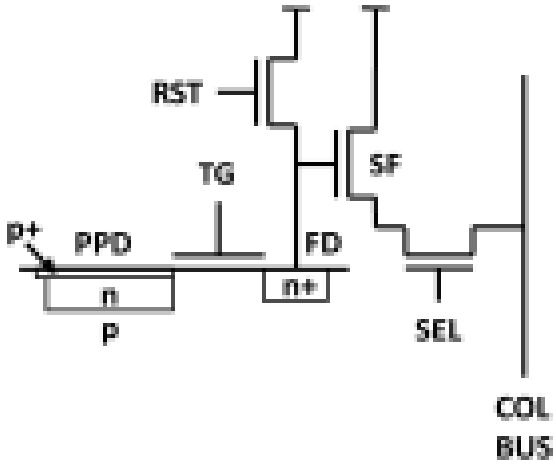

Fig. 3. Schematic of CMOS APS pixel with PPD.

1982 paper they also added a vertical anti-blooming structure (i.e. $p+npn$) or vertical overflow drain (VOD) so that when the capacity of the n storage region was filled, excess carriers would drain to the substrate rather than bloom to neighboring pixel storage areas or into the CCD readout device. Another nice feature of the device was that the $p+$ cap layer was integrally tied to the other p layer like the Noble device.

In 1984, the structure received the name "pinned photodiode" (a.k.a. PPD) in a paper published by Burkey et al. at Kodak [21]. In this paper, the improved blue QE of the structure (due to the thin pinning layer) and its high charge capacity were emphasized. Starting in 1987 the PPD was incorporated into most ILT CCD architectures [22] and became a fixture in consumer electronics video cameras and, later, in digital still CCD cameras. A review of various photodetector elements for ILT CCDs was presented by Kodak in 1991 [23].

C. Other Contributions to the PPD Invention

The PPD structure, while invented for low lag ILT CCD application, shares a strong resemblance to the Hynecek virtual-phase CCD structure, with the exception of the VOD. The two inventions were solving different problems with essentially the same device structure and operating principles.

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NEC paper was published. However, the "narrow-gate" CCD with an open p-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

The PPD, as it is most commonly used today, bears the strongest resemblance to the Teranishi et al. ILT CCD device. Thus, these days Teranishi is considered as the primary inventor of the modern PPD [29].

D. Application to CMOS Active Pixel Image Sensors

In 1993, a CMOS active pixel image sensor (APS) with intra-pixel charge transfer was proposed by Fossum et al. at JPL [30], [31]. Performance improvement using backside illumination (BSI) and a pinned photodiode was suggested in 1994 [32]. A CMOS APS pixel with a PPD is shown schematically in Fig. 3. Signal charge collected by the pixel photodetector is transferred to a floating diffusion (FD) whose potential is monitored by a source-follower (SF) within the pixel. FD is reset by transistor reset signal (RST) prior to transfer and the source-follower is connected to the column bus line (COL BUS) using a row-select transistor (SEL).

Implementing a pinned photodiode (PPD) with a CMOS APS was technically challenging since the CCD PPD required high transfer gate voltages to reduce any potential barriers and achieve complete charge transfer. Such high voltages (12-15 V) were not generally compatible with CMOS processes. Integrating the CCD PPD into a CMOS APS was first reported in 1995 from a JPL and Kodak collaboration in which Kodak developed a low voltage PPD implementation [33]. Further refinement [34–36] and widespread adoption of the PPD in CMOS image sensors occurred in the early 2000's and helped CMOS APS achieve imaging performance on par with, or exceeding, CCDs.

Since the PPD is often used in pixels with nominally four (4) transistor gates, such a CMOS APS pixel is often referred to as a "4T" pixel. (This is in contrast to a "3T" pixel which refers to CMOS active pixel sensors where the photodiode is directly connected to the in-pixel source-follower, and complete intrapixel charge transfer from the photodiode is not performed. Sometimes "partially pinned photodiodes" [37] were used in 3T CMOS APS devices.)

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Fossum insulted Hagiwara 1996 by many false statements.

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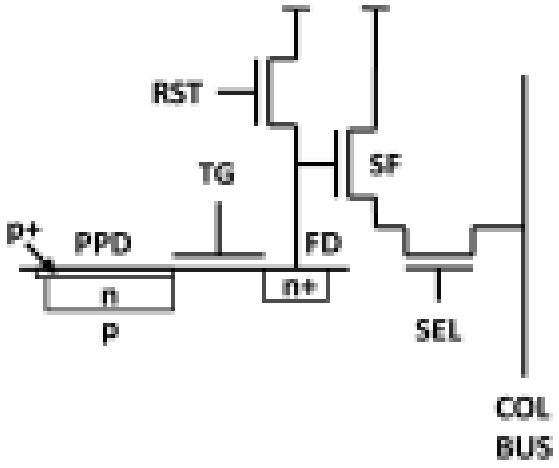

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This is not true. The 1975 applications did show these features.

Fossum did not see Fig 6 of JPA1975-134985 by Hagiwara. Fossum did not see the evidence shown in JPA1975-127646, JPA1975-127647 and JPA1975-134985. Fossum obviously did not read the three Japanese patent applications in details to form the correct point of views. This paper has many misleading incorrect explanations. A fake paper.

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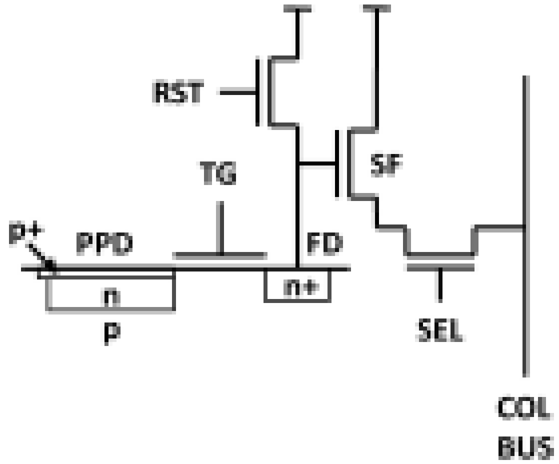

Fig. 1. Schematic of CMOS APS pixel with PPD.

1982 paper they also added a vertical anti-blooming structure

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Fossum did not quote the in-pixel source-follower Active Circuit invented by Peter Noble in 1966. Fossum did not invent Active Image Sensor (APS).

In 1993, a CMOS active pixel image sensor (APS) with intra-pixel charge transfer was proposed by Fossum et al. at JPL [30], [31]. Performance improvement using backside

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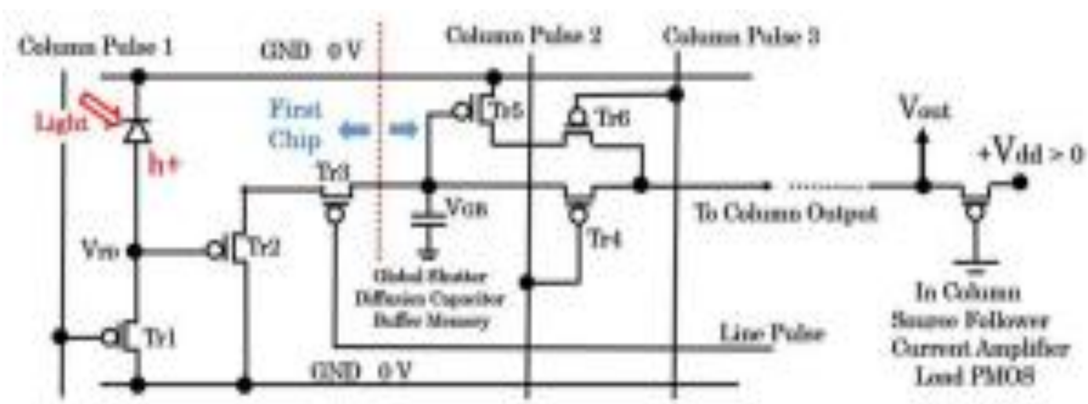

Active Pixel Sensor invented by Peter Noble in 1968 used widely in Modern CMOS Image sensors

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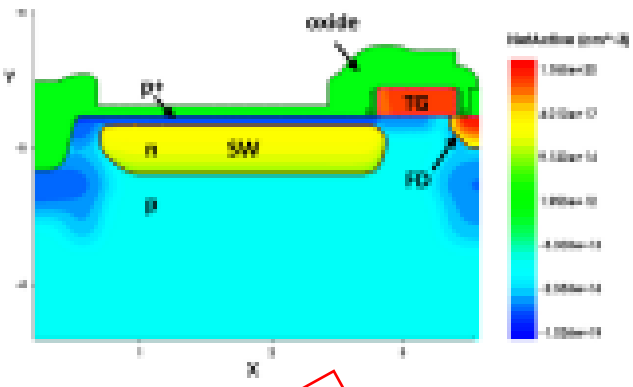

Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentration (horizontal units are microns).

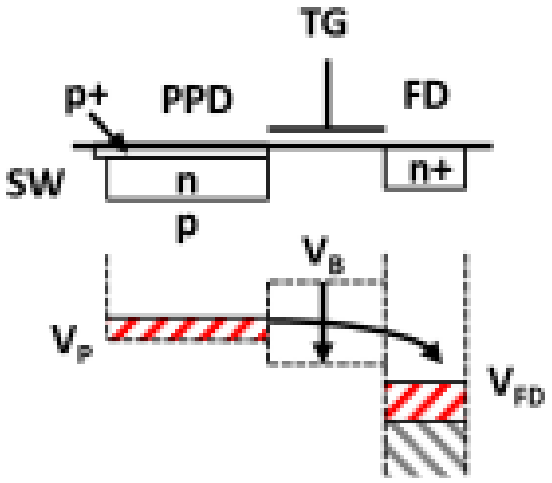

Fig. 5. Ideal potential well diagram for FSI PPD. Turning on transfer gate TG.

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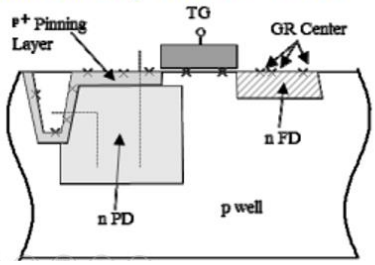
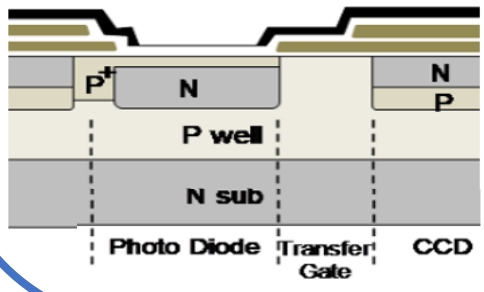
Sony does not use the LOCOS Isolation which has the serious thermal oxidation stress and degrades the image sensor chip-yield and causing surface dark and crystal defects. Sony use the defect-free high energy ion implantation and the Lamp Anneal Process invented and developed by Kazuo Nishiyama at Sony in 1978.

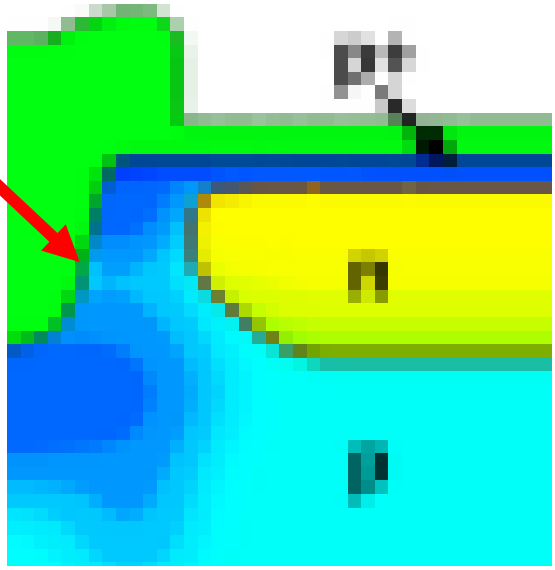
P+ surface may become Floating High Resistivity

Pinned Photodiode with LOCOS Isolation described by Teranishi in 2014

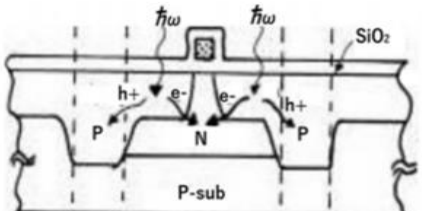


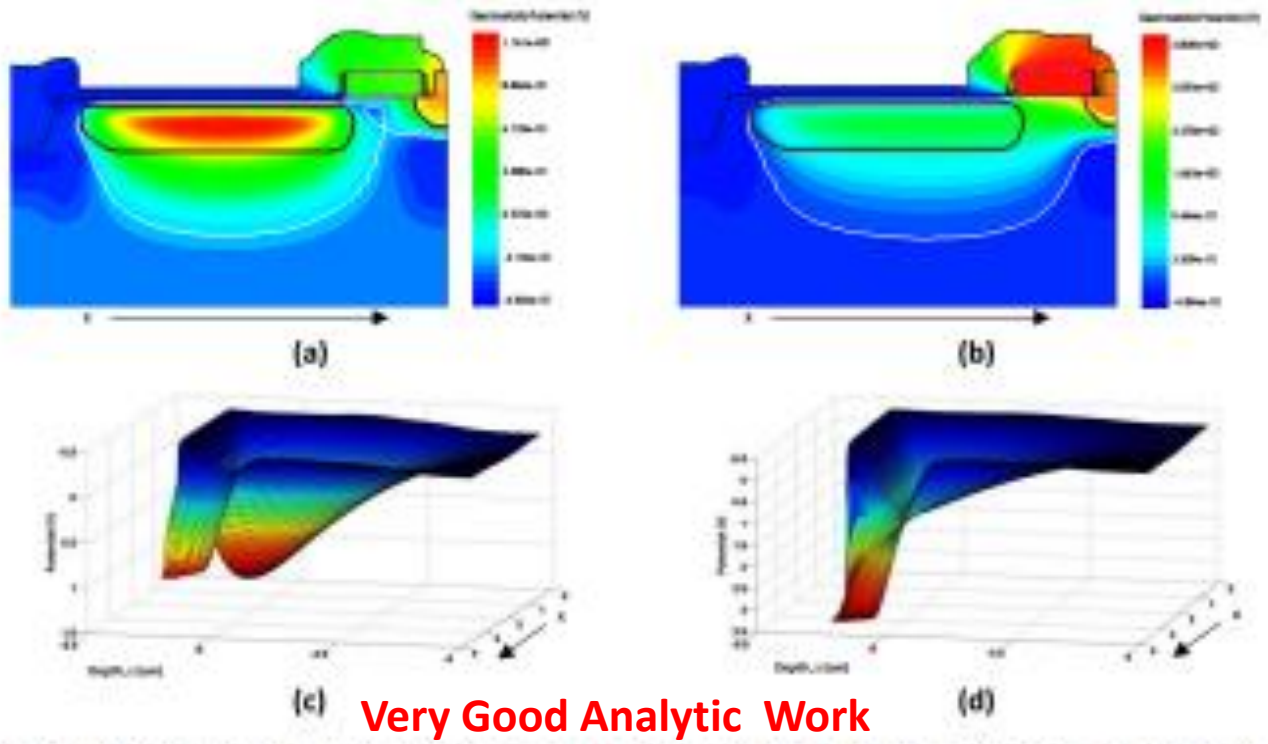
Pinned Photodiode defined by Semiconductor History Museum





Pinned Photodiode reported at SSDM1978 by Sony(Hagiwara)





Very Good Analytic Work

Fig. 6. Potentials inside the PPD. (a) Empty SW with TG "off" and some signal on FD. (b) Empty SW with TG "on" showing monotonically increasing potential from SW to FD. FD has been reset. (c) 3D visualization of potential corresponding to (a), with depth, y, into semiconductor from left to right, surface at left, and x position as labeled with TG barrier front and left. (d) 3D visualization of potential corresponding to (b). Note change in potential scale between figures. Scale for x-axis in microns. Depth scale origin set by TCAD prior to epitaxial layer growth step.

extend the depletion region as deeply as possible to improve collection efficiency and reduce crosstalk. Tailoring of doping profiles has been suggested for individual red, green and blue pixels [57]. Retrograde doping in the p-region can aid carrier collection due to a built-in electric field in the undepleted region below the storage well [58]–[60]. Longer wavelength (e.g. near-infrared or NIR) photons may be absorbed deeply in the $p+$ substrate and the signal carriers recombine before diffusing to the SW region, or in the case of VOD, blocked by a potential barrier. Shallow trench isolation (STI) is most commonly used for pixel isolation although deep trench isolation is being explored for improved cross talk reduction [61], [62]. A more heavily doped p-type region under FD and in other places helps repel photoelectrons so they may be collected by the storage well.

B. Basic Operation

Signal carriers are collected and integrated in the SW prior to readout. The SW is isolated from FD by a low voltage on TG. To achieve correlated double sampling of the signal carriers, FD is reset by the reset transistor (RST) as the first step in the readout cycle and then left floating. The floating potential of FD is sampled by the readout signal chain using source-follower SF. TG is then pulsed high to transfer signal carriers from SW to under TG and on to FD. The TG pulse voltage, the doping profile under TG, and the FD potential must cause a monotonic increase in potential from the SW to FD to allow complete transfer of all signal carriers from SW to FD. Any carriers under TG at the end of the transfer should be subsequently transferred to FD at the end of the pulse period and not back to SW. An example of a monotonically increasing potential is shown in Fig. 6.

The change in potential ΔVon FD is determined by the capacitance C of the FD node and the photogenerated charge Q_{pe} transferred from SW to FD. The ratio of $q\Delta V/Q_{pe}$ is the conversion gain with value of the order of 50 uV/e-. If not limited by the readout signal chain, the full well of the pinned photodiode N_{FW}, measured in signal carriers, is determined by the lesser of the capacity of SW or the capacity of FD for complete charge transfer. Generally, increasing the dopants in the SW increases its capacity but also increases the maximum potential of the empty SW and makes complete charge transfer more difficult to achieve for the same transfer gate voltage. Increasing the FD capacity for a given reset potential reduces the conversion gain of the pixel (volts/electron) and increases input-referred read noise.

The primary challenge in fabricating the PPD is achieving both good full-well capacity and complete charge transfer. The challenge increases with reduced operating voltages and smaller pixel size. Secondary challenges include reducing leakage and dark current from the transfer gate, and decreasing charge transfer times.

C. Full Well

The nominal full-well capacity of the SW is evident from Fig. 5 simply as

$$N_{FW} = \frac{1}{q} C_{FD} \left(V_r - V_R \right) \tag{3}$$

where C_{PPD} is the average capacitance of the PPD. The capacitance C_{PPD} is typically dominated by the $p+n$ junction capacitance and can be readily estimated, but the pinning potential V_p is more challenging to estimate accurately. The pinning potential has been determined analytically by Krymski [63], and more recently by Pelamatti et al. [64]. For more accurate results, TCAD simulation in 2D, or for smaller pixels (e.g. 2.2 um pitch or less), simulation in 3D is required since 2D and 3D effects become important.

The estimate of N_{FW} from (3) is likely high since it is not practically possible to fill a potential well to the brim. This is because of thermionic emission and diffusion of carriers over the barrier in any realistic structure and the need for a practical storage time. It is estimated that an extra barrier height of about 0.5 volts ($20kT$) is required to keep electrons in the well [65], [66] although thermionic emission occurs at all barrier heights and there is no absolute cut off for the process. Under illumination, it is possible that optical carrier generation balances emission across the barrier and a solar-cell-like logarithmic dependence of full well as a function of illumination level might be realized [64].

Good image quality typically requires at least 3,000 electrons full-well capacity since 3,000 electrons with 3 e- rms read noise yields a maximum dynamic range $DR = 20\log(\frac{3000}{3})$ of 60 dB [67]. A SNR of 30[illegible] by reduci[illegible] address[illegible] by op[illegible] pitch, full w[illegible] maxim[illegible]

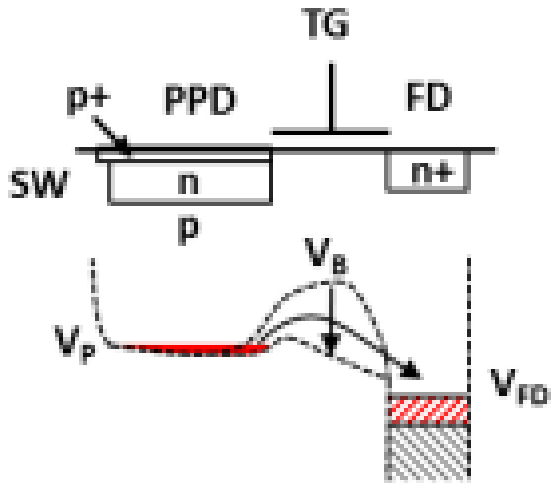
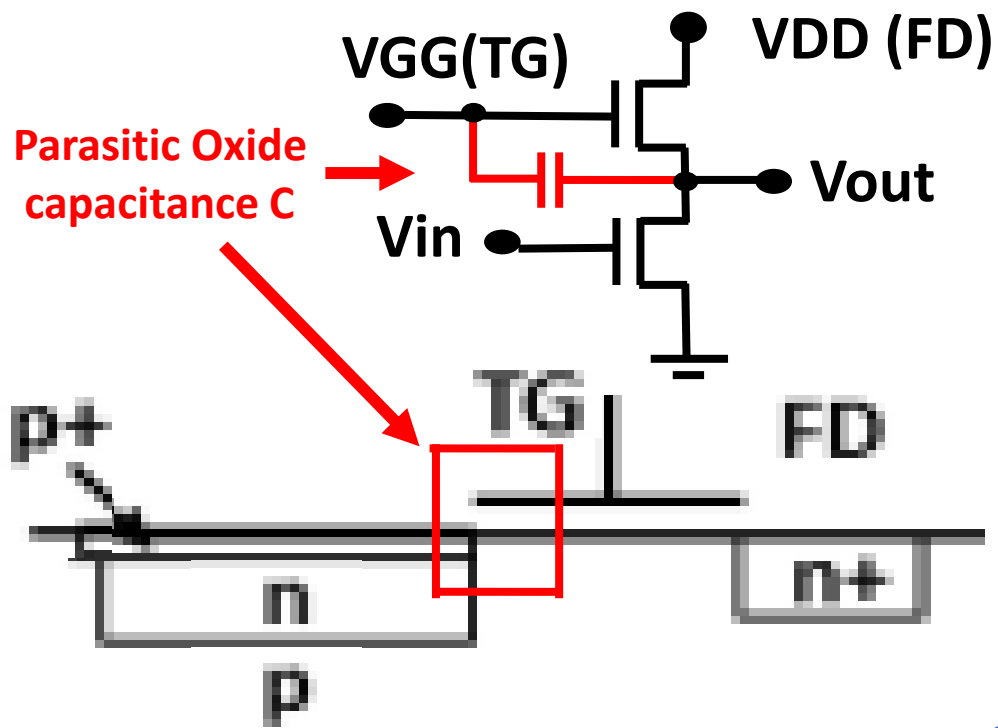


Fig. 7. Example of a barrier that can lead to incomplete charge transfer, lag and noise.

arise from carrier tr[illegible]g by defects either in the SW, or under TG. The use [illegible] VOD structure can reduce lag and carrier crosstalk d[illegible] deeply generated carriers by blocking them from the [illegible]2]. However, this is often more easily accomplished by [illegible] 3-7 microns of p-epitaxial layer on $p+$ substrate where these deep generated photocarriers can

This paper has no consideration on the parasitic capacitance effect between the gate oxide and the Charge Transfer (CT) Gate, which is widely known as the Bootstrap Effect by Classical MOS IC circuit designers.



D. No[illegible]

No[illegible] electr[illegible] the Pl[illegible] on Fl[illegible] comm[illegible] reduc[illegible] handli[illegible]

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Lag ca[illegible] are not colle[illegible] becomes more acute at longer wavelengths and when emission is the carrier collection mechanism for SW. Lag can also

[illegible]similar to [illegible]time and [illegible]-induced [illegible]or small [illegible]sfer. For [illegible]scales as [illegible]th by an [illegible]d lateral [illegible]th "flat" [illegible]nited for [illegible]s $1^2/D_n$ [illegible]n start to [illegible]5.6 um, [illegible]grows to [illegible]r may be [illegible]transfer, [illegible]plants or [illegible]r time is [illegible]he width [illegible]such that [illegible]channel [illegible]This can [illegible]er of the

[illegible]ll well capacity of the SW is exceeded. In essence, the PPD becomes a photovoltaic device and excess carriers diffuse away from the

SW. However, the diffusion process is greatly affected by the potential profile in the vicinity of the PPD and carriers typically preferentially diffuse under TG to FD. From FD, further diffusion can occur under the reset gate to the reset drain. In essence, the reset transistor becomes a built-in lateral overflow drain. Thus, blooming in the PPD in a CMOS image sensor is not as consequential as it is in a CCD ILT pixel where the excess carriers bloom into the readout CCD and contaminate many other pixels in the image (although adjacent pixels may be impacted in CIS [80].) Hence, the advantage of a VOD structure is relatively moot in a CMOS implementation of the PPD except for rejecting deeply generated carriers. VOD implementation is also not readily possible with BSI.

Dark current in image sensors can vary significantly from pixel to pixel depending on local defects and statistical process variations, leading to some pixels with very high dark current. These outlier pixels result in "white spot" blemishes in the image. Compared to other photogate structures (e.g. MOS), the PPD has very low average dark current with state-of-the-art values below 15 e-/s at 60C for a 1.4 um pixel and concomitant fewer white spots [81]. The shallow $p+$ pinning layer maintains the Si-SiO_2 surface in thermal equilibrium and the high surface hole concentration ensures that Si-SiO_2 interface states are starved by an absence of electrons. Furthermore, the absence of a metal contact (and alloyed spikes) on the $p+$ layer also contributes to the low dark current. Similarly, with almost the remainder of the SW surrounded by high quality neutral silicon with long minority carrier lifetime, dark current collection by diffusion is also very low. Higher doping concentrations, especially in the SW to increase N_{PW}, can increase electric field strengths resulting in higher average dark current and more white spots. However, reduction of dark current is a never-ending quest and recurring issue as new processes are introduced as part of pixel shrink.

The weak link in dark current is the adjacent TG. Depending on the 3D doping profile and biasing of the TG, dark current can be generated by Si-SiO_2 interface states, or by defects below the surface, and collected in the SW. It is not surprising that the detailed fabrication process around the edge of the TG is highly engineered in a PPD. Not only must the profile result in no significant barrier for complete charge transfer, but defects must also be minimized. A small built-in field under TG that drives dark current to FD instead of SW is sometimes introduced [82]. Negative bias on TG during signal integration can help draw holes to under the PPD edge of TG and suppress dark current generation from Si-SiO_2 interface states [83]–[85]. Negative bias on TG can also help increase the full-well capacity by increasing the barrier between SW and FD and/or reduce leakage current from SW to FD. Increased gate length of TG beyond minimum length improves fabrication ease and improves barrier control.

IV. Fabrication

The fabrication processes that have been used for making PPD devices have been rarely published except in the patent publication literature until recently [86]. For the PPD, the

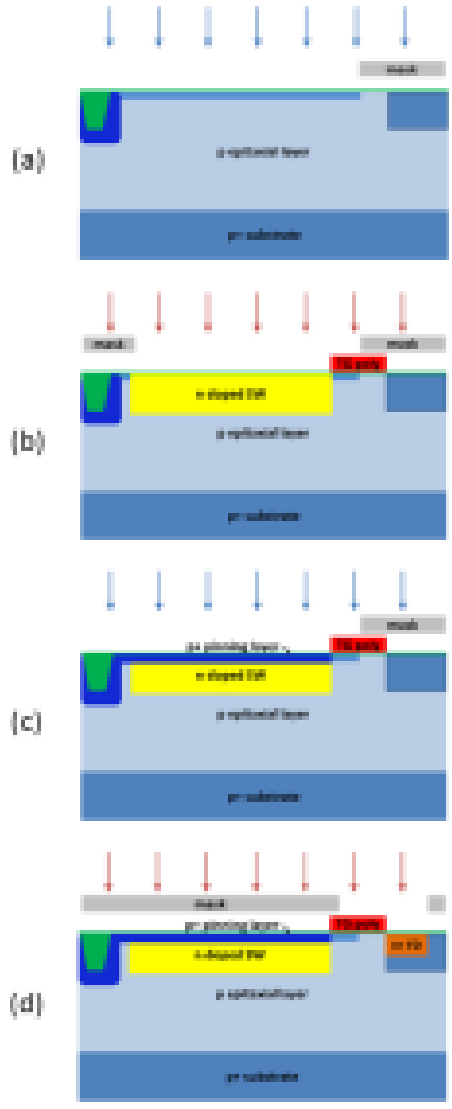

Fig. 8. Examples of essential PPD fabrication implants: (a) TG threshold adjust: B 1.5×10^{12}/cm^2 at 10keV. (b) SW formation: p 2.5×10^{12}/cm^2 at 65keV. (c) pinning layer formation: BF_2 1×10^{13}/cm^2 at 10keV. (d) FD formation: As 1.8×10^{13}/cm^2 at 35 keV plus P 7×10^{11}/cm^2 at 20keV.

Very Good Explanation but this LOCOS Device Isolation Process is not used.

alignments between the pinning layer edge, storage well edge, and the transfer gate TG, are critical, and depend on doping and operational conditions. In the past, spacer and dummy layers and angled implants were often used to achieve the desired alignments to reduce barriers and dark current [87]. In more recent devices, angled implants are not typically used because of shrinking dimensions, better lithography, and better modeling. Eliminating angled implants (aside from normal tilt) simplifies shared-readout layout.

For educational purposes, in Fig. 8 we present a hypothetical fabrication process flow (focused on the PPD) for which TCAD shows the desired functionality. These fabrication conditions result in the structure and potentials shown in Figs. 4-6.

An example of a fabricated 1.4 um pitch, 1.35T (8-way shared readout) commercial BSI CMOS image sensor is shown below in Figs. 9–11 [88].

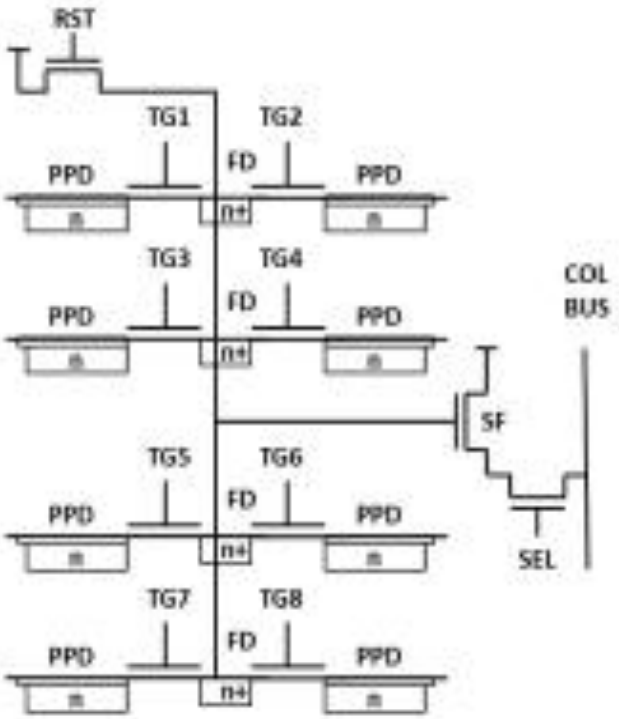

Fig. 9. 8-way shared readout 1.35T pixel schematic.

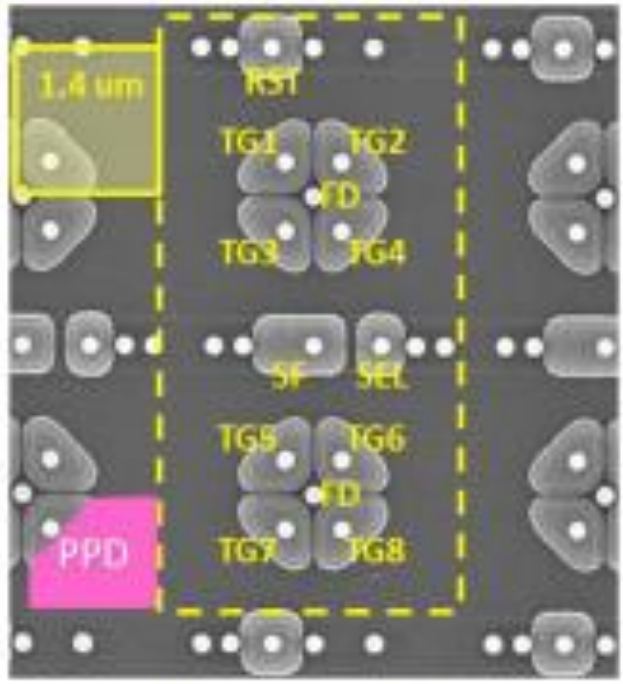

Fig. 10. Annotated micrograph of partially etched frontside surface of 1.375T BSI CMOS image sensor showing clover leaf clusters of shared readout transfer gates. The dashed line encloses 8 pixels with one shared readout. One PPD region is shown in pink (from SEM data). Photo courtesy of R. Fontaine/Chipworks.

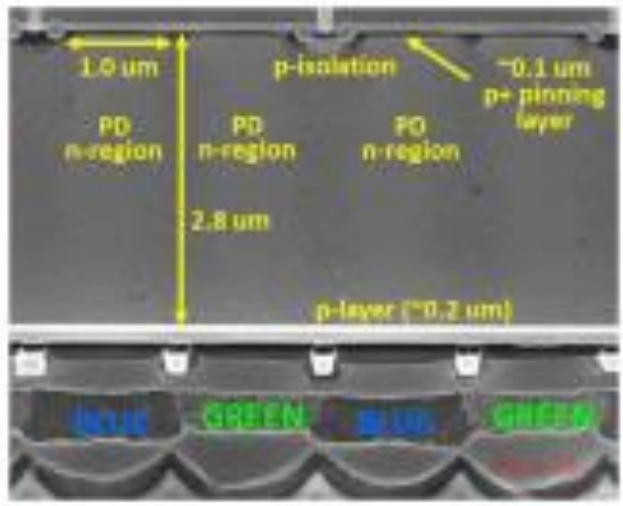

Fig. 11. Annotated micrograph of cross-section of BSI CMOS image sensor. For BSI, light enters at the bottom, travelling through microlenses and color filters before entering the backside of the silicon chip. Photo courtesy of R. Fontaine/Chipworks.

V. Pixel Shrink

Scaling of pixels is an important aspect of image sensor technology roadmaps [89], [90]. Generally, pixel pitch follows Moore's Law; the number of transistors per unit area doubles every two years – which for pixels suggests the pitch should halve every four years [91]. If the minimum feature size (or technology node) is L, pixels typically scale between $10L$ to $20L$ [89], [91], [92] depending on shared readout and other design factors. This is illustrated in Fig. 12. The number of pixels in 0.18 um technology reflects the accessibility of this node by users in a number of communities.

Recently, there has been a slowing of pixel size shrink rate to below that anticipated by the simple Moore's Law. This is due to both technological and physical challenges of making sub-diffraction limit (SDL) pixels as well as relaxation of the market-driven race for more megapixels per sensor. The same data of Fig. 12 is replotted in Fig. 13 as a function of reported year. A line showing the Moore's Law slope is shown for reference.

Reduction of operating voltages continues to challenge the complete transfer of charge from the PPD SW. To partially compensate, the pinning voltage of the PPD has been reduced. Combined with the reduced area of shrunken pixels, the full-well capacity of the PPD has emerged as a major issue in scaling. Better use of the vertical dimension and corrugated topology to increase charge handling capacity is expected in the future. [93]–[96]. Compensating small full well through faster readout times and digital integration has been proposed as an alternative approach. [97]–[99].

One fundamental property that is not scalable is photon absorption length. As pixels shrink, the aspect ratio of pixel pitch to absorption length has inverted from greater than unity to substantially less than one. This exacerbates issues with optical crosstalk between adjacent pixels.

VI. Use in Other Applications

The CMOS active pixel sensor combined with the pinned photodiode has found use in applications adjacent to consumer cameras as discussed below.

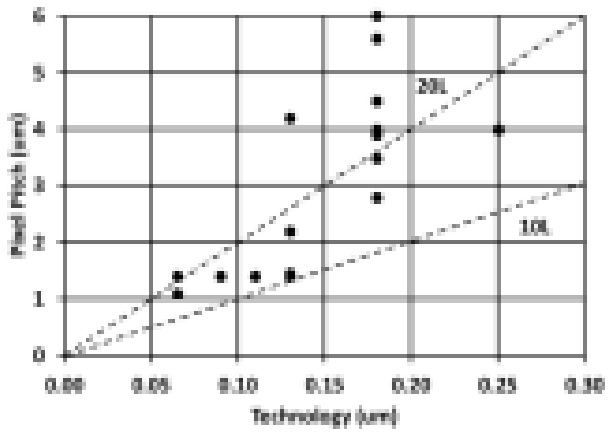

Fig. 12. Sampling of reported pixel pitch as a function of technology node. Both 2X and 1X scaling shown by dashed lines.

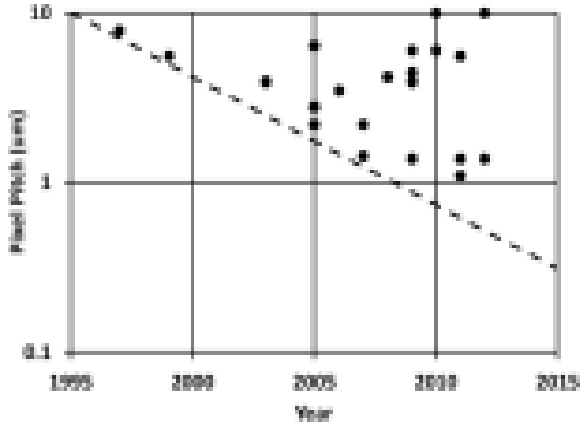

Fig. 13. Sampling of reported pixel pitch as a function of year. The Moore's Law slope is shown for reference.

A. Global Shutter

Global shutter is important for some imaging applications that cannot tolerate artifacts generated by a rolling shutter such as high speed motion capture cameras. Adding a global shutter function to the pixel invariably increases minimum pixel size. It can be implemented by adding another charge transfer stage to each pixel so that charge is transferred from the pinned photodiode SW to a second storage area. For readout, charge is transferred from storage area to the FD. Proposed in the mid-nineties [100], it was first reported using pinned-photodiode technology in 2000 [101]. A novel pump-gate global shutter using two pinned diode structures was presented by Aptina in 2013 [102]. The CMOS image sensor global shutter can also be implemented in-pixel with sample-hold circuits which may be more compatible with BSI technology due to possible optical contamination of the stored signal, though CDS may be more challenging.

B. Time-of-Flight Ranging Application

Time-of-flight (ToF) sensors used for measuring the distance to objects in the scene have also used the pinned photodiode. In this application, typically two or more output ports, or transfer gates from the pinned region are used and modulated at high frequency. [103], [104]. Due to the short transit times required, e.g. under 10 nsec, either small pixel sizes or channels with lateral drift field are required [105]. Mixed mode color and ToF sensors, so-called RGBZ sensors, have also employed pinned photodiode devices [106], [107].

C. Radiation Effects

The use of CMOS image sensors in space and high energy physics experiments has led to a number of recent studies on the radiation hardness of PPDs in CMOS image sensors [108]–[110]. Generally, compared to CCDs, CMOS image sensors are quite radiation hard. However, an increase in room temperature dark current with total dose, typically associated with the transfer gate, remains an issue.

VII. Conclusion

The pinned photodiode has been in use for nearly 30 years and has been utilized in both first generation and second generation solid-state image sensors. It will not be surprising if the PPD is adopted for use in some third generation solid-state image sensor in the future. It is likely that the essential concepts of the PPD will be retained, such as storage well isolation from surface effects and complete charge transfer, whereas the detailed structure may change. If new materials replace silicon as the primary photodetector, they will have a difficult time achieving the high performance of the silicon pinned photodiode.

Acknowledgments

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The PNP device defined as Pinned Photodiode by Fossum has the surface P+ region is floating with RC delay, actually causing the serious image lag. This is a misleading and a fake paper.

Fossum did not explain the important detailed efforts and achievements of Peter Noble reported in the paper,

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[24] Y. Hagiwara, Japanese Patent App 50-134985, 1975.

[25] Y. Hagiwara, "High-density and high-quality frame transfer CCD imager with very low smear, low dark current and very high blue sensitivity," *IEEE Trans. Electron Devices*, vol. 43, no. 12, pp. 2122–2130, Dec. 1996.

[26] Y. Hagiwara, "Microelectronics for home entertainment," in *Proc. ESSCIRC*, Sep. 2001, pp. 153–161.

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Evidence that Yoshiaki Hagiwara at Sony in 1975 invented Pinned Buried Photodiode with the complete charge transfer capability of the no-image-lag feature and the Anti-blooming Vertical Overflow Drain (VOD) in order to realize the completely-mechanical-parts-free electrical Shutter. Hagiwara invented Electrical Shutter.

Japanese Patent Application JPA1975-127646

Japanese Patent Application JPA1975-127647

Japanese Patent Application JPA1975-134985

Japanese Patent Application JPA1977-126885

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Hagiwara_SSDM1978_Paper_on_Pinned_Buried_Photodiode.pdf

an invited Talk at CCD'79 Conference

"ADVANCES in CCD Imager " Technical Digest of IEEE International Conference

IEEE1996_Review_Paper_on_Sony_1980_One_Chip_FT_CCD_Image_Sensor with_Pinned_Buried_Photodiode

an invited ESSCIRC2001 Plenary Talk,

"Micro-Electronics for Home Entertainment"

IEEE IEDM2004 Conference Short Course

Turorial Short Cource on Image Sesnors by Yoshiaki Hagiwara.pdf

an invited ESSCIRC2008 Plenary Talk,

"SOI Design in Cell Processor and Beyond"

Invited Plenary Panel Talk at ISSCCC2013 on Feb. 2013 on Image Sensors

"Multichip CMOS Image Sensor Structure for Flash Image Acquisition"

"Simulation and Device Characterization of the P+PN+P Junction Type Pinned Photodiode and Schottky Barrier Photodiode"

"Electrostatic and Dynamic Analysis of P+PNP Double Junction Type

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