IEEE Symposium on Low-Power and High-Speed Chips

COOL Chips 20

YokohamaJoho Bunka Center, Yokohama, Japan
(Yokohama Media & Communications Center)

April 19-21, 2017

Panel Discussion

Topics: "Cool chips for the next decade"

Yoshiaki Hagiwara

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Consumer Electronics from HOT Chips to COOL Chips.

“Cool chips for the next decade”

A cool chip can be created by low power efforts on the device, circuit and system architecture.

“Cool chips for the next decade”

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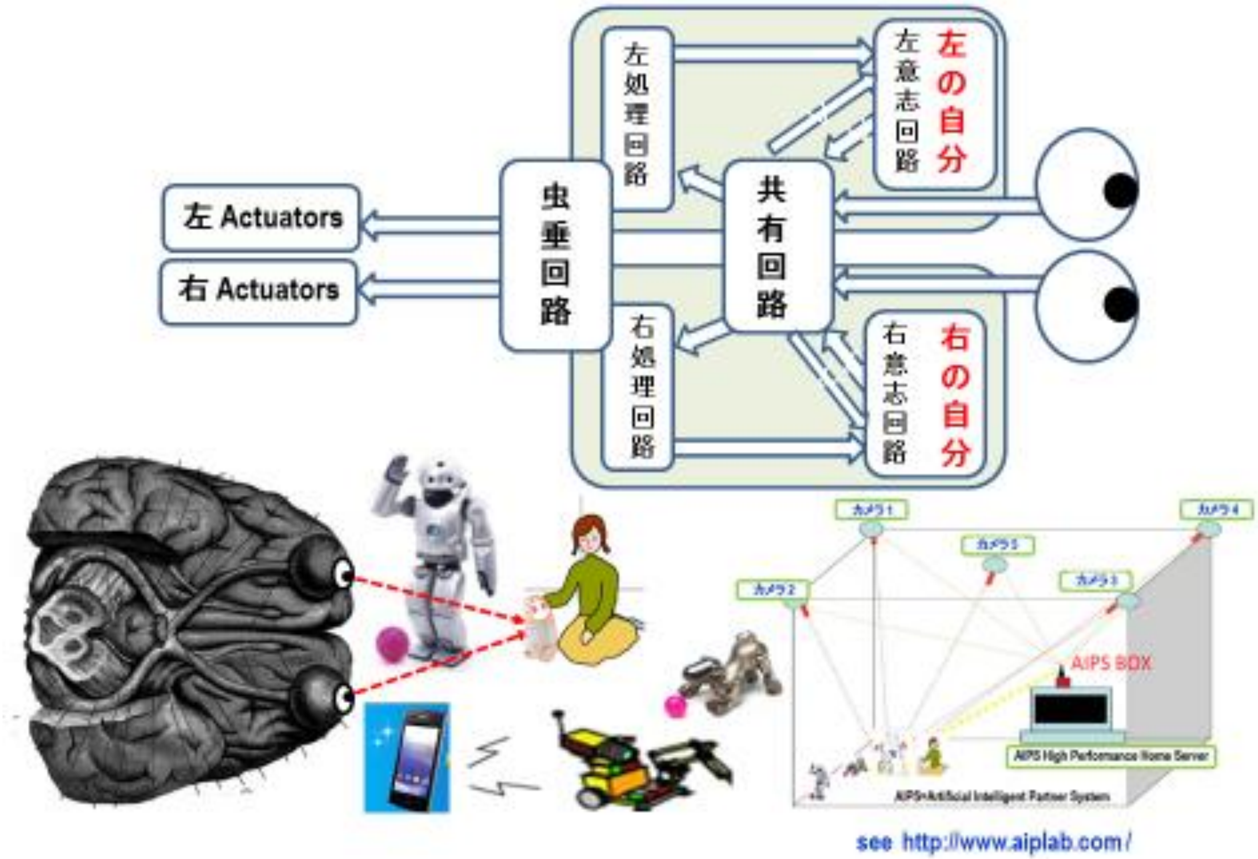

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2017	10 nm
2019	7 nm
2021	5 nm
2023	~4 nm
2025	~3 nm
2027	~2 nm ---- 20 Å = 20 atoms !

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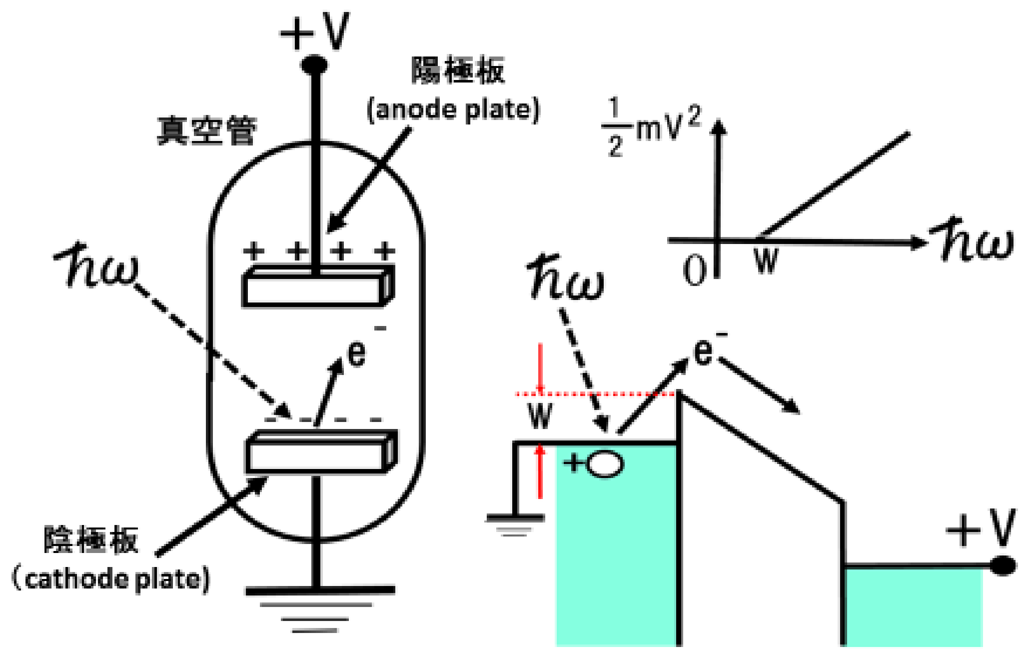

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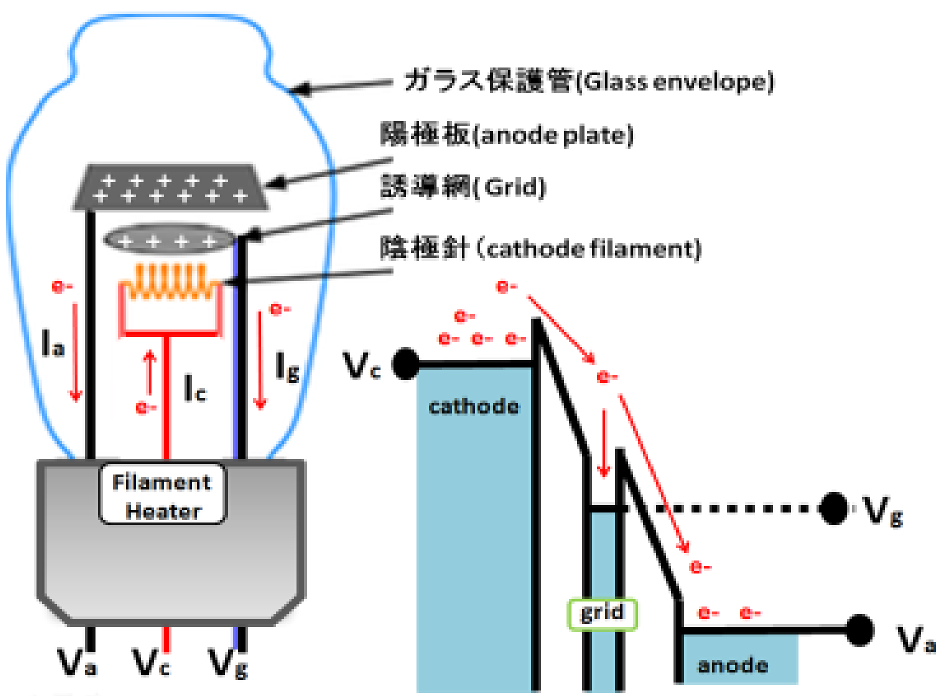

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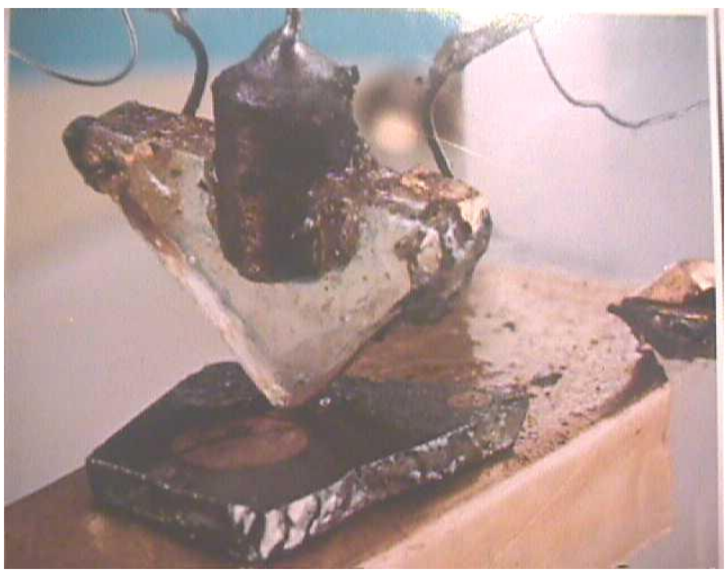

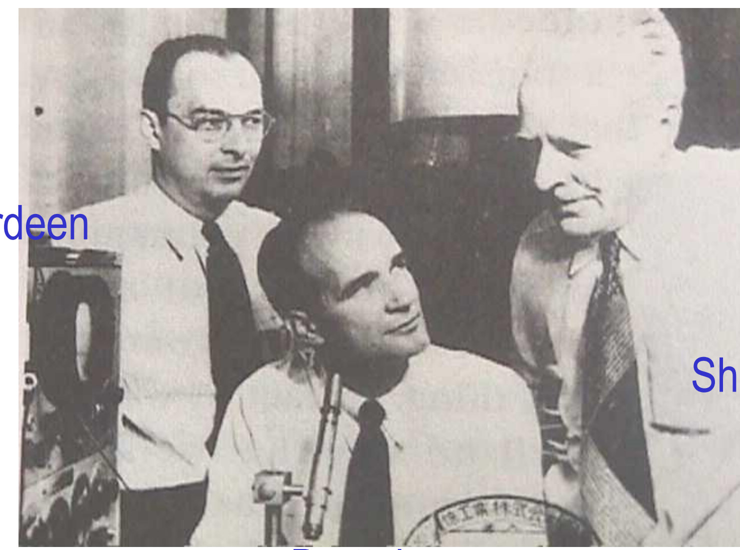

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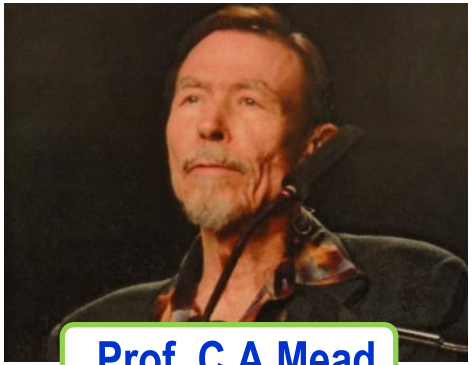
Prof. C.A.Mead

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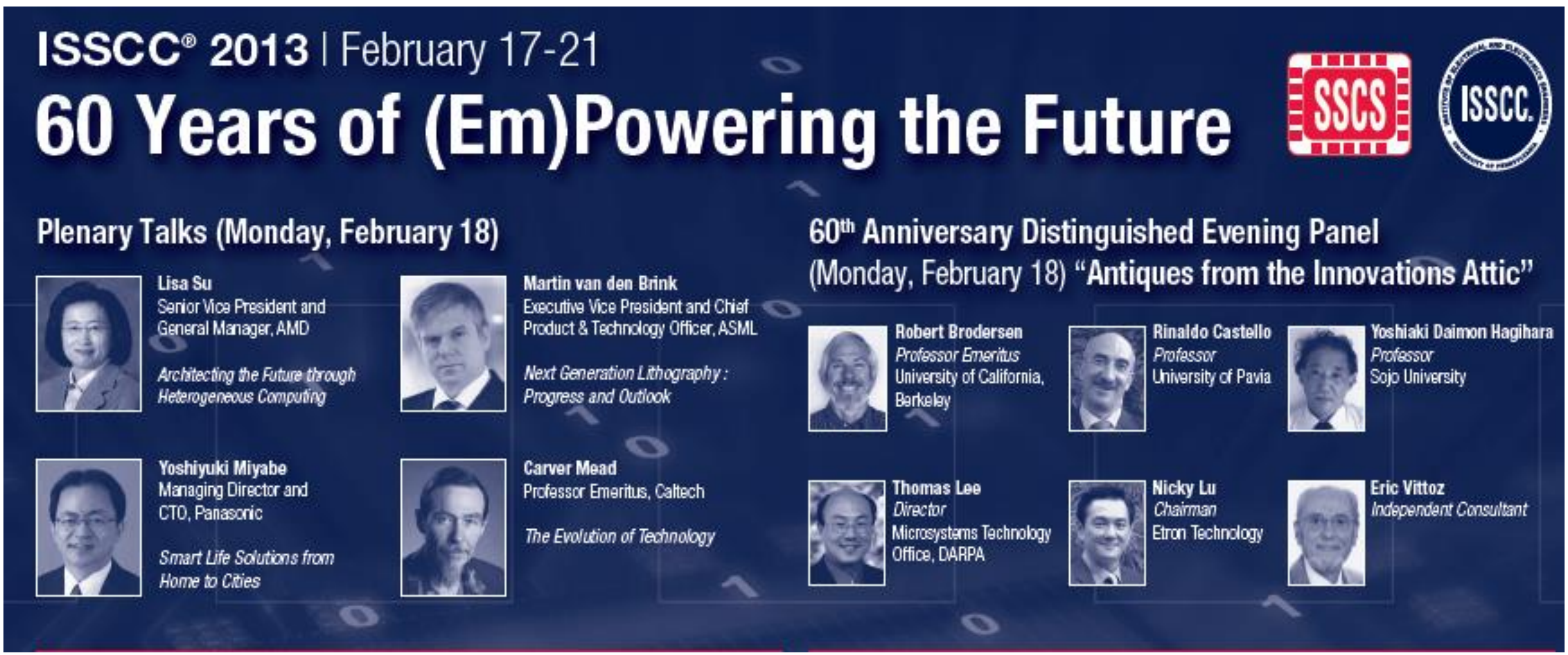

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International Solid State Circuits Conference

1954-2013

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International Solid State Circuits Conference

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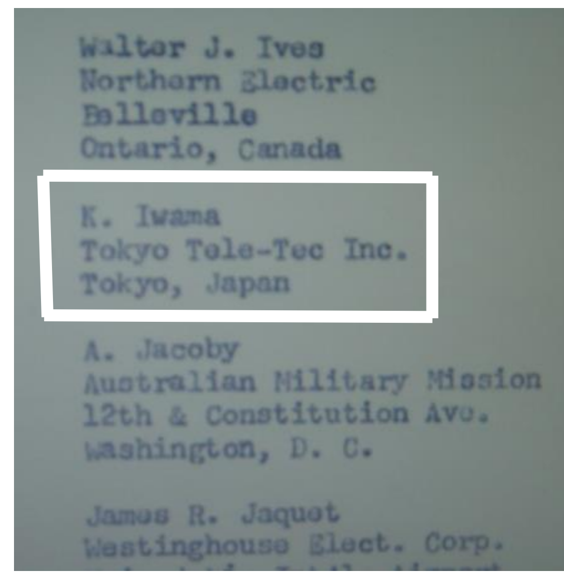

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Belleville
Ontario, Canada

K. Iwama
Tokyo Tele-Tec Inc.
Tokyo, Japan

A. Jacoby
Australian Military Mission
12th & Constitution Ave.
Washington, D. C.

James R. Jaquet
Westinghouse Elect. Corp.

Kazuo Iwama in ICTC (ISSCC) 1954

Attendee List @ University of Pennsylvania, Philadelphia

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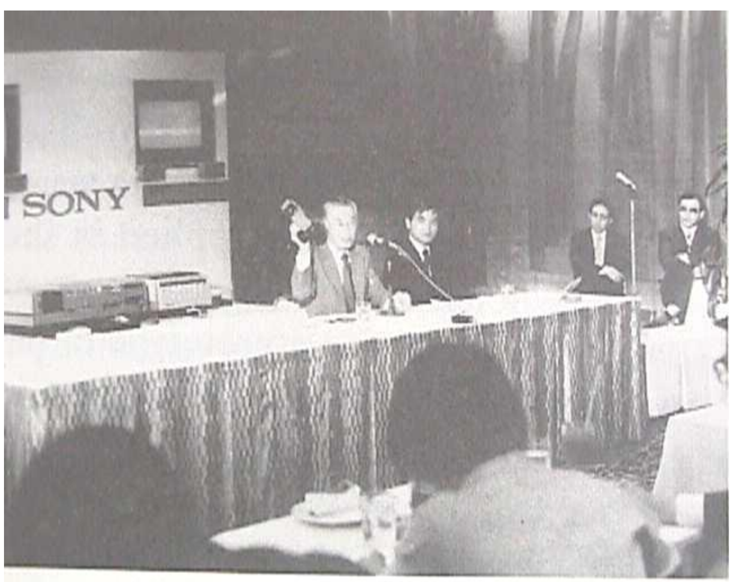
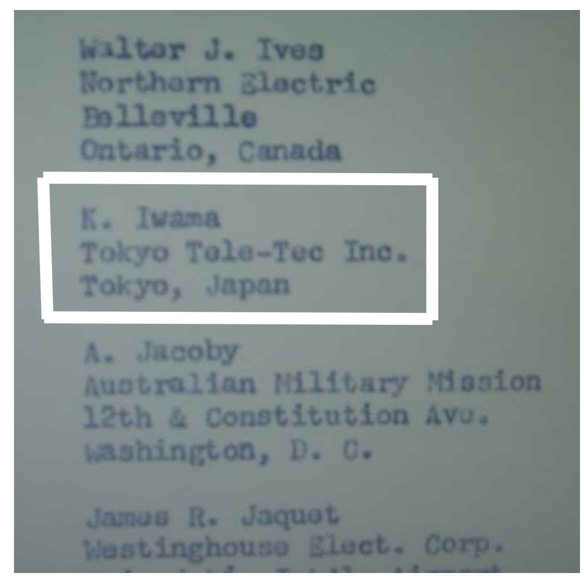
Kazuo Iwama (Sony) @ Tokyo Press Conference 1978

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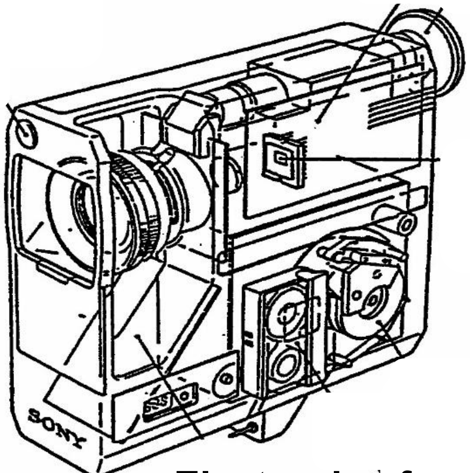
570H x 498V One-Chip FT CCD Color Imager, 1978



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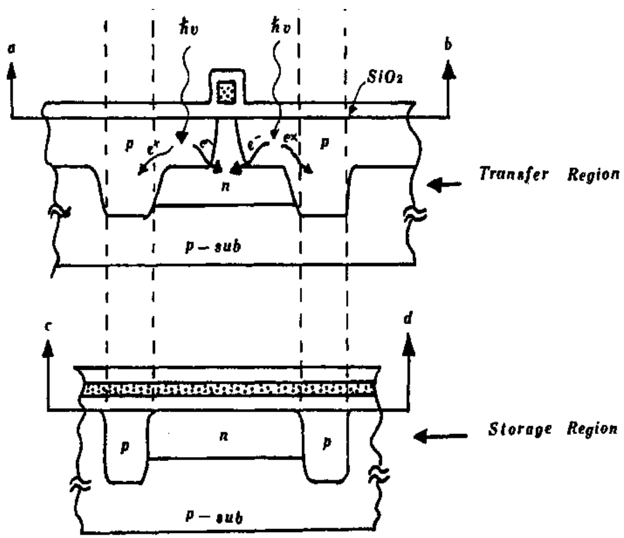

highly light sensitive P+NP (HAD) sensor, 1975

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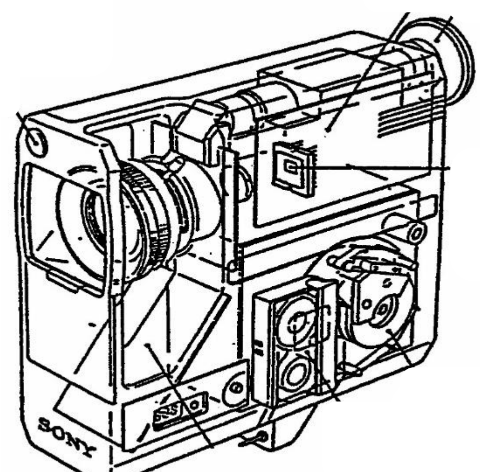

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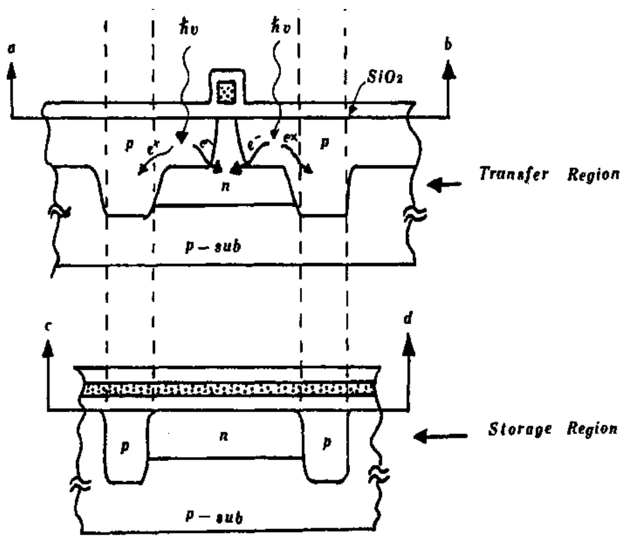

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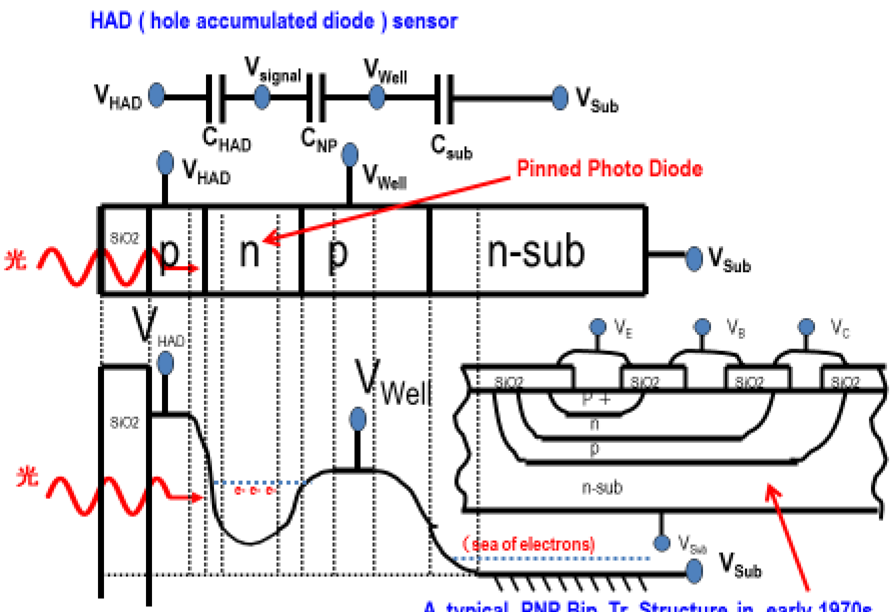

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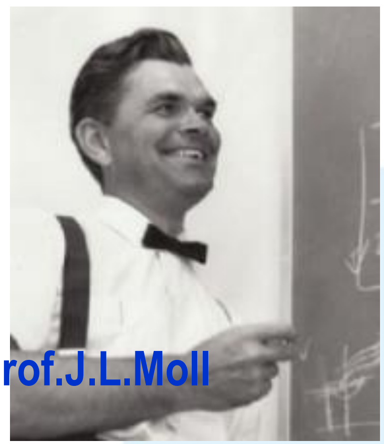


Prof.J.L.Moll

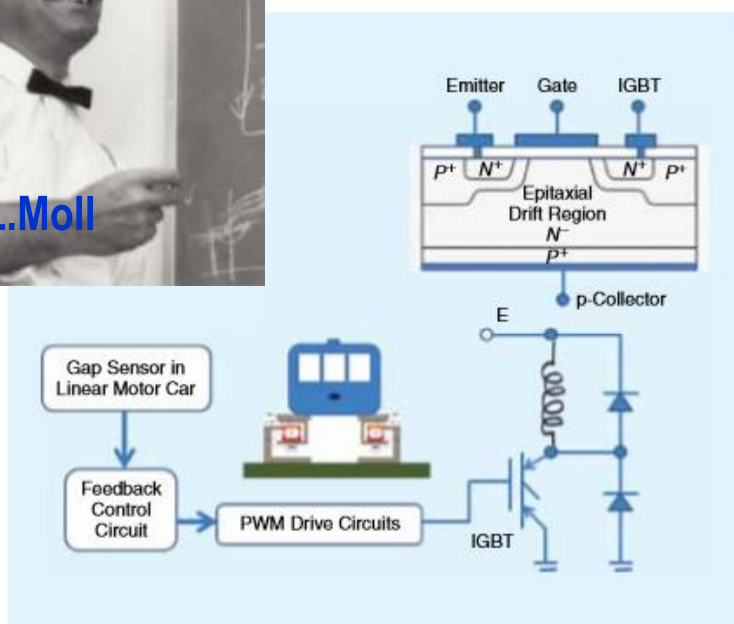
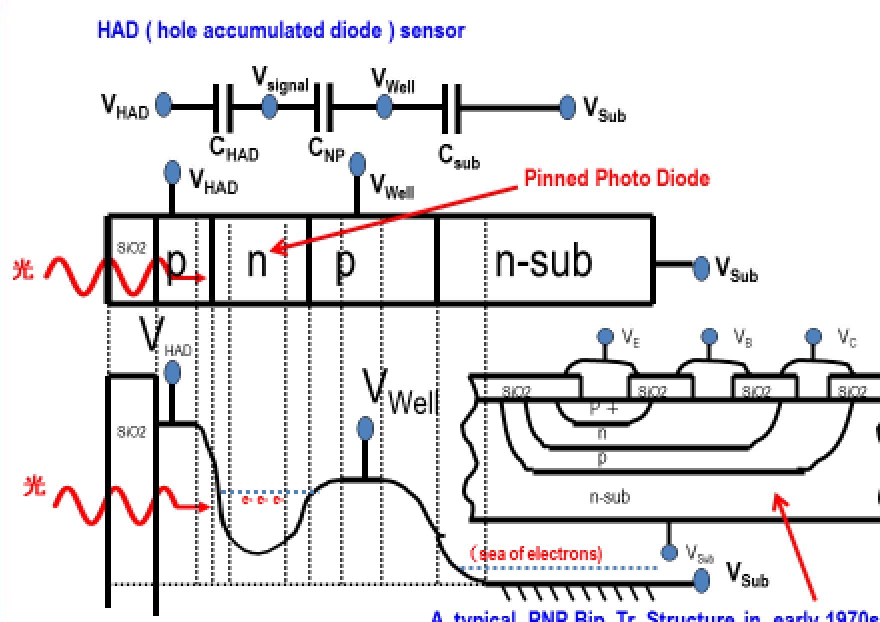


FIGURE 9: The p-n-p-n switch diode for a modern linear motor car.



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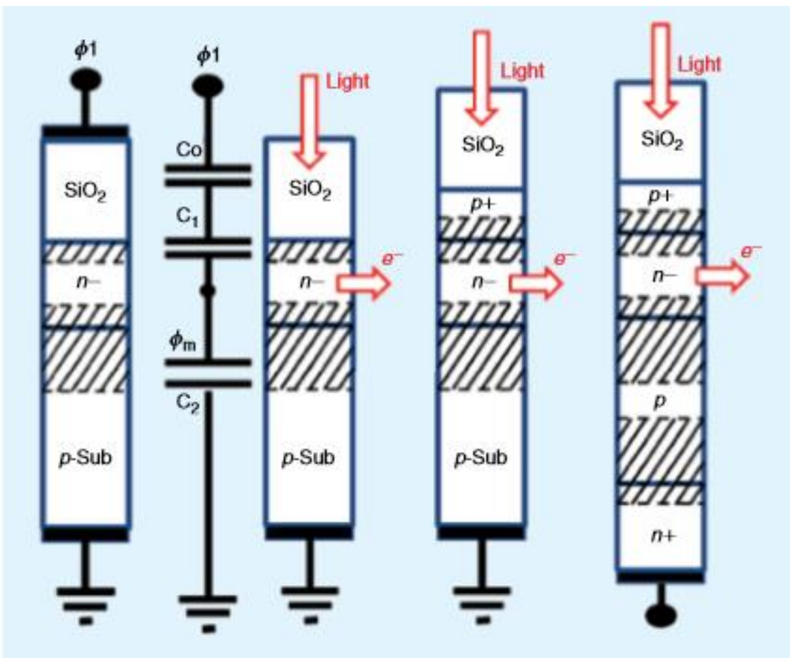
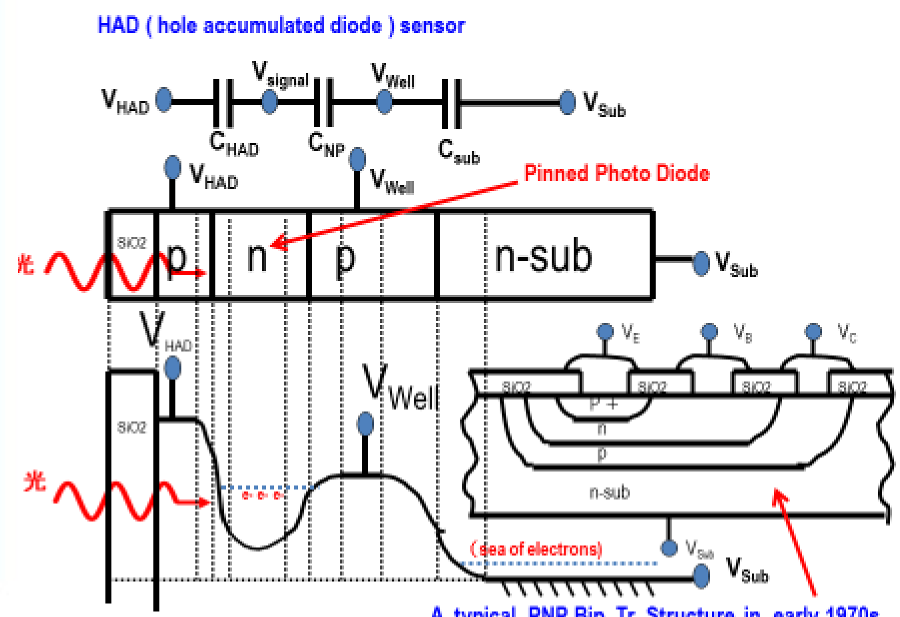


FIGURE 10: From CCD to the dynamic p-n-p-n diode capacitors.



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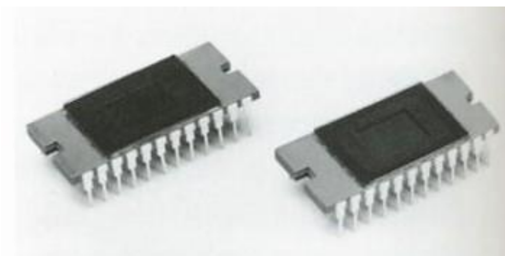
XC-1 1980
Two-Chip Color Video Camera

<ICX008>
2/3 Inch 120K Pixel
IT CCD Imager designed



Technical Report represented at Japan SSD conference Tokyo, May 1978

all solid state = robustness

Yoshiaki Higihara: The p-n-p-n Diode in Future Linear Motor Cars and in Modern Imagers

John Louis Moll (1921–2011) was studying a p-n-p-n diode switch in his Ph.D. dissertation work when the first ISSCC was held in 1954. In a normal operation mode, this device works as a thyristor, which can drive a large current and is the key device structure of an IGBT applied for a linear motor car of the future (see Figure 9). In a dynamic operation mode, this device may work as a simple p-n-p-n dynamic capacitance that can detect and store one single electron, which is a key device structure of the modern image sensor (see Figure 10).

I recall, when I was taking his physics course at Caltech, that Feynman once said that an electron is always free, moving around rapidly in free space, even in solid, and it

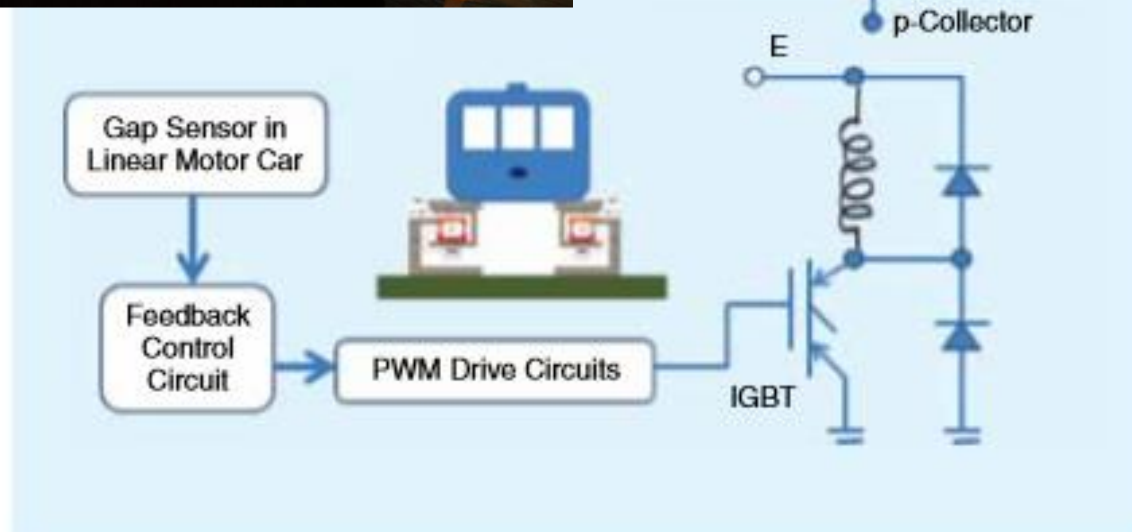


FIGURE 9: T...

Consumer Electronics from HOT Chips to COOL Chips.

Yoshi Hagihara, Eric Vittoz and Bob Brodersen.

Yoshiaki Hagihara shared his memories of Richard Feynman, his mentor and educator at Caltech, and how he learned from him that control of electrons is at the heart of all electronic devices. As an example from his attic, he pointed to the old p-n-p-n junctions that are now incorporated in modern-day image sensors.

never stops. It is very hard to catch an electron because we do not know exactly where it is. Our civilization today is based on a technology that controls electrons, down to a single one.

Imagine a photon incident to a bipolar transistor base region. The photon energy creates an electron-hole pair. And the photo-electron can be stored in the base region as one single majority carrier. That is, a bipolar transistor can also function as a photon detector and/or a storage container. I thought that a room in a hotel must be empty and clean before the first hotel guest arrives. So must be this transistor base region empty and clean with no guest electrons at the beginning. This transistor in a dynamic p-n-p capacitor mode is useful since it can capture, confine, and control one single electron. But as a

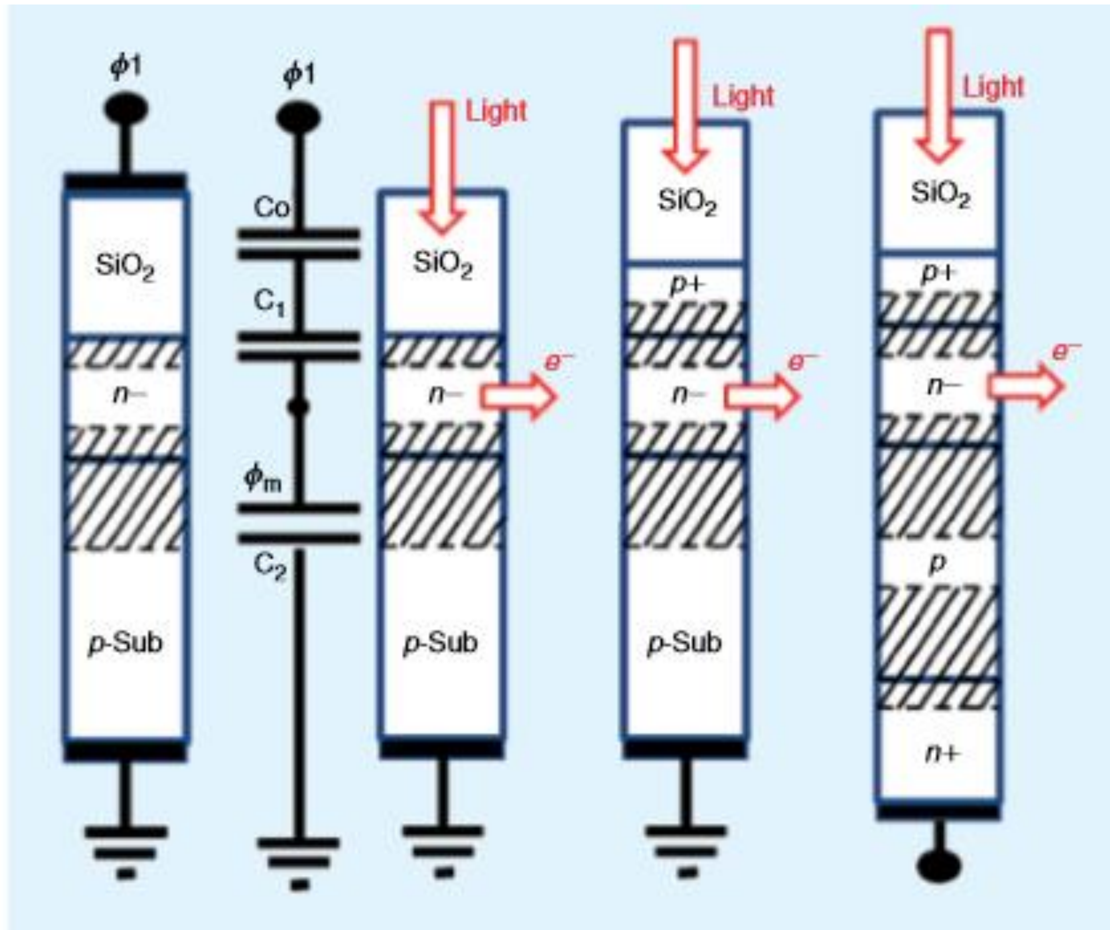


FIGURE 10: From CCD to the dynamic p-n-p-n diode capacitors.

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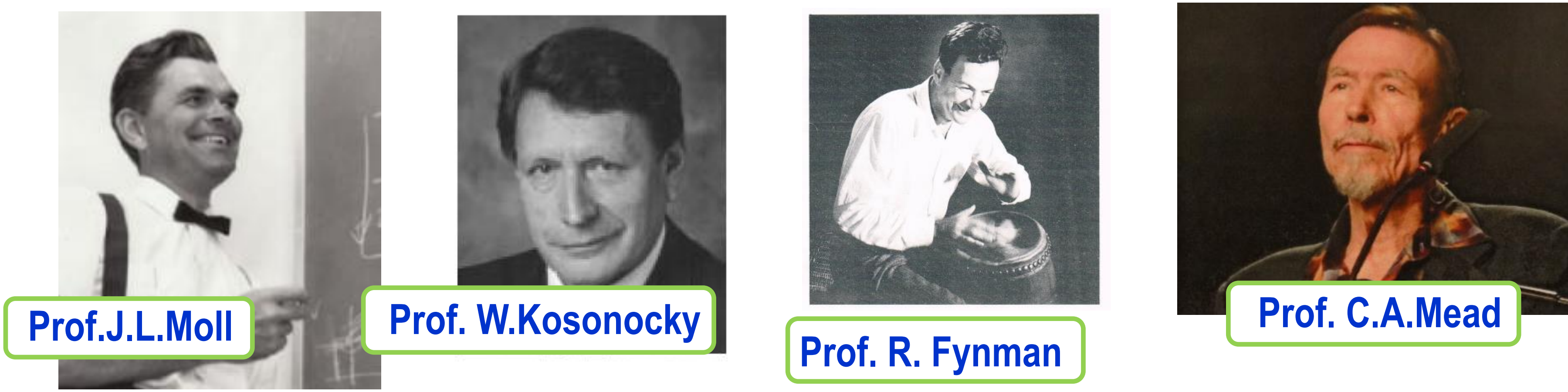
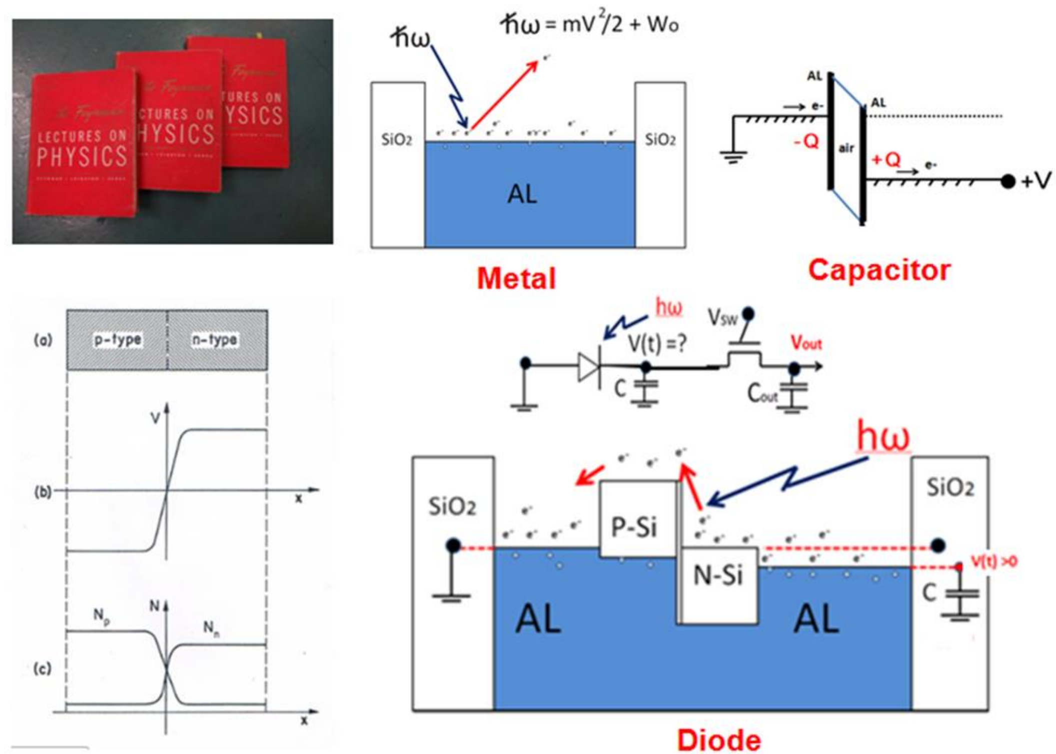


student, I did not know yet how to move that single photoelectron sitting in the base region to the outside world so that we can make use of it as a signal. I had no way yet to know whether the hotel guest has arrived and is resting in the hotel room or not. We had no way yet to ask the hotel guest to come up to the hotel lobby to meet me. I had to wait a few more years (until 1970 in my senior year in college) to find the answer. We all know now it is the CCD structure that can store and transfer one single electron. With a precharge reset set gate and a source-follower circuit, a scheme invented by Walter Kosonocky. We could finally meet our hotel guest at the hotel lobby.

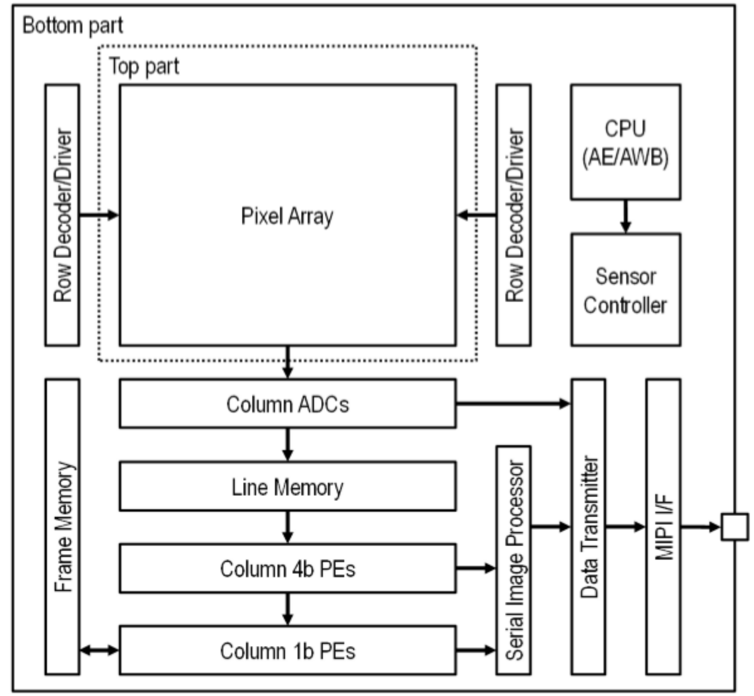


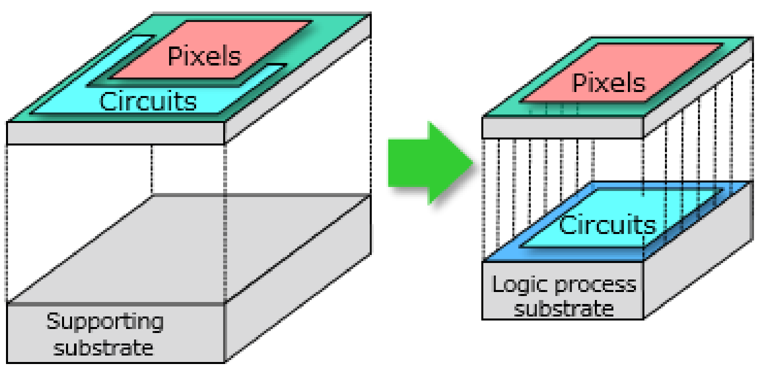
4.9 A 1ms High-Speed Vision Chip with 3D-Stacked 140GOPS Column-Parallel PEs for Spatio-Temporal Image Processing

Tomohiro Yamazaki[1], Hironobu Katayama[1], Shuji Uehara[1], Atsushi Nose[1], Masatsugu Kobayashi[1], Sayaka Shida[1], Masaki Odahara[2], Kenichi Takamiya[2], Yasuaki Hisamatsu[2], Shizunori Matsumoto[2], Leo Miyashita[3], Yoshihiro Watanabe[3], Takashi Izawa[1], Yoshinori Muramatsu[1], Masatoshi Ishikawa[3]

[1]Sony Semiconductor Solutions, Atsugi, Japan
[2]Sony LSI Design, Atsugi, Japan
[3]University of Tokyo, Bunkyo, Japan

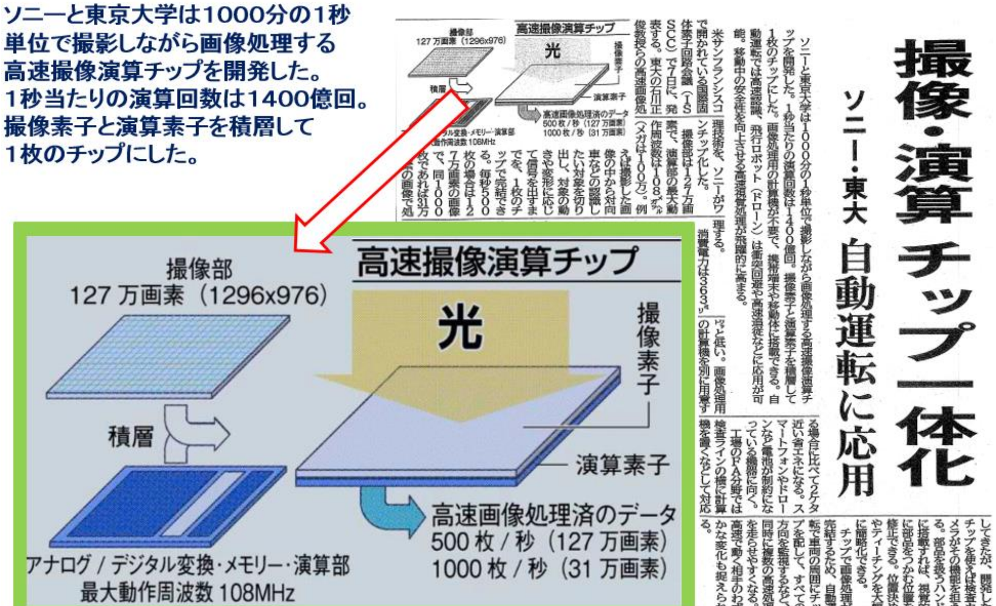
High-speed vision systems that combine high-frame-rate imaging and highly parallel signal processing enable instantaneous visual feedback to rapidly control machines over human-visual-recognition speeds.





Conventional CIS **Stacked CIS**

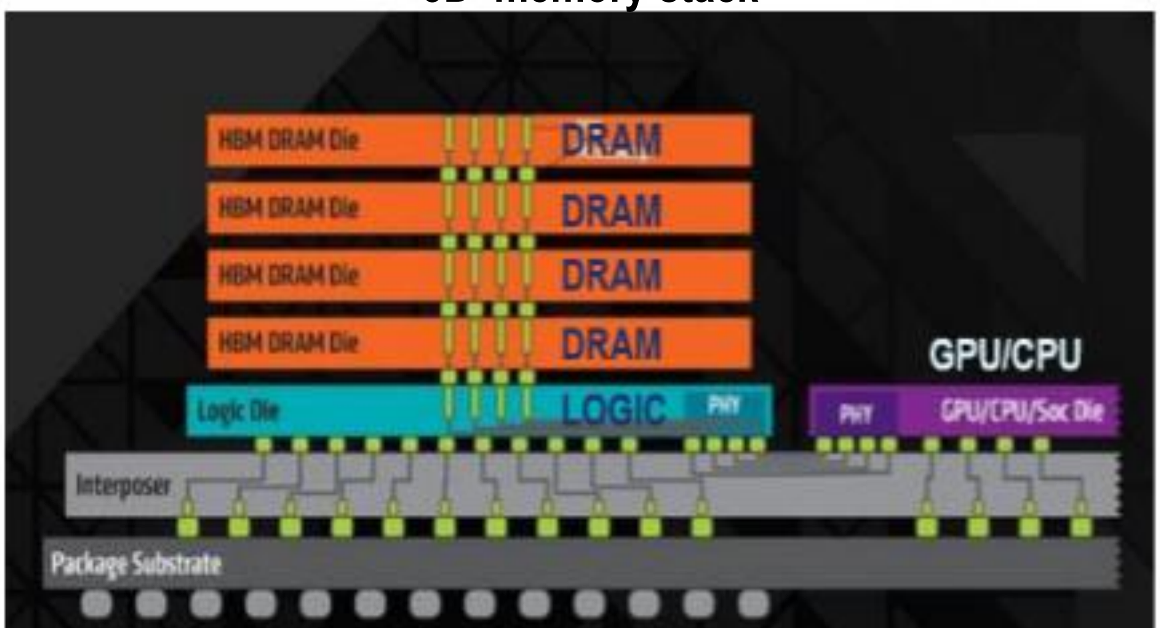
ソニーと東京大学は1000分の1秒単位で撮影しながら画像処理する高速撮像演算チップを開発した。1秒当たりの演算回数は1400億回。撮像素子と演算素子を積層して1枚のチップにした。

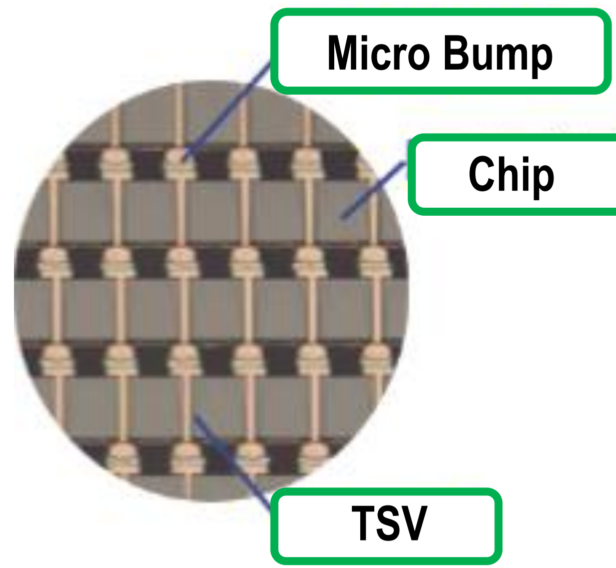


Next Generation Memory

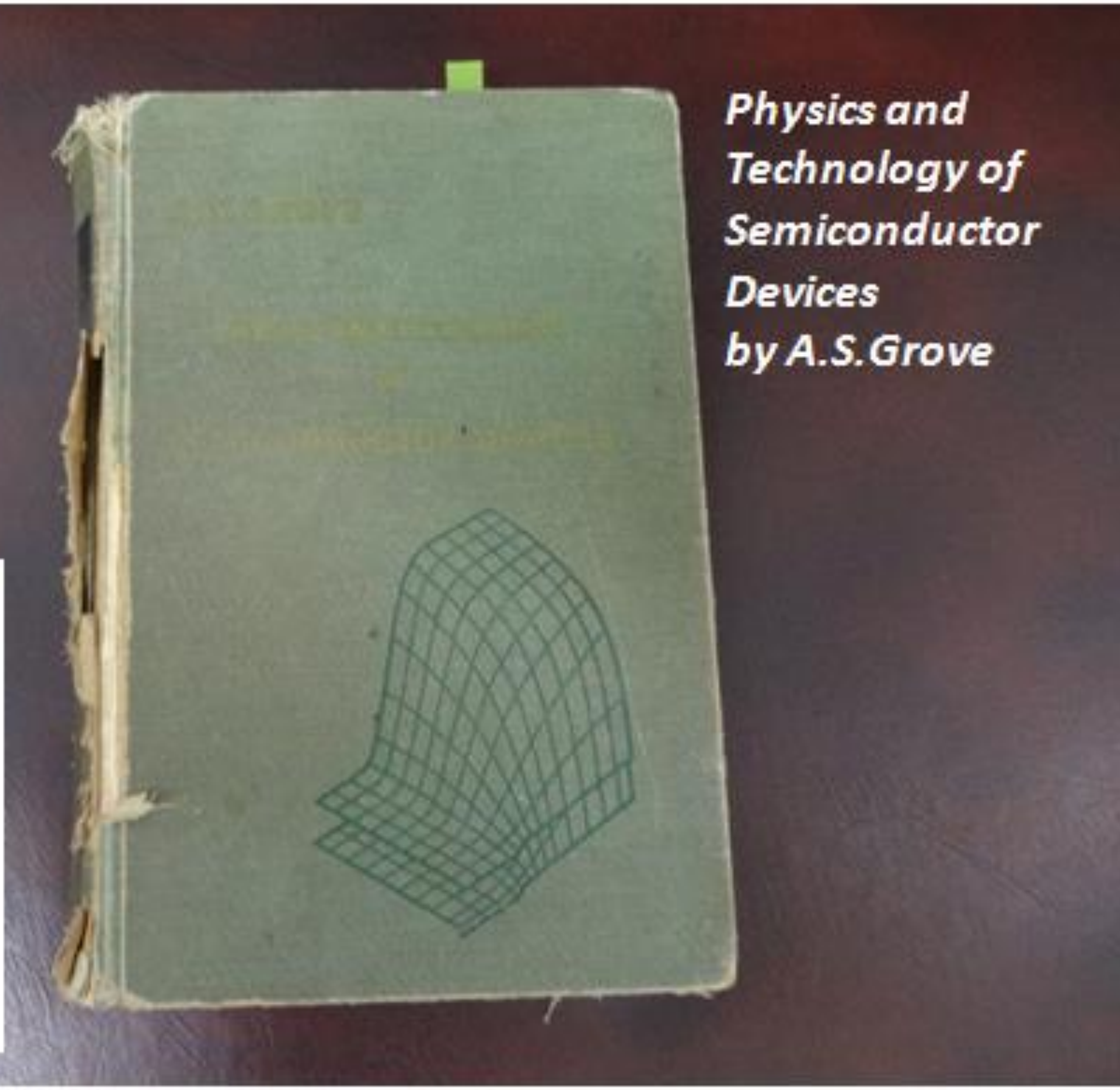
	FeRAM	MRAM	STT-MRAM	PRAM	ReRAM
信号比	10	1	6	100	10,000
微細化	×⇒○	×	○	○	○
読み出し	破壊	非破壊	非破壊	非破壊	非破壊
書換寿命	10^{12}	10^{16}	10^{16}	10^{12}	＞10^{6}
書込時間	50n～100ns	10ns	＜10ns	＞30ns	＜10ns
セルサイズ	～$15F^2$	～$8F^2$	～$8F^2$	$4F^2$～$6F^2$	$4F^2$

3D memory stack

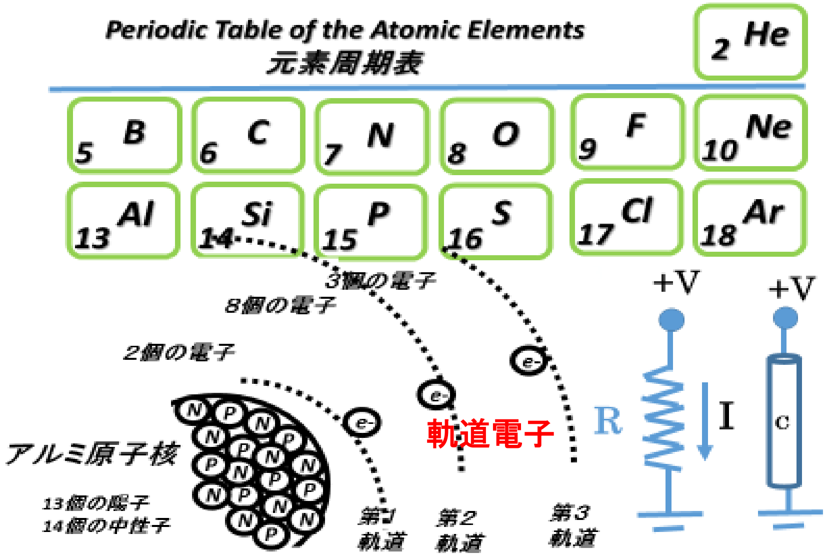


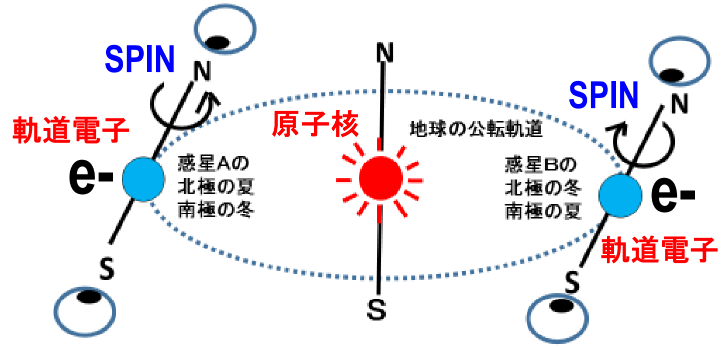


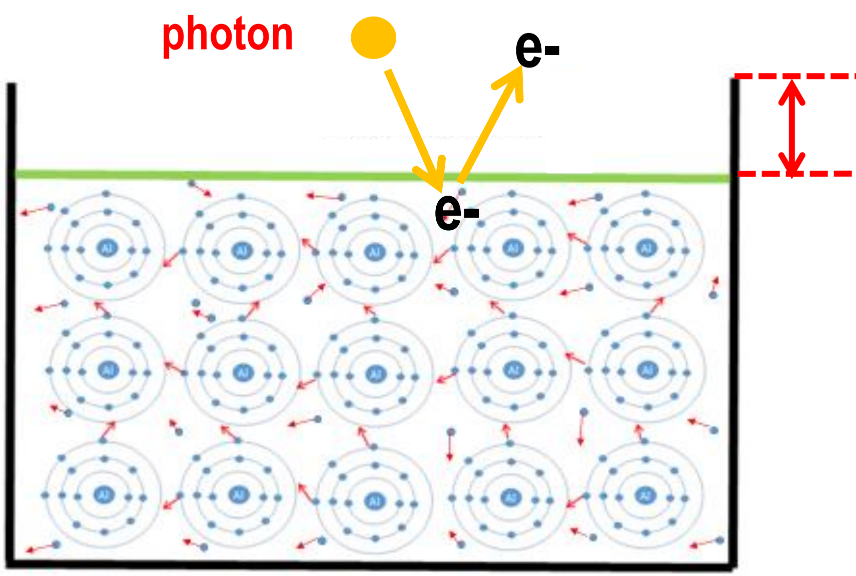
TSV=through Silicon Via

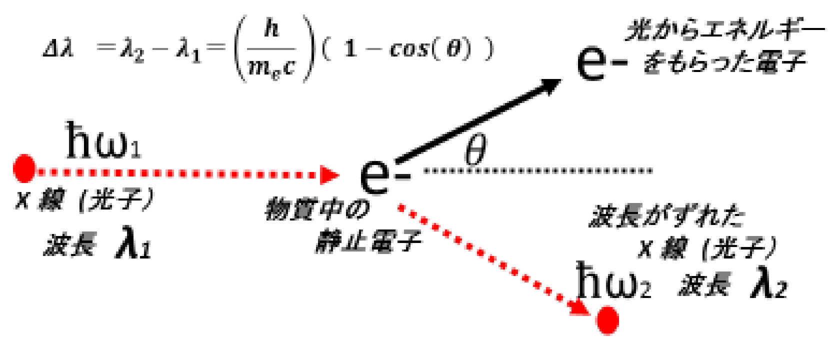


Prof. James McCaldin









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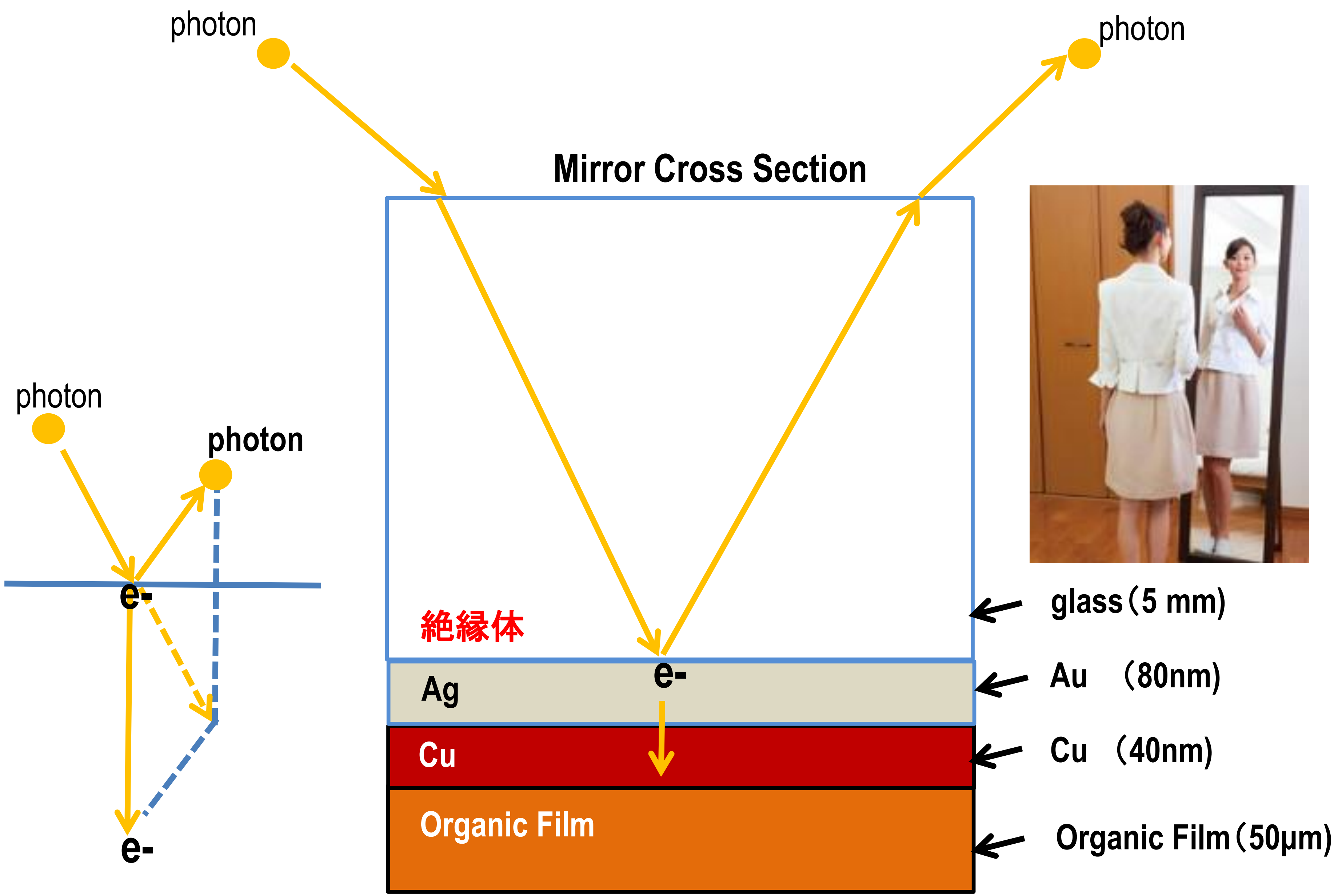

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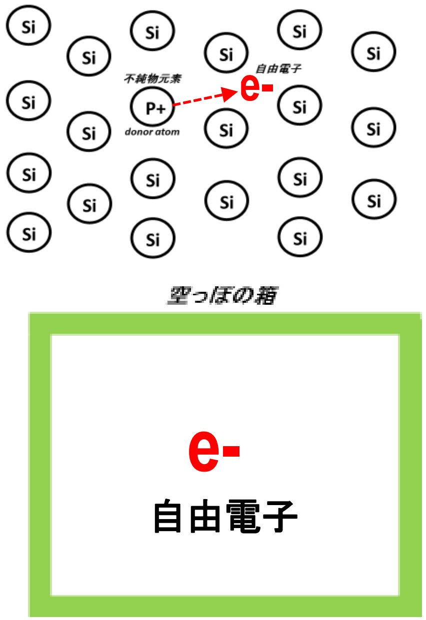
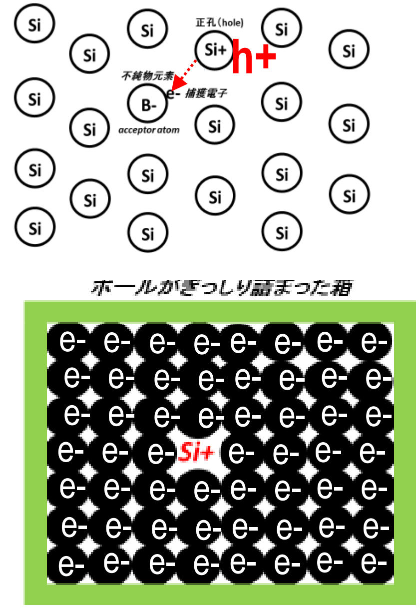
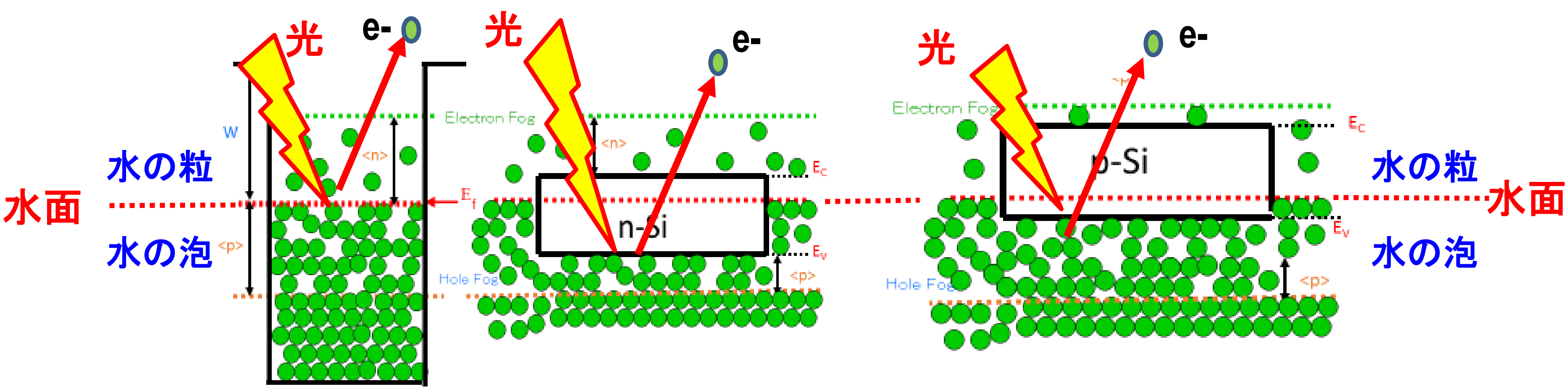
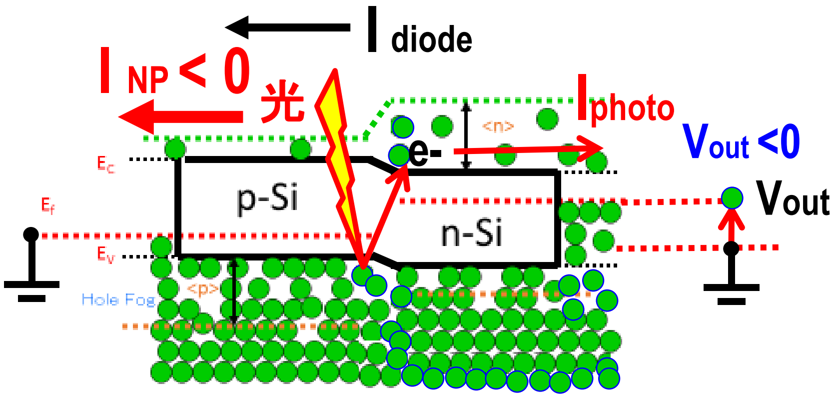

Si
P+
donor atom
不純物元素
自由電子
e-
空っぽの箱
e-
自由電子

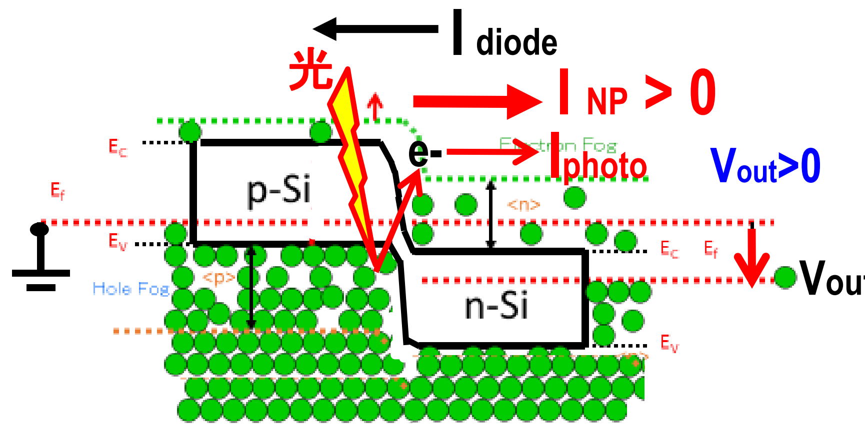

Si
Si+
h+
正孔 (hole)
B-
acceptor atom
不純物元素
捕獲電子
e-
ホールがぎっしり詰まった箱
Si+


光
e-
水面
水の粒
水の泡
W
Electron Fog
Hole Fog
<n>
<p>
E_f
E_c
E_v
n-Si
p-Si

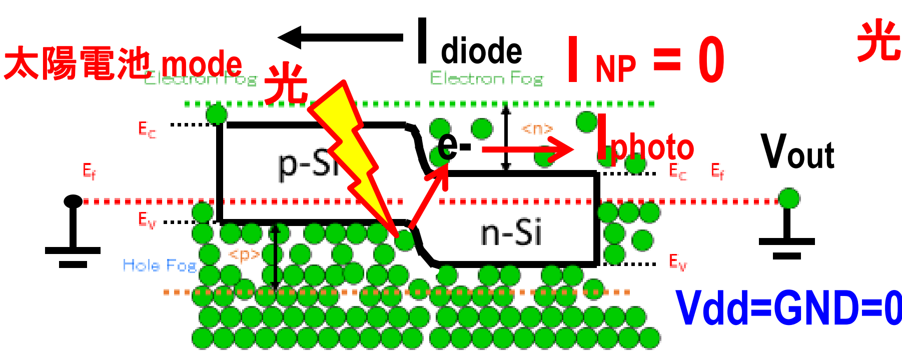
(1)電源電圧　Vdd<0 (順バイアス mode)　の場合

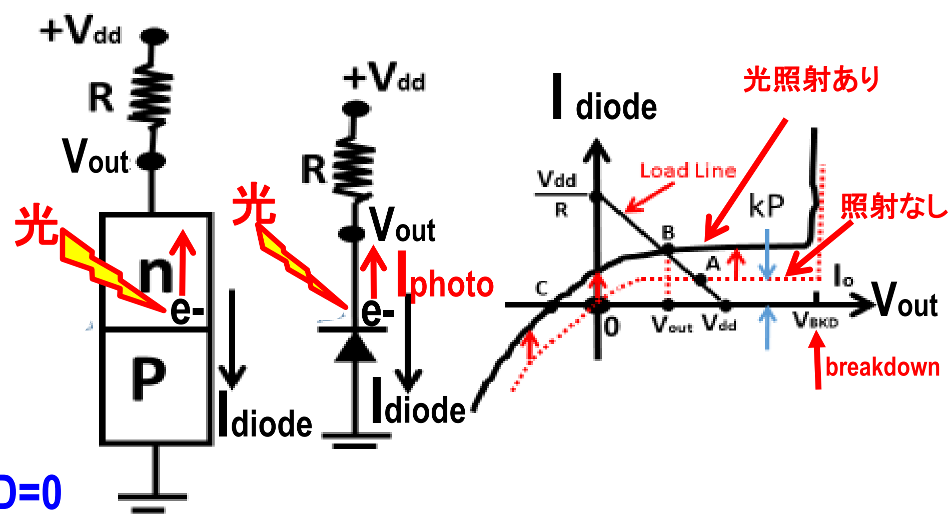


(3)電源電圧　Vdd>0 (逆バイアス mode)の場合

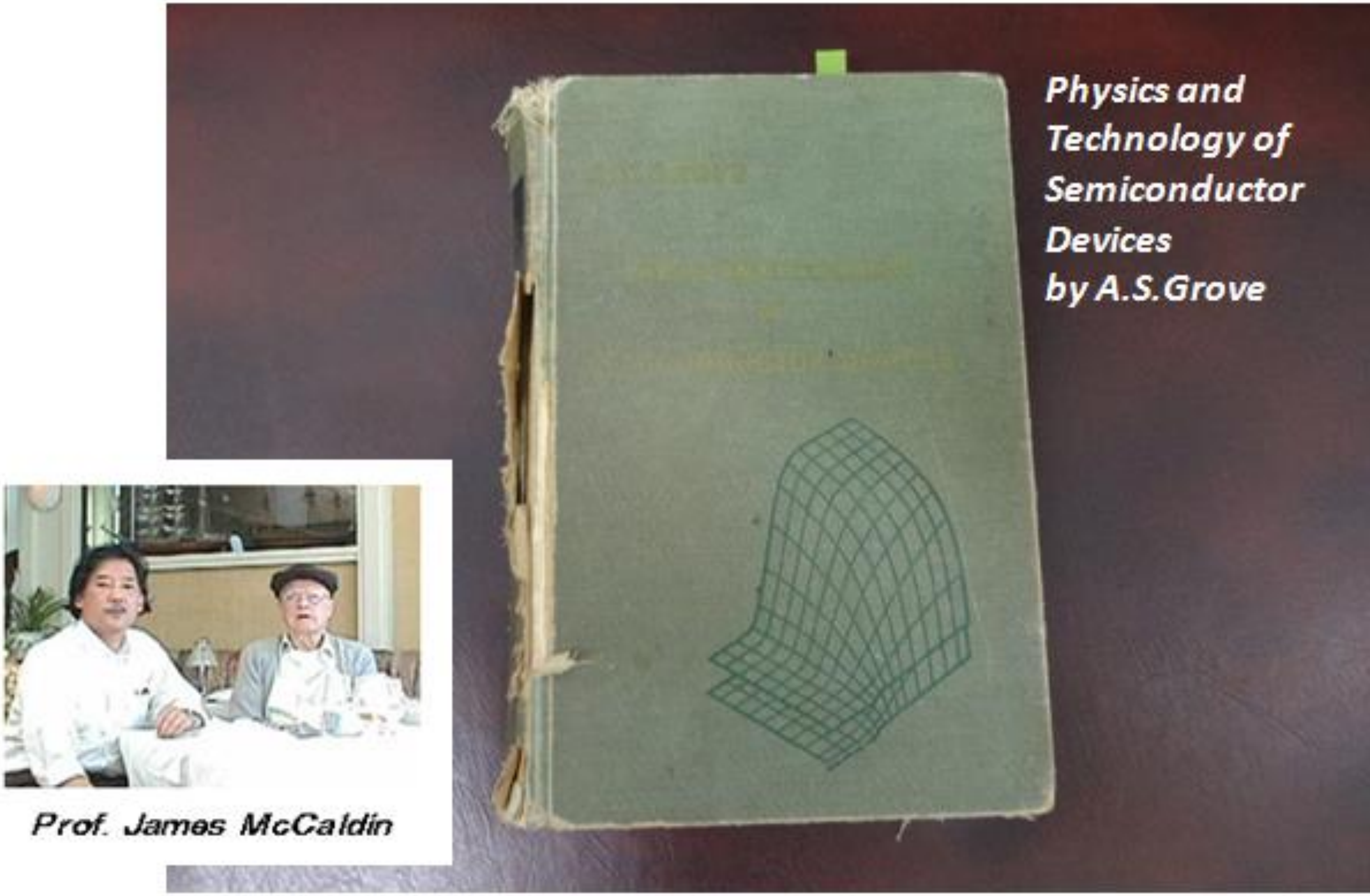


(2)電源電圧　Vdd=GND=0 (NOバイアス mode)の場合

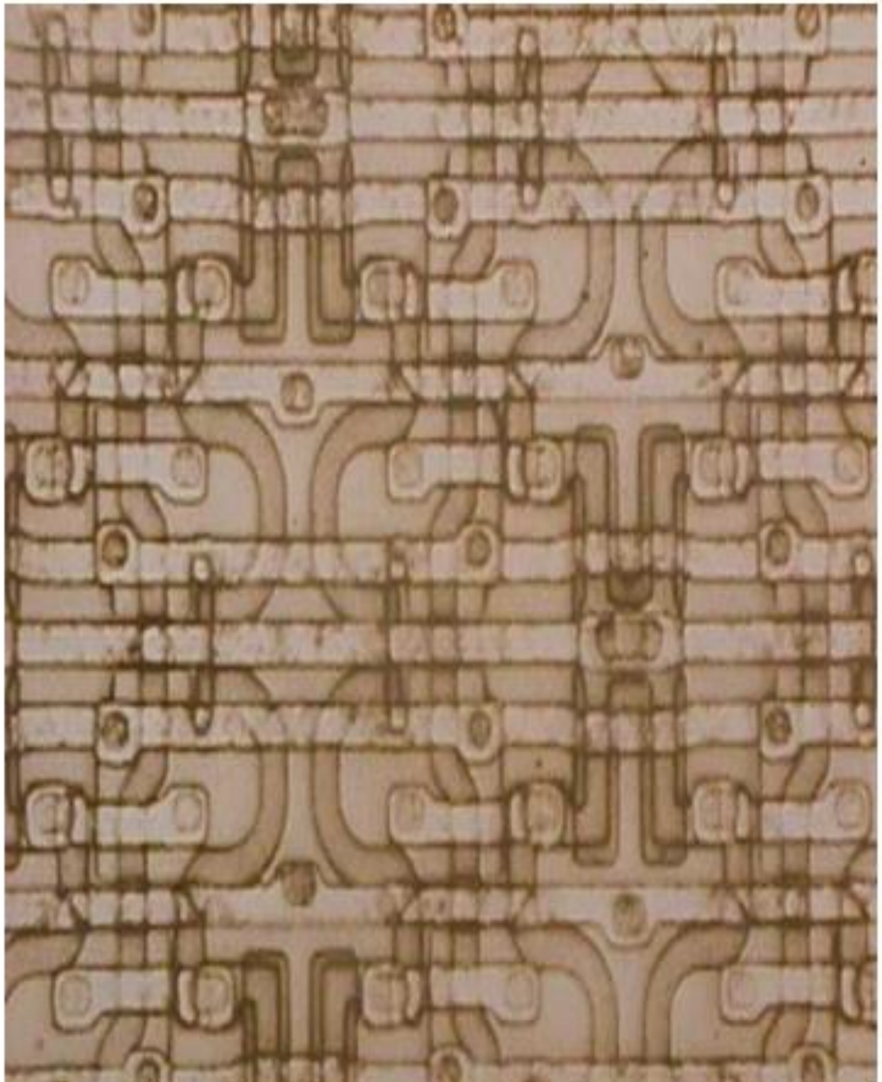




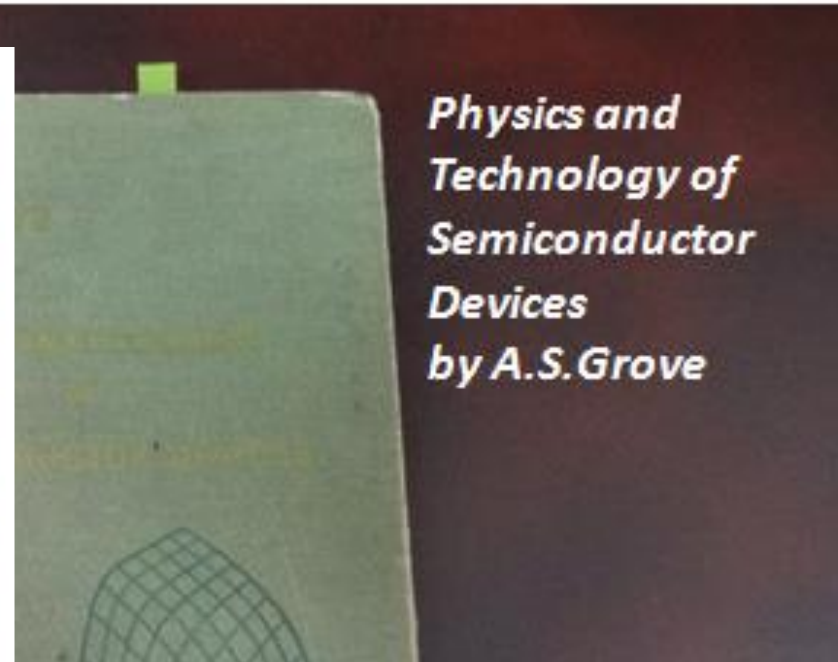
光を照射すると電流が流れる！

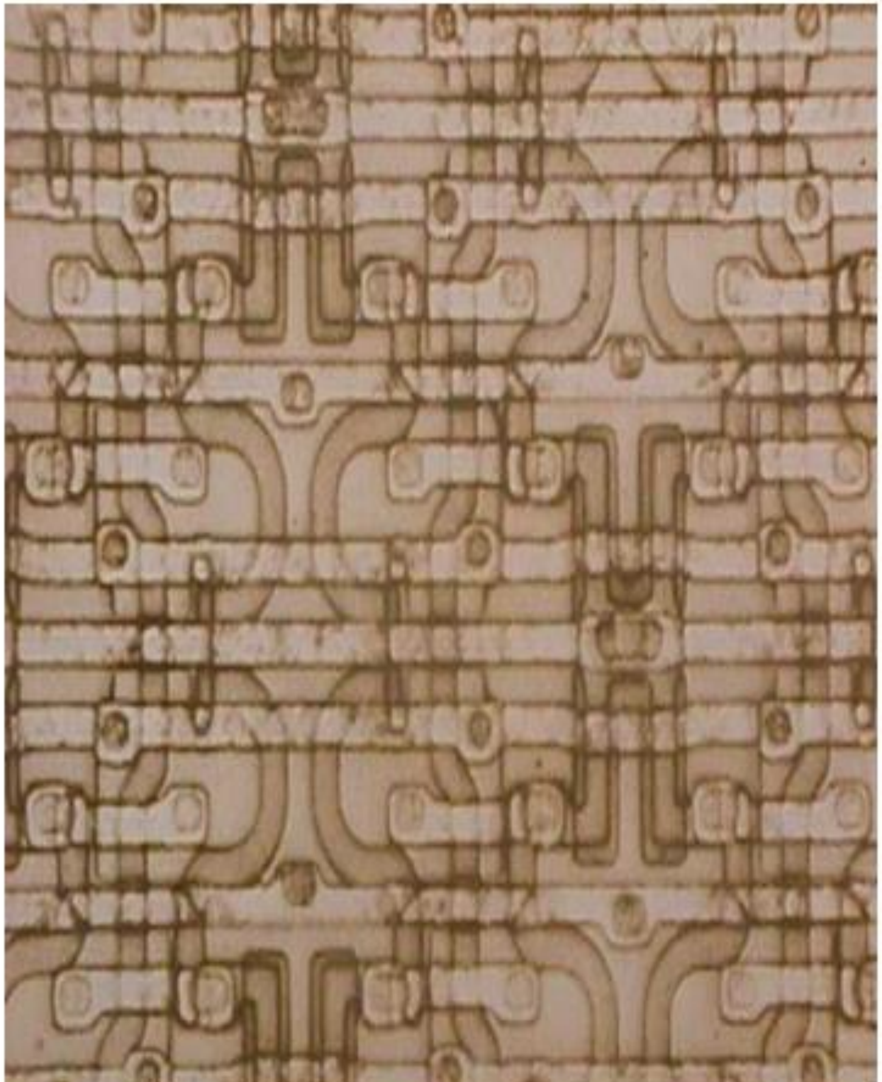


Prof. James McCaldin



1971 Intel 1101 256bit RAM





1971 Intel 1101 256bit RAM

Prof.CA Mead and myself, Sept 1972

128 bit data comparator chip designed by CalTech and fabricated in Intel, 1972.

128-Bit Multicomparator

CARVER A. MEAD, RICHARD D. PASHLEY, MEMBER, IEEE, LEE D. BRITTON, YOSHIAKI T. DAIMON, AND STEWART F. SANDO, JR., MEMBER, IEEE

Abstract—A 128-bit multicomparator was designed to perform the search-sort function on arbitrary length data strings. Devices can be cascaded for longer block lengths or paralleled for bit-parallel, word-serial applications. The circuit utilizes a 3-phase static-dynamic shift register cell for data handling and a unique gated EXCLUSIVE-NOR circuit to accomplish the compare function. The compare operation is performed bit parallel between a "data" register and a "key" register with a third "mask" register containing DON'T CARE bits that disable the comparator. The multicomparator was fabricated using p-channel silicon-gate metal-oxide-semiconductor (MOS) technology on a 107 × 150 mil chip containing 3350 devices. With transistor-transistor logic (TTL) input, data rates in excess of 2 MHz have been attained. The average power dissipation was 250 mW in the dynamic mode and 300 mW in the static mode.

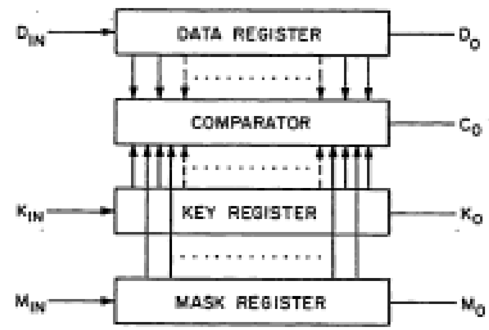
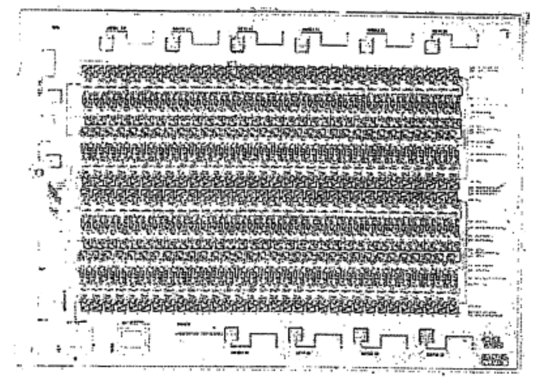
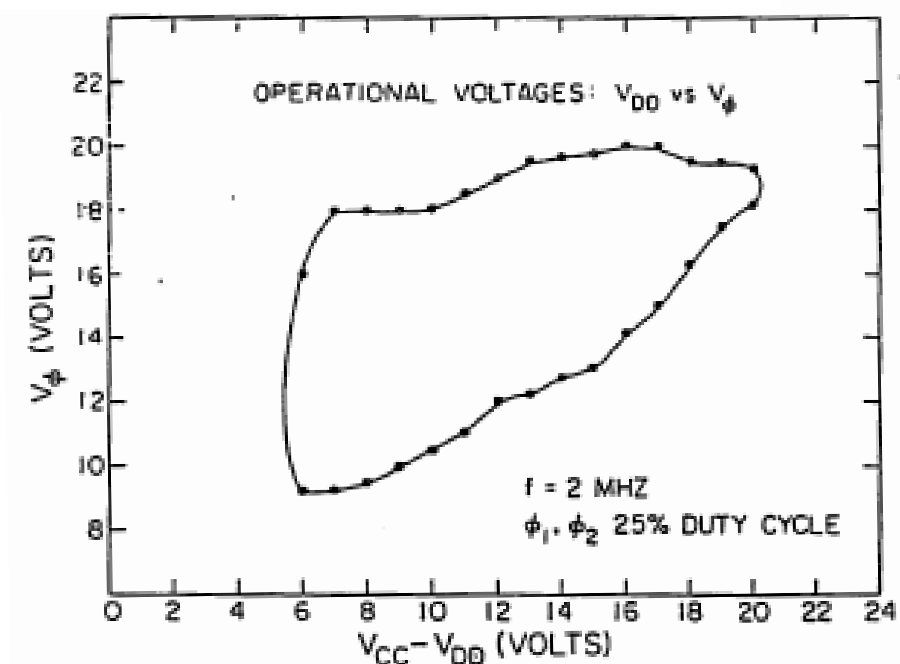


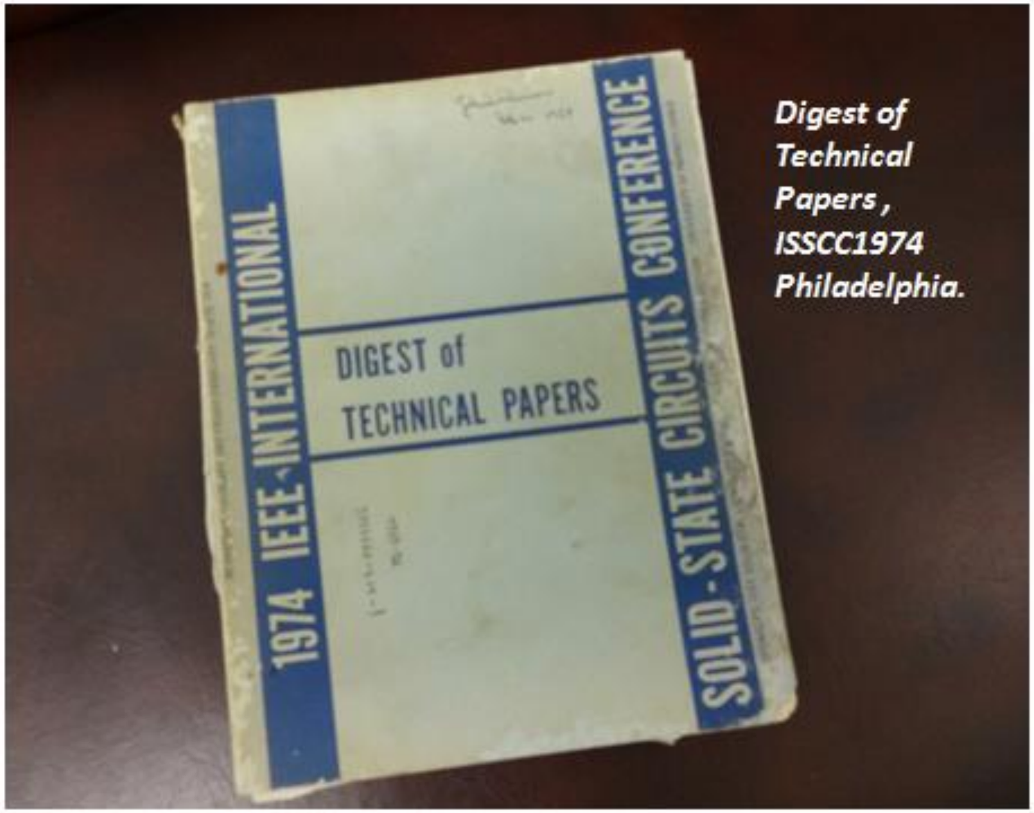
Fig. 1. Block diagram of multicomparator.





Prof.CA Mead and myself, Sept 1972

Consumer Electronics from HOT Chips to COOL Chips.



Digest of Technical Papers, ISSCC1974 Philadelphia.

Charge-Coupled Devices and Applications

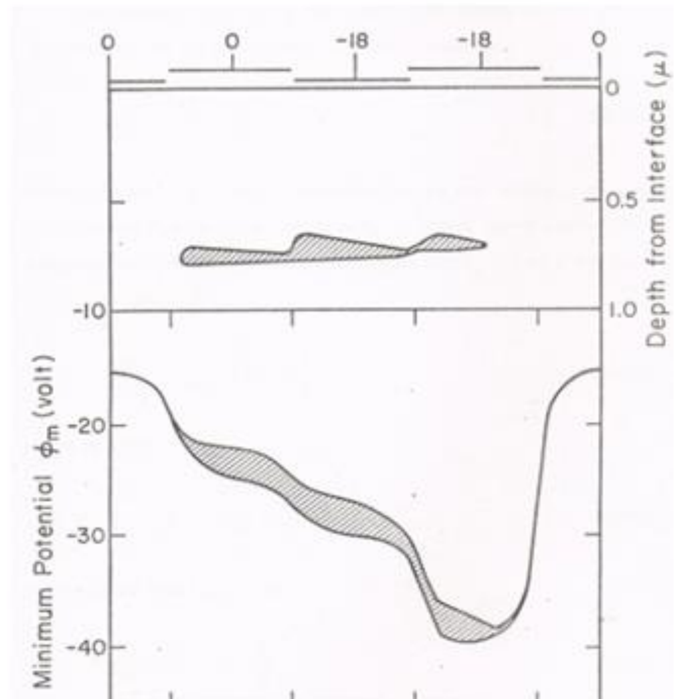
Chairman

Lewis M. Terman

Testimonial to the importance of the charge-transfer phenomenon is attested to by the Morris N. Liebmann and the David A. Sarnoff awards this year to the originators of the charge-coupled and bucket-brigade devices, respectively. The papers in this session concentrate on the former.

ISSCC1974 PhD Student Paper on buried channel CCD

Prof. T. C. McGill



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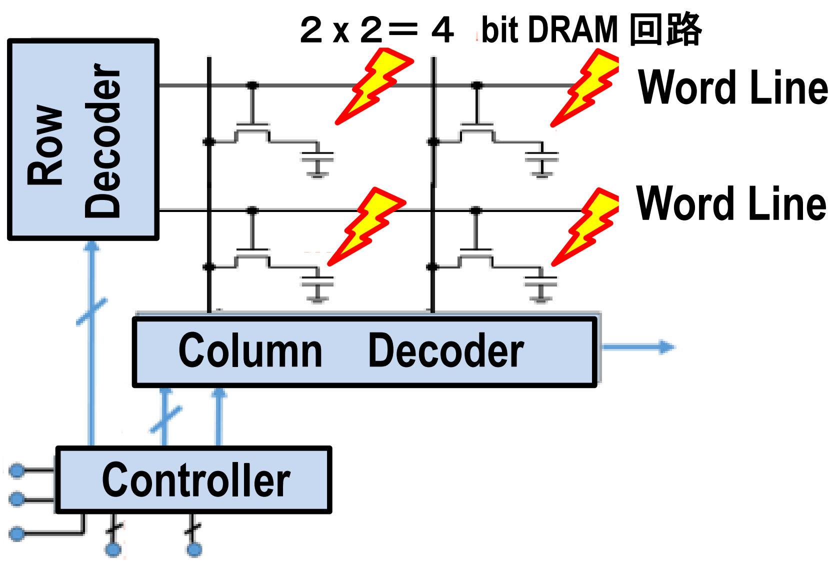

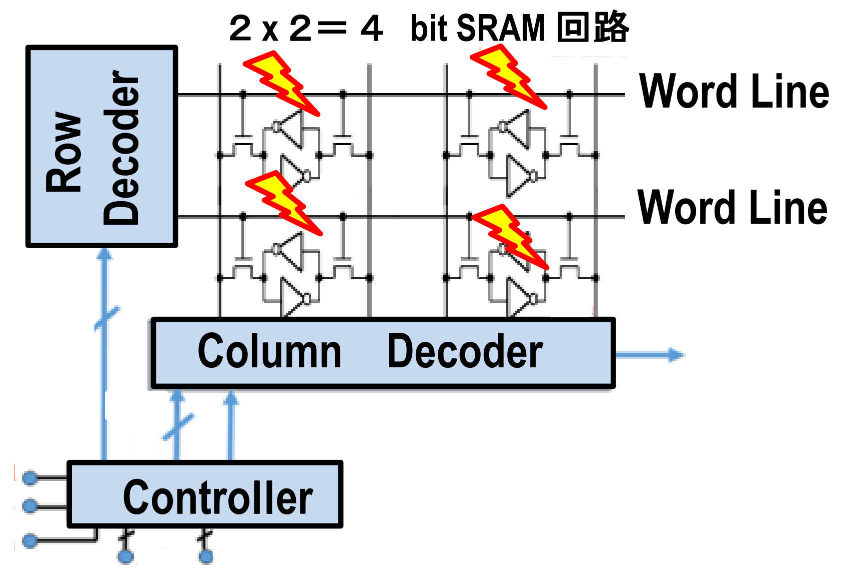

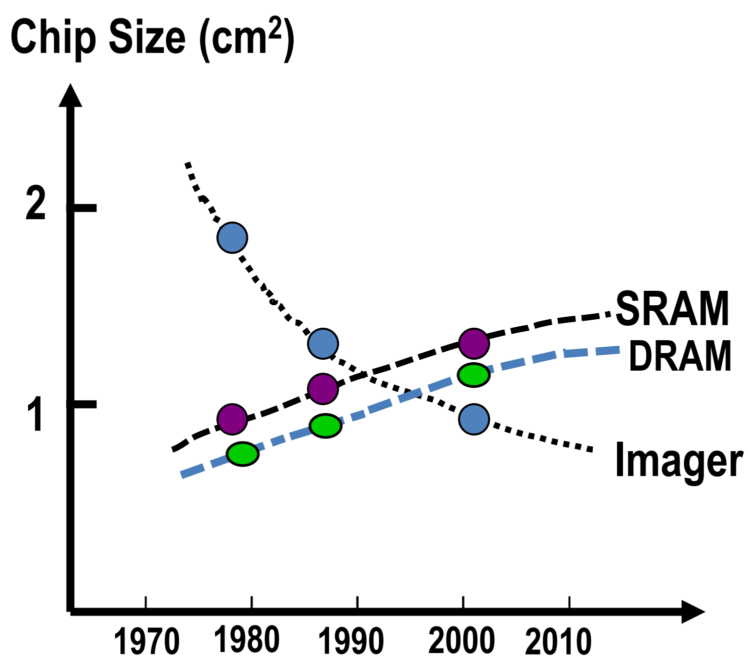

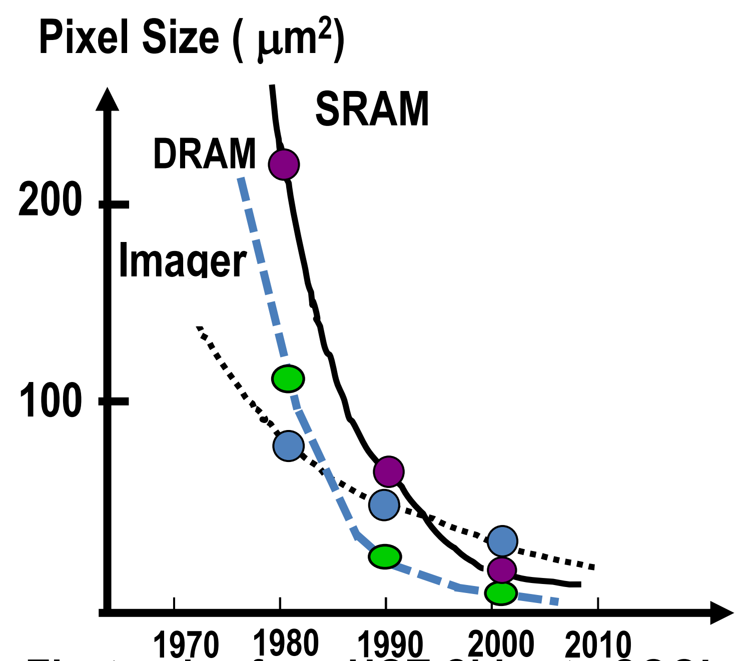

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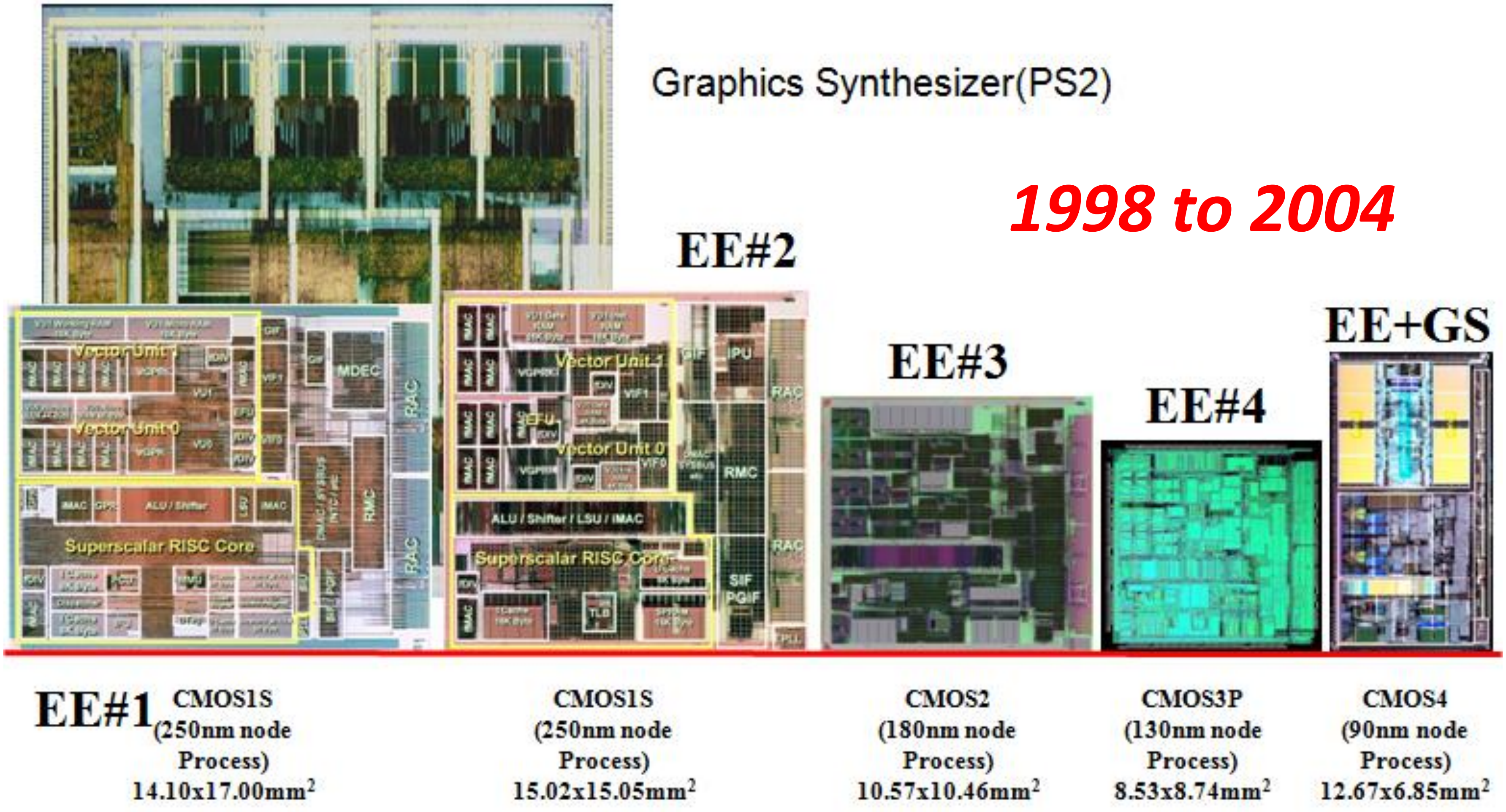
1975-1982 Engineer in CCD Imagers and Camera System
1983-1989 Engineering Manager in SRAM/DRAM/ADC
1990-1998 General manager in Sony /NVM/MCU/PS1
1998-2008 Executive Staff Sony Semiconductor
Strategic Planning PS2/PS3
IEEE Computer Elemets Workshop
@ Vail, Colorado, 1995
Mitsuo Saito（Toshiba)
Bob Guensey（IBM)
Ken Kutaragi
Yoshiiaki Hagihara
Consumer Electronics from HOT Chips to COOL Chips.

EE Development History



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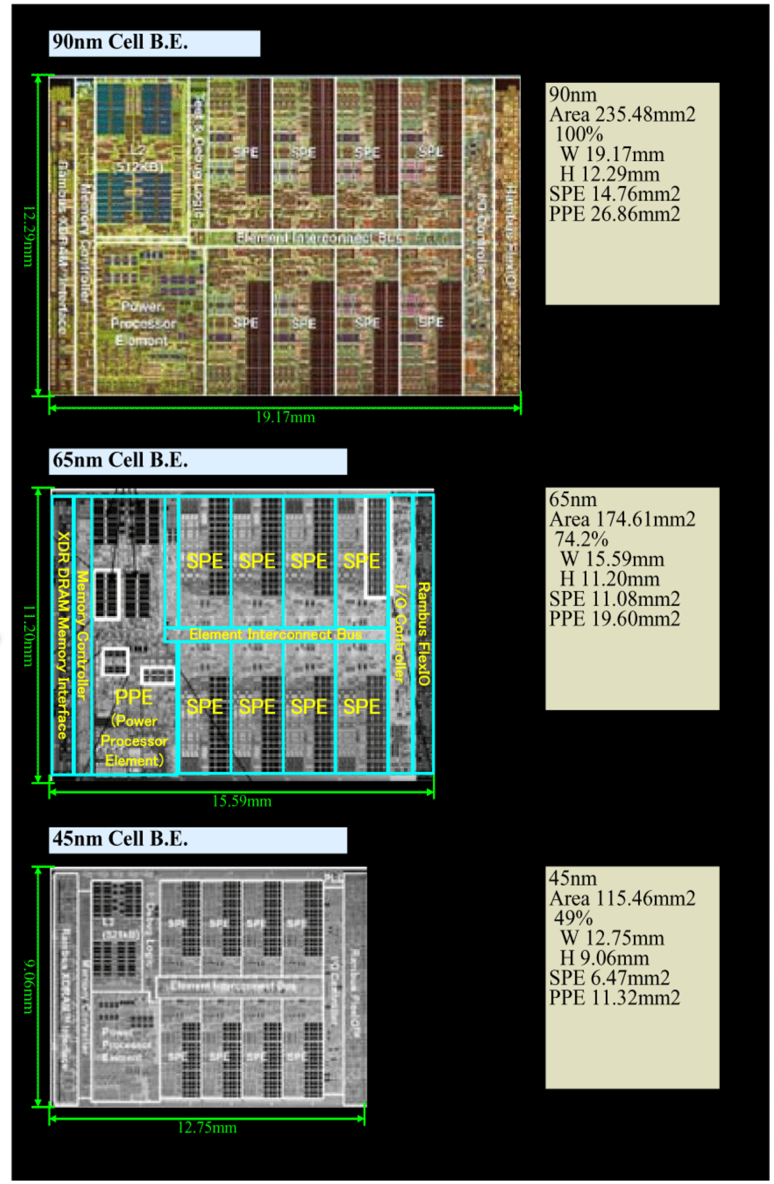
PS3 Cell Processor Chip Size scaling

PS3 2005 model

Cell B.E. 90nm, 65nm, 45nm



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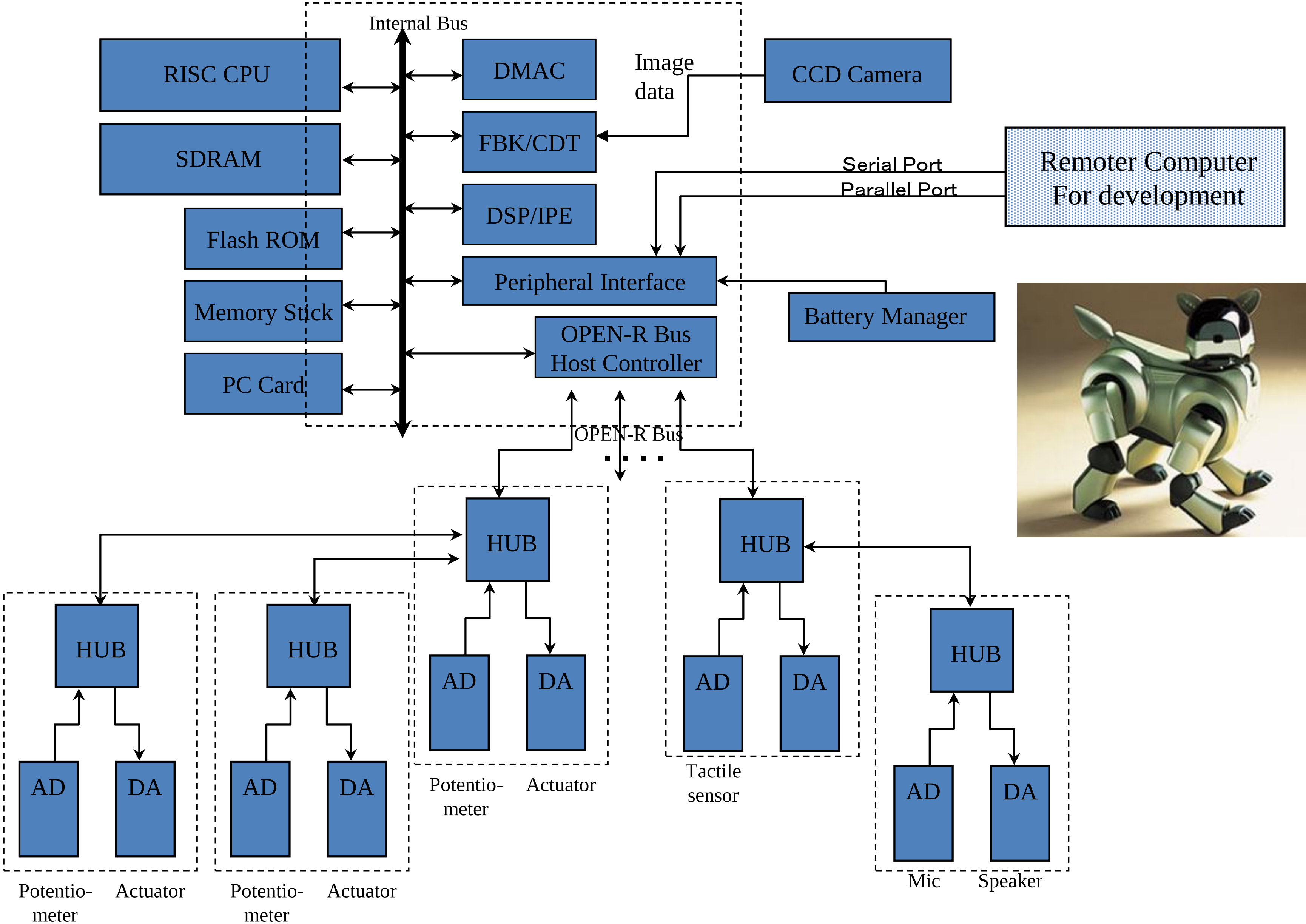
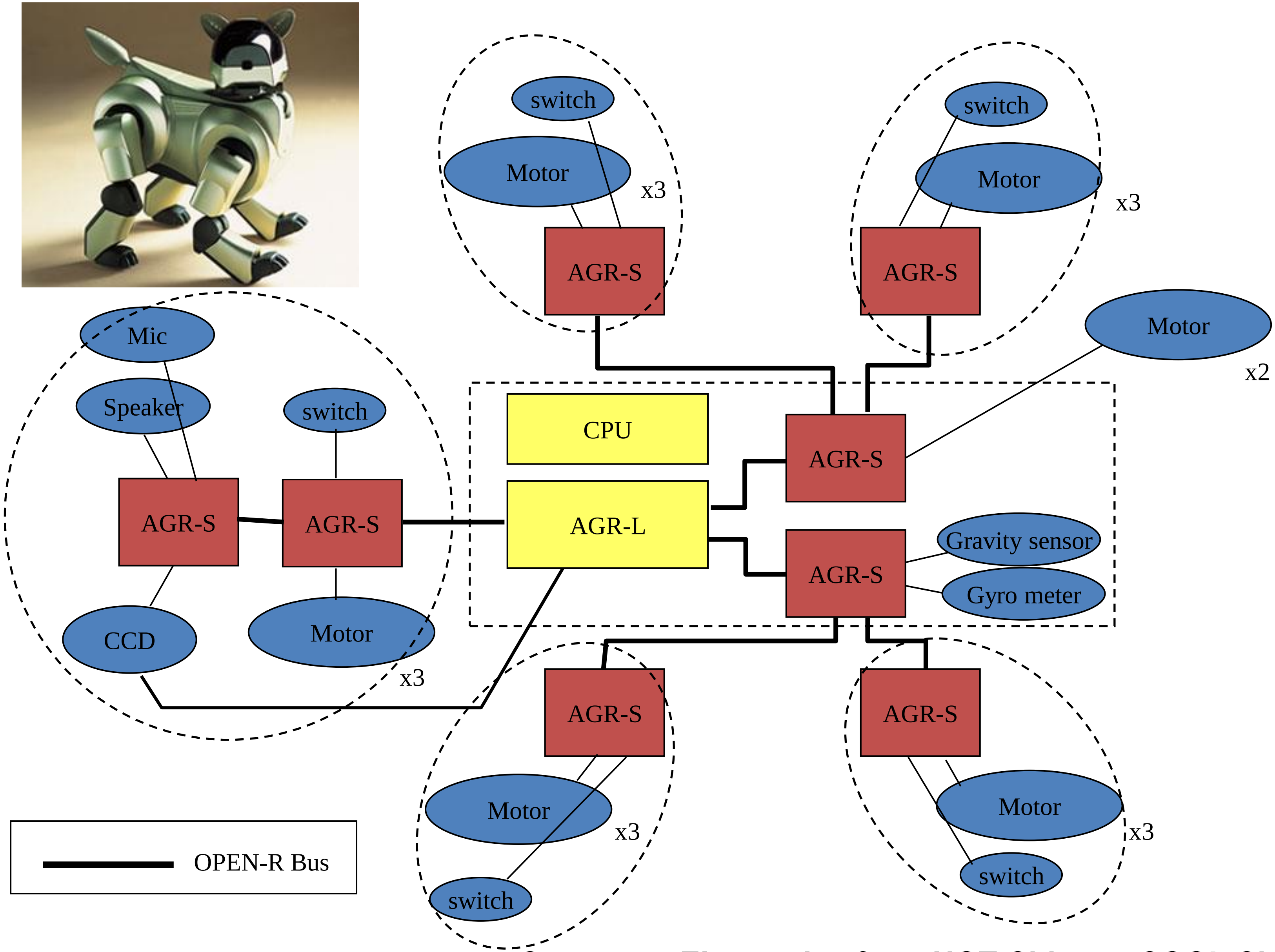
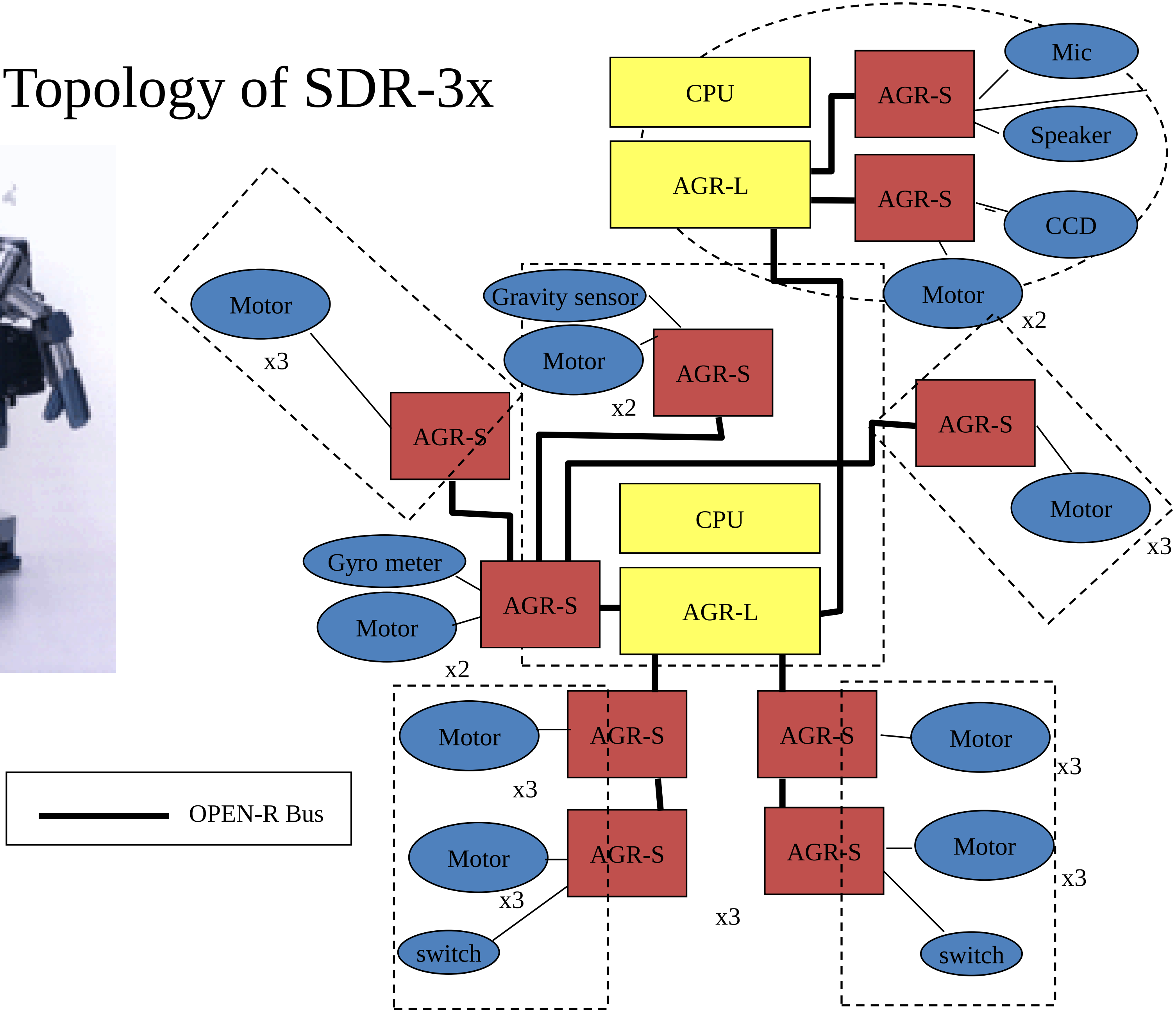
Logical Hardware Block Diagram

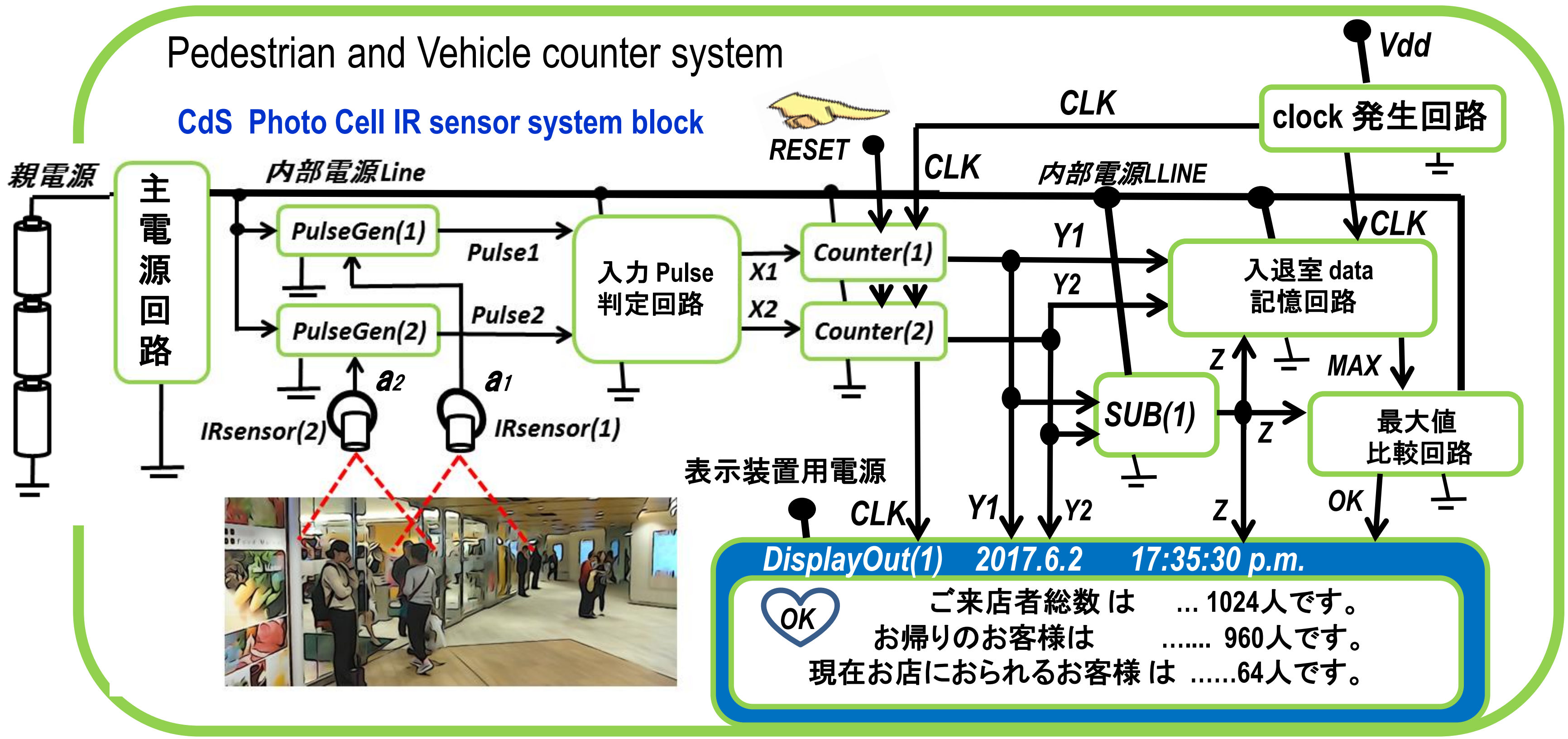


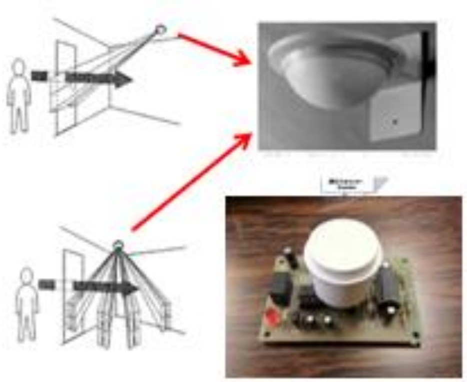
Topology of ERS-110

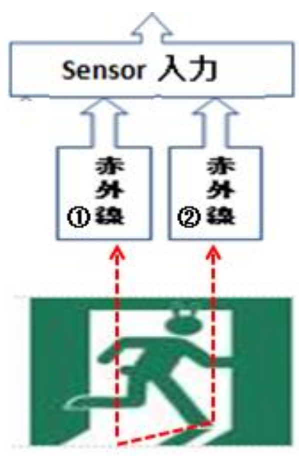


Topology of SDR-3x









街中での通行人の映像

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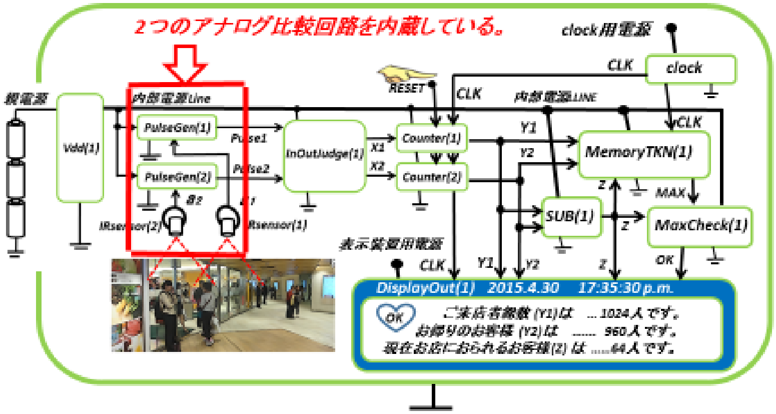
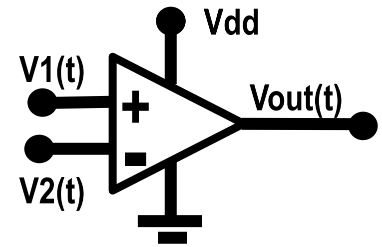
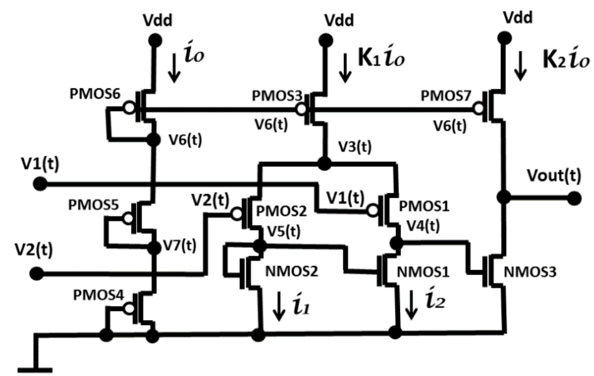
光伝導Cell (CdS) Sensor System 例



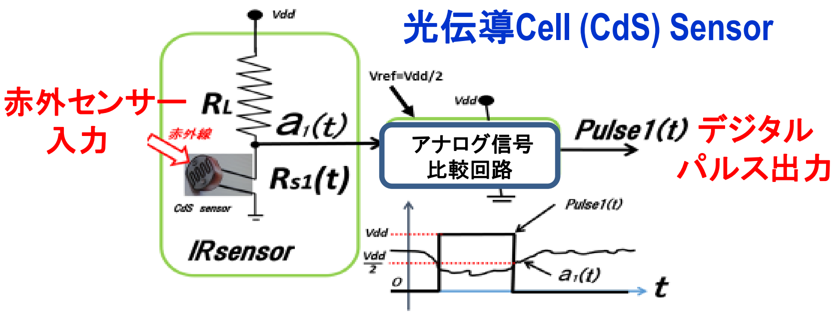
アナログ信号比較回路 （単純な１bit の A/D変換器）



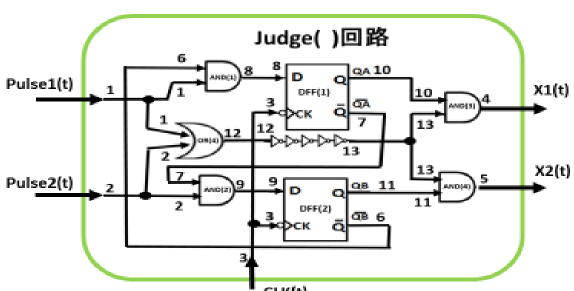
CMOS回路で構成されたアナログ信号比較回路



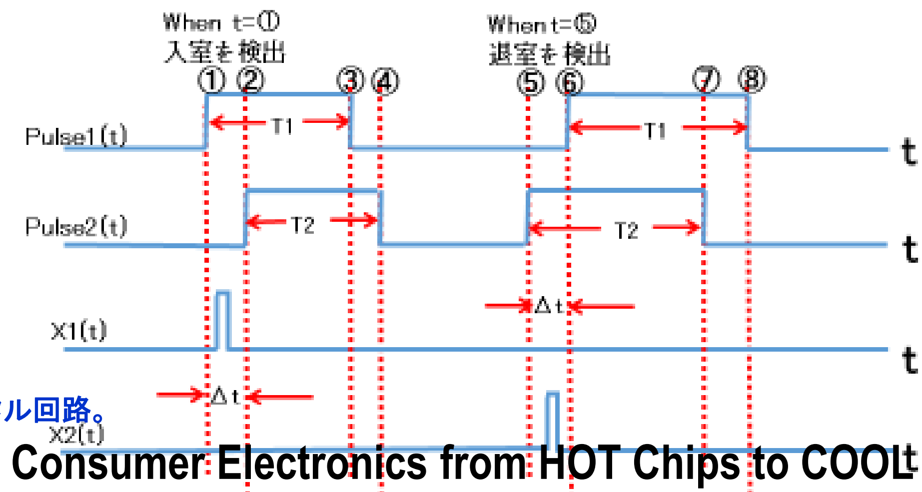
光伝導Cell (CdS) Sensor



相対Pulse遅延判定回路



2つのPulse信号のうちどちらが早いかを判定するCMOSデジタル回路。



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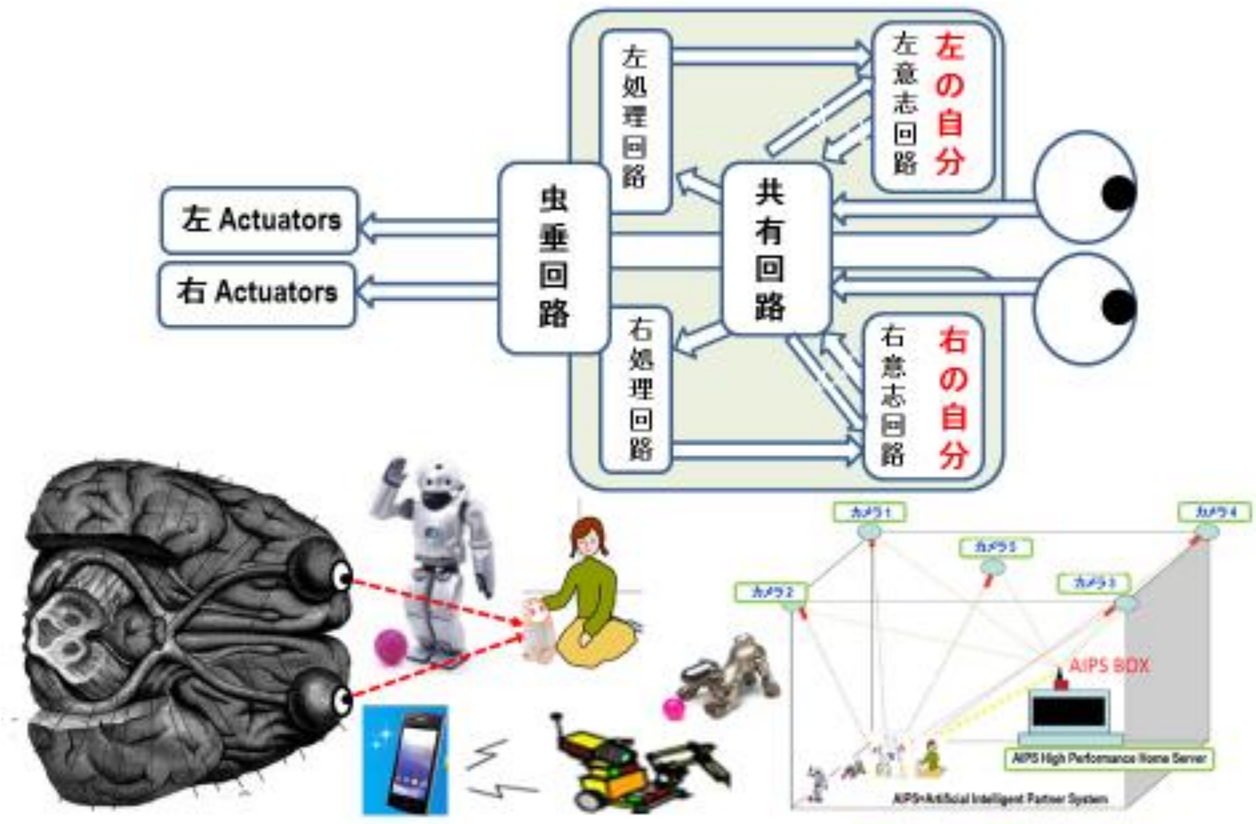
“Cool chips for the next decade”

A cool chip can be created by low power efforts on the device, circuit and system architecture.



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