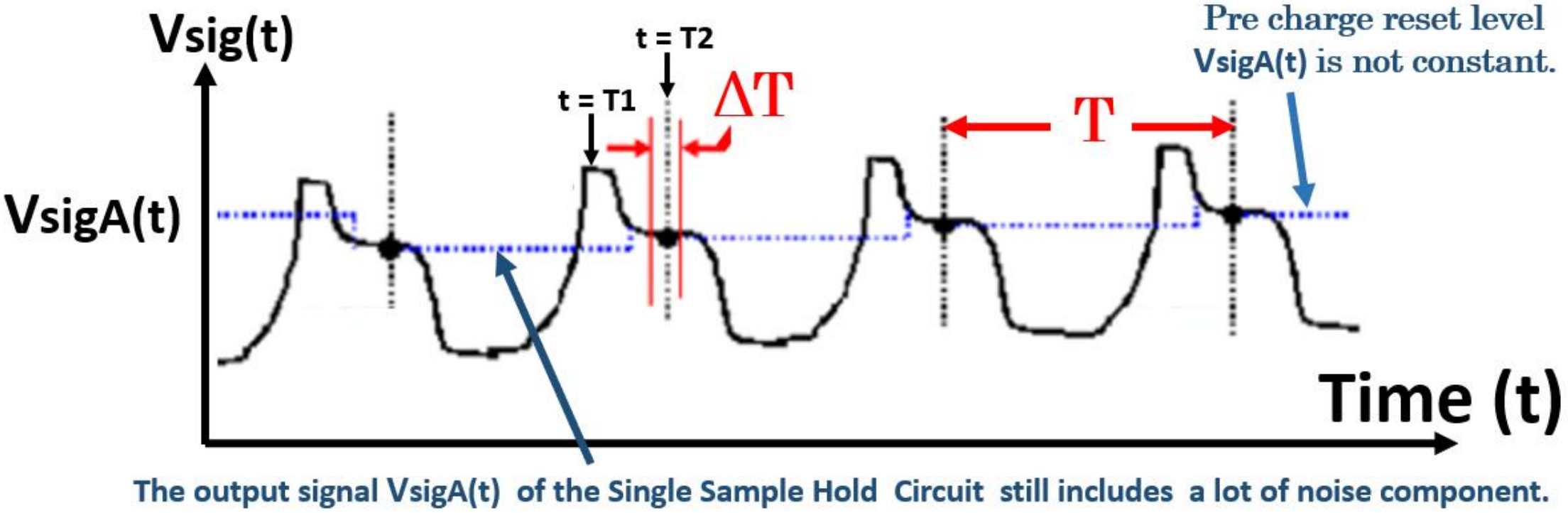
7 In Pixel Correlation Double Sampling (CDS) circuit

Under Construction

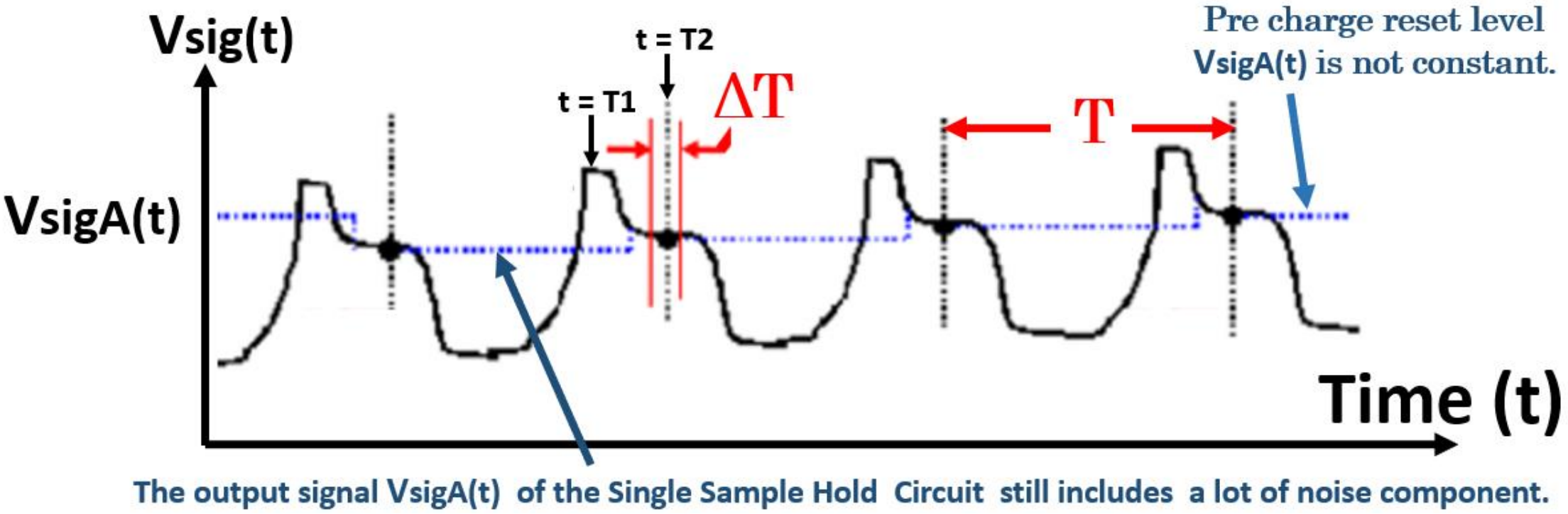
7 In Pixel Correlation Double Sampling (CDS) circuit

The output signal of an image sensor is buried in many kinds of noises and appears only in a short time slot ΔT during the total cycle time T.



7 In Pixel Correlation Double Sampling (CDS) circuit

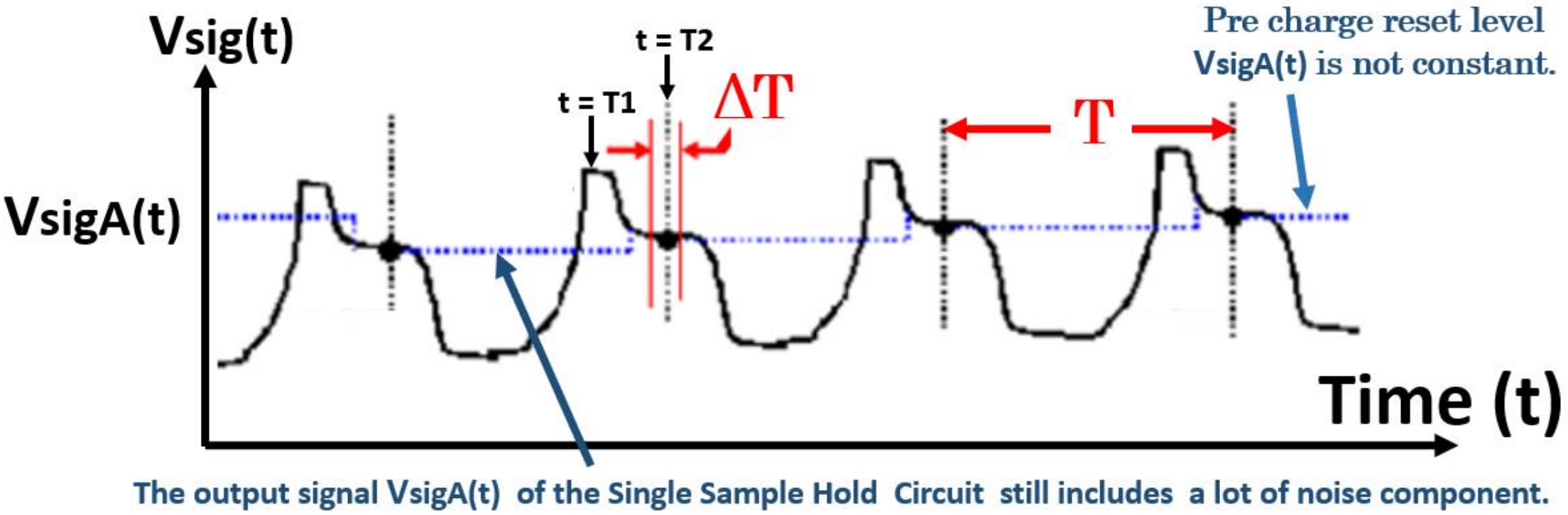
The dominant noise is the clocking noise coupled by the parasitic oxide capacitance between the reset gate and the floating signal output diffusion. Others are white noise, 1/f noise and CkT noise.



H. Nyquist, "Thermal agitation of electric charge in conductors," Phys. Rev. 32, 110–113 (1928).

7 In Pixel Correlation Double Sampling (CDS) circuit

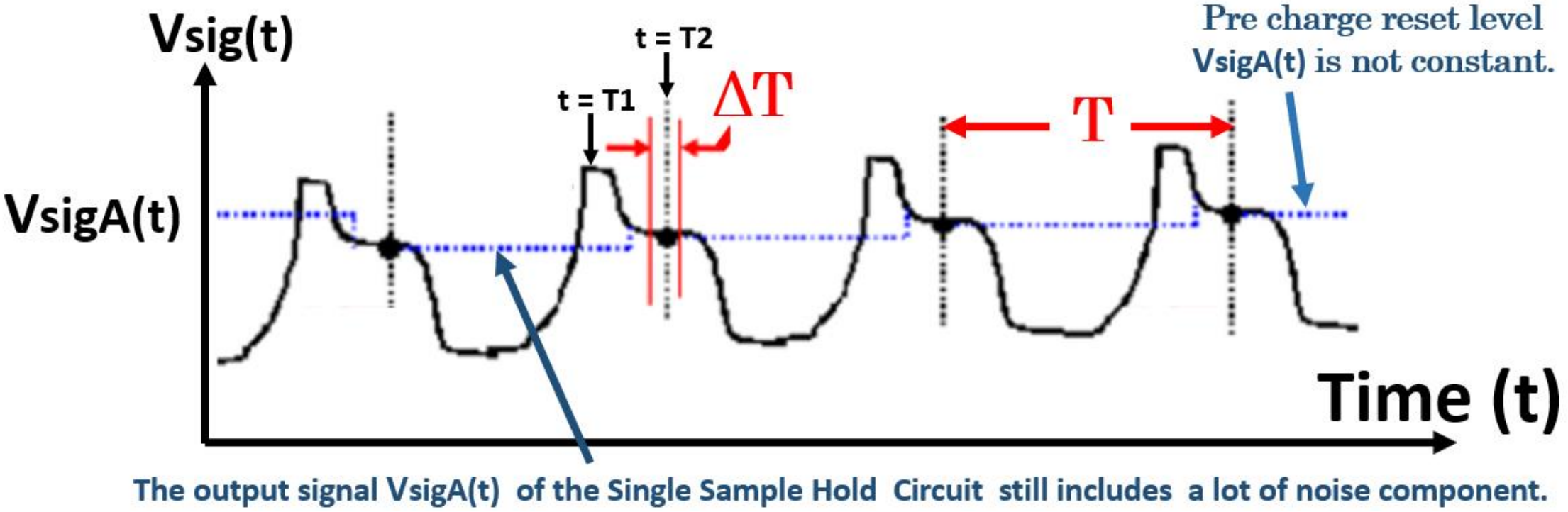
The CkT noise is proportional to the large and long dimension of the floating diffusion signal line between the pixel and the output circuit.



H. Nyquist, "Thermal agitation of electric charge in conductors," Phys. Rev. 32, 110–113 (1928).

7 In Pixel Correlation Double Sampling (CDS) circuit

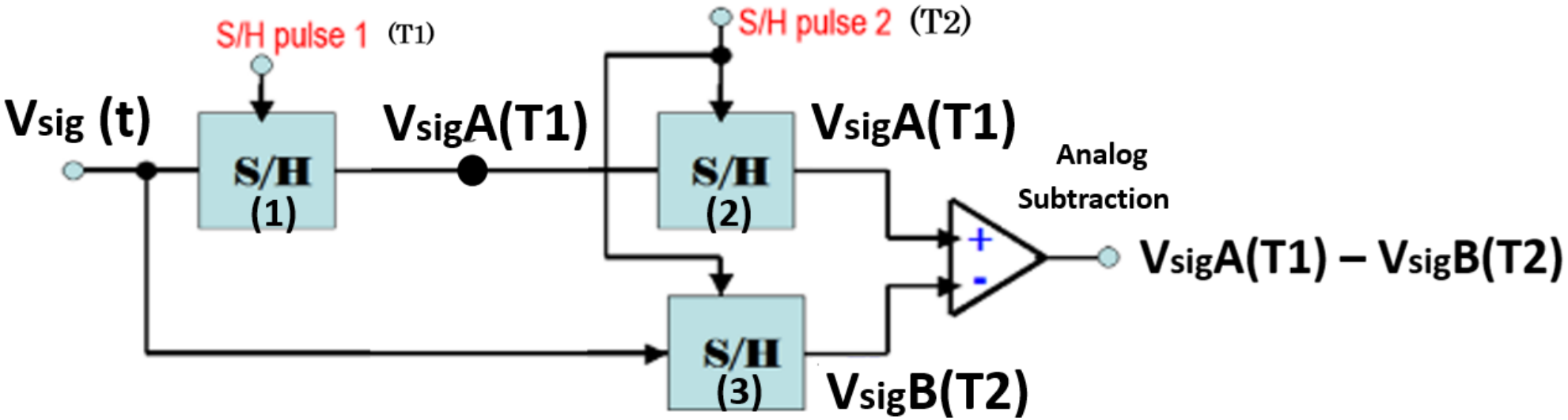
One single sample hold circuit was not enough to eliminate all of the undesired noise components because the pre charge reset level **VsigA(t)** of the output signal **Vsig(t)** itself is not constant and has fluctuations.



H. Nyquist, "Thermal agitation of electric charge in conductors," Phys. Rev. 32, 110–113 (1928).

7 In Pixel Correlation Double Sampling (CDS) circuit

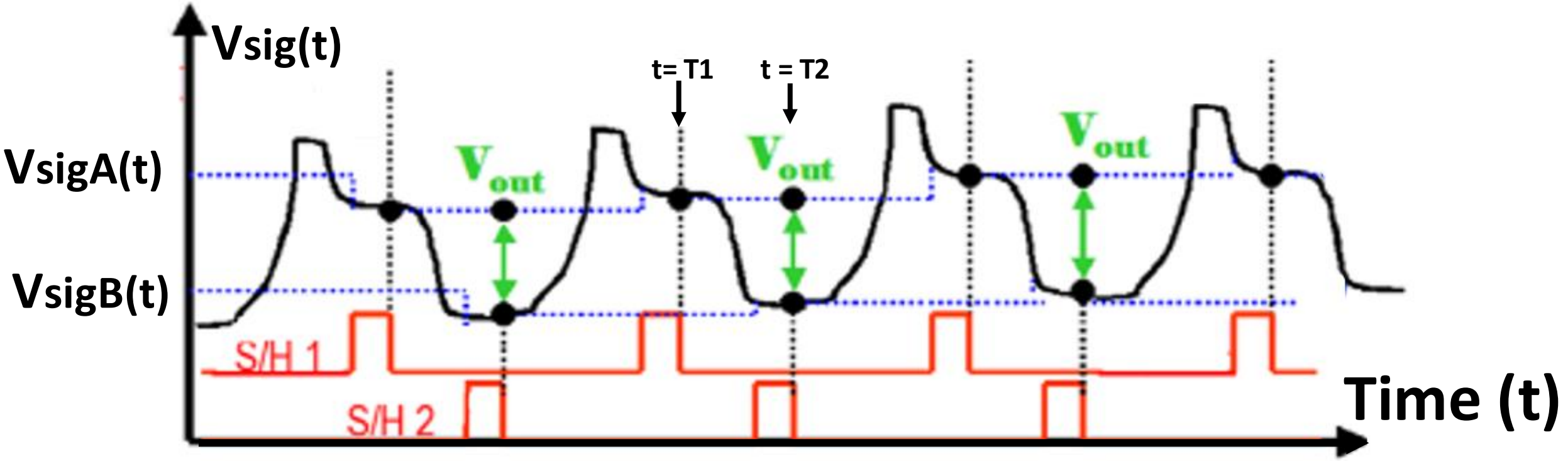
In 1972, M. White proposed Correlated Double Sample (CDS) circuit which has three sample hold circuits and one analog subtraction circuit to delete the undesired noise components of the output signal of CCD image sensors.



M .H. White, D. R. Lanpe, F. C. Blaha and I. A . Mack,
"Characterization of surface Channel CCD Image Arrays at Low Light Level",
IEEE Journal of Solid State Circuits, SC-9, pp.1-13 (1974)

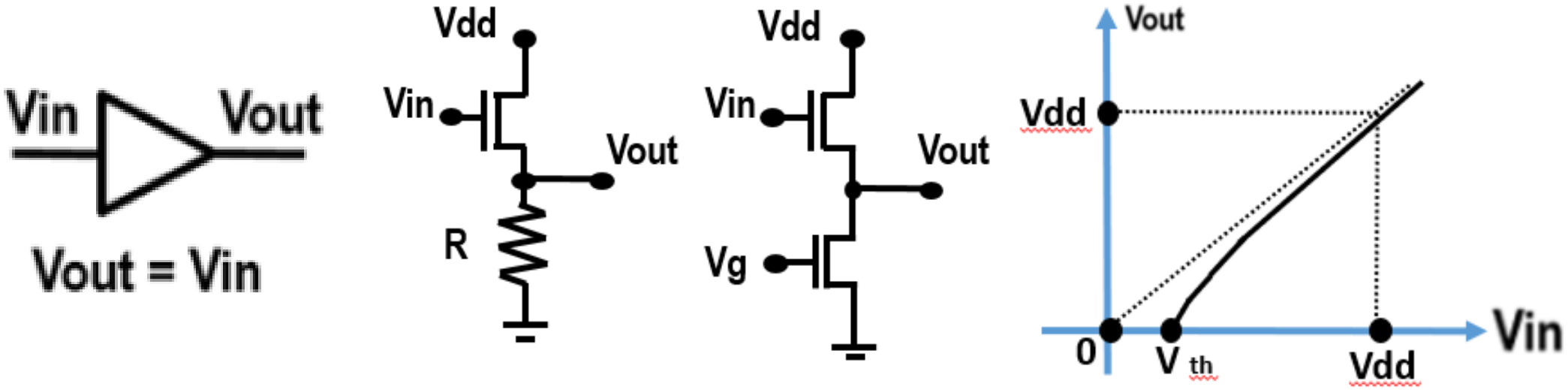
7 In Pixel Correlation Double Sampling (CDS) circuit

CDS processing typically consists of subtracting the reset nose components **VsigA(t)** of the SH(1) and SH(2) circuits from the integrated video signal output **VsigB(t)** obtained from the SH(3) circuit.



7 In Pixel Correlation Double Sampling (CDS) circuit

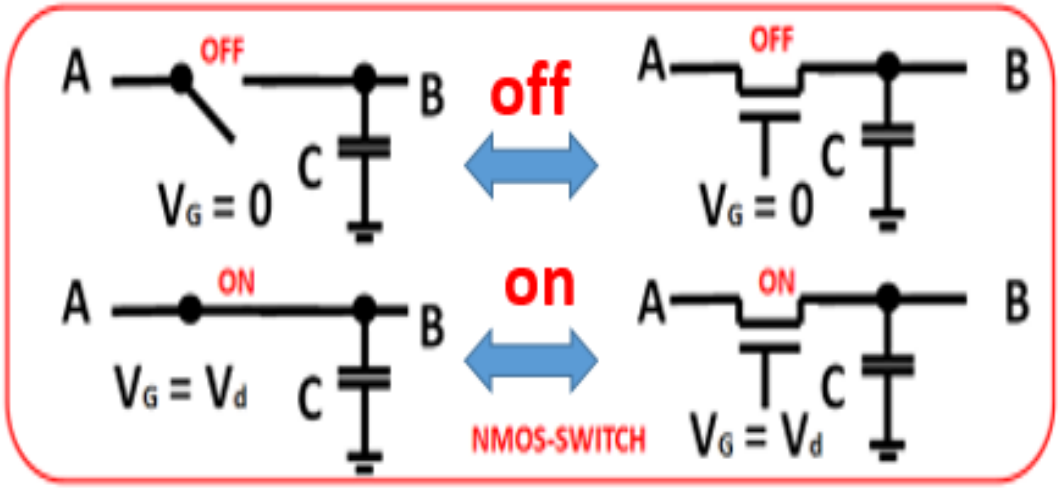
The noise reduction circuit for image sensors, now called as the correlated double sampling (CDS) circuit, worked very well not only for CCD image sensors but also specially for MOS image sensors which had serious column line fixed pattern noise and large CkT noises.

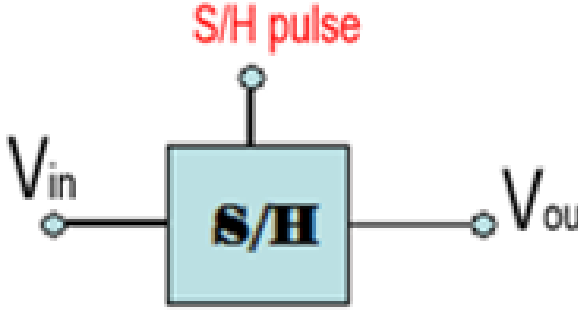


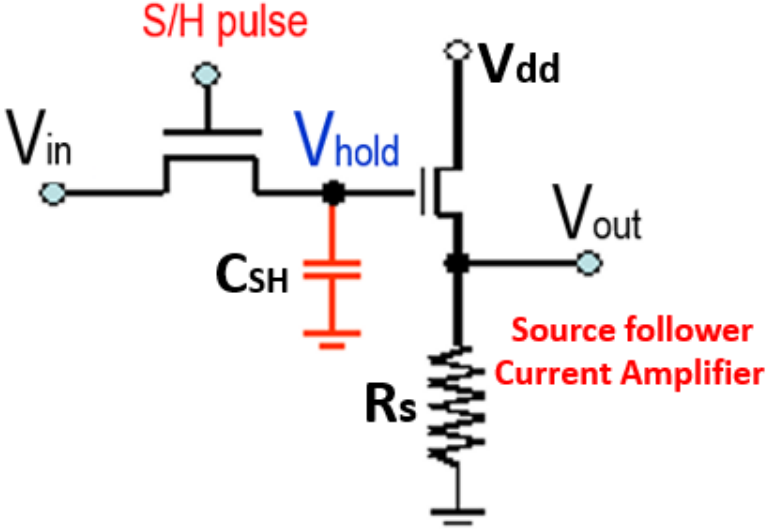
Source Follower Current Amplifier Circuit used in Sample Hold Circuit

7 In Pixel Correlation Double Sampling (CDS) circuit

The correlated double sampling (CDS) circuit was expected to reduce not only the clocking noise coupled by the parasitic oxide capacitance between the reset gate and the floating signal output diffusion but also the white noise, 1/f noise and CkT noise. But the truth was not so easy.



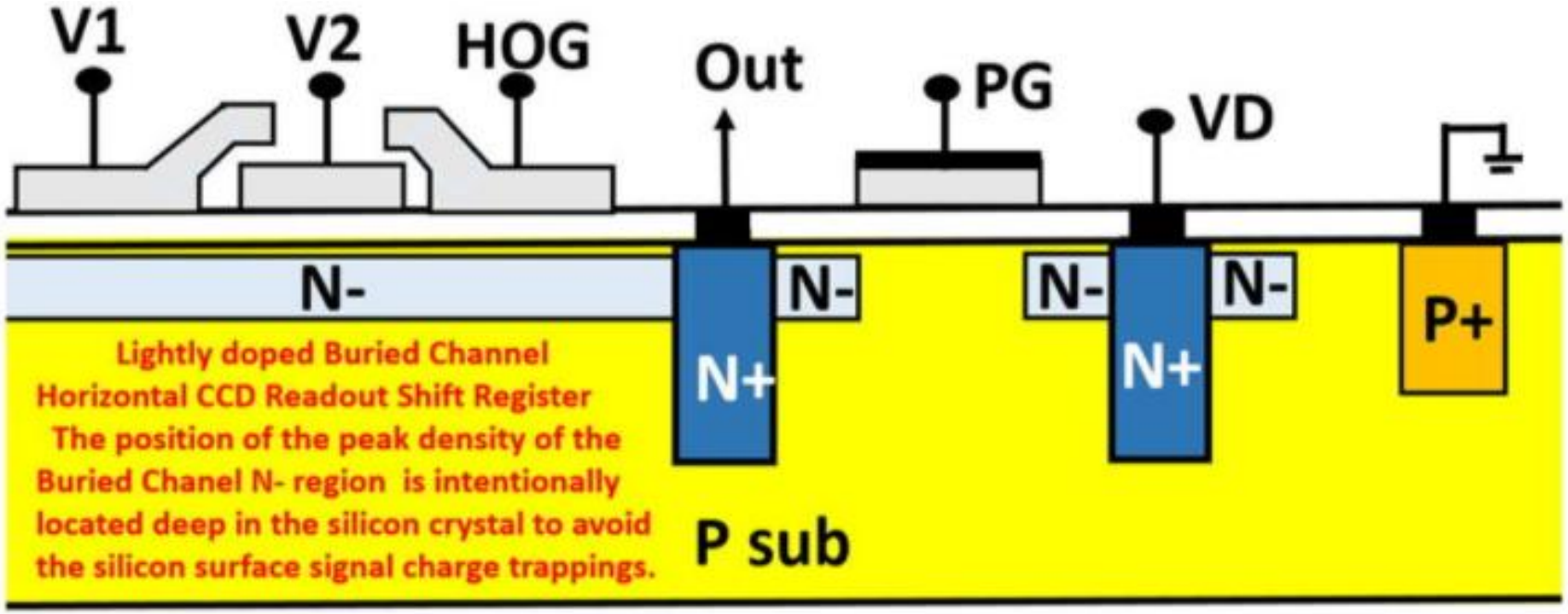




Sample Hold Circuit used in Correlated Double Sampling (CDS) circuit

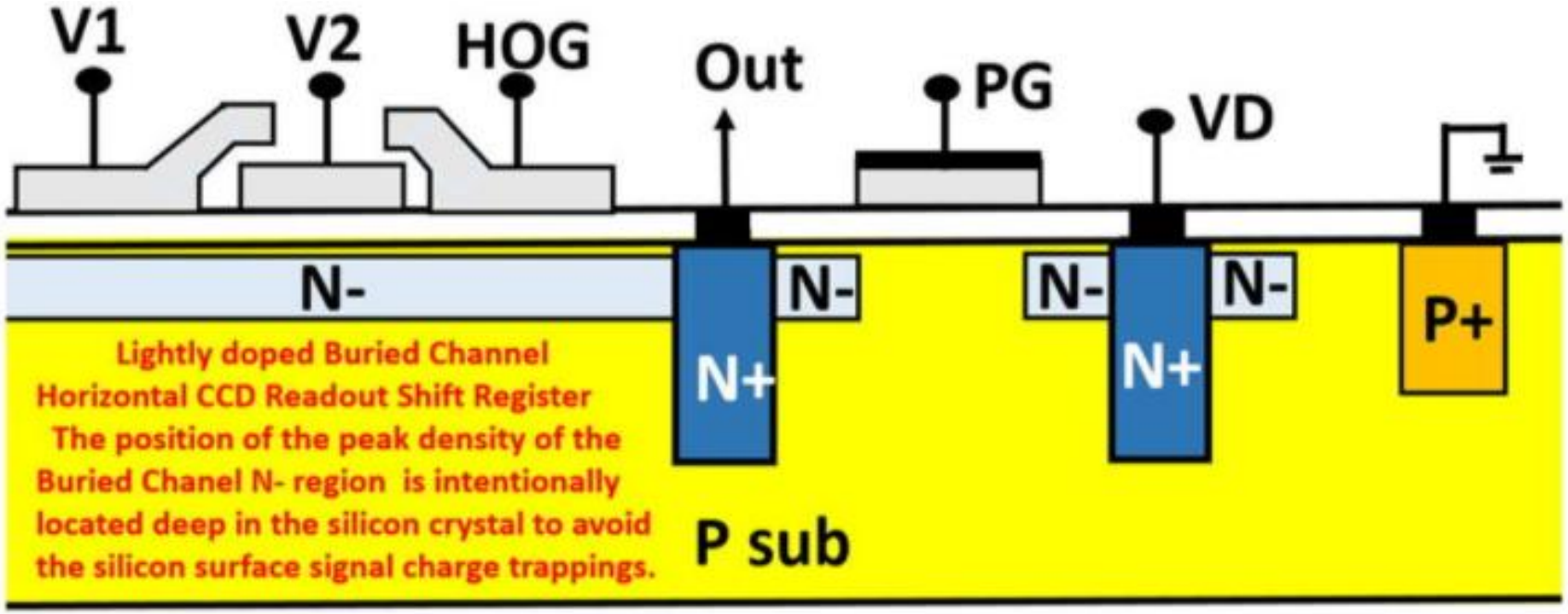
7 In Pixel Correlation Double Sampling (CDS) circuit

The 1/f noise was a serious problem. Originally the buried channel CCD was proposed to protect the photo signal charge from the semiconductor surface interface trapping site which is the cause of 1/f noise.



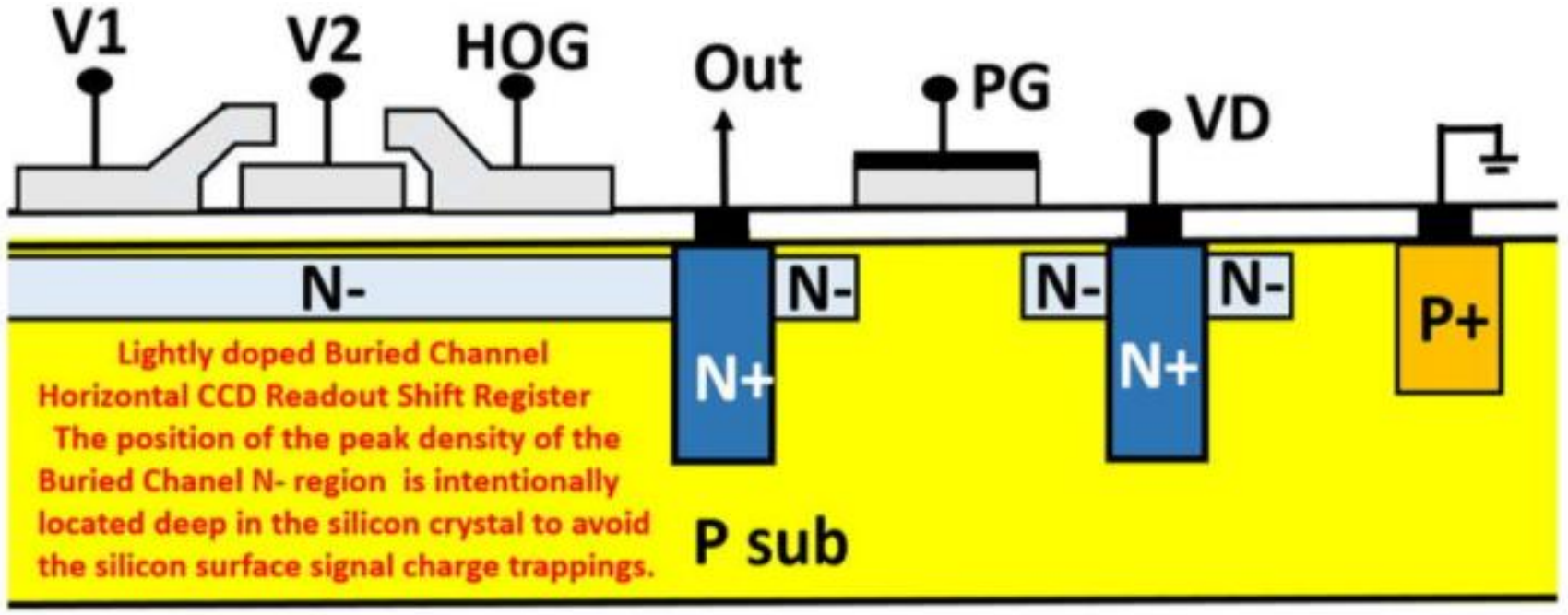
7 In Pixel Correlation Double Sampling (CDS) circuit

However, originally the horizontal output gate (HOG) and the pre charge reset gate (PG) both were of the surface channel MOS transistor type. And they did have the surface trap 1/f noise problem.



7 In Pixel Correlation Double Sampling (CDS) circuit

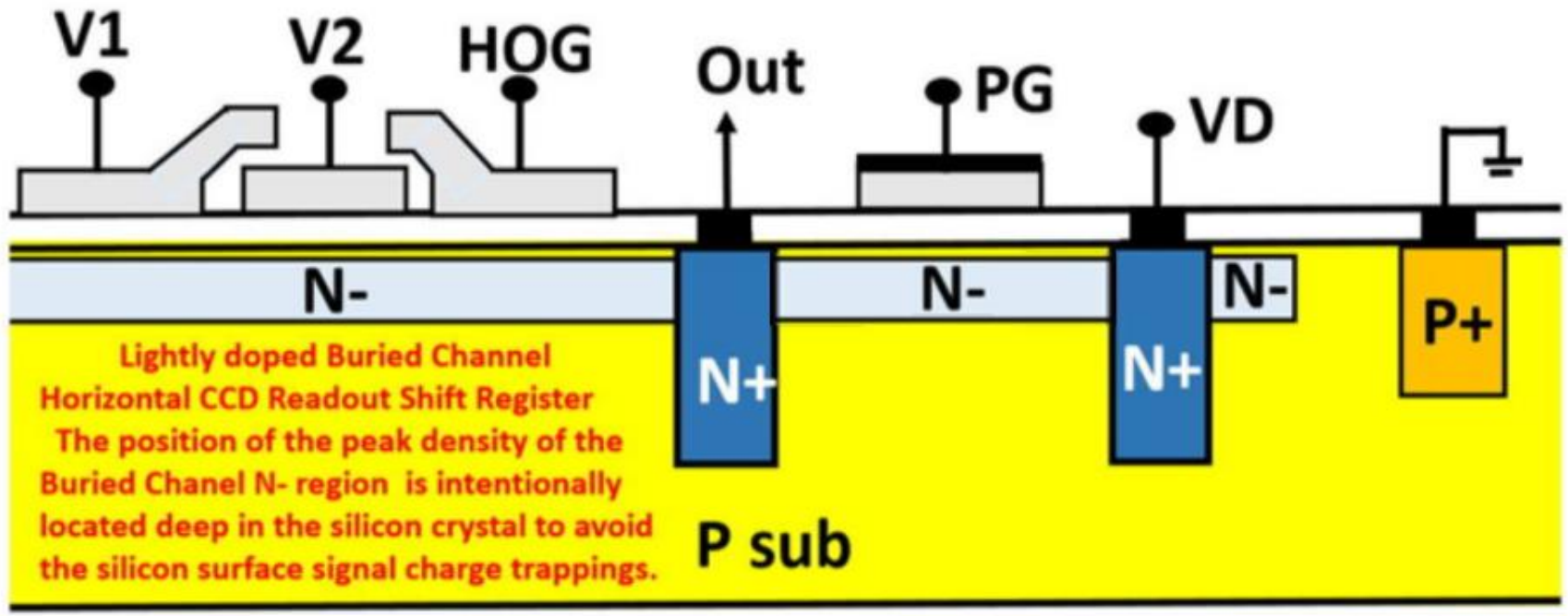
First the horizontal output gate (HOG) was made with the buried channel depletion mode MOS transistor type. And some decrease of the surface trap 1/f noise was observed, but not enough.



Lowly Doped Drain (LDD) MOS Pre-charge Reset Gate used in Sony CCD Image sensors unpublished works by Hagiwara at Sony in late 1970s.

7 In Pixel Correlation Double Sampling (CDS) circuit

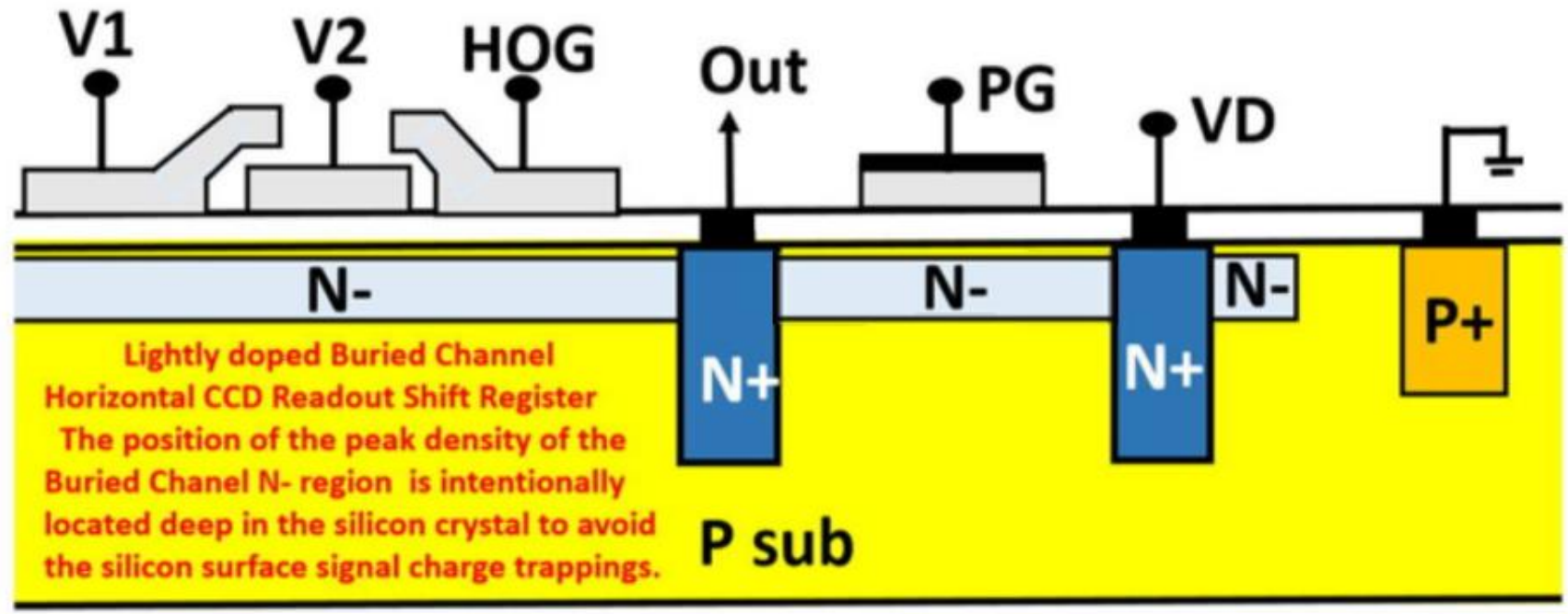
Then the pre charge reset gate (PG) was also made with the buried channel type depletion mode MOS transistor. And the surface trap 1/f noise was finally minimized as expected theoretically.



Lowly Doped Drain (LDD) MOS Pre-charge Reset Gate used in Sony CCD Image sensors unpublished works by Hagiwara at Sony in late 1970s.

7 In Pixel Correlation Double Sampling (CDS) circuit

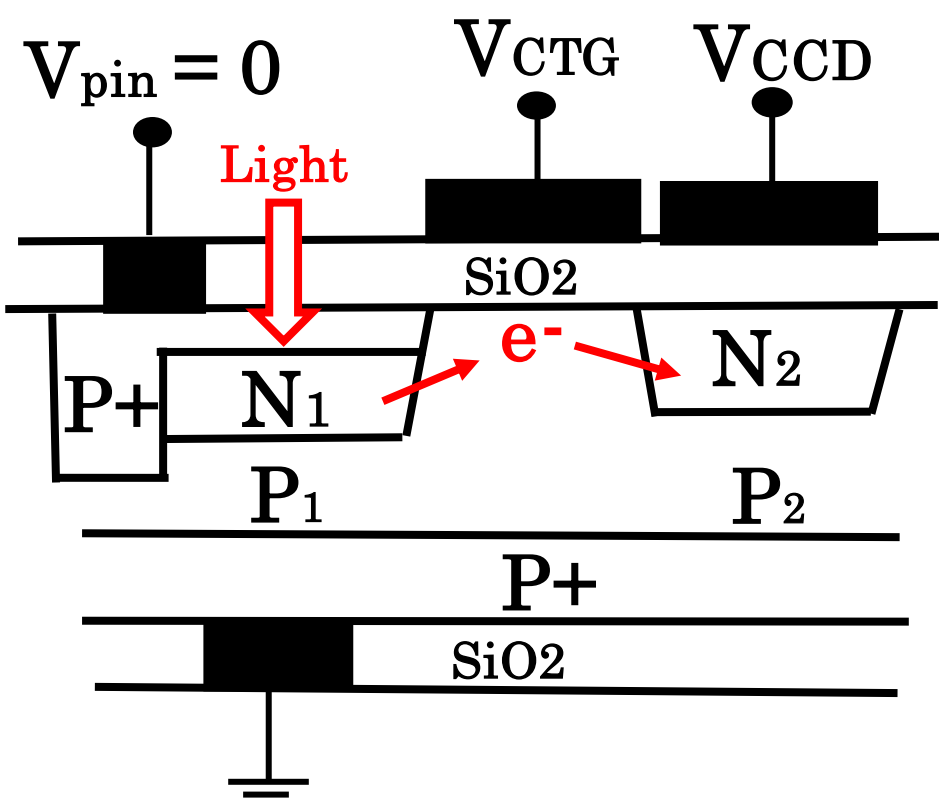
In the late 1970s, Sony(Hagiwara) needed the CCD clock frequency of NTSC 14.31818 MHz for the one chip CCD imager sensor operations. And a very large pre-charge clock swing and a very large drain voltage were required. Hagiwara at Sony used the lightly doped CCD buried channel N- layer also in the side regions of the pre-charge reset gate in order to avoid undesired punch thru effects. However, the lightly doped N- region was not self-aligned. But it worked well. Unpublished.

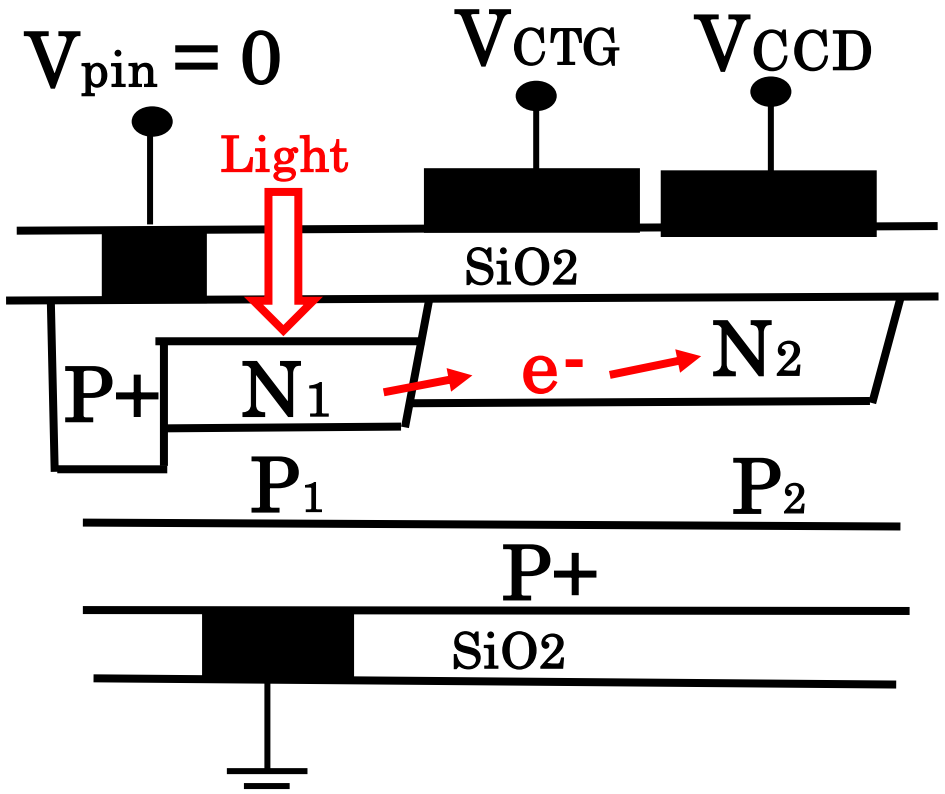


Lowly Doped Drain (LDD) MOS Pre-charge Reset Gate used in Sony CCD Image sensors unpublished works by Hagiwara at Sony in late 1970s.

7 In Pixel Correlation Double Sampling (CDS) circuit

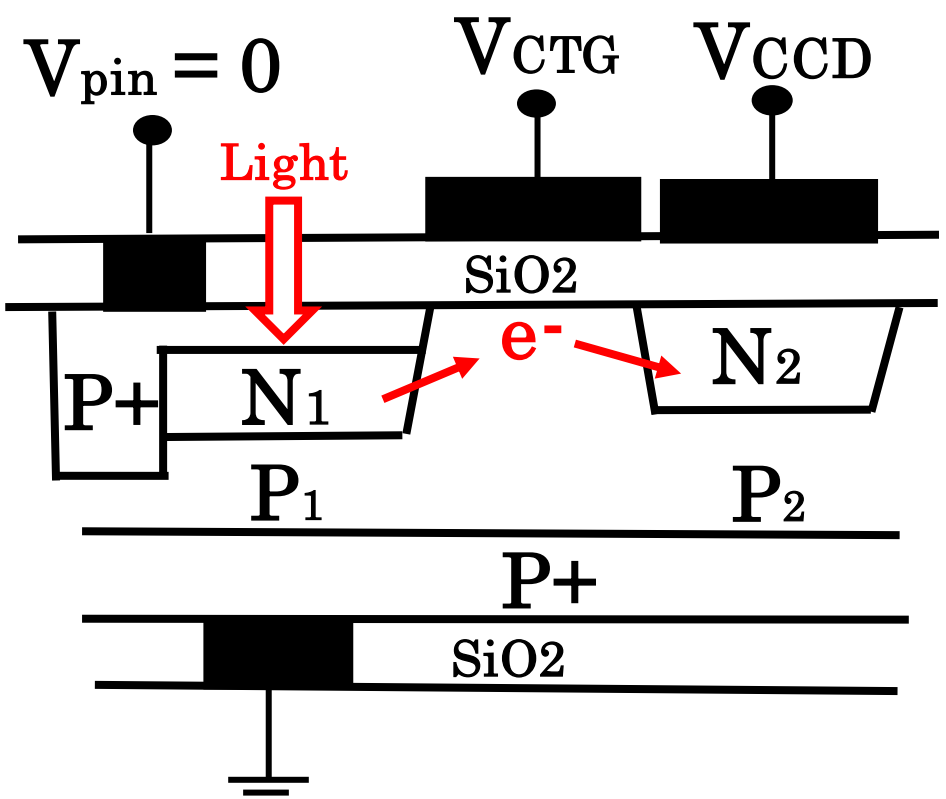
The signal charge must be protected from the surface charge trapping site completely. But the charge transfer gate (CTD) in pixel is also the surface channel type with the surface trap noise problem.

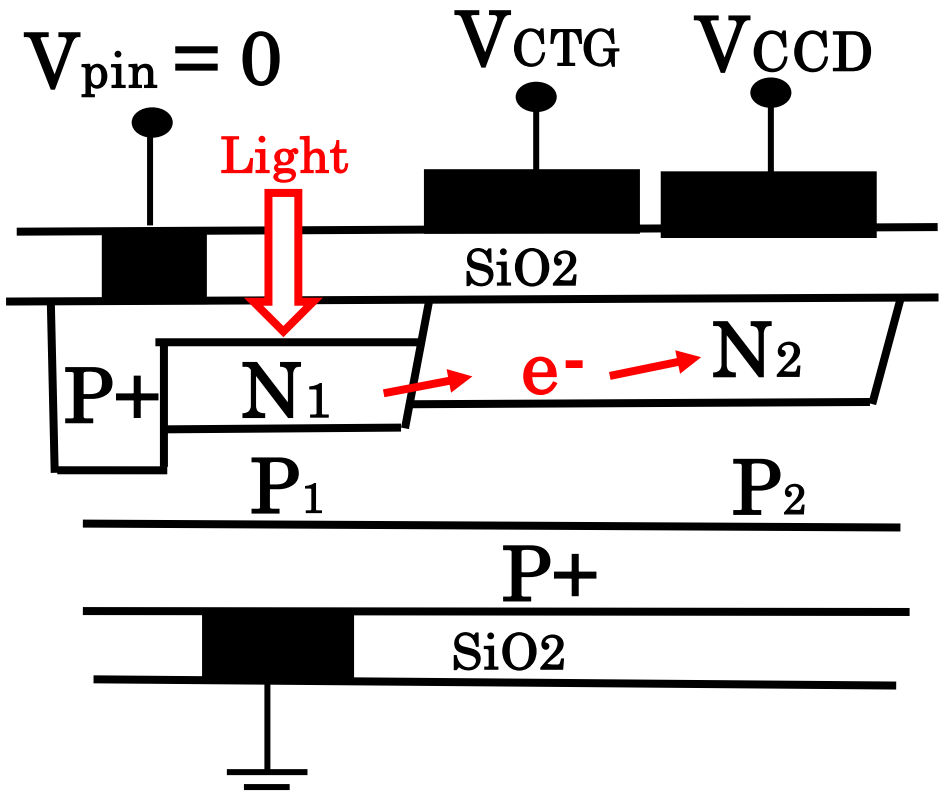




7 In Pixel Correlation Double Sampling (CDS) circuit

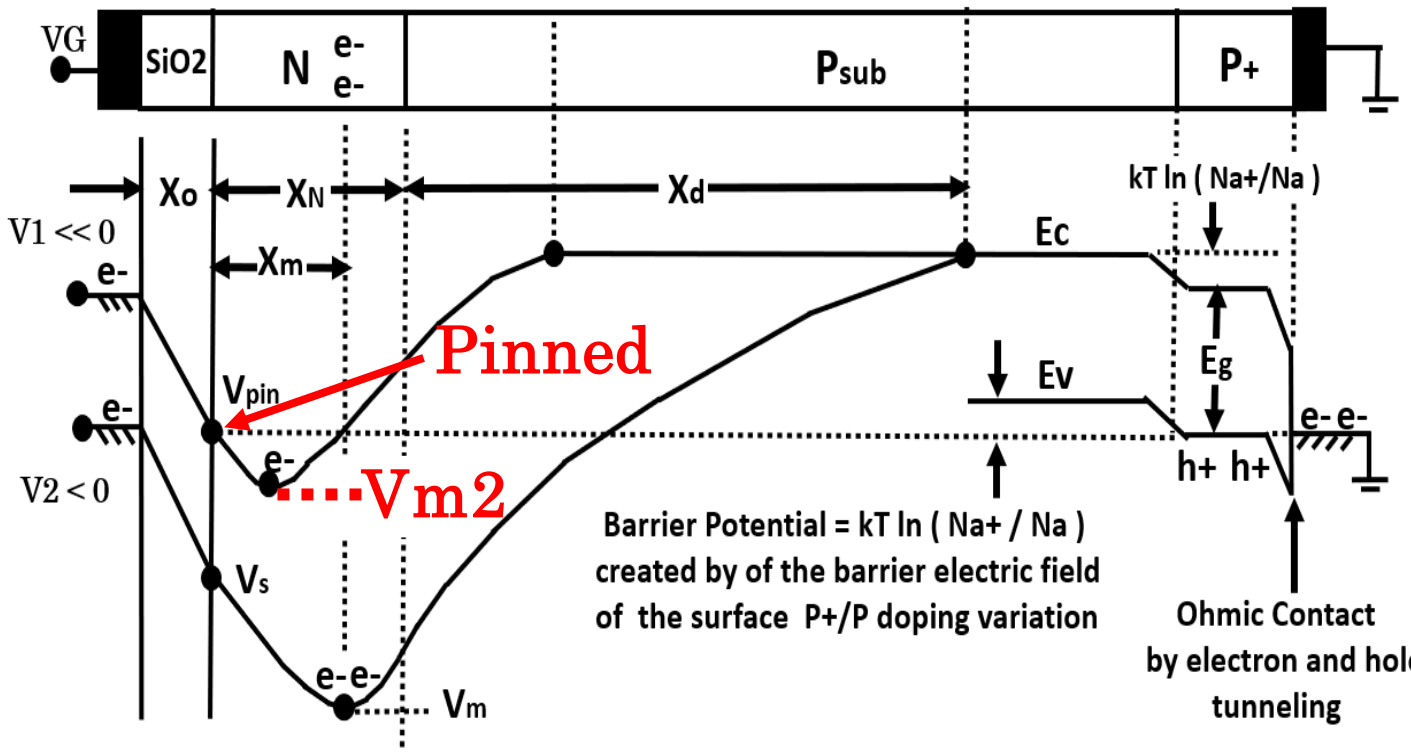
So the buried channel type BCCD/MOS transfer gate (CTD) was tried. But it did not work at the initial attempts.

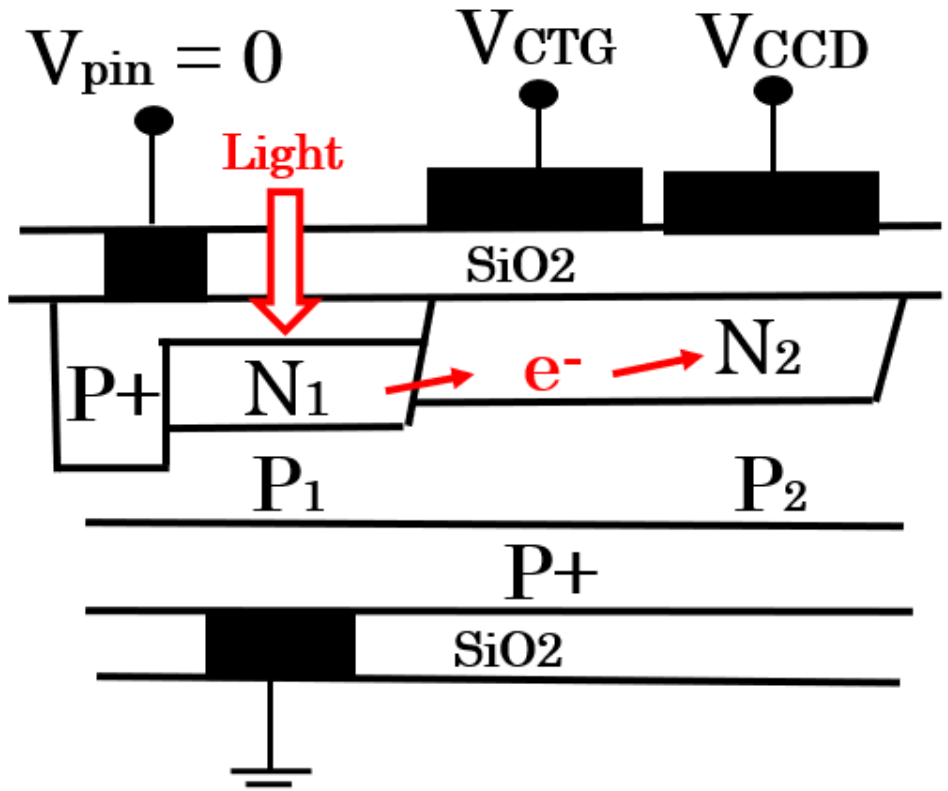




7 In Pixel Correlation Double Sampling (CDS) circuit

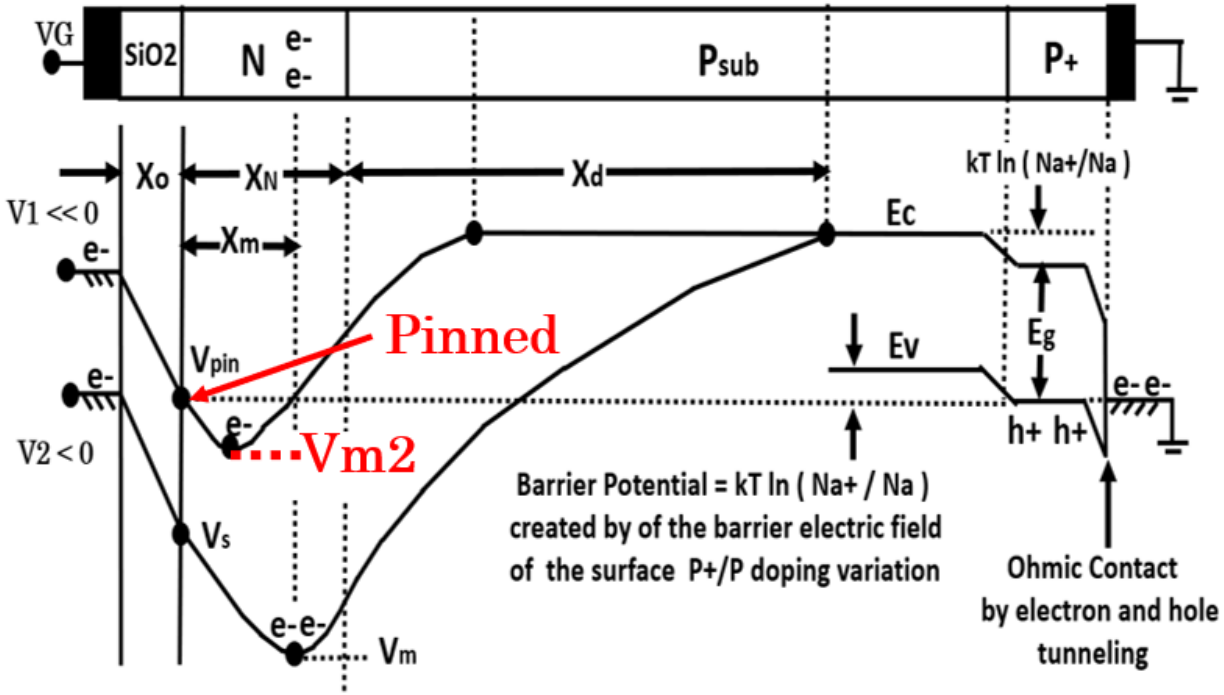
Following observation was responsible, the empty potential well Vm_2 of the buried channel under the charge transfer gate (CTG) is pinned and grounded when the CTG voltage becomes a large negative value.

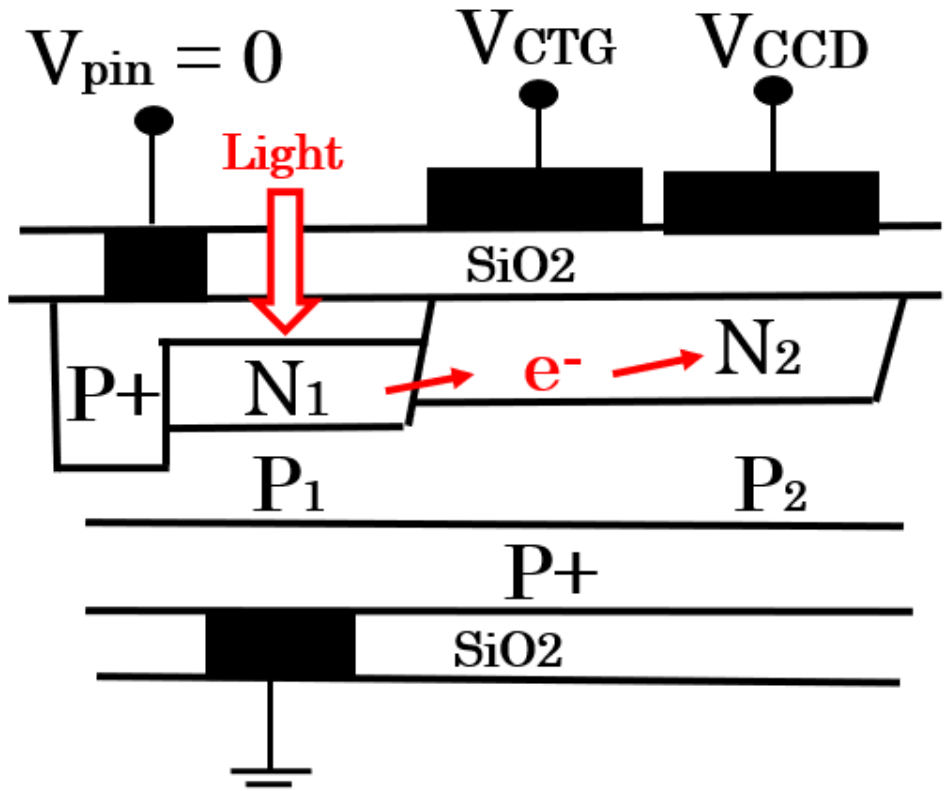




7 In Pixel Correlation Double Sampling (CDS) circuit

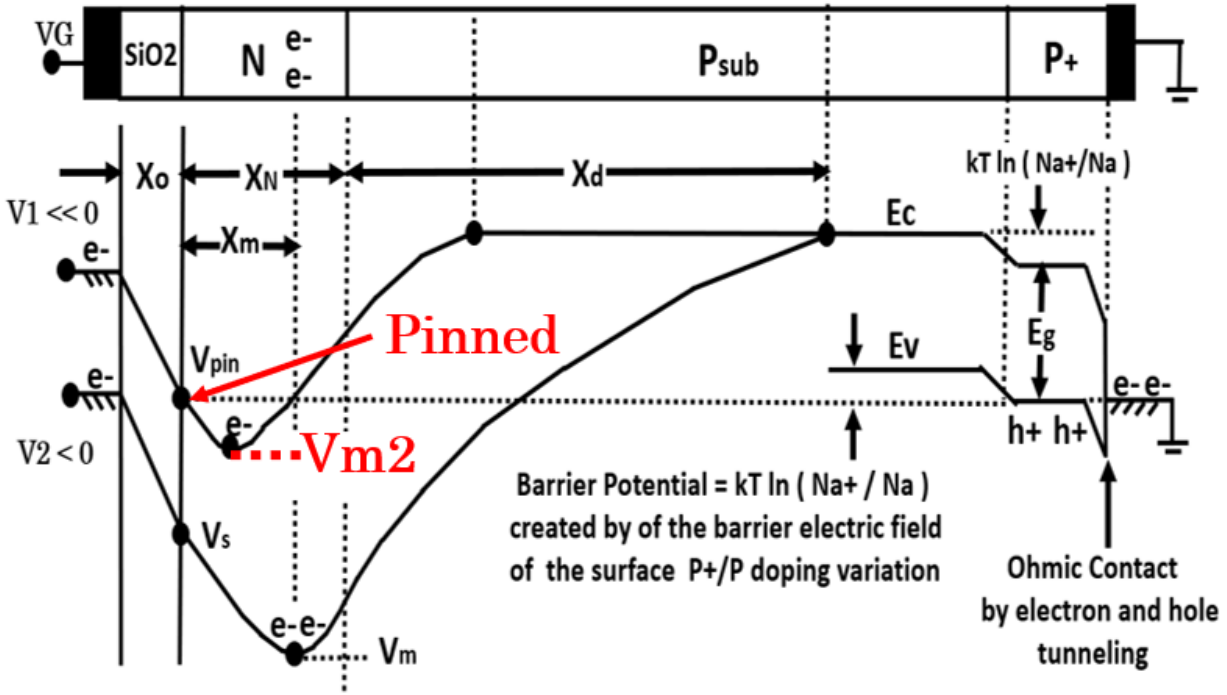
The semiconductor surface under the charge transfer gate (CTG) is inverted into the hole accumulation state and pinned to the ground potential by the accumulated hole majority carriers which were moved in from the adjacent heavily doped and grounded P+ channel stops.

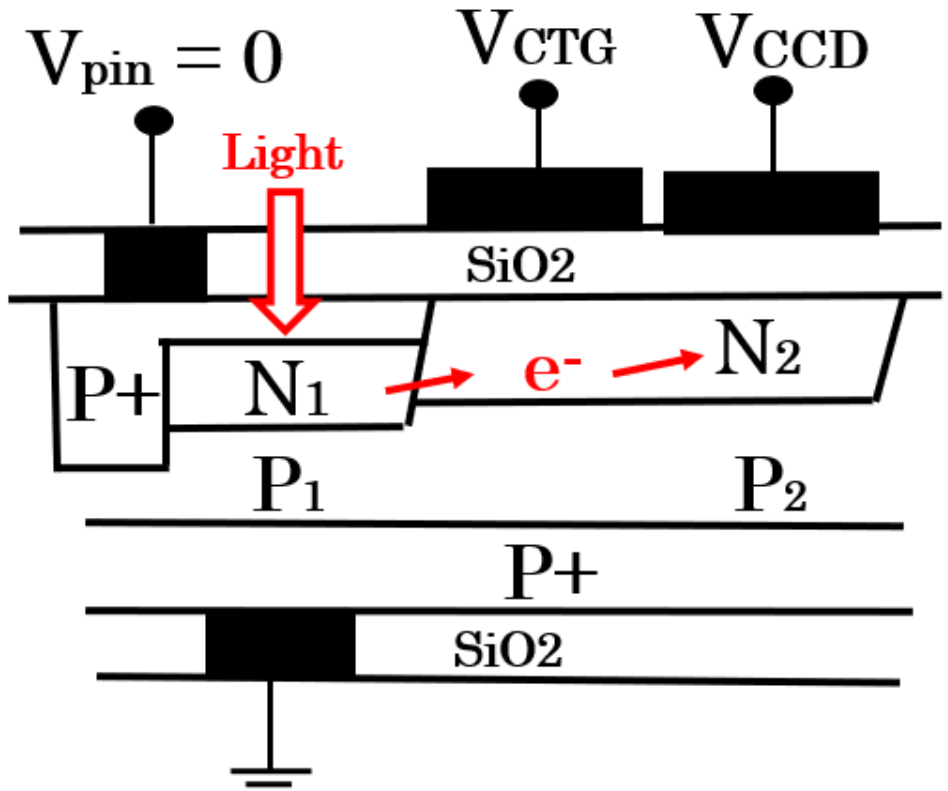




7 In Pixel Correlation Double Sampling (CDS) circuit

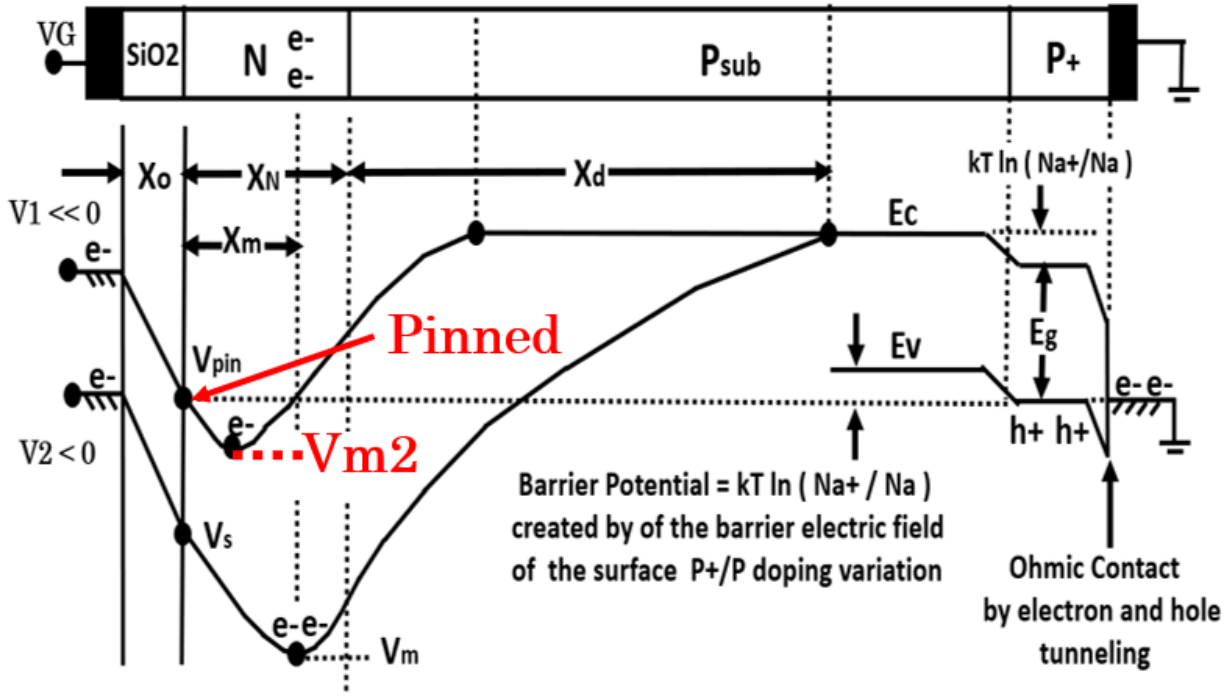
The pinned potential Vm_2 of the buried empty channel potential well under the charge transfer gate (CTG) will be always deeper than the pinned empty potential well Vm_1 of the P+N1+P1P+ double junction type Pinned Photodiode.

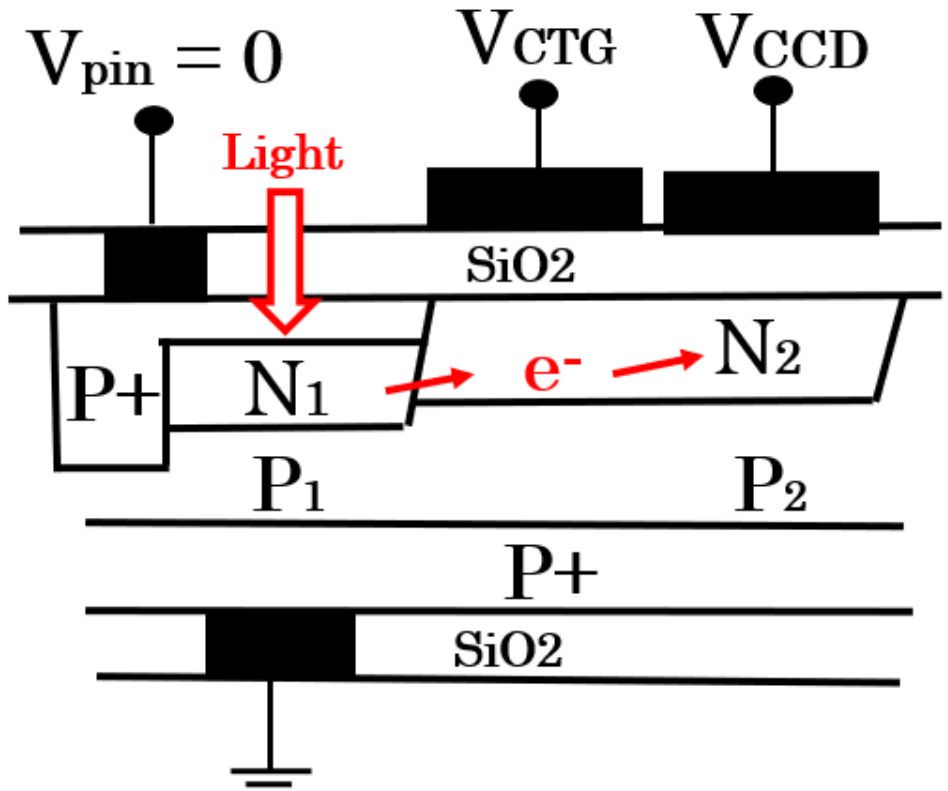




7 In Pixel Correlation Double Sampling (CDS) circuit

The charge transfer gate (CTG) cannot be kept closed during the photo charge integration time. The P+N1+P1P+ double junction type Pinned Photodiode does not serve as the photo charge storage in this case.





7 In Pixel Correlation Double Sampling (CDS) circuit

The governing equations to obtain the pinned minimum potential well Vm1 and Vm2 are identical since the surface potential Vs is pinned and grounded in both cases . We have Vs = Vs1 = Vs2 = 0 v.

$$Vm = \frac{Nd\,Xm^2}{2\varepsilon_{Si}}$$

$$Nd\,(Xd - Xm) = N_A\,Xp$$

$$Vs = Vpin = 0$$

$$Vm = \frac{Nd\,(Xd - Xm)^2}{2\varepsilon_{Si}} + \frac{N_A\,Xp^2}{2\varepsilon_{Si}} - \left\{ E_G + kT\ln\left(\frac{N_A^+}{N_A}\right)\right\}$$

Governing equations to obtain the pinned minimum well potential Vm.

7 In Pixel Correlation Double Sampling (CDS) circuit

Deleting the parameter of the depletion width Xp extended into the P silicon substrate, we obtain the following relationships between the pinned and buried minimum empty potential Vm and its depth Xm only.

$$Vm = \frac{Nd\,Xm^2}{2\varepsilon_{Si}}$$

$$Nd\,(Xd - Xm) = N_A\,Xp$$

$$Vs = Vpin = 0$$

$$Vm = \left\{1 + \frac{N_d}{N_A}\right\} \frac{Nd\,(Xd - Xm)^2}{2\varepsilon_{Si}} - \left\{E_G + kT\ln\left(\frac{N_A^+}{N_A}\right)\right\}$$

Governing equations to obtain the pinned minimum well potential Vm.

7 In Pixel Correlation Double Sampling (CDS) circuit

We first obtain the equation for the depth Xm of the minimum empty potential well in the buried N charge storage region under the silicon surface. The offset constant voltage of the silicon energy gap E_G and the barrier potential kT ln (N_A+/N_A) created the surface P+P Gaussian doping profile is denoted here as V_{offset}.

$$Vs = Vpin = 0$$

$$V_{offset} = E_G + kT \ln \left(\frac{N_A^+}{N_A} \right)$$

$$Qd = Nd\, Xd$$

$$Vm = \frac{Nd\, Xm^2}{2\varepsilon_{Si}} = \left\{ 1 + \frac{N_d}{N_A} \right\} \frac{Nd\,(Xd - Xm)^2}{2\varepsilon_{Si}} - V_{offset}$$

Governing equations to obtain the pinned minimum well potential Vm.

7 In Pixel Correlation Double Sampling (CDS) circuit

Further, introducing the salient physical parameter V_{QD} we obtain the following relationships for the depth Xm of the pinned and buried minimum empty potential well.

$$Vs = Vpin = 0$$

$$V_{offset} = E_G + kT \ln\left(\frac{N_A^+}{N_A}\right)$$

$$Qd = Nd\,Xd$$

$$V_{QD} = \frac{Q_d Xd}{2\varepsilon_{Si}}$$

$$\left\{\frac{Xm}{Xd}\right\}^2 = \left\{1 + \frac{Nd}{N_A}\right\}\left\{1 - \frac{Xm}{Xd}\right\}^2 - \frac{V_{offset}}{V_{QD}}$$

Governing equations to obtain the pinned minimum well potential Vm.

7 In Pixel Correlation Double Sampling (CDS) circuit

Then, solving the equation for the depth of the minimum empty potential well Xm under the silicon surface, we finally obtain the following result.

$$V_{offset} = E_G + kT \ln\left(\frac{N_A^+}{N_A}\right)$$

$$V_{QD} = \frac{Q_d X_d}{2\varepsilon_{Si}}$$

$$\frac{V_m}{V_{QD}} = \left\{\frac{X_m}{X_d}\right\}^2$$

$$\frac{X_m}{X_d} = \frac{1 + \frac{N_A}{N_d}\left\{1 - \frac{V_{offset}}{V_{QD}}\right\}}{\left\{1 + \frac{N_A}{N_d}\right\} + \sqrt{\left\{\frac{N_A}{N_d}\right\}\left\{1 + \frac{N_A}{N_d} + \frac{V_{offset}}{V_{QD}}\right\}}}$$

7 In Pixel Correlation Double Sampling (CDS) circuit

If we have Na<<Nd, we have Na/Nd goes to zero as Nd increases. And also V_{offset} / V_{QD} also goes to zero. Hence Xm / Xd goes to 1 as expected.

$$V_{offset} = E_G + kT \ln \left(\frac{N_A^+}{N_A} \right)$$

$$V_{QD} = \frac{Q_d X_d}{2 \varepsilon_{Si}}$$

$$\frac{V_m}{V_{QD}} = \left\{ \frac{X_m}{X_d} \right\}^2$$

$$\frac{X_m}{X_d} = \frac{1 + \frac{N_A}{N_d} \left\{ 1 - \frac{V_{offset}}{V_{QD}} \right\}}{\left\{ 1 + \frac{N_A}{N_d} \right\} + \sqrt{\left\{ \frac{N_A}{N_d} \right\} \left\{ 1 + \frac{N_A}{N_d} + \frac{V_{offset}}{V_{QD}} \right\}}}$$

7 In Pixel Correlation Double Sampling (CDS) circuit

Since the potential Vm of the pinned buried minimum empty well is expressed in terms of its depth Xm as shown below, we have the value of Vm goes to V_{QD}.

$$V_{offset} = E_G + kT \ln\left(\frac{N_A^+}{N_A}\right)$$

$$V_{QD} = \frac{Q_d X_d}{2\varepsilon_{Si}}$$

$$\frac{Vm}{V_{QD}} = \left\{\frac{Xm}{Xd}\right\}^2$$

$$\frac{Xm}{Xd} = \frac{1 + \frac{N_A}{N_d}\left\{1 - \frac{V_{offset}}{V_{QD}}\right\}}{\left\{1 + \frac{N_A}{N_d}\right\} + \sqrt{\left\{\frac{N_A}{N_d}\right\}\left\{1 + \frac{N_A}{N_d} + \frac{V_{offset}}{V_{QD}}\right\}}}$$

7 In Pixel Correlation Double Sampling (CDS) circuit

If we have Na<<Nd, as Nd increases, we have Na / Nd goes to zero and also Voffset / V_{QD} also goes to zero. Hence Xm / Xd goes to 1 as expected.

$$V_{offset} = E_G + kT \ln\left(\frac{N_A^+}{N_A}\right)$$

$$V_{QD} = \frac{Q_d X_d}{2\varepsilon_{Si}}$$

$$\frac{Vm}{V_{QD}} = \left\{\frac{Xm}{Xd}\right\}^2$$

$$\frac{Xm}{Xd} = \frac{1 + \frac{N_A}{N_d}\left\{1 - \frac{V_{offset}}{V_{QD}}\right\}}{\left\{1 + \frac{N_A}{N_d}\right\} + \sqrt{\left\{\frac{N_A}{N_d}\right\}\left\{1 + \frac{N_A}{N_d} + \frac{V_{offset}}{V_{QD}}\right\}}}$$

7 In Pixel Correlation Double Sampling (CDS) circuit

It is easily misunderstood that the doping level Nd of the buried N region must be low enough in order to be completely depleted and at the same time to keep the buried pinned empty minimum potential Vm at a practical and low value.

$$V_{offset} = E_G + kT \ln\left(\frac{N_A^+}{N_A}\right)$$

$$V_{QD} = \frac{Q_d X_d}{2\varepsilon_{Si}}$$

$$\frac{V_m}{V_{QD}} = \left\{\frac{X_m}{X_d}\right\}^2$$

$$\frac{X_m}{X_d} = \frac{1 + \frac{N_A}{N_d}\left\{1 - \frac{V_{offset}}{V_{QD}}\right\}}{\left\{1 + \frac{N_A}{N_d}\right\} + \sqrt{\left\{\frac{N_A}{N_d}\right\}\left\{1 + \frac{N_A}{N_d} + \frac{V_{offset}}{V_{QD}}\right\}}}$$

7 In Pixel Correlation Double Sampling (CDS) circuit

But the truth is not so. Note that the doping level Nd of the buried charge storage region does not have to be low if we have the Qd and X_d product kept small enough.

$$V_{offset} = E_G + kT \ln\left(\frac{N_A^+}{N_A}\right)$$

$$V_{QD} = \frac{Q_d X_d}{2\varepsilon_{Si}}$$

$$\frac{Vm}{V_{QD}} = \left\{\frac{Xm}{Xd}\right\}^2$$

$$\frac{Xm}{Xd} = \frac{1 + \frac{N_A}{Nd}\left\{1 - \frac{V_{offset}}{V_{QD}}\right\}}{\left\{1 + \frac{N_A}{Nd}\right\} + \sqrt{\left\{\frac{N_A}{Nd}\right\}\left\{1 + \frac{N_A}{Nd} + \frac{V_{offset}}{V_{QD}}\right\}}}$$

7 In Pixel Correlation Double Sampling (CDS) circuit

We may have a very heavily doped +Nd with a large value of Qd of the buried charge storage region but with a narrow width Xd. In this way, we still can keep the value of V_{QD} unchanged and have a rasonable value.

$$V_{offset} = E_G + kT \ln\left(\frac{N_A^+}{N_A}\right)$$

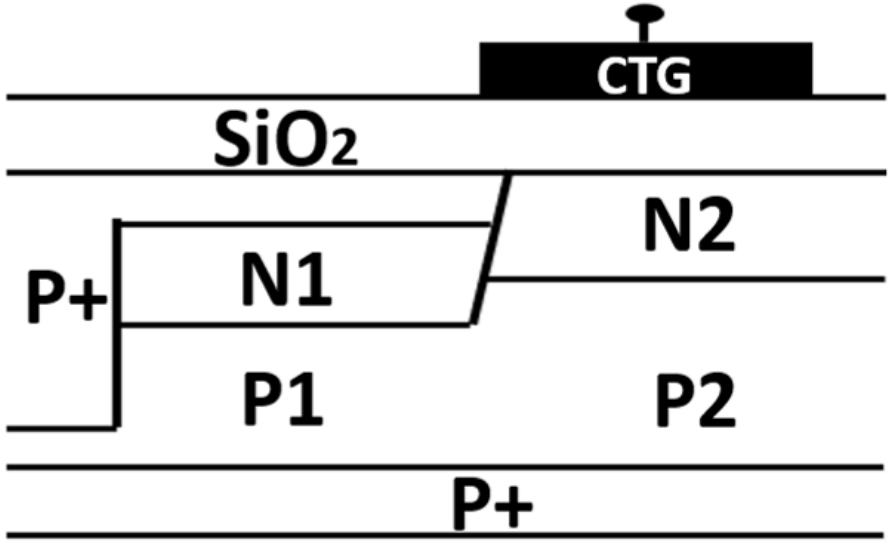
$$V_{QD} = \frac{Q_d X_d}{2\varepsilon_{Si}}$$

$$\frac{Vm}{V_{QD}} = \left\{\frac{Xm}{Xd}\right\}^2$$

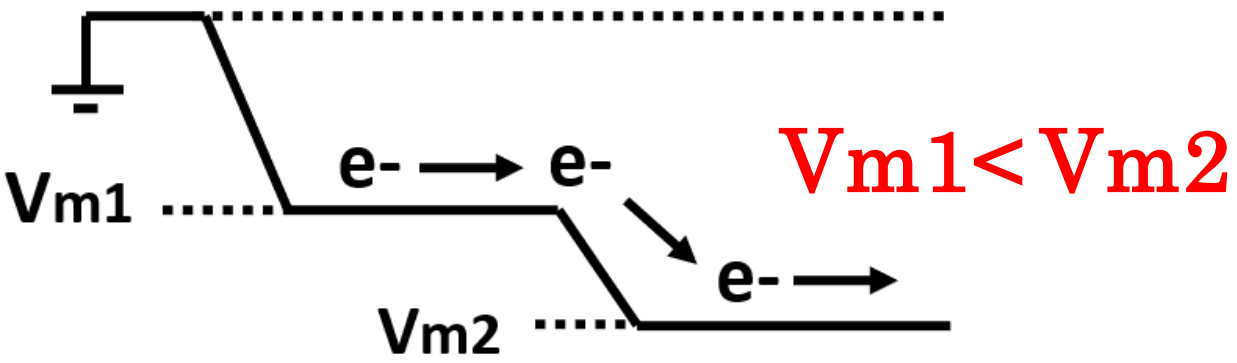
$$\frac{Xm}{Xd} = \frac{1 + \frac{N_A}{N_d}\left\{1 - \frac{V_{offset}}{V_{QD}}\right\}}{\left\{1 + \frac{N_A}{N_d}\right\} + \sqrt{\left\{\frac{N_A}{N_d}\right\}\left\{1 + \frac{N_A}{N_d} + \frac{V_{offset}}{V_{QD}}\right\}}}$$

7 In Pixel Correlation Double Sampling (CDS) circuit

The total dose Qd1 of the P+N1P1P+ junction Pinned Photodiode has a lower value than the total dose Qd2 of the buried CCD/MOS N2P2P+ junction channel. That is, QD1 < QD2 and Vm1 < Vm2.

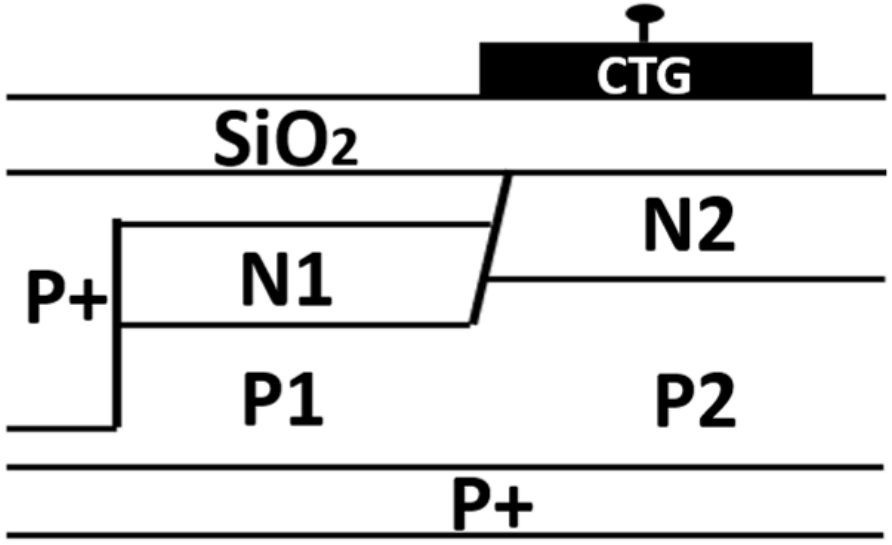


$$Qd1 = N_1 X_{d1} < Qd2 = N_2 X_{d2}$$

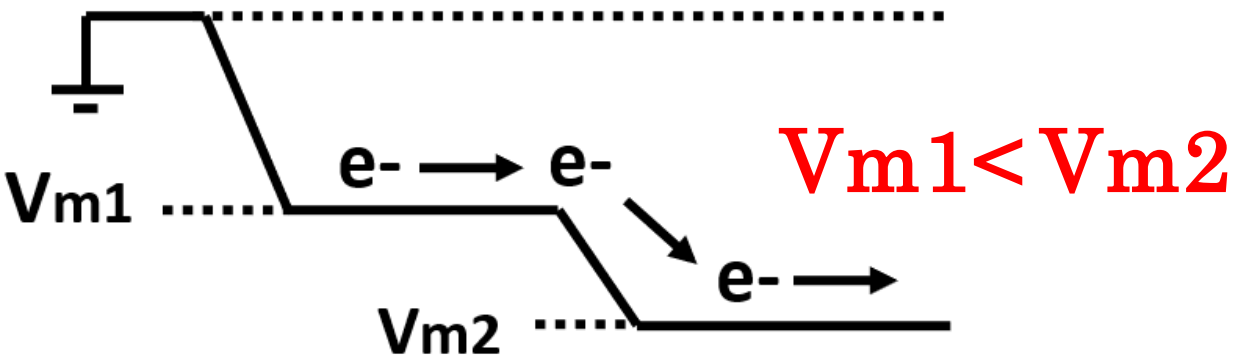


7 In Pixel Correlation Double Sampling (CDS) circuit

The channel potential Vm2 is deeper than the empty potential well Vm1. And this is why the buried channel charge transfer gate cannot be closed completely to store the photo charge in the Pinned Buried Empty Potential Well Vm1 properly during the photo charge integration time.



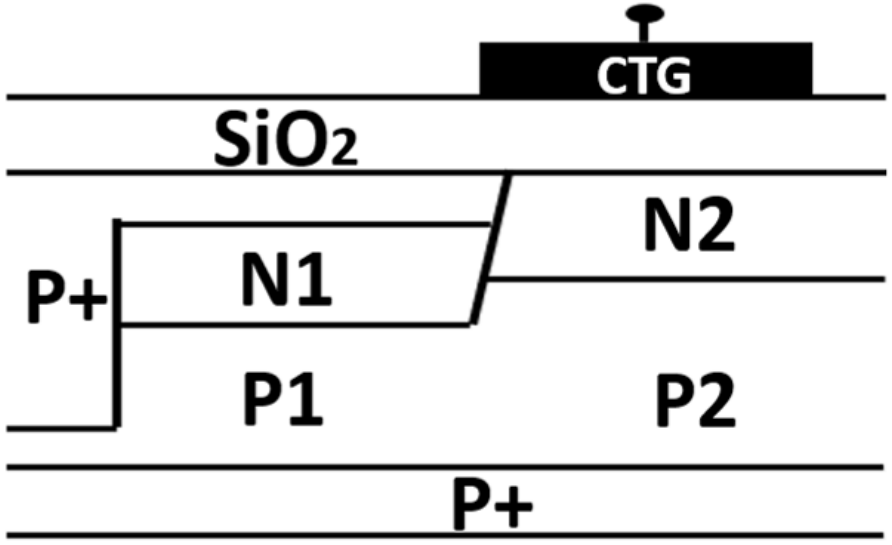
$$Qd1 = N1\,Xd1 < Qd2 = N2\,Xd2$$



7 In Pixel Correlation Double Sampling (CDS) circuit

However, the proper photo charge integration time can be achieved by implanting the extra dosage Qd1 > Qd2 by the self aligned ion implantation masked by the charge transfer gate (CTG). Then we have Vm1 < Vm2.

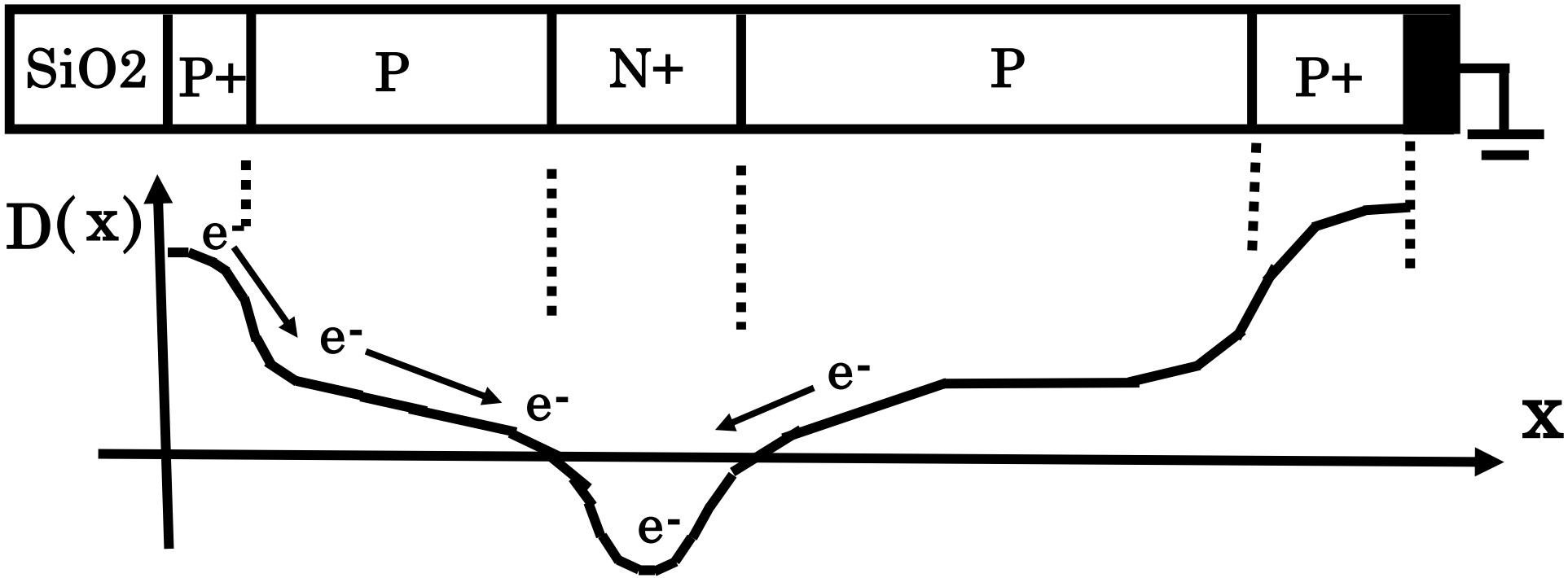
The signal charge is then protected from surface trapping sites completely.



$$Qd1 = N1\,Xd1 > Qd2 = N2\,Xd2$$

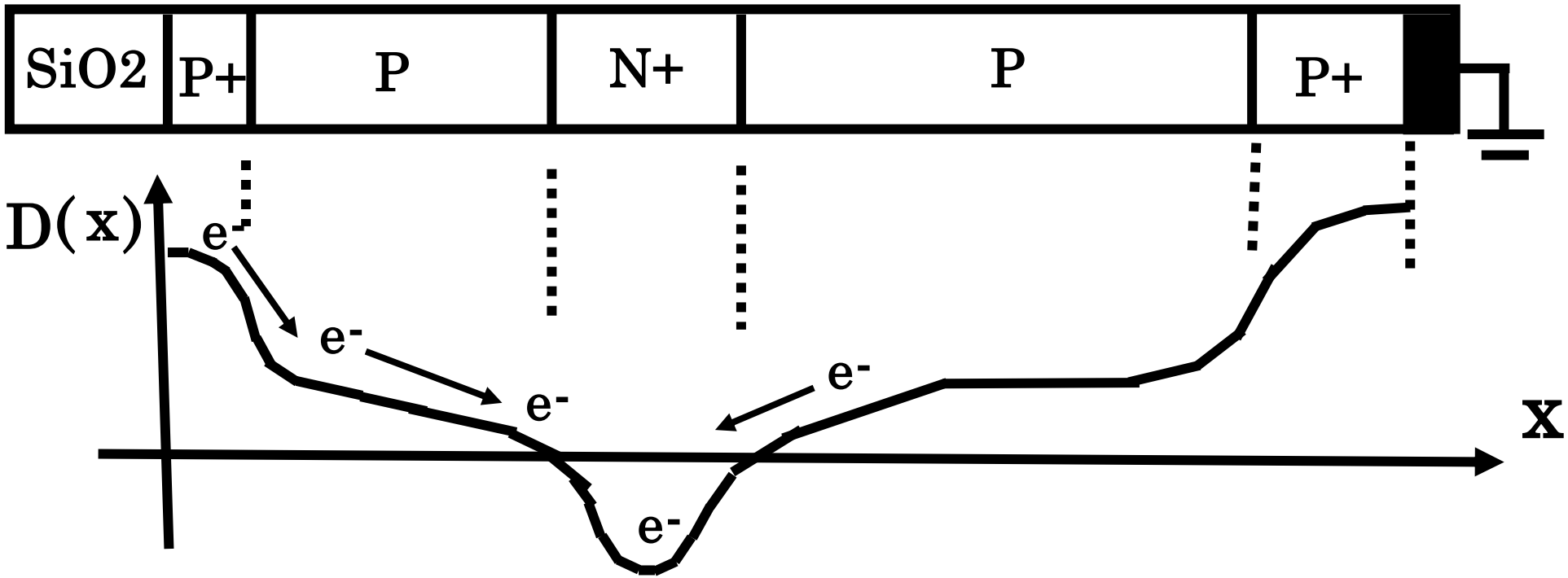
7 In Pixel Correlation Double Sampling (CDS) circuit

The P+NP double junction type Pinned Buried Photodiode proposed in 1975 by Hagiwara actually has the P+P surface Gaussian doping profile. It was a natural result of the regular surface ion implantation techniques.



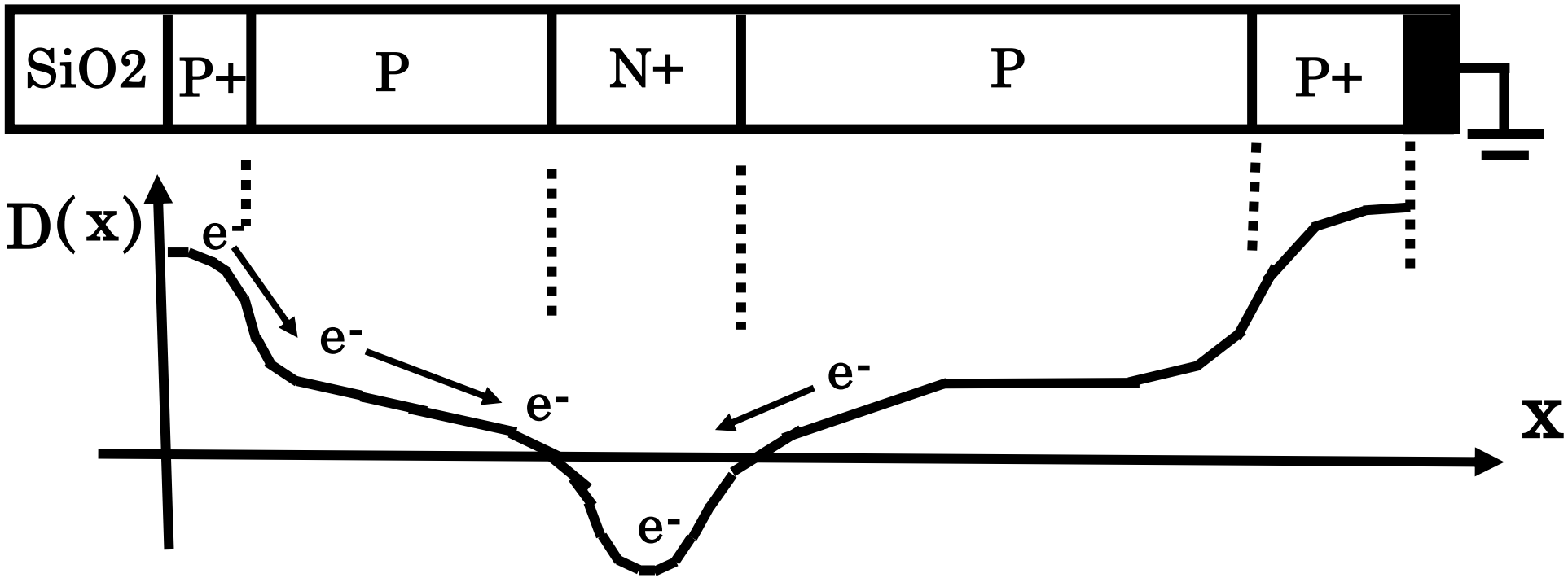
7 In Pixel Correlation Double Sampling (CDS) circuit

On the other hand, the pinned buried N+ region was implanted with the peak doping position located in the deep semiconductor substrate, away from the surface 1/f trapping sites to protect the signal charge.



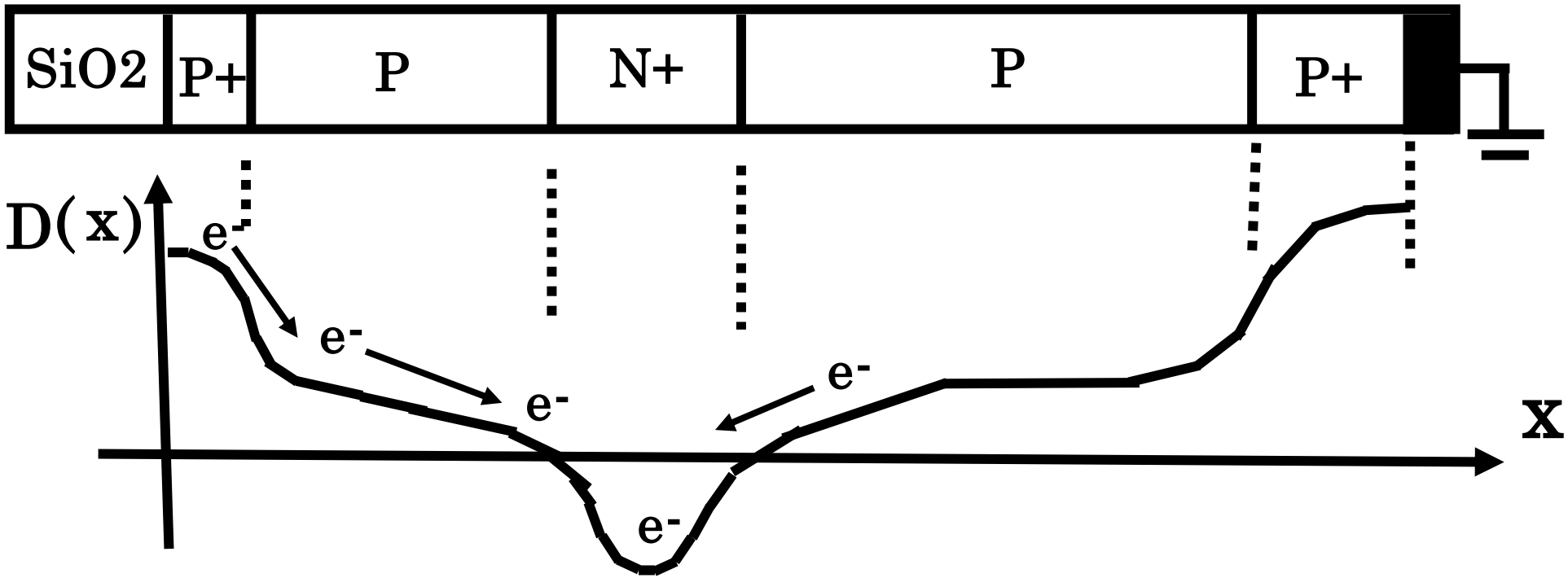
7 In Pixel Correlation Double Sampling (CDS) circuit

The width Xd was designed to be narrow while the peak dose level Nd of the buried charge storage region has a freedom to be heavily doped while keeping the total dose Qd = Xd Nd to be a constant value.



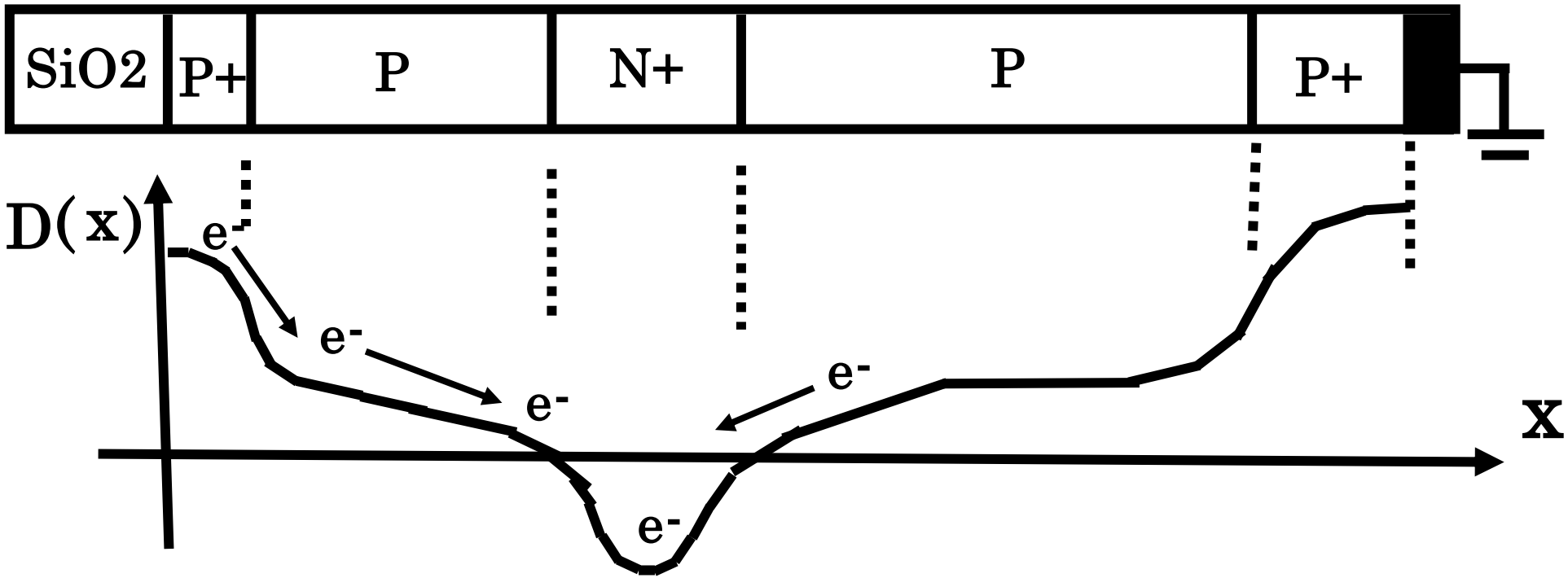
7 In Pixel Correlation Double Sampling (CDS) circuit

The pinned buried N storage region is placed quite far away from the silicon surface protecting the photo charge from being trapped in the surface trap centers which is the cause of the undesired 1/f noise.



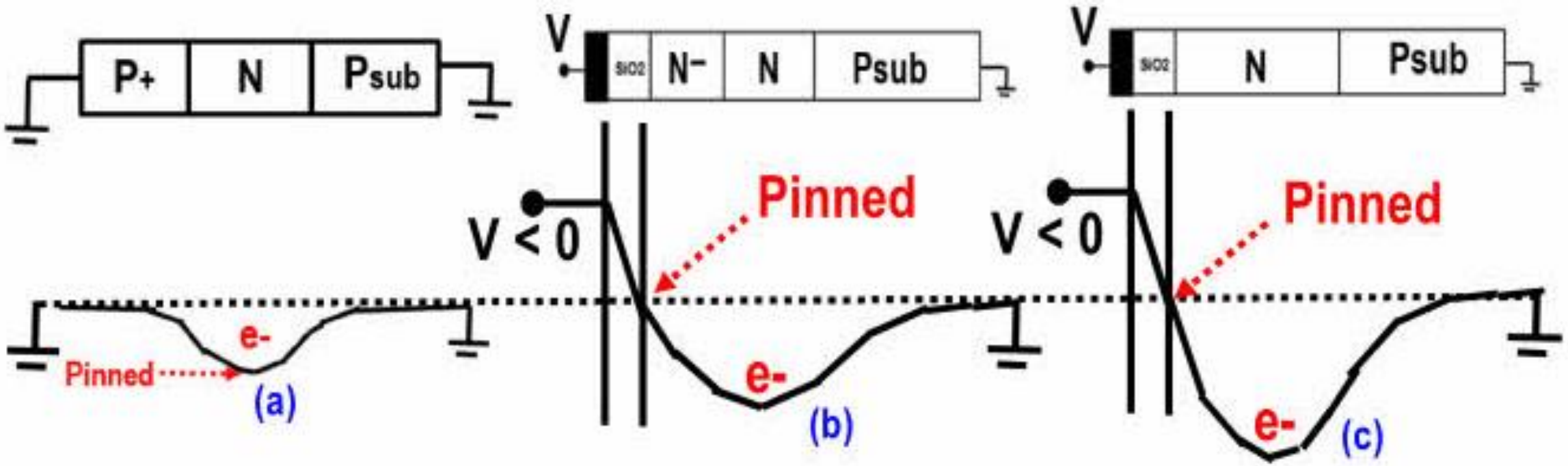
7 In Pixel Correlation Double Sampling (CDS) circuit

The P+P surface Gaussian doping variation creates the surface barrier potential (kT) ln (P+ / P) which enhances the photo electron hole pair generation at the semiconductor surface.



7 In Pixel Correlation Double Sampling (CDS) circuit

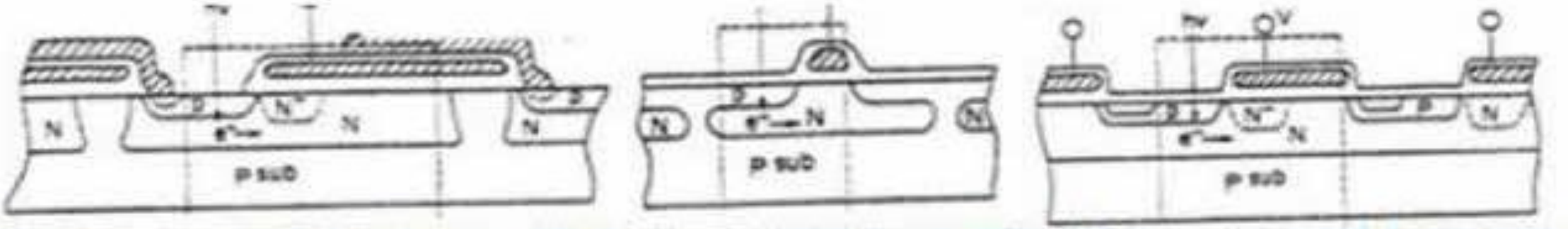
Even though the gate voltage V < 0 is set at a strong negative value , the silicon surface potential will be in the hole accumulation condition with the Pinned grounded voltage level. The buried channel CCD potentials (b) and (c) are always deeper than the Pinned Empty Potential (a) of the Pinned Photodiode.



7 In Pixel Correlation Double Sampling (CDS) circuit

Besides the CDS circuit approach, the buried channel process design effort and the Pinned Buried Photodiode device design effort are also diligent noise reduction efforts performed for many years to realize the high performance solid state image sensors.

.



7 In Pixel Correlation Double Sampling (CDS) circuit

Besides the CDS circuit approach, the buried channel process design effort and the Pinned Buried Photodiode device design effort are also diligent noise reduction efforts performed for many years to realize the high performance solid state image sensors.

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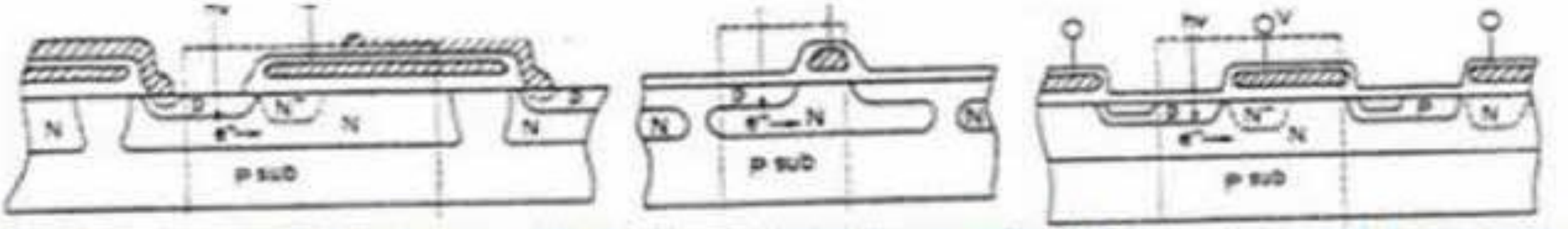
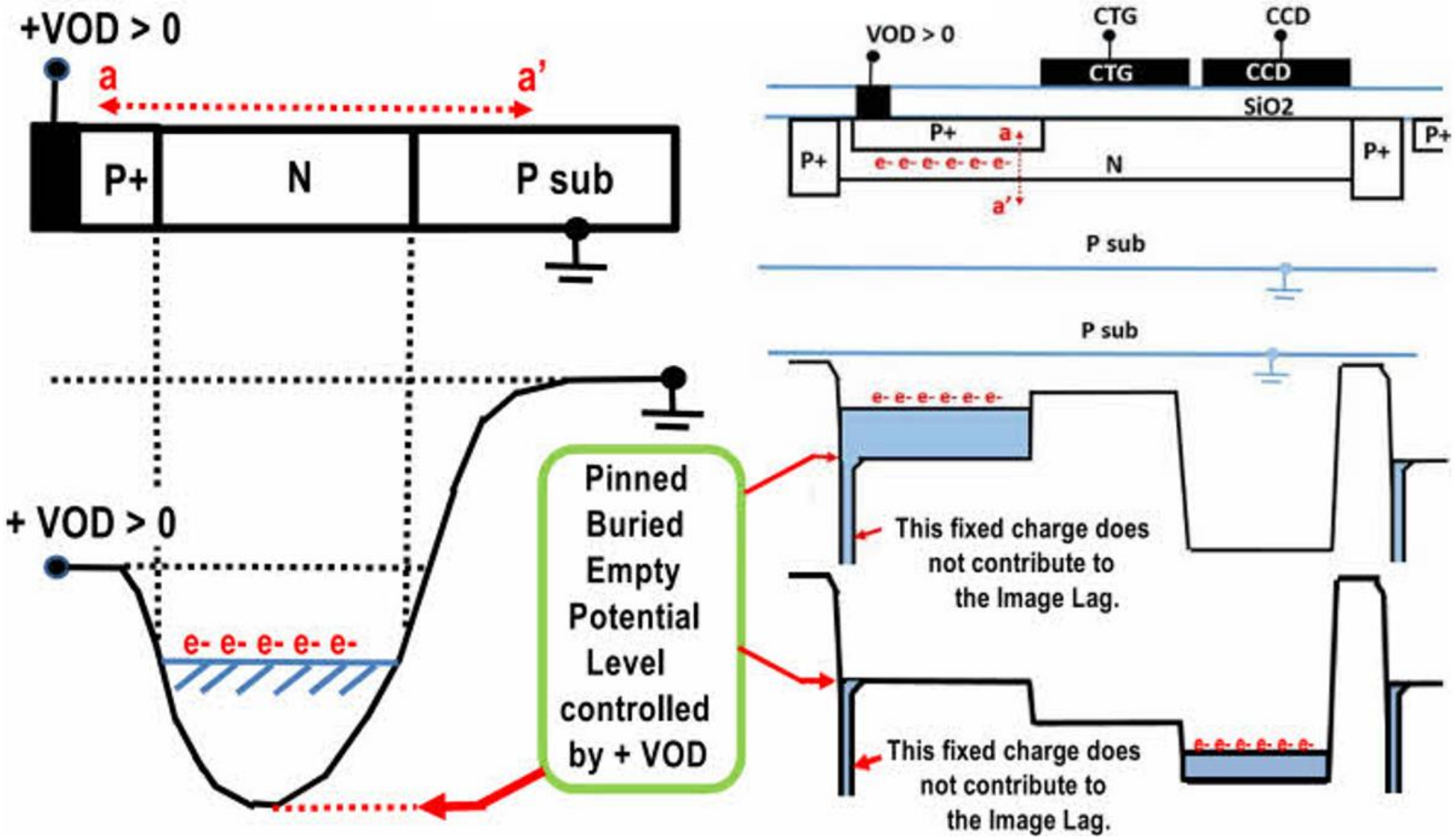
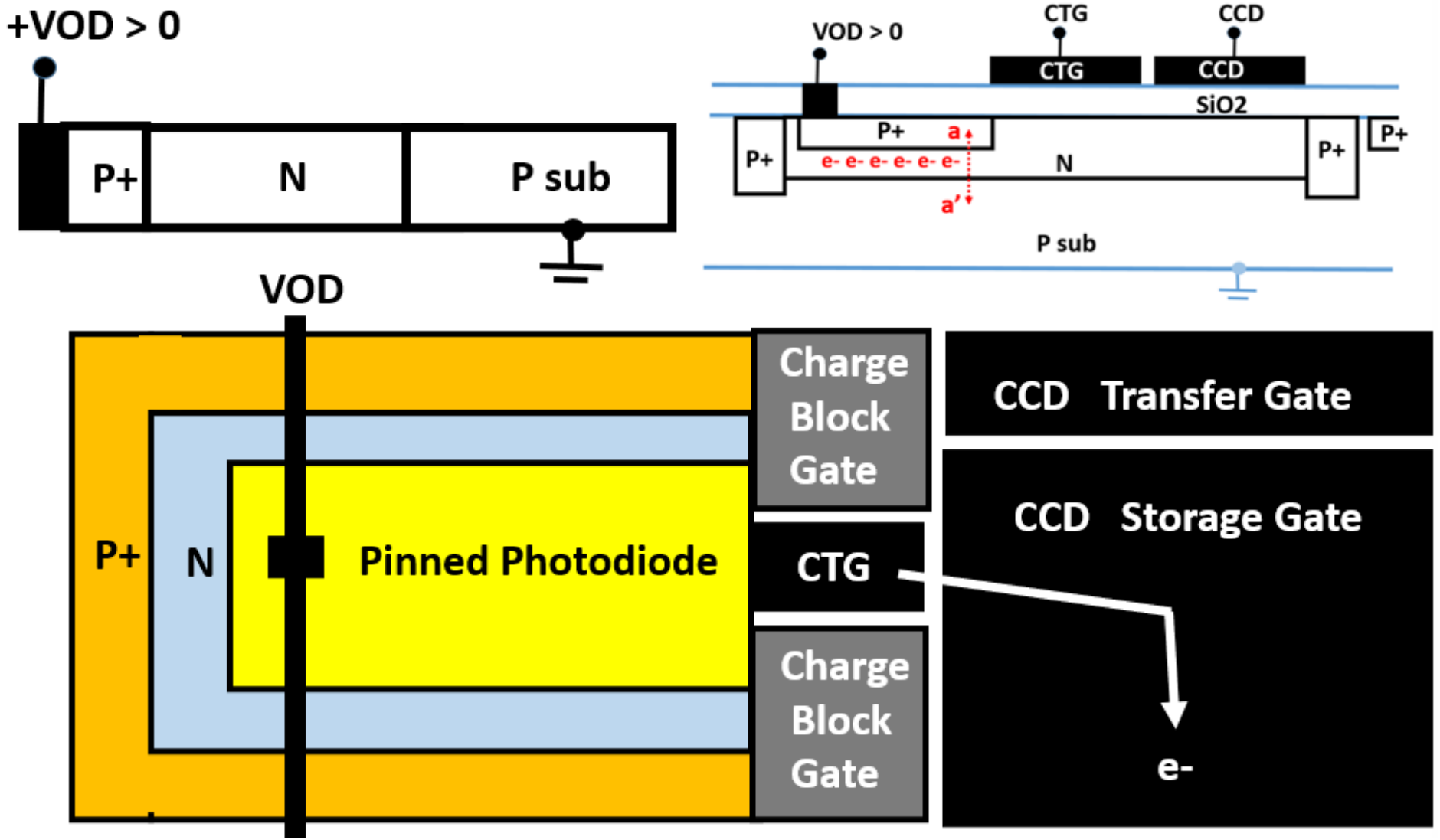


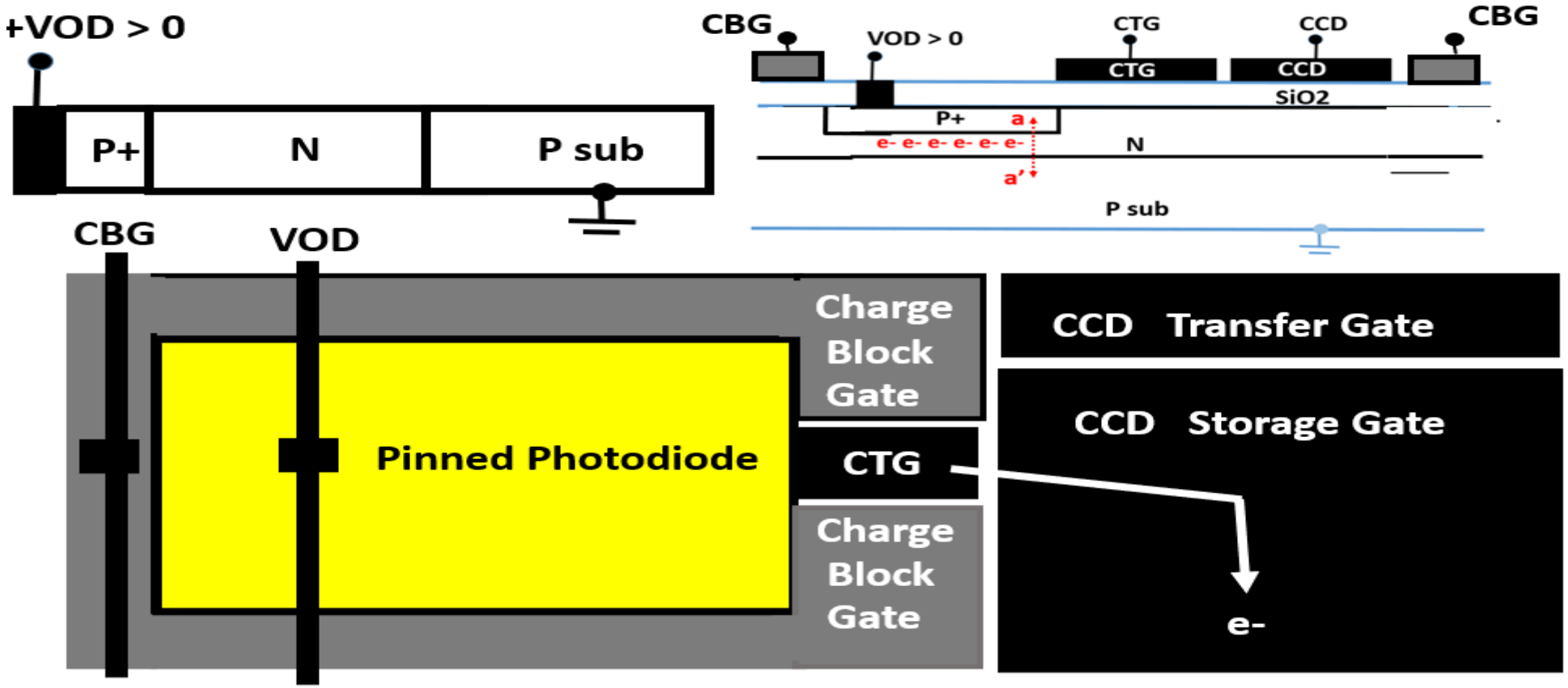
An example of the Pinned Photodiode with VOD function



An example of the Pinned Photodiode with a VOD function

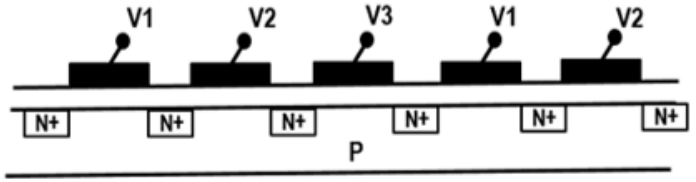


An example of the P+NP Pinned Photodiode with the top VOD metal wire without the P+ heavily doped channel stops region in pixel area which is a source of the undesired dark current.

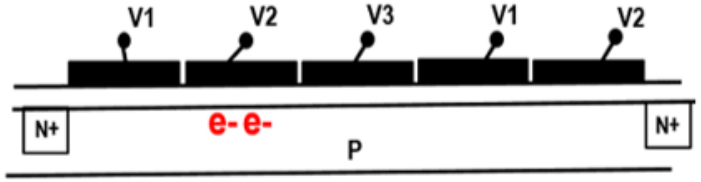


For many years of diligent charge loss and noise reduction efforts

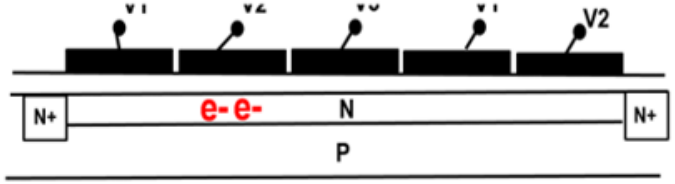
(1) Bucket Brigate Device (BBD)



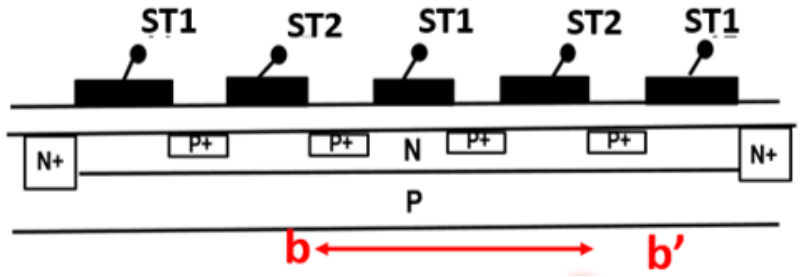
(2) Surface Channel CCD



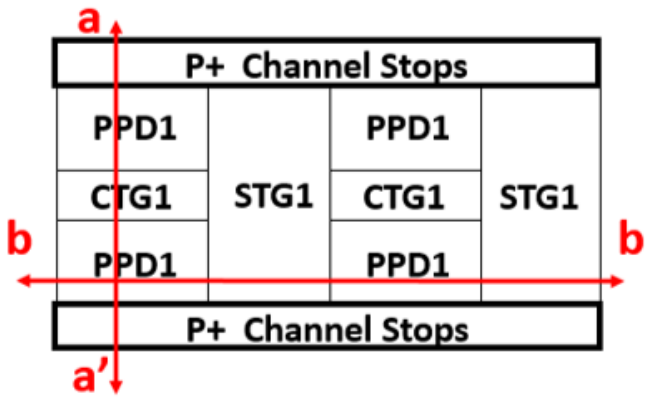
(3) Buried Channel CCD



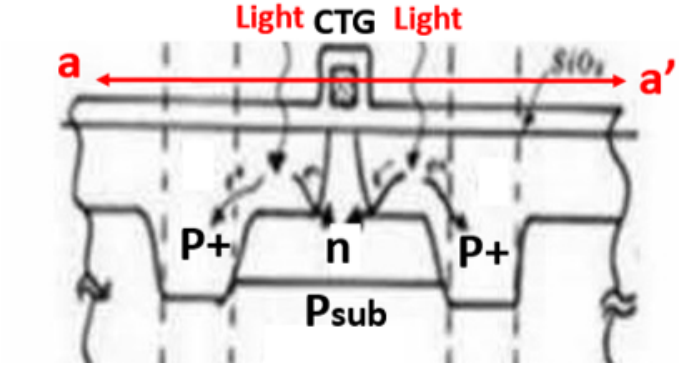
(4) Pinned Photodiode reported at SSDM 1978



Narrow Charge Transfer Gate (CTG)
and Pinned Photodiode (PPD)
with the adjacent P+ channel stops

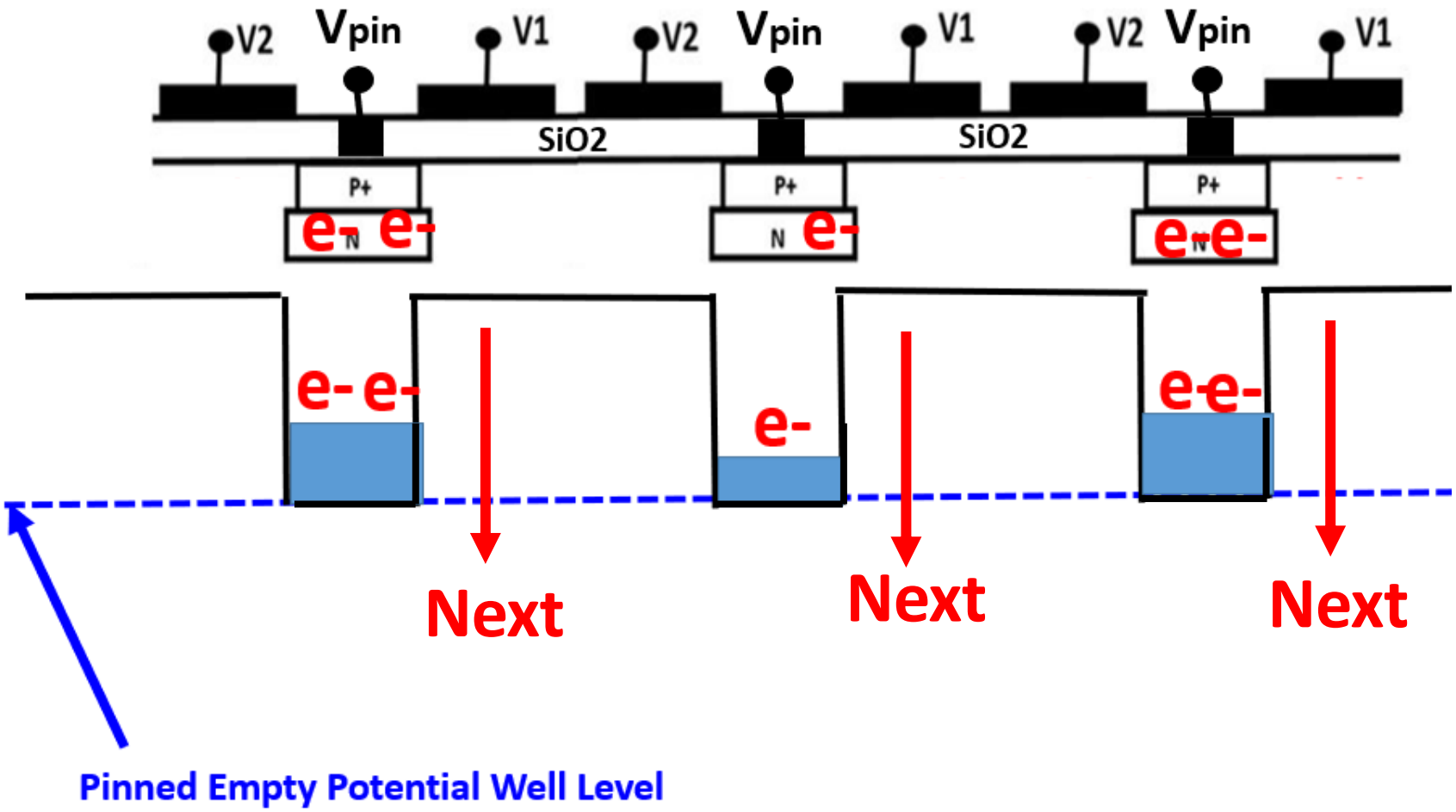


The first Pinned Photodiode(PPD)
developed in 1978 by Hagiwara
and reported at SSDM1978 in Tokyo



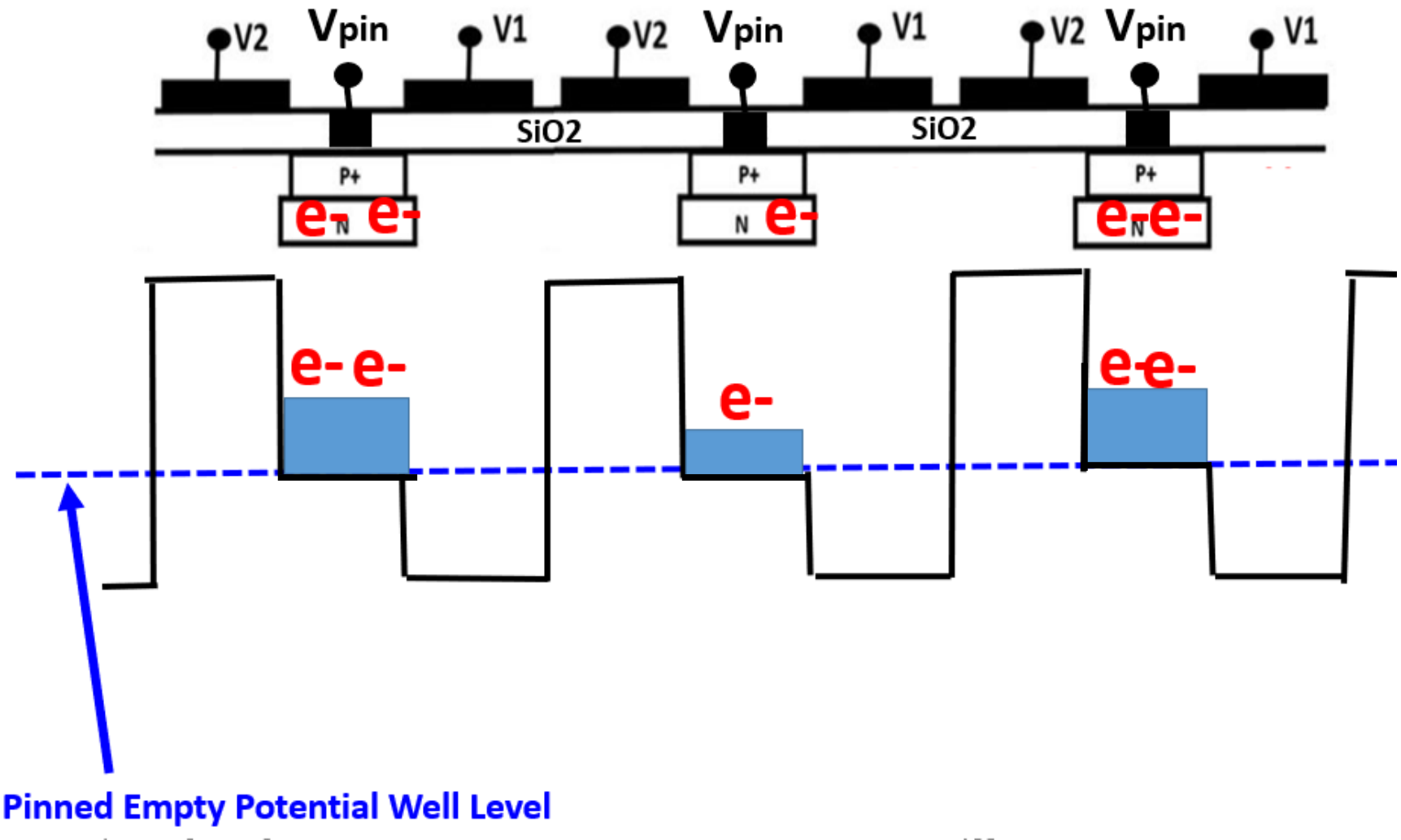
The Virtual Charge Transfer Operation using the P+NPN double junction Pinned Buried Photodiode invented by Yoshiaki Hagiwara in 1975. See JPA 1975-127646, JPA 1975-127647 and JPA 1975-134985

t = T1



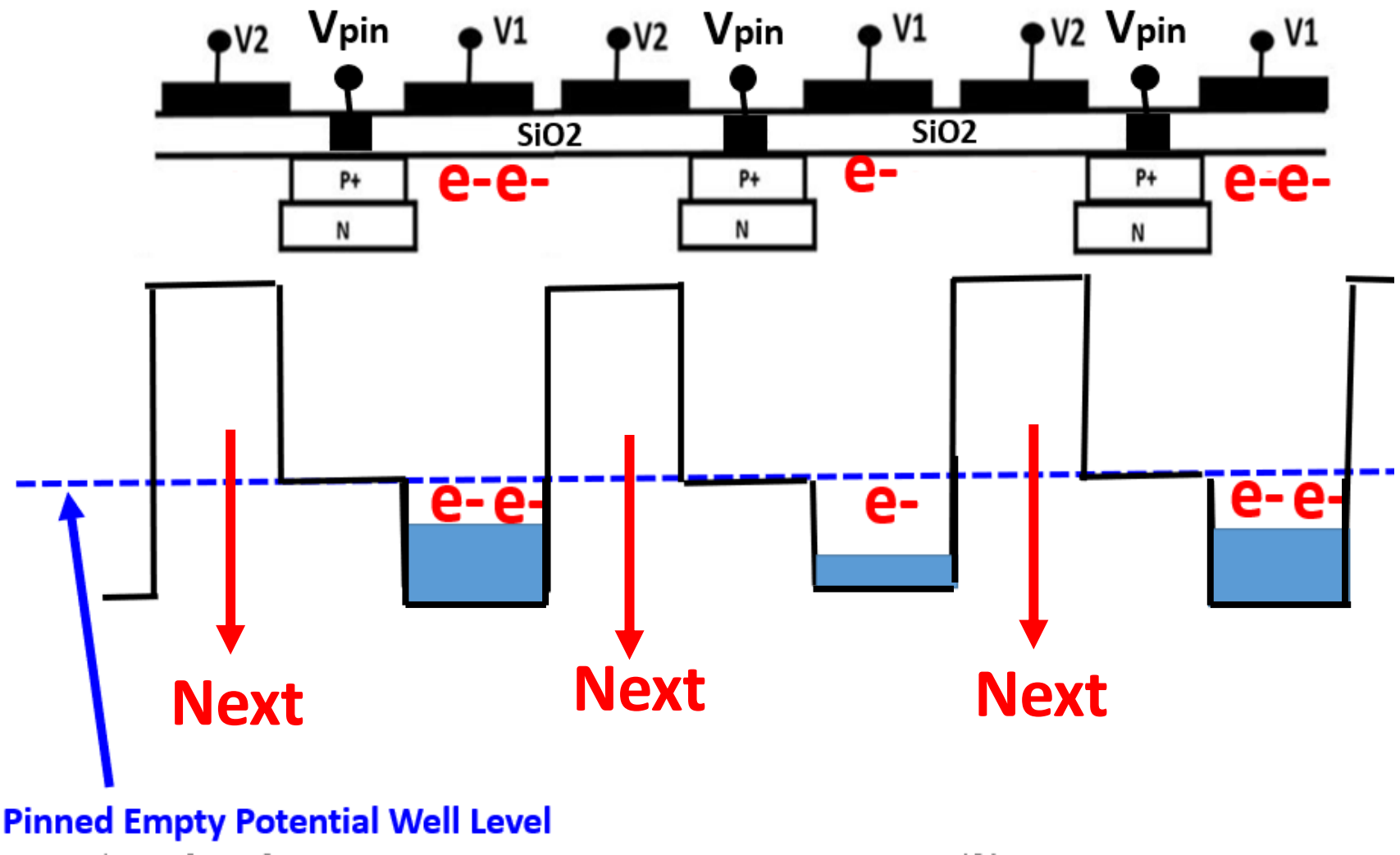
The Virtual Charge Transfer Operation using the P+NPN double junction Pinned Buried Photodiode invented by Yoshiaki Hagiwara in 1975. See JPA 1975-127646, JPA 1975-127647 and JPA 1975-134985

t = T2



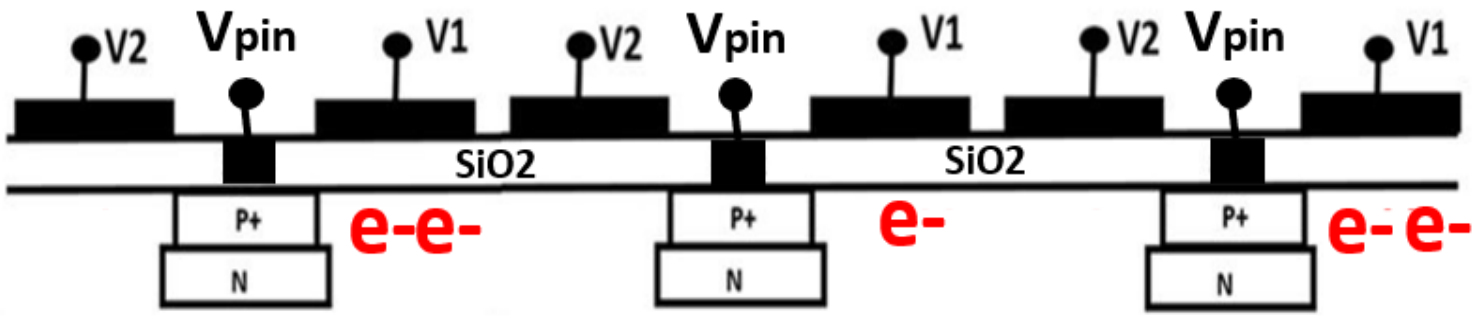
The Virtual Charge Transfer Operation using the P+NPN double junction Pinned Buried Photodiode invented by Yoshiaki Hagiwara in 1975. See JPA 1975-127646, JPA 1975-127647 and JPA 1975-134985

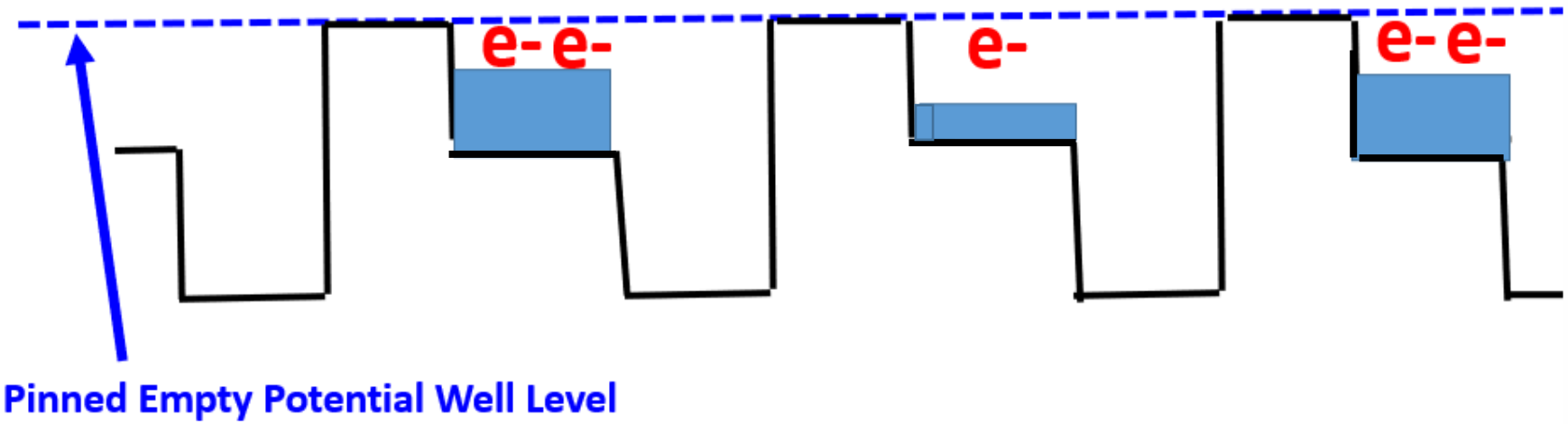
t = T3



The Virtual Charge Transfer Operation using the P+NPN double junction Pinned Buried Photodiode invented by Yoshiaki Hagiwara in 1975. See JPA 1975-127646, JPA 1975-127647 and JPA 1975-134985

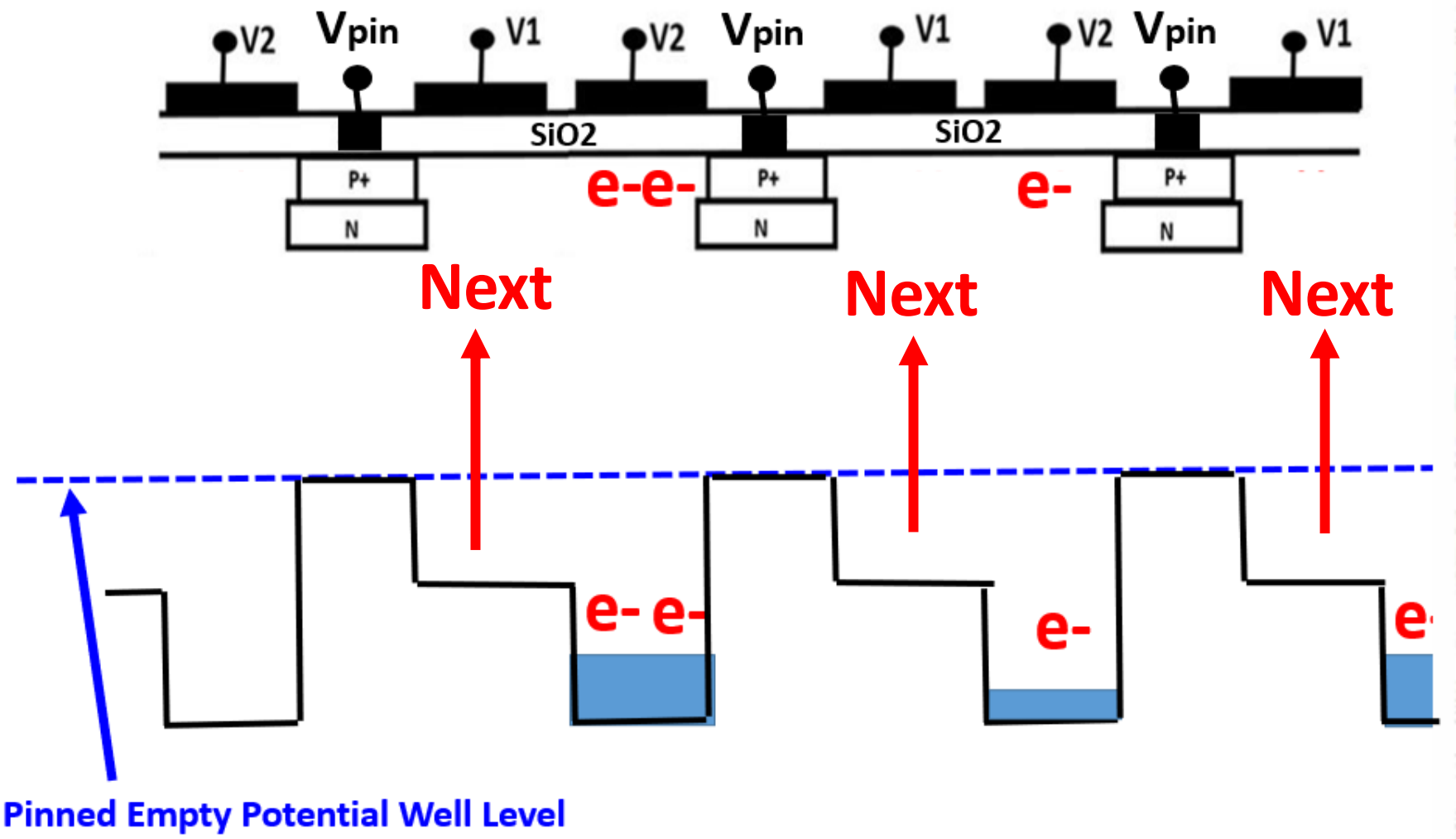
t = T4





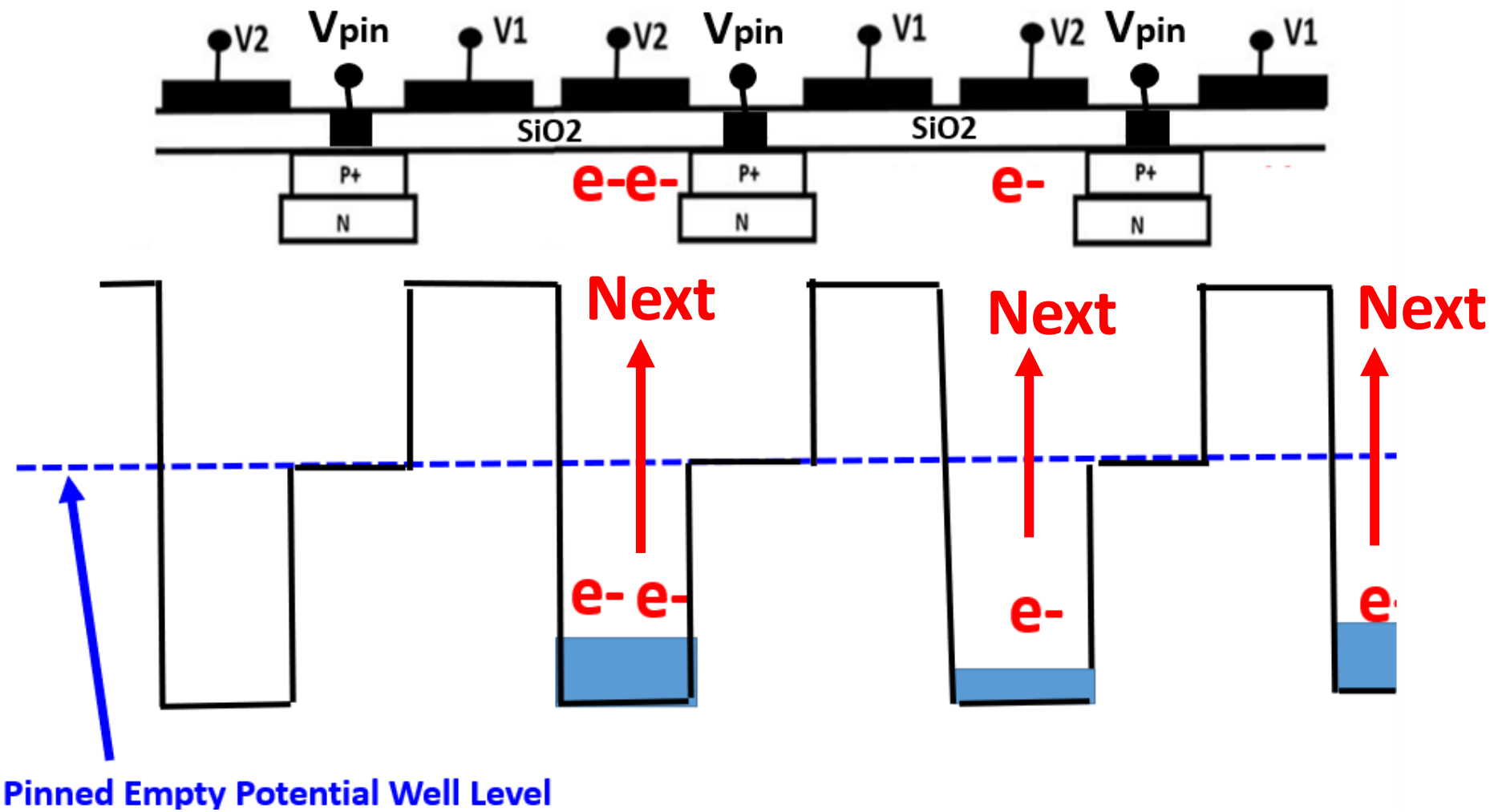
The Virtual Charge Transfer Operation using the P+NPN double junction Pinned Buried Photodiode invented by Yoshiaki Hagiwara in 1975. See JPA 1975-127646, JPA 1975-127647 and JPA 1975-134985

t = T5



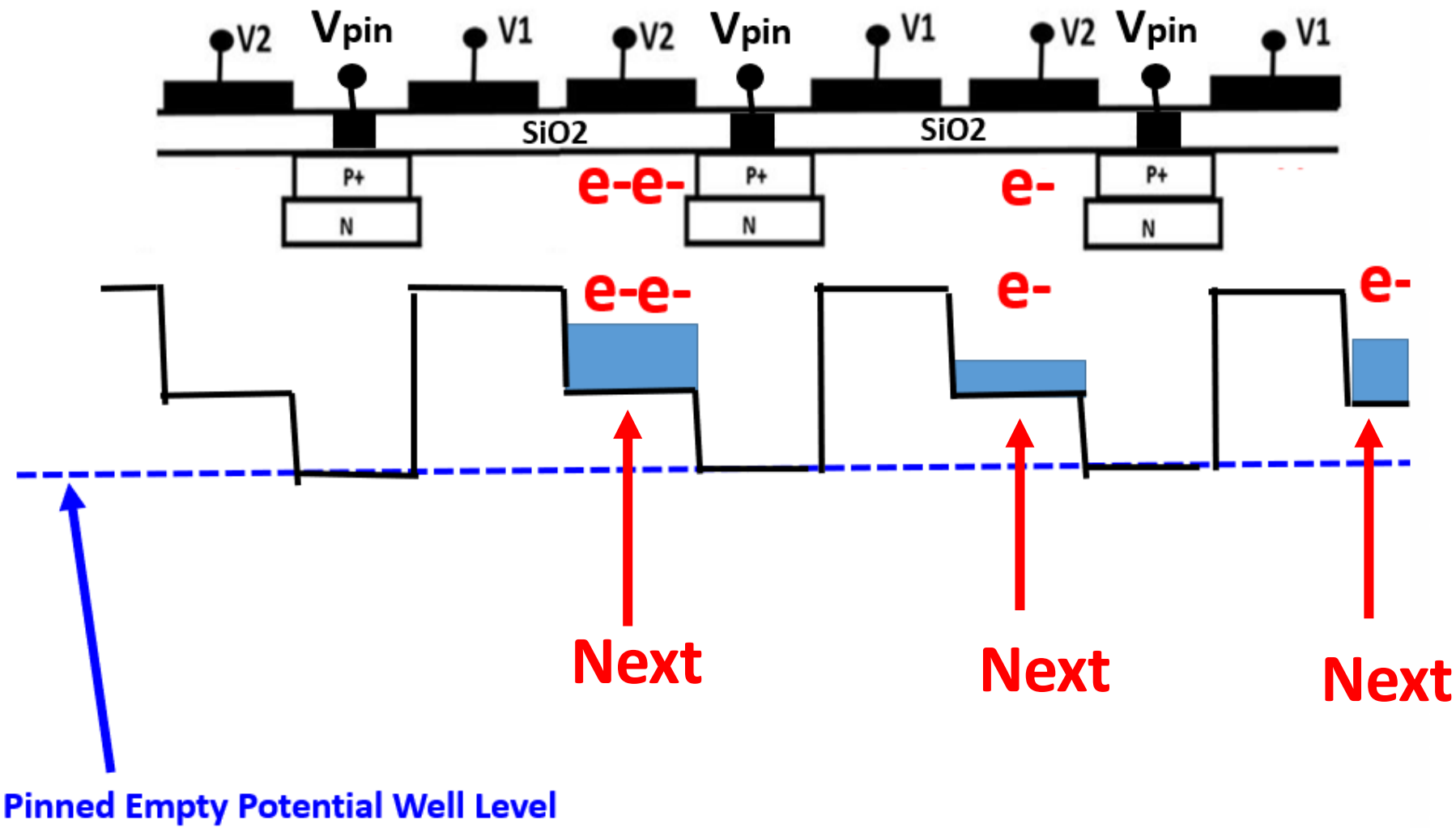
The Virtual Charge Transfer Operation using the P+NPN double junction Pinned Buried Photodiode invented by Yoshiaki Hagiwara in 1975. See JPA 1975-127646, JPA 1975-127647 and JPA 1975-134985

t = T6



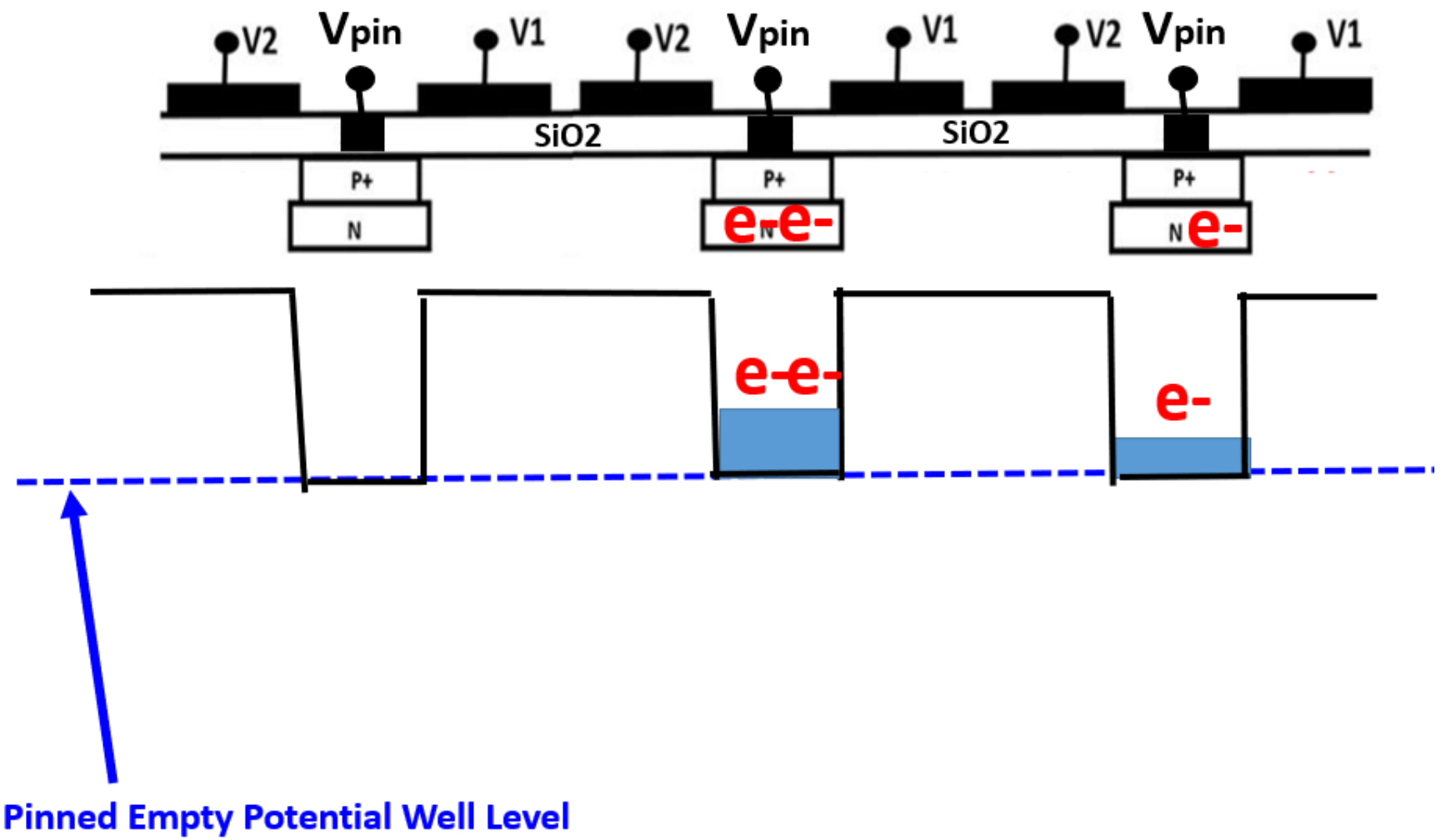
The Virtual Charge Transfer Operation using the P+NPN double junction Pinned Buried Photodiode invented by Yoshiaki Hagiwara in 1975. See JPA 1975-127646, JPA 1975-127647 and JPA 1975-134985

t = T7



The Virtual Charge Transfer Operation using the P+NPN double junction Pinned Buried Photodiode invented by Yoshiaki Hagiwara in 1975. See JPA 1975-127646, JPA 1975-127647 and JPA 1975-134985

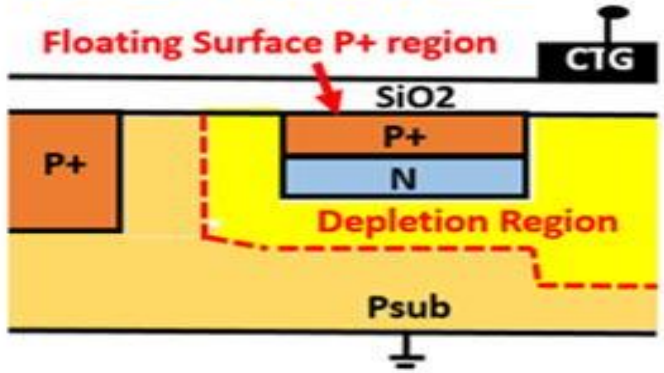
t = T8 =T1



Difference of Buried Photodiode and Pinned Photodiode

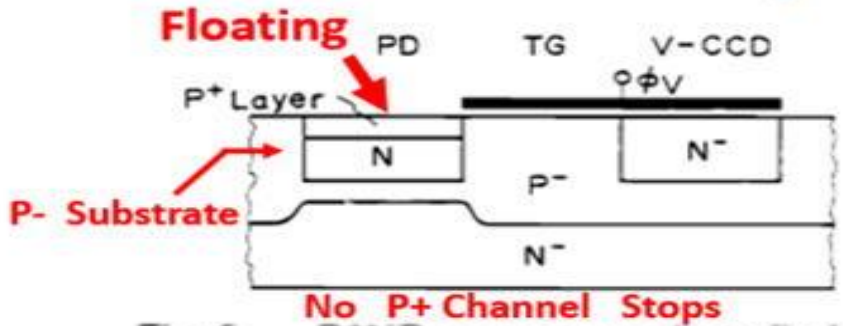
Figure 5 does not have the P+ channel stop nearby.

Buried Photodiode



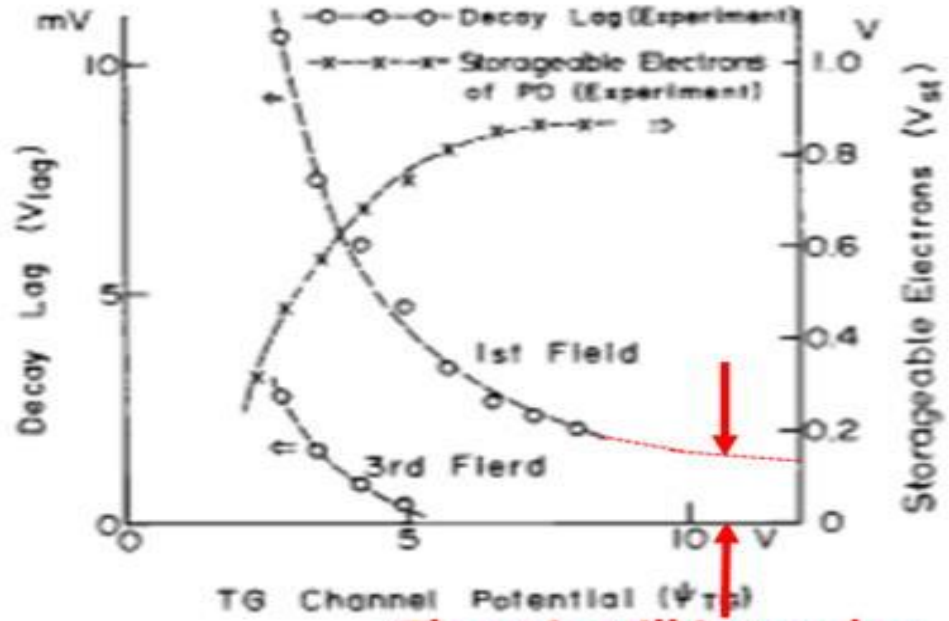
Serious Image Lag Problem

NEC IEDM1982 Paper



No P+ Channel Stops

Fig.5. P⁺NP⁻ structure photodiode
(a) Unit cell cross sectional view



There is still image lag
at the CTD gate voltage more than 10 volt.

Fig.6. Storageable electrons vs. transfer gate channel potential, and decay lag vs. transfer gate channel potential in the P⁺NP⁻ structure photodiode

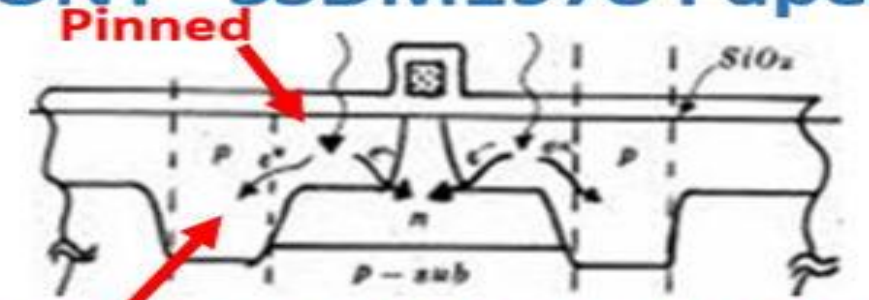
NEC IEDM1982 Paper reported Image Lag

Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 volt.

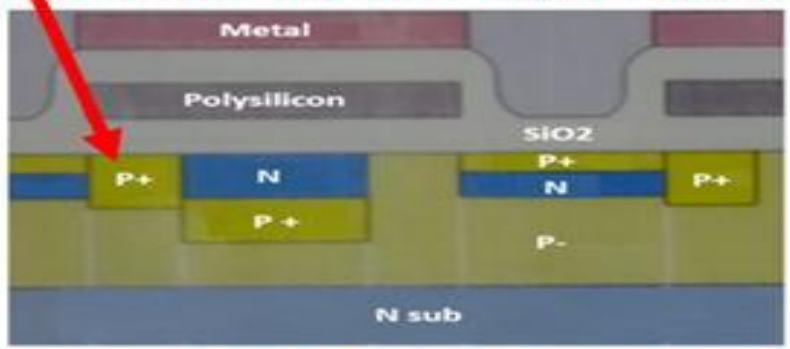
Difference of Buried Photodiode and Pinned Photodiode

Pinned Photodiode

SONY SSDM1978 Paper

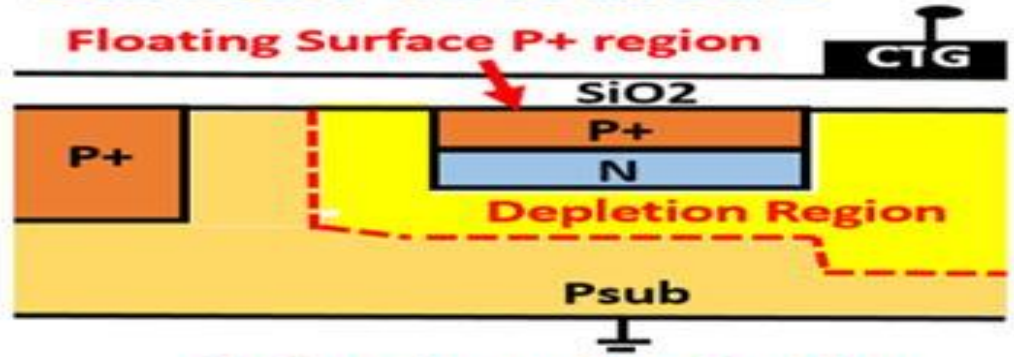


P+ Channel Stops and no Image Lag Problem



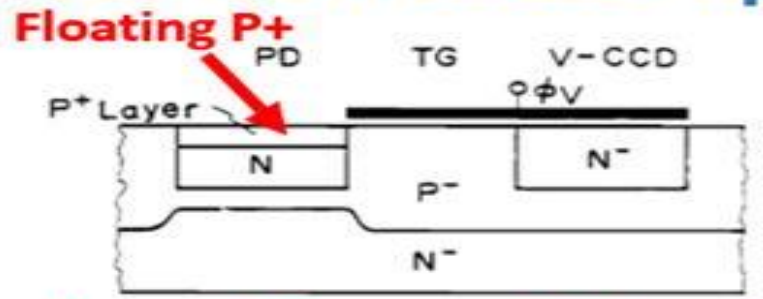
SONY 1987 HAD Sensor

Buried Photodiode

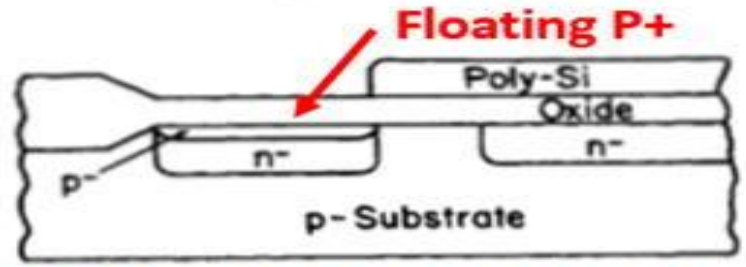


Serious Image Lag Problem

NEC IEDM1982 Paper



No P+ Channel Stops and Serious Image Lag



KODAK IEDM1984 Paper

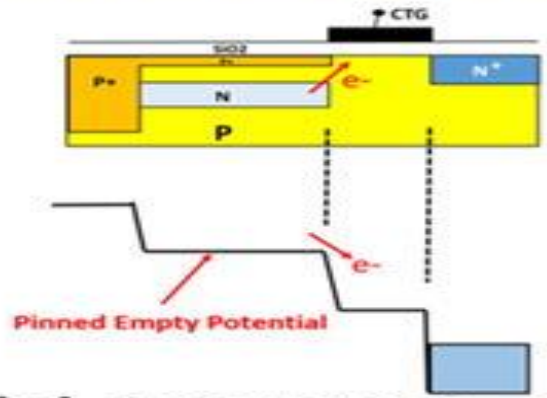
Difference of Pinned Photodiode and Buried Photodiode

Pinned Photodiode must have the P+ heavy doped channel stops nearby.

Pinned Photodiode must be a buried photodiode.

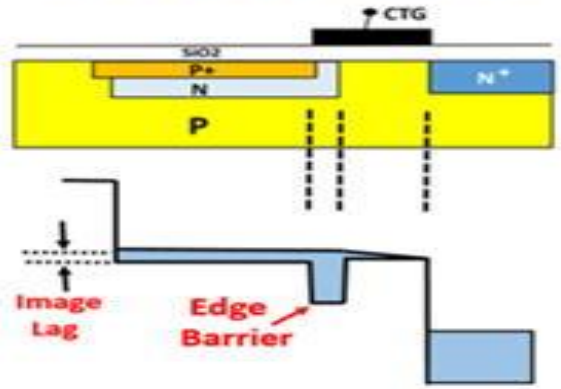
Pinned Photodiode must not have the edge barrier to the Charge Transfer Gate

Pinned Buried Photodiode does not have the edge barrier



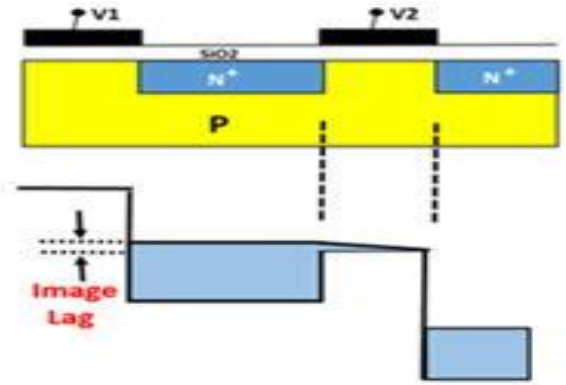
(1) Pinned Photodiode with No Image Lag

Buried Photodiode with the edge barrier



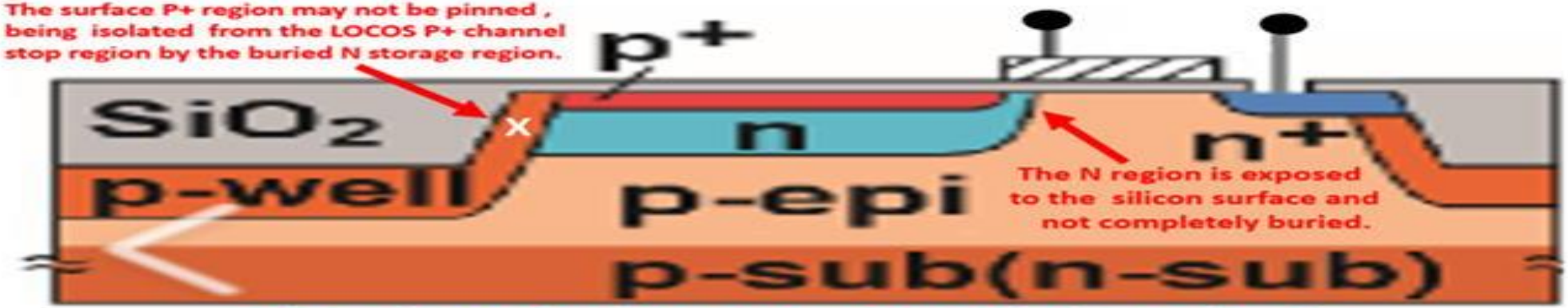
(2) Buried Photodiode with BBD Barrier

Bucket Bridgade Device (BBD) with Serious Image Lag



(3) Bucket Brigade Device (BBD)

The surface P+ region may not be pinned , being isolated from the LOCOS P+ channel stop region by the buried N storage region.



This photodiode is not Pinned Photodiode since the N storage region is not completely buried.

Albert J.P. Theuwissen, Jan T.J. Bosiers, Edwin Roks, " The Hole Role ", an invited paper at IEDM2005, Washington DC, Techn. Dig. , 2005.

But in the case that parts of the depleted n-type CCD channels are not covered by gate material, their surface potential is undefined ! Such a structure will suffer from charge transport issues during operation, because charge can be trapped in local potential pockets. The effect can be solved by defining the potential in the open areas through an extension of the p^+ channel stopper. A simple self-aligned implant of $2x10^{13}$ /cm^2 boron ions is sufficient to extend the channel stop areas to the gate edge and consequently fix the potential in the open areas [2]. The result after this self-aligned implant is shown in Figure 3. The presence of enough holes plays a crucial role in fixing the potential for the regions "beyond control" of the gates. (Is this structure the mother of the pinned-photodiode or buried diode or hole-accumulation device ?)

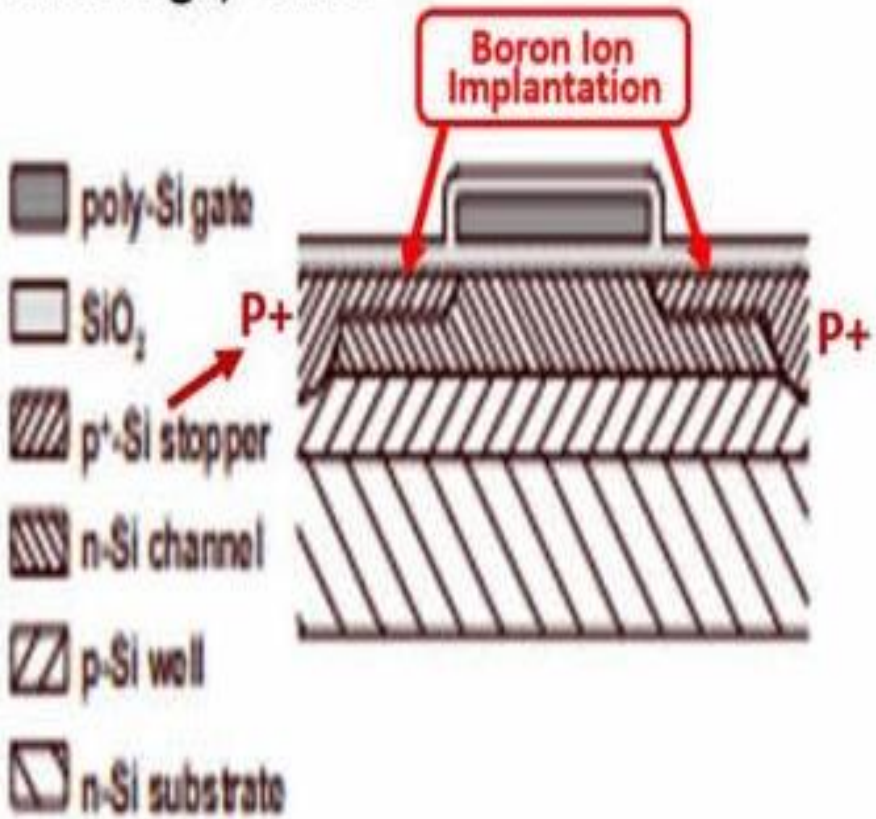


Figure 3. Cross section of a buried-channel CCD on n-Si substrate including light windows and pinned interface potential in the non-covered CCD channels (the cross section is made perpendicular to the CCD channel).

[2] Y. Daimon-Hagiwara et.al., Proc. 10th Conf. on Solid-State Devices, Tokyo, 1978, pp.335-340.

Semiconductor History Museum of Japan

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

In 1975, Sony proposed using a PNP transistor as the photodetector [3]. By providing a P + layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated, greatly improving the light sensitivity. This P + layer was also a proposal to reduce the dark current and image lag which became the basis of the pinned photodiode.

In 1978, Sony presented a 93,000-pixel FT (Frame Transfer) -CCD image sensor compliant with the Analog TV Broadcasting Standard (SDTV) for the first time in the world [5], using the photodiode with the same structure as above. Sony succeeded in 1981 in trial production of a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor by further improvement of this technology [6].

The Pinned Photodiode is a photodiode in which the entire N layer is covered with a P layer. The part of the P layer on the light incident surface is heavily doped P+ (Fig-1). Kodak named this structure Pinned Photodiode in 1984 because the P + surface of the light incident surface was pinned to the substrate potential. This device has features such as high light sensitivity, wide dynamic range, image lag free, much smaller dark current due to reduced influence of GR center on the light receiving surface, and no white scars.

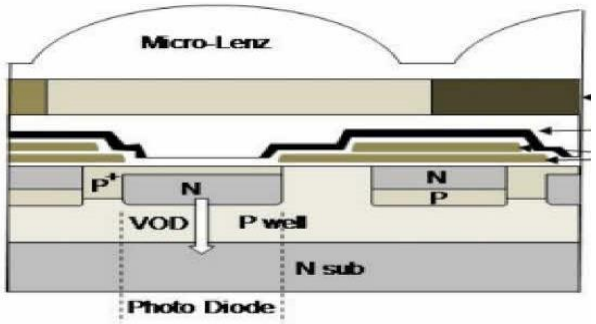
References:

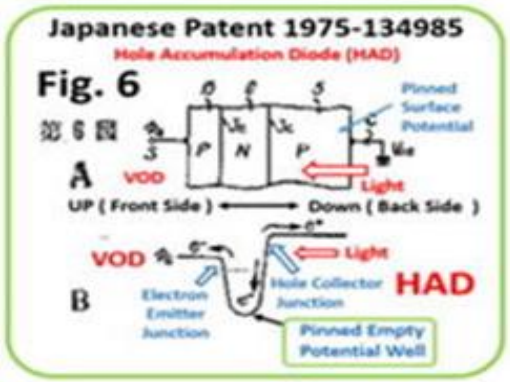
【1】M. Hamasaki, T. Suzuki, Y. Kagawa, K. Ishikawa, K. Miyata and H. Kambe, "An IT-CCD imager with electronically variable shutter speed" , Technical Report of The Institute of Image Information and Television Engineers. vol. 12, no. 12, pp. 31-36, (1988)

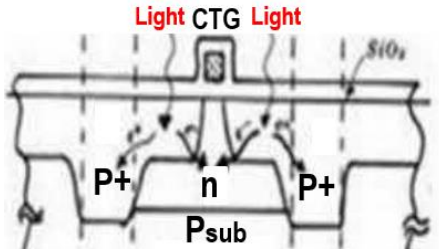
【3】Y. Hagiwara, Japanese Patent JP1975—134985

【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

【6】I. Kajino, M. Shimada, Y. Nakada, Y. Hirata and Y. Hagiwara, "Single Chip Color Camera Using Narrow channel CCD Imager with Over Flow Drain", Technical Report of The Institute of Image Information and Television Engineers, vol. 5, no. 29, pp.







Pinned Photodiode reported at SSDM 1978

Sony's Representative Inventions Supporting Stacked Multi-Functional CMOS Image Sensors

Sony Corporation
Sony Semiconductor Solutions Corporation

https://www.sony.net/SonyInfo/News/notice/20200626/

Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

Why is SONY so strong in Semiconductor Business from the beginning to now ?

(0) Sony could purchase the Bipolar Transistor Patent Right with a very low price of $ 500 (?) from Bell Lab USA in 1954.

(1) Kawana, Yoshiyuki at Sony invented the low collector On-Resistance N+PN junction type Bipolar transistor by thinning the back side of silicon wafer, a technique now used for the backside illumination CMOS image sensors widely to improve sensitivity.

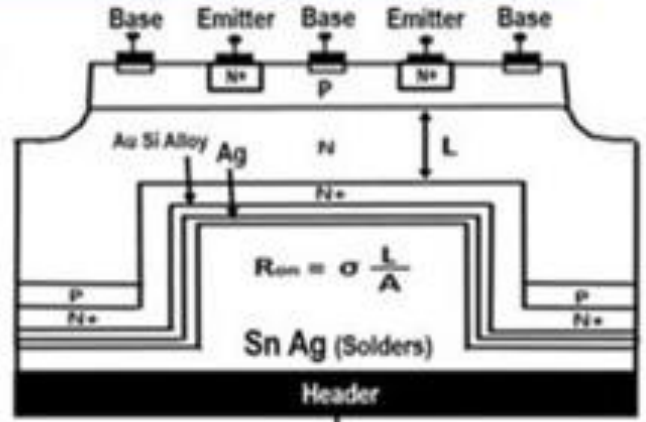
(2) Kato, Toshio at Sony invented the silicon surface light etching and new SiO2 Passivation technique for the N+PN junction type Bipolar transistor with the MESA like isolation, which is now known as the shallow trench isolation with the excellent side wall SiO2 formation to reduce the leakage current.

(3) Hagiwara, Yoshiaki at Sony invented the P+NPNsub junction (thyristor) type Pinned Photodiode, which is identical to SONY Hole Accumulation Diode (HAD), with the built-in vertical overflow drain (VOD) function, the image lag free electric shutter function and good light sensitivity to realize fast action video cameras.

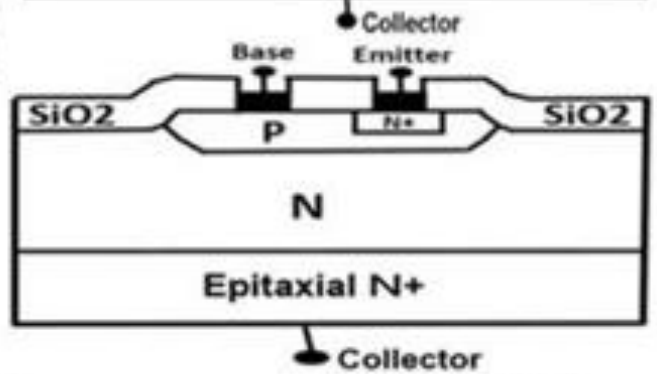
See Japanese Patent 1975-134985

Hagiwara invented SONY HAD which is identical to the Pinned Photodiode which is also the Depletion Photodiode and the Buried Photodiode.

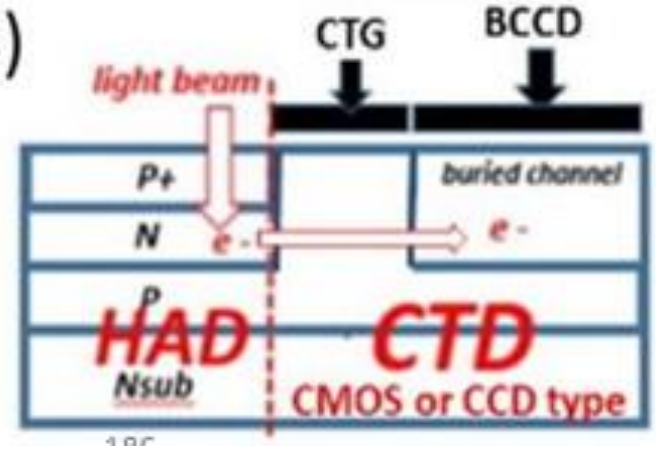
(1)



(2)



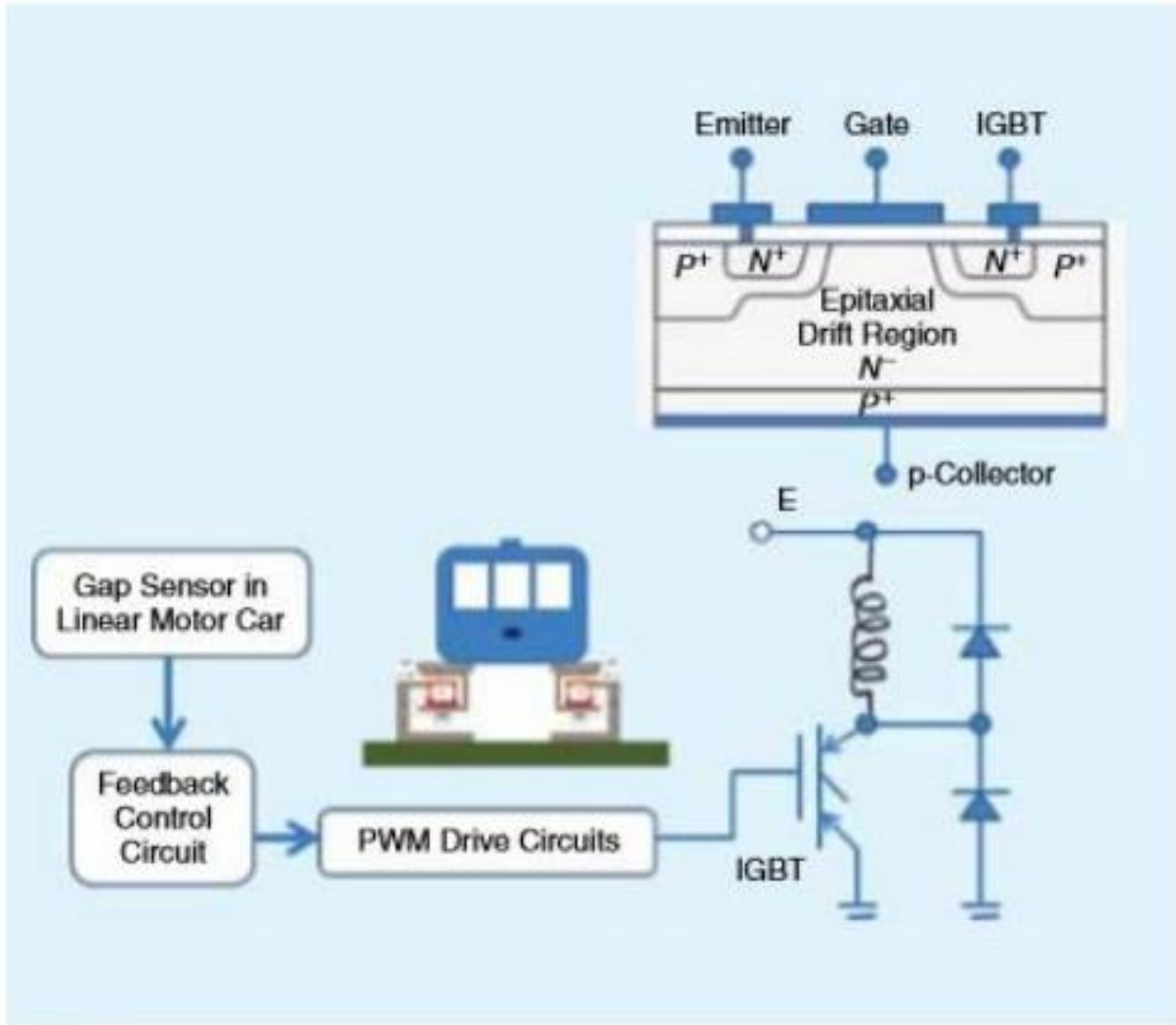
(3)



Yoshiaki Higihara: The p-n-p-n Diode in Future Linear Motor Cars and in Modern Imagers

John Louis Moll (1921–2011) was studying a p-n-p-n diode switch in his Ph.D. dissertation work when the first ISSCC was held in 1954. In a normal operation mode, this device works as a thyristor, which can drive a large current and is the key device structure of an IGBT applied for a linear motor car of the future (see Figure 9). In a dynamic operation mode, this device may work as a simple p-n-p-n dynamic capacitance that can detect and store one single electron, which is a key device structure of the modern image sensor (see Figure 10).

I recall, when I was taking his physics course at Caltech, that Feynman once said that an electron is always free, moving around rapidly in free space, even in solid, and it never stops. It is very hard to catch an electron because we do not know exactly where it is. Our civilization today is based on a technology that controls electrons, down to a single one.



GURE 9: The p-n-p-n switch diode for a modern linear motor car.

Imagine a photon incident to a bipolar transistor base region. The photon energy creates an electron-hole pair. And the photo-electron can be stored in the base region as one single majority carrier. That is, a bipolar transistor can also function as a photon detector and/or a storage container. I thought that a room in a hotel must be empty and clean before the first hotel guest arrives. So must be this transistor base region empty and clean with no guest electrons at the beginning. This transistor in a dynamic p-n-p capacitor mode is useful since it can capture, confine, and control one single electron. But as a student, I did not know yet how to move that single photoelectron sitting in the base region to the outside world so that we can make use of it as a signal. I had no way yet to know whether the hotel guest has arrived and is resting in the hotel room or not. We had no way yet to ask the hotel guest to come up to the hotel lobby to meet me. I had to wait a few more years (until 1970

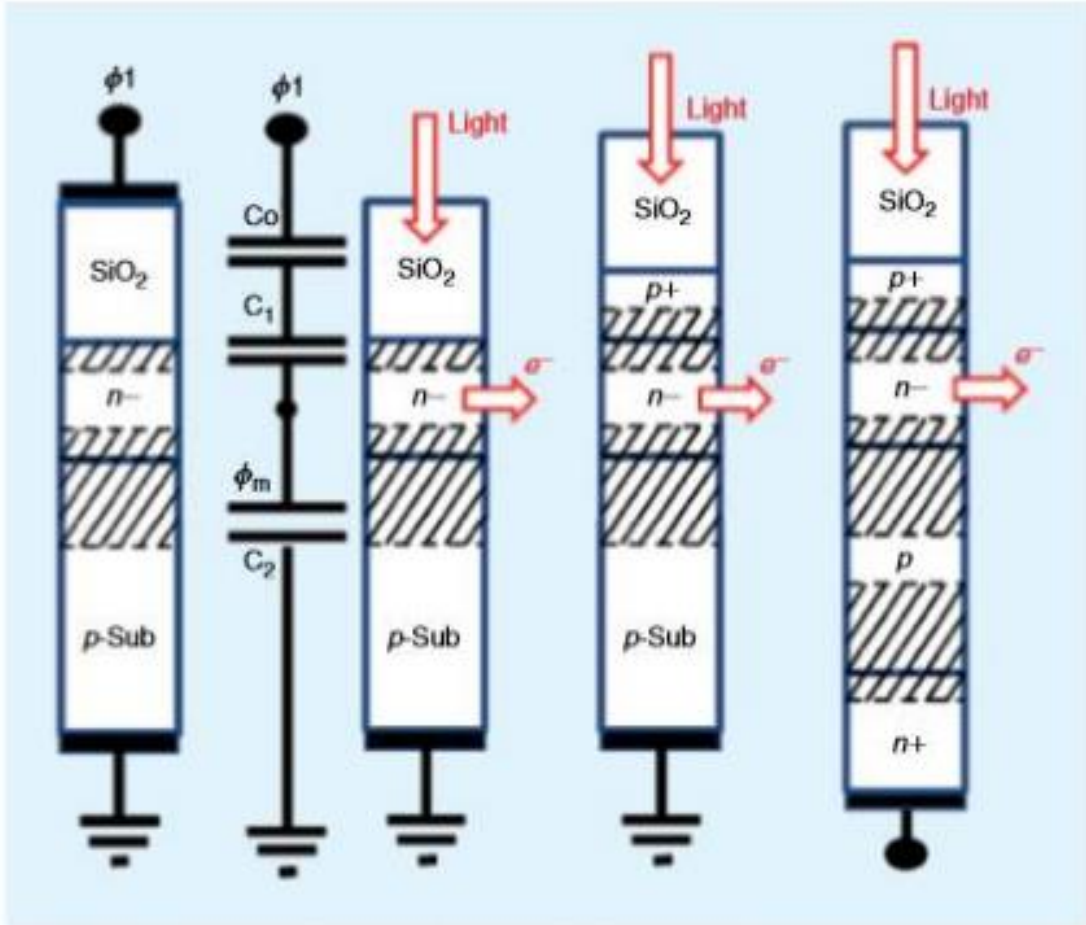
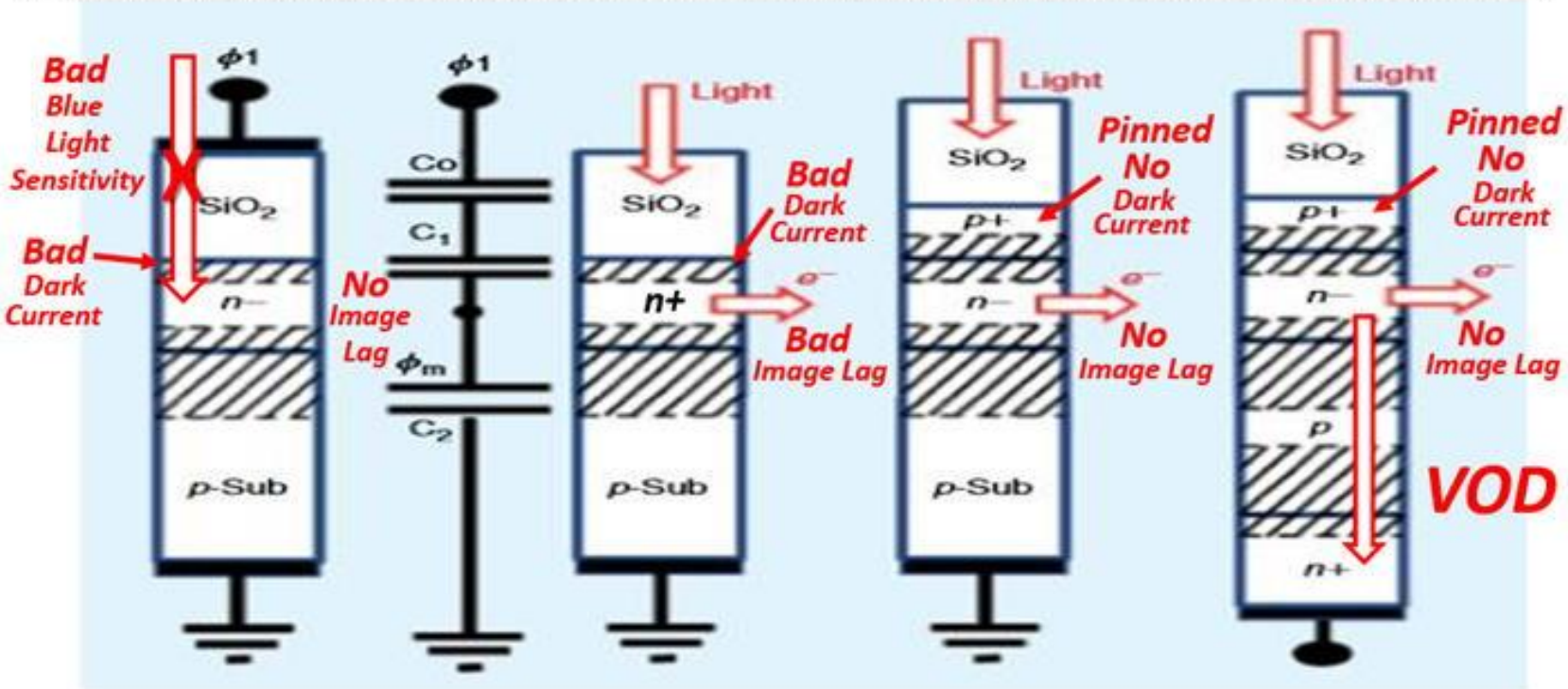


FIGURE 10: From CCD to the dynamic p-n-p-n diode capacitors.

in my senior year in college) to find the answer. We all know now it is the CCD structure that can store and transfer one single electron. With a precharge reset set gate and a source-follower circuit, a scheme invented by Walter Kosonocky. We could finally meet our hotel guest at the hotel lobby.

History of dynamic Solid State image sensing structure from BCCD type MOS capacitor to the P+NPN junction Pinned Photodiode capacitor



(1) CCD type invented by Bell Lab in 1968

(2) N+P type The classical photodiode with serious image lag

(3) P+NP type (4) P+NPN type (3) and (4) are the P+NP junction type Pinned Photodiode invented by Yoshiaki Hagiwara, 1975

In Japanese patent 1975-134985, Hagiwara at Sony invented the Pinned photodiode with very low dark current, which is also the completely depleted Buried Photodiode with image lag free picture quality, and also with the built-in vertical overflow drain (VOD) function.

Reference: IEEE Solid-STATE CIRCUITS MAGAZINE, SUMMER 2013 issue pp. 6～

27.5 High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor

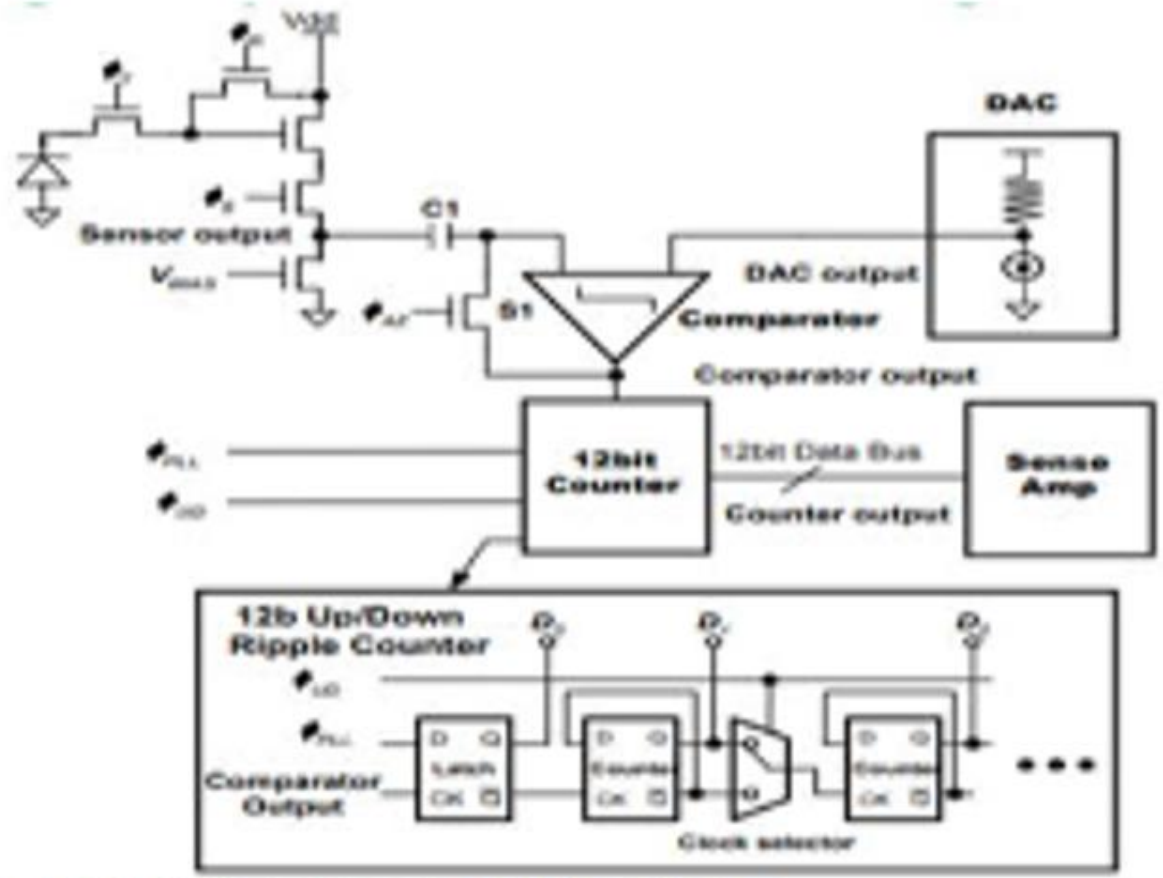


Figure 27.5.2: Column-inline dual CDS architecture.

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Modern CMOS Image Sensors have (1) HAD (2) APS and (3) CDS.

(1) HAD (PPD) was invented by Y. Hagiwara in 1975.
(2) APS was invented by Peter Noble in 1968.
(3) CDS was invented by M. White in 1972.
(4) Sony engineers perfected these technologies in 2006.

27.5 High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor

Yoshikazu Nitta, Yoshinori Muramatsu, Kiyotaka Amano, Takayuki Toyama, JunYamamoto, Koji Mishina, Atsushi Suzuki, Tadayuki Taura, Akihiko Kato, Masaru Kikuchi, Yukihiro Yasui, Hideo Nomura, Noriyuki Fukushima

Sony, Atsugi, Japan

Traditionally, the advantages of compact image sensors (CISs) over CCDs have been low power consumption and the capability for system integration. Additionally, the image quality of CISs has recently begun to rival and even surpass that of CCDs in the area of high-speed imaging [1]. Compared to high-speed CCDs, CISs utilize the advantage of a column-parallel pixel readout.

The pixels are conventional 4T active pixel sensor (APS) pixels that use hole accumulation diodes (HADs). HADs enable image sensors such as CCDs and CISs to realize ideal properties of low dark current, no kTC noise, and no image lag [2]

Digital double-sampling architecture is proposed to remove device variation and circuit offset that cause vertical FPN [3]. Our column-inline dual-CDS architecture (Fig. 27.5.2) implements digital double-sampling (digital CDS) and analog CDS in parallel columns. A high-speed 297MHz clock is utilized to reduce the double digital sampling period. Additionally, an analog CDS is used to reduce the ADC period for the reset signal V_{RST} by eliminating the analog offset of the pixel and the comparator output.

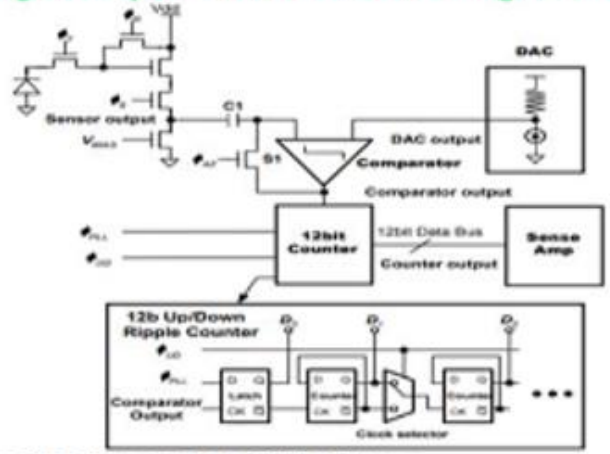

Figure 27.5.2: Column-inline dual CDS architecture.

References:

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Hagiwara 1975 invention (JPA 1975-134985)

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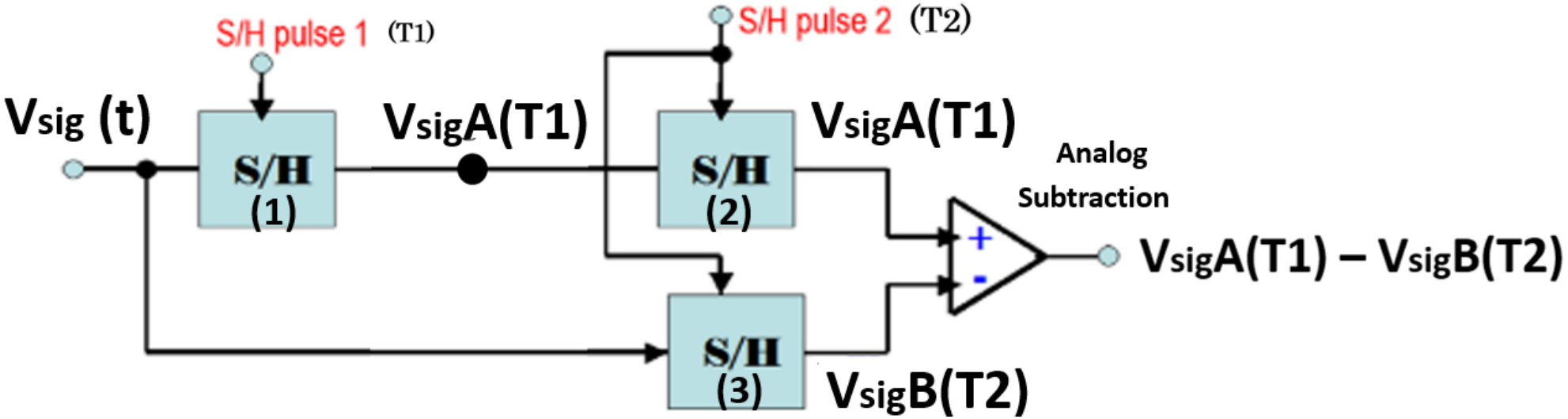
7 In Pixel Correlation Double Sampling (CDS) circuit

For many years of diligent noise reduction efforts including the CDS circuit design, the buried channel process design and the Pinned Buried Photodiode device design powered by the advanced CMOS process scaling technology made possible to realize high performance CMOS image sensors.



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