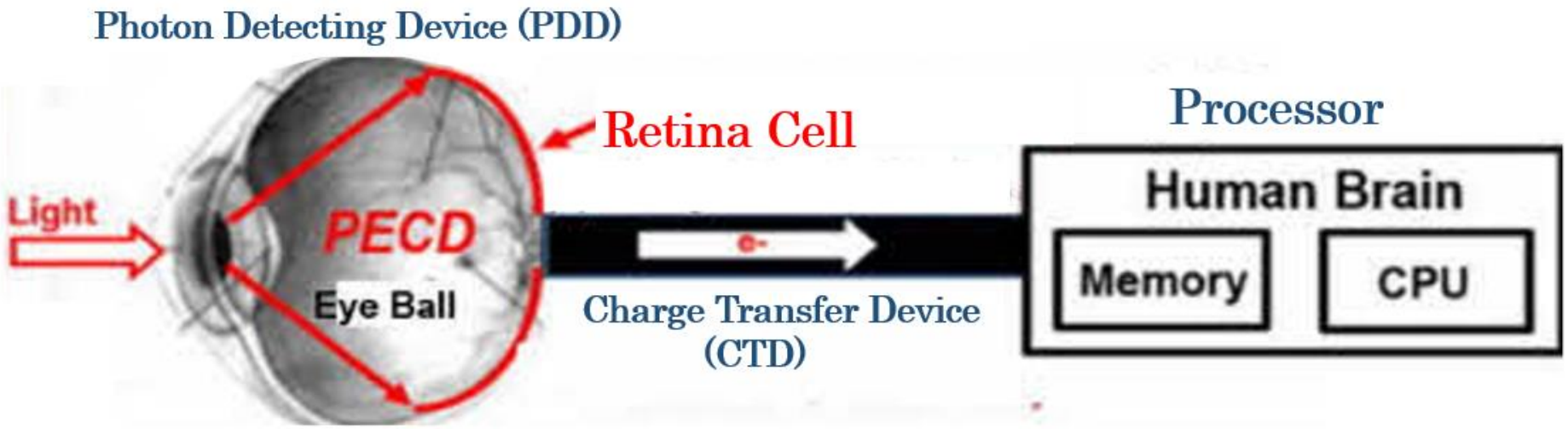
5 Double and Triple junction Dynamic Photo Transistors

Under Construction

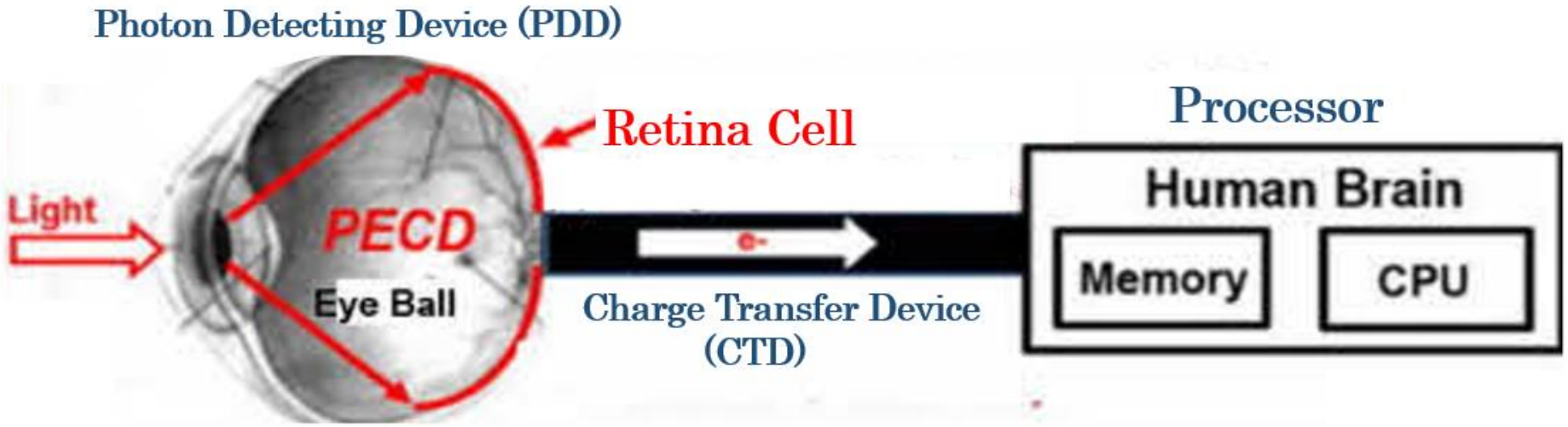
5 Double and Triple junction Dynamic Photo Transistors

An intelligent image sensor is composed of a photon detecting device (PDD), a charge transfer device (CTD) and an CMOS digital output circuit connected to the external artificial intelligent processor system unit for real time cache memory, pattern recognition and intelligent judgement task for many useful applications.



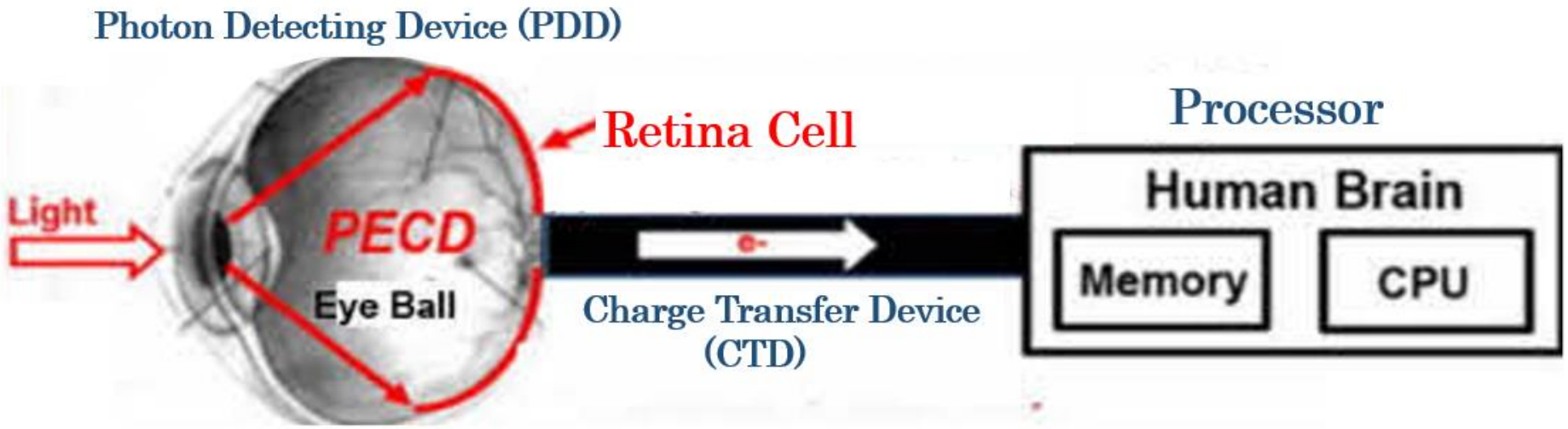
5 Double and Triple junction Dynamic Photo Transistors

A typical classical image sensor had a single N+P floating junction type PDD and a simple MOS One Transistor One Capacitor (1T1C) DRAM type CTD while CCD/MOS dynamic capacitor type PDD and CTD were used widely in high performance solid image sensors. However, presently active pixel AMP CMOS image sensors have replaced CCD image sensors completely in the image sensor market.



5 Double and Triple junction Dynamic Photo Transistors

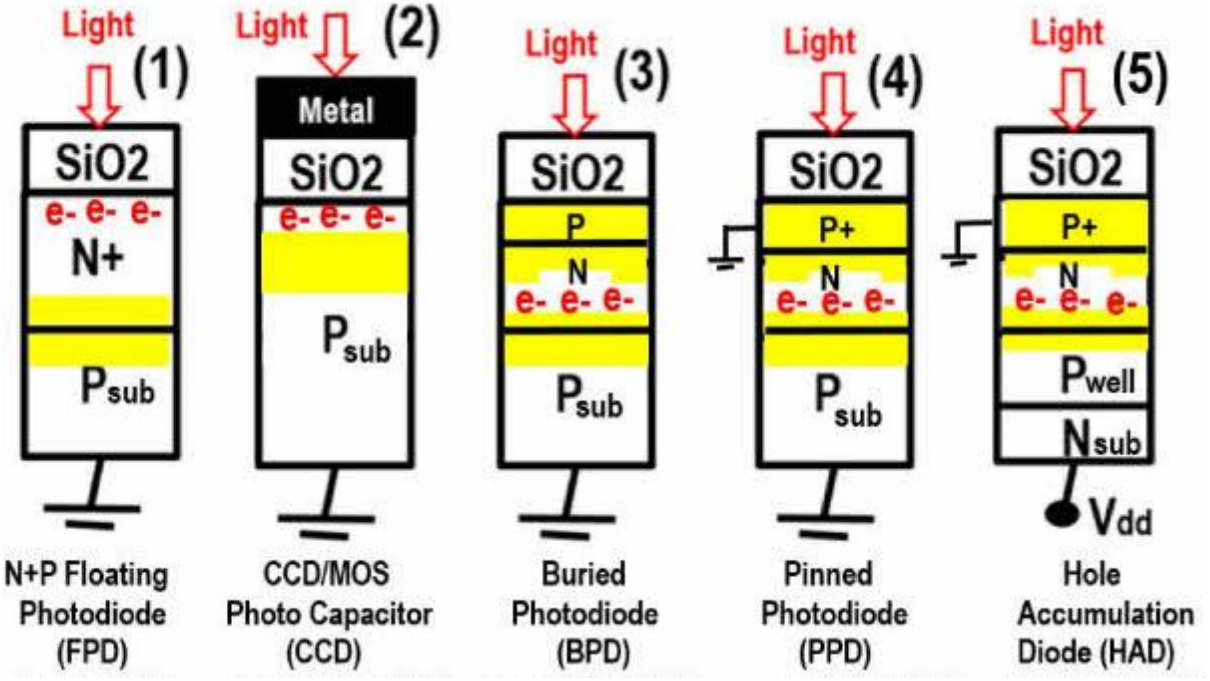
A modern CMOS image sensor is also composed of three parts, PDD, CTD and output circuit. However, a modern CMOS image sensors now has much improved parts.



5 Double and Triple junction Dynamic Photo Transistors

Both the single N+P floating junction type PDD and the CCD/MOS type photon detecting device (PPD) are now completely replaced by the double and triple dynamic junction type dynamic photo transistors.

Different kinds of Photon Detecting Device (PDD)

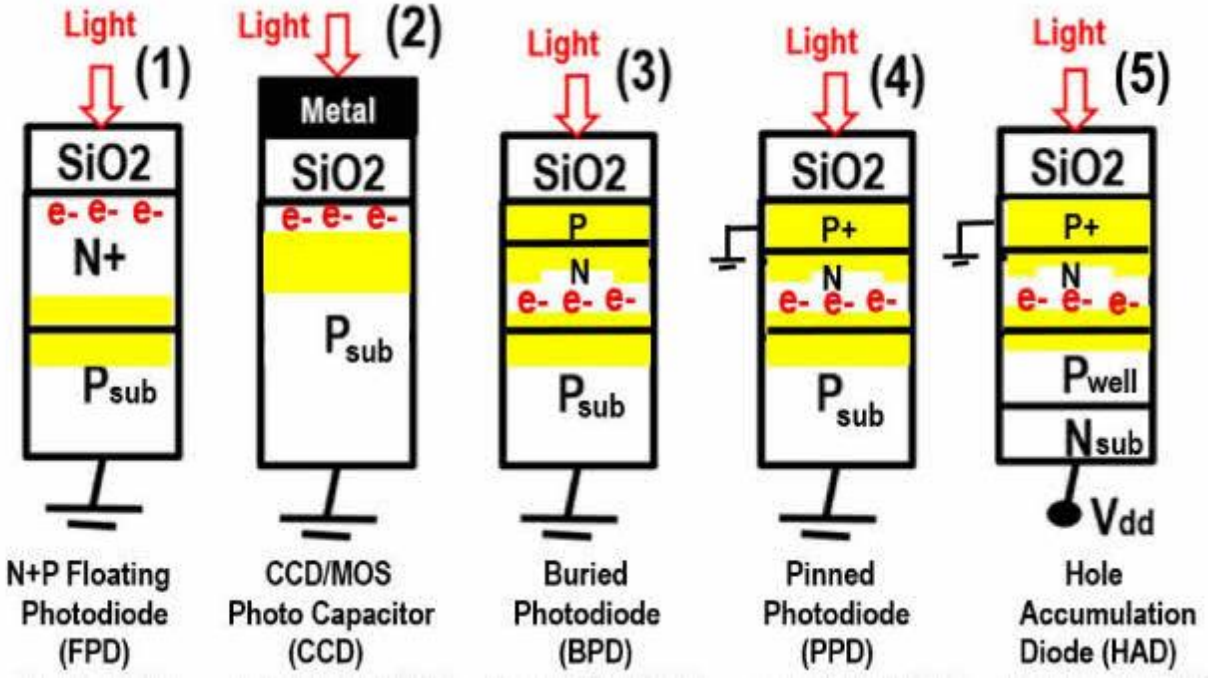


Yoshiaki. Hagiwara, Japanese Patent Applications JPA 1975-127647, JPA 1975-127647 and JPA 1975-134985.

5 Double and Triple junction Dynamic Photo Transistors

The double and triple dynamic junction type dynamic photo transistors have the built-in vertical overflow drain (VOD) function, with the completely mechanical free shutter function which enables fast acquisitions of high speed action pictures.

Different kinds of Photon Detecting Device (PDD)

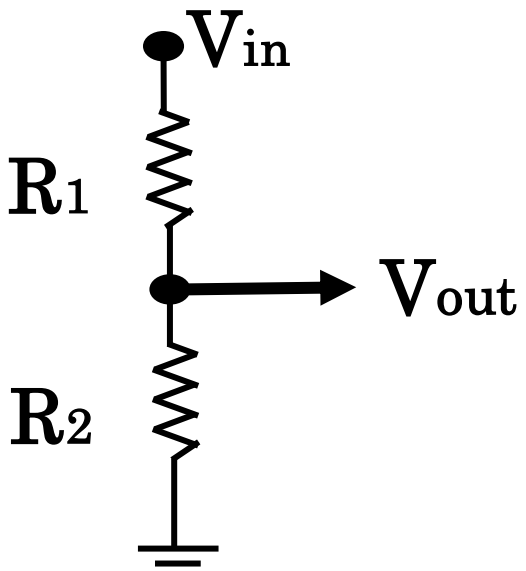


Yoshiaki. Hagiwara, Japanese Patent Applications JPA 1975-127647, JPA 1975-127647 and JPA 1975-134985.

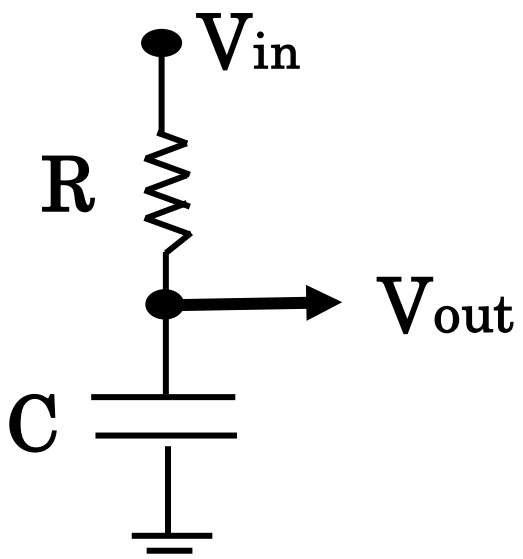
5 Double and Triple junction Dynamic Photo Transistors

In electrical circuits, resistors (R) and capacitors (C) are used as most common elementary circuit elements. A circuit composed of only resistors (R) is called a static circuit while a circuit composed of resistors (R) and Capacitors (C) is called as a dynamic circuit.

A simple static R_1R_2 circuit



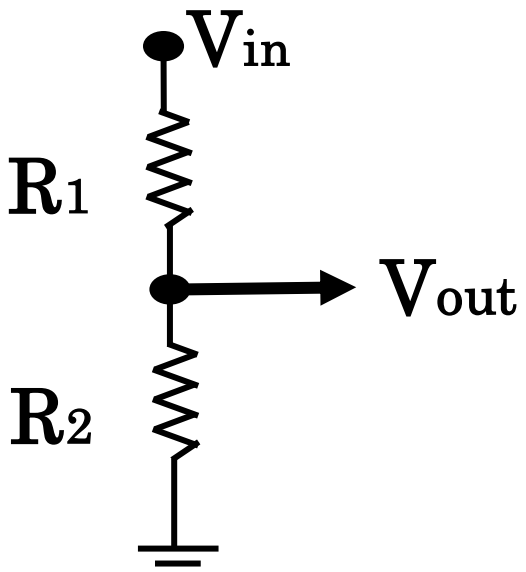
A simple dynamic RC circuit



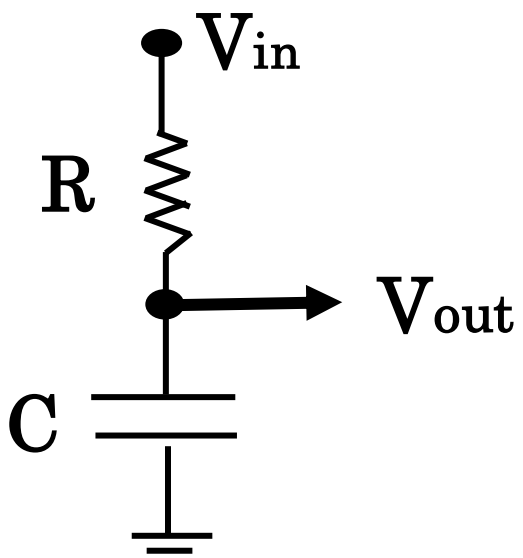
5 Double and Triple junction Dynamic Photo Transistors

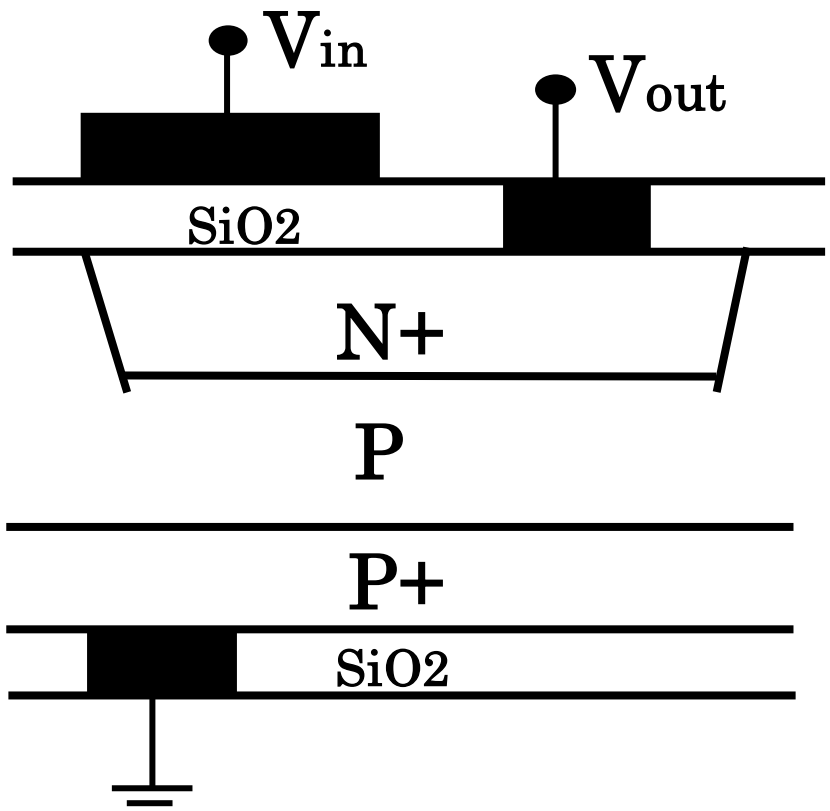
A simple structure of a heavily doped N+ diffusion region in the P type semiconductor substrate with a metal gate on the SiO2 layer can be modeled as a dynamic electrical circuit with resistor (R) and capacitor (C) circuit components.

A simple static R1R2 circuit



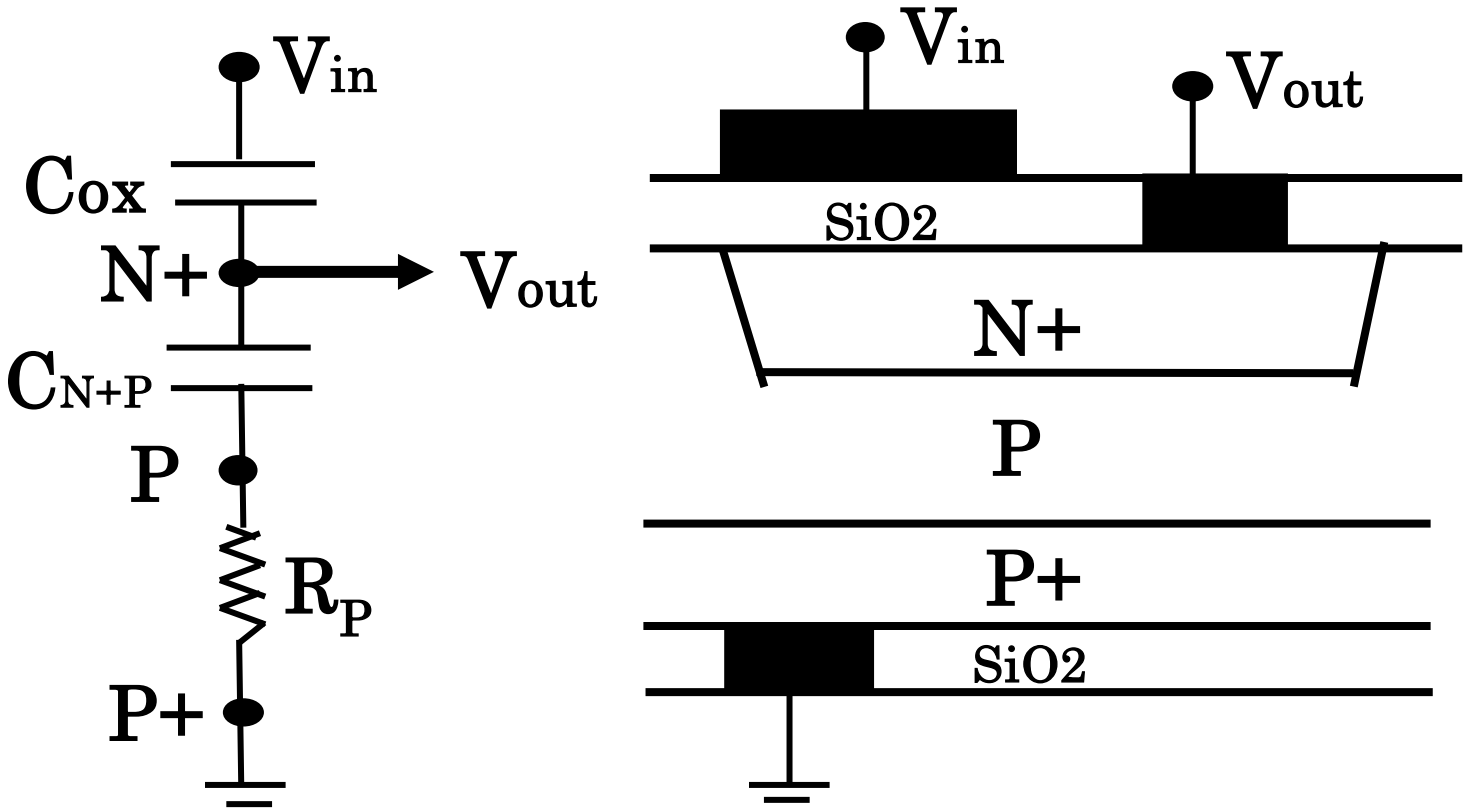
A simple dynamic RC circuit





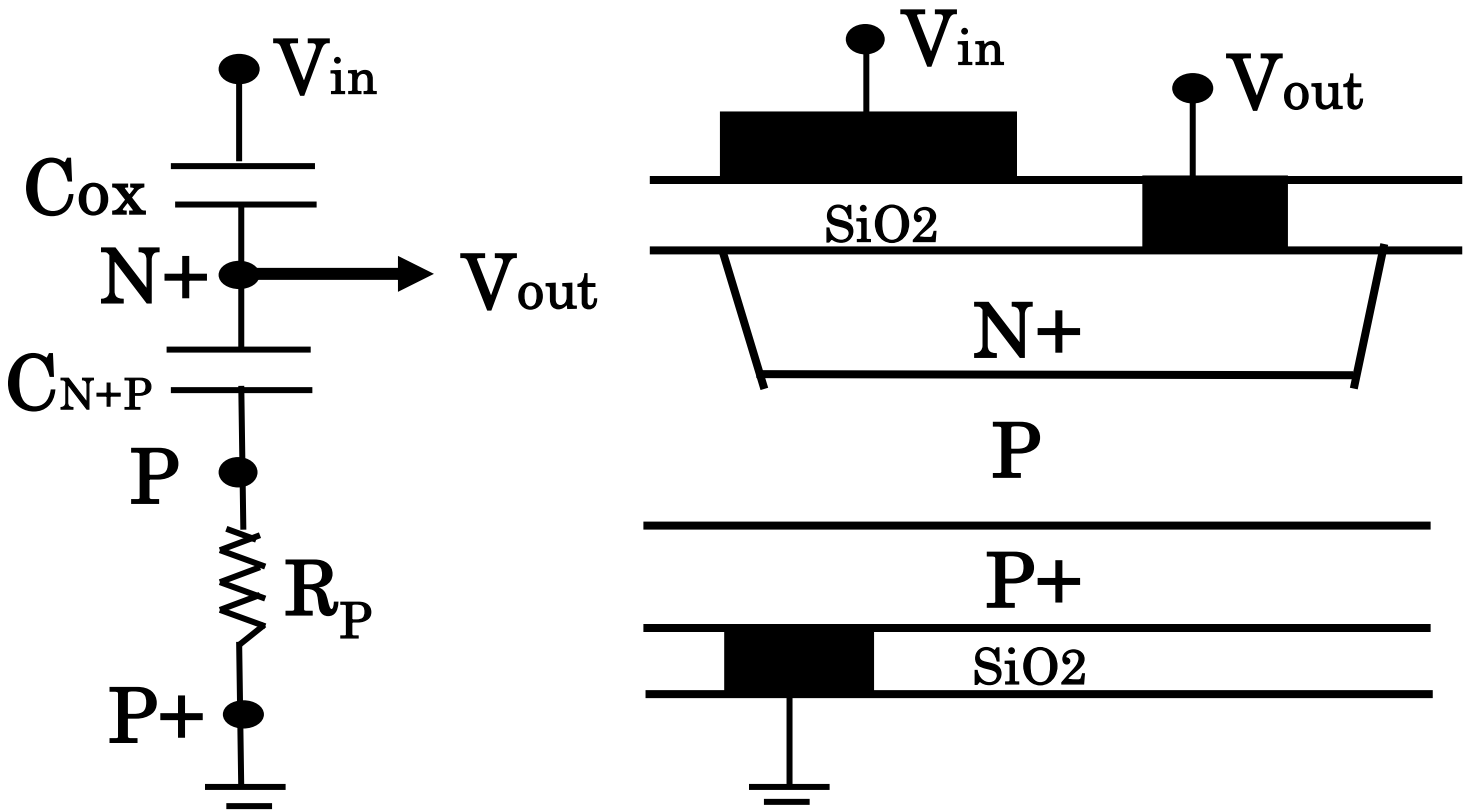
5 Double and Triple junction Dynamic Photo Transistors

We assume that the heavily doped N+ and P+ regions have no resistance but the P region has a resistance R_P. There is also the N+P junction diode depletion region capacitance C_{N+P} and the oxide capacitance C_{ox} in series.



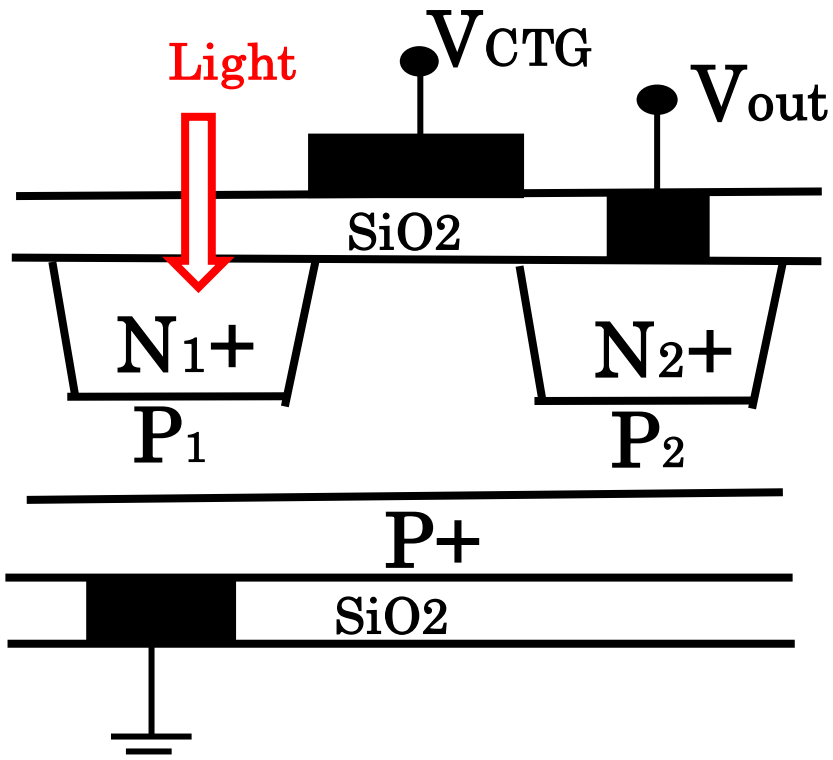
5 Double and Triple junction Dynamic Photo Transistors

When the N+P junction diode is reversely biased, the diode leakage current is negligible and we model the N+P junction diode simply as a dynamic capacitor circuit element C_{N+P}.



5 Double and Triple junction Dynamic Photo Transistors

The floating N+P single junction Photodiode under our study can also be modeled similarly as a circuit composed of simple resistors (R) and capacitors (C) .



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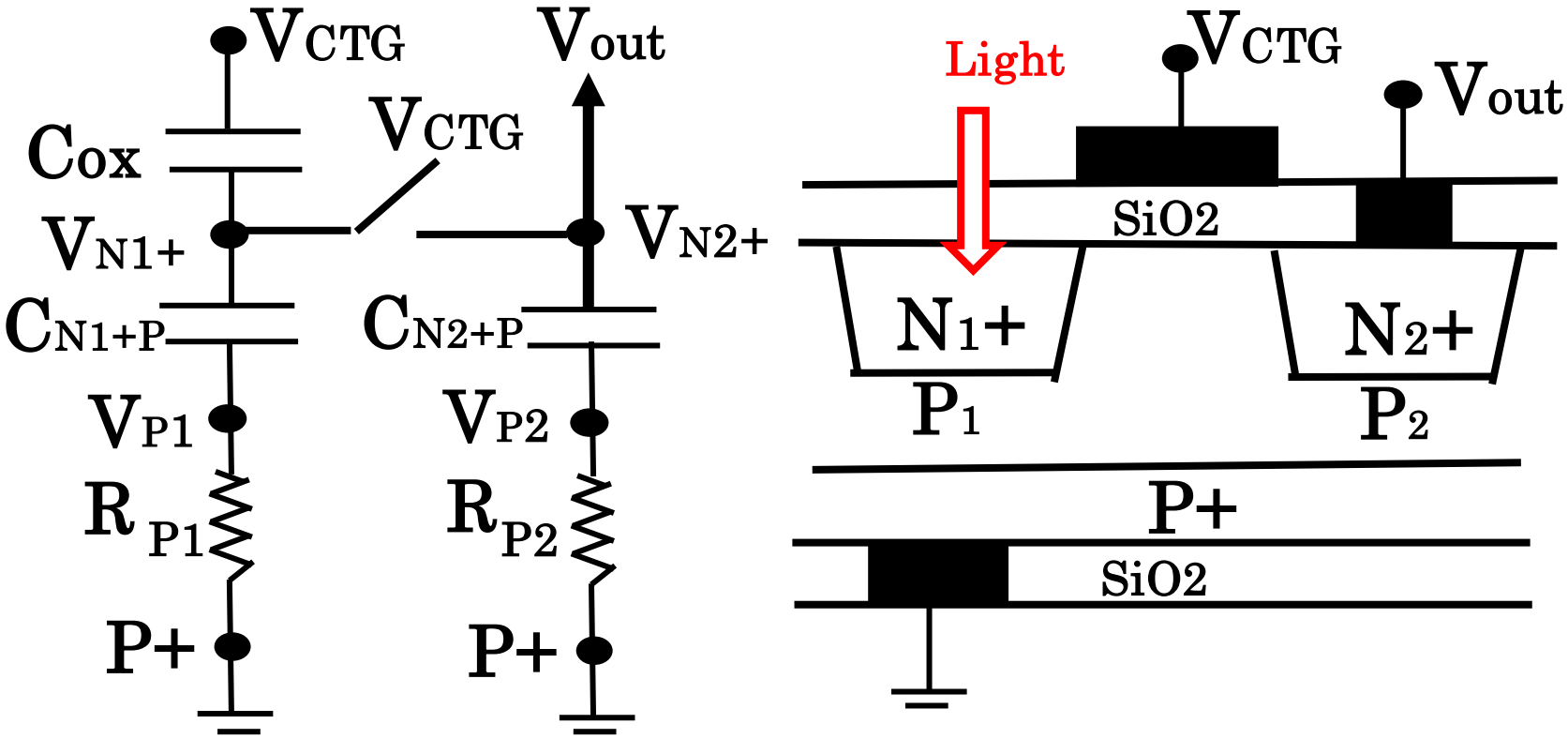
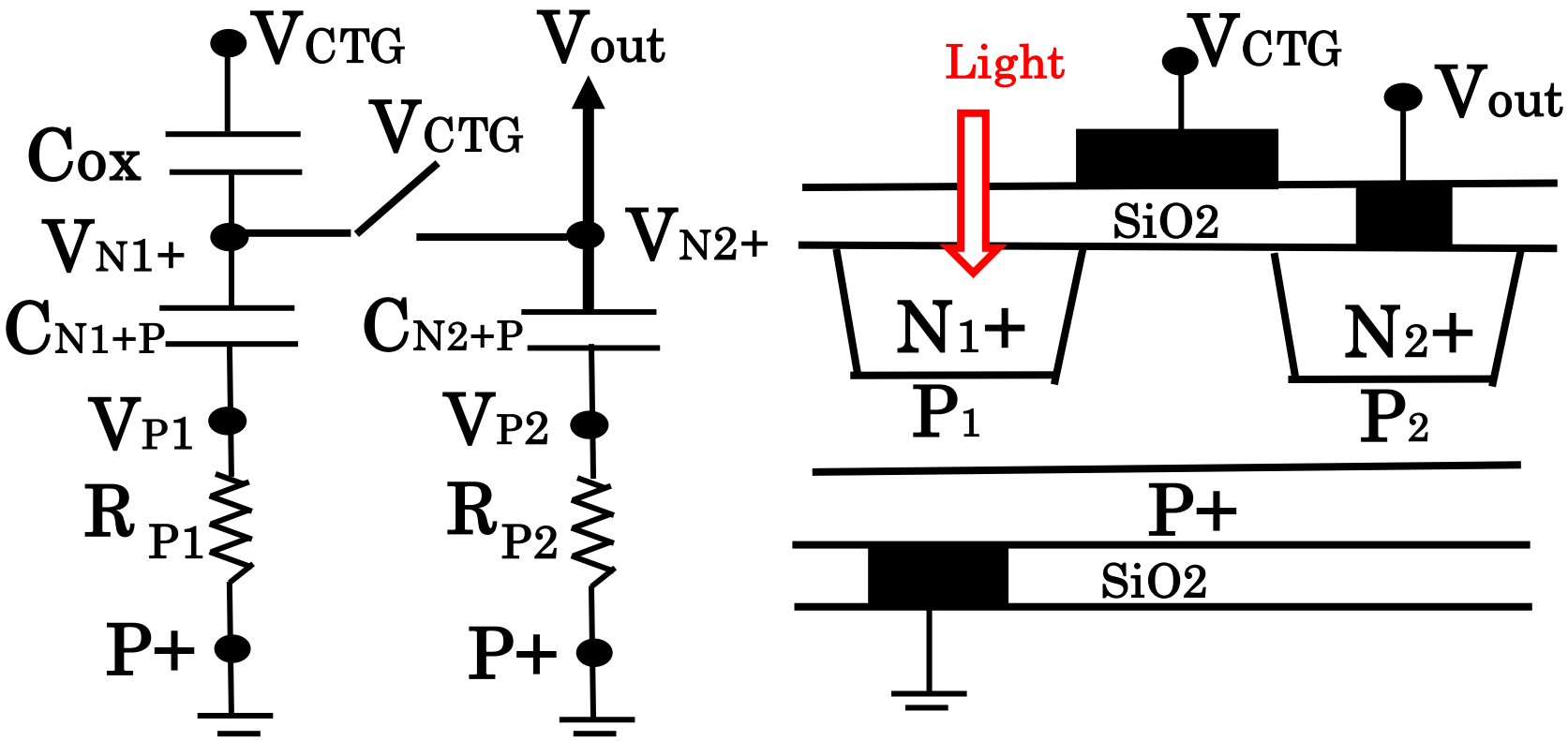


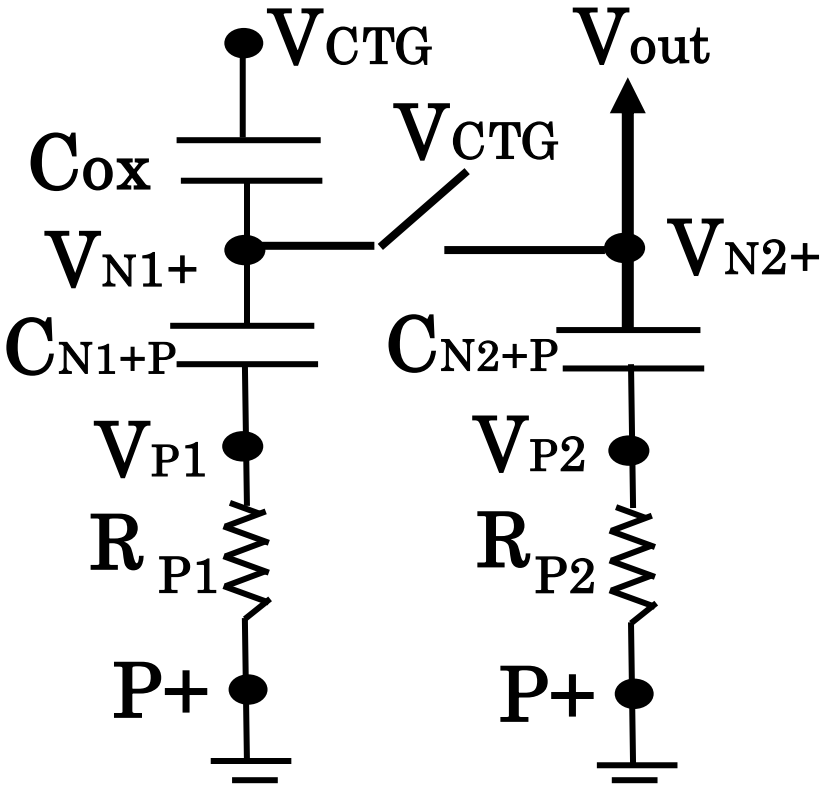
5 Double and Triple junction Dynamic Photo Transistors

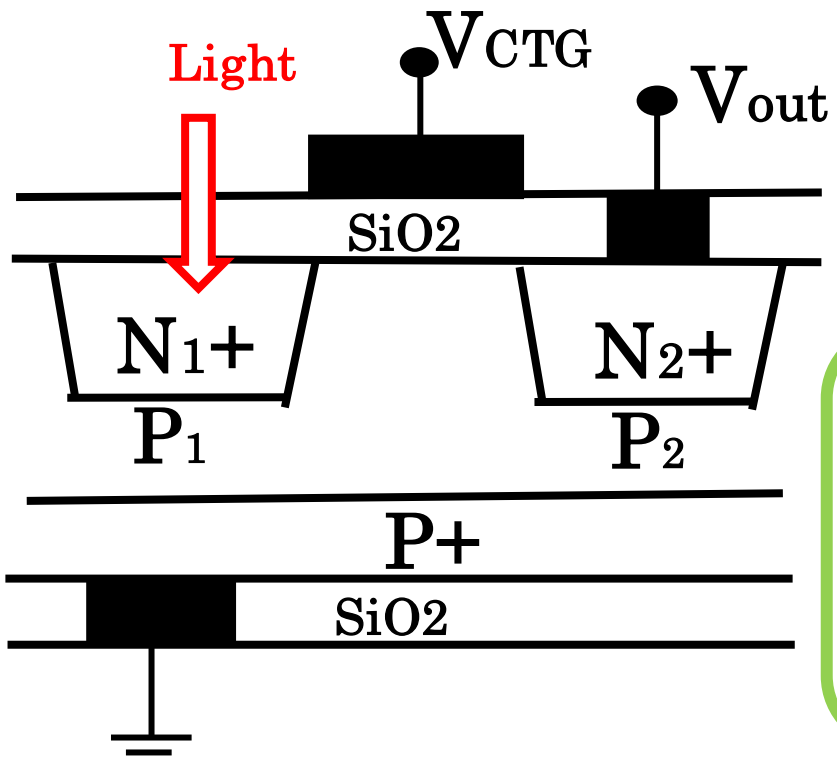
MOS charge transfer gate (CTG) is modeled as a switch with the source terminal as the floating N_1+ charge storage region.



5 Double and Triple junction Dynamic Photo Transistors

The potential V_{N1+} of the floating N_1+ charge storage region is coupled to the charge transfer gate voltage V_{CTD} by the SiO2 oxide capacitance Cox.





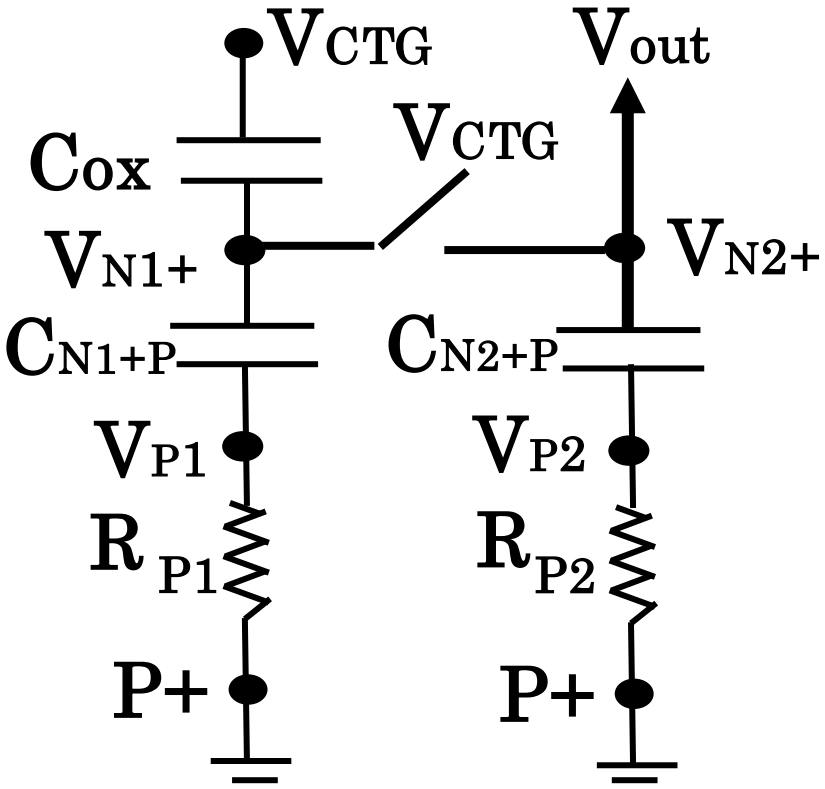
The floating N+P single junction Photodiode has a serious undesired Image Lag Problem.

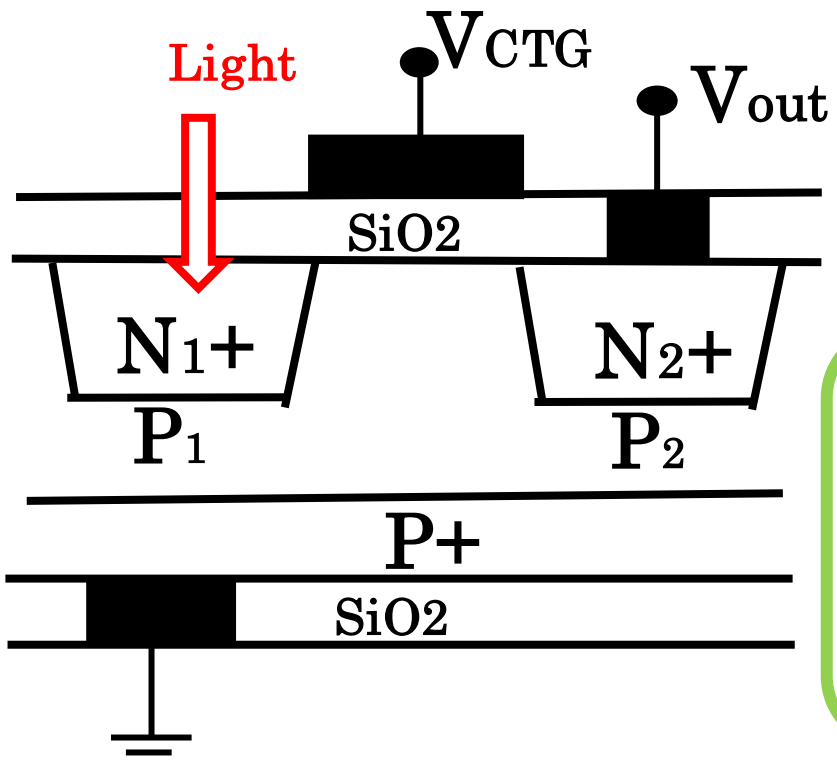
$$C_{N1+P} << C_{N2+P}$$

$$\Delta V_{N1} = \frac{Cox\,\Delta V_{CTG}}{C_{N1+P}}$$

5 Double and Triple junction Dynamic Photo Transistors

Undesired fluctuation ΔV_{N1} proportional to the CTG voltage pulse ΔV_{CTG} appears in the floating N_1+ charge storage region .





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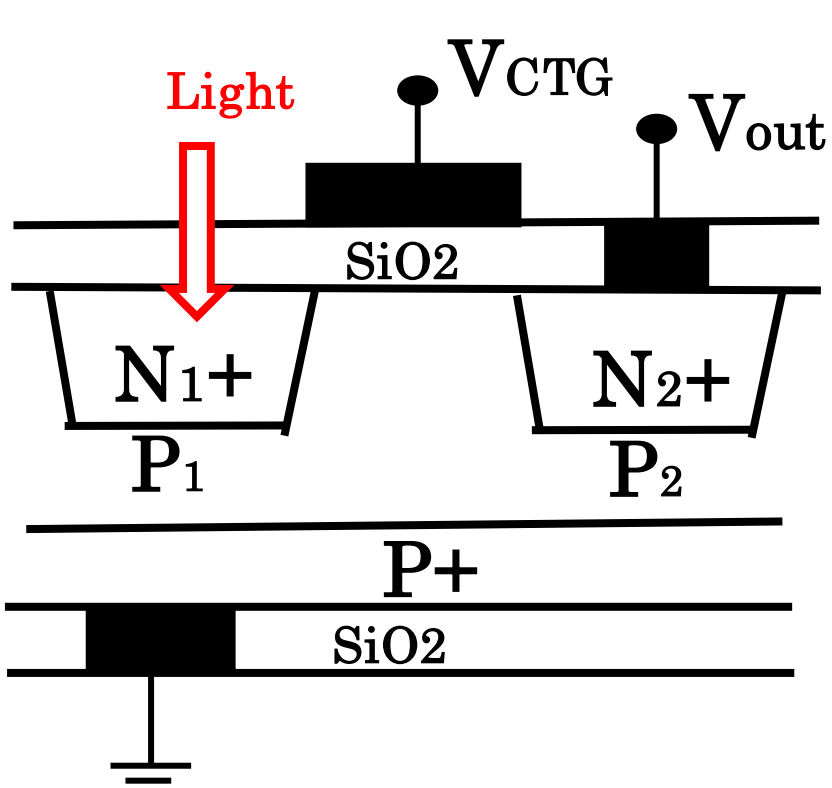
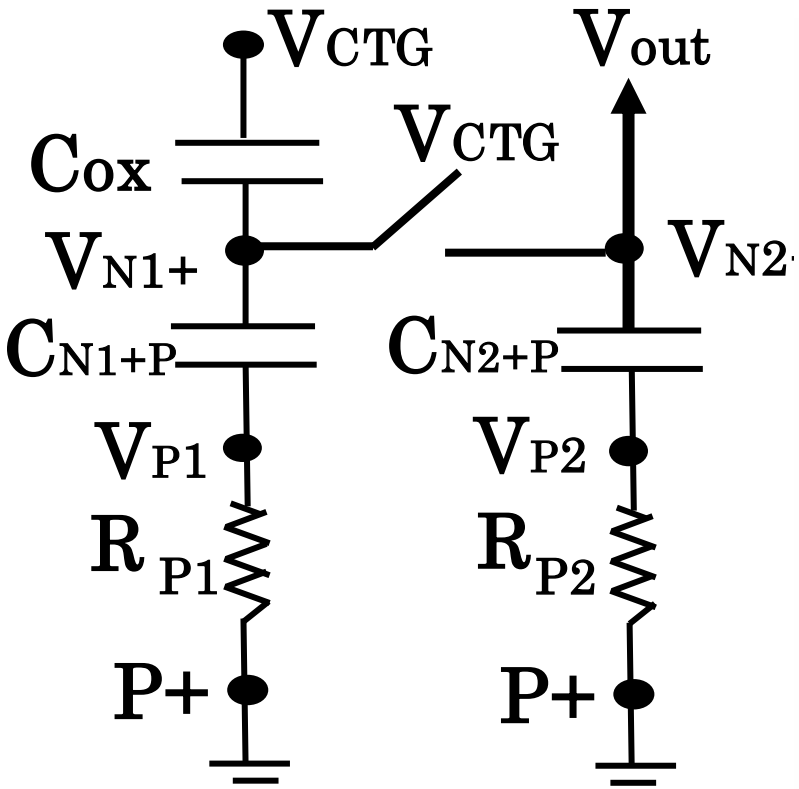
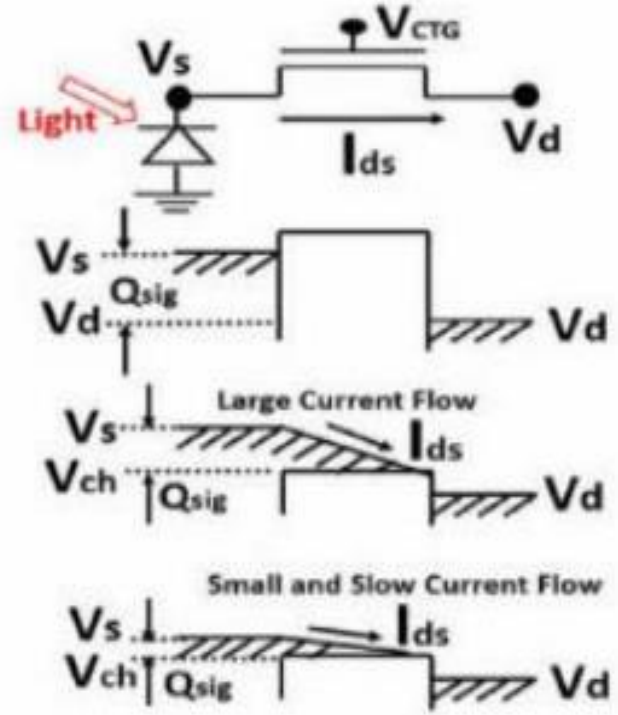
5 Double and Triple junction Dynamic Photo Transistors

Besides, when the floating surface N+ potential V_{N1+} becomes close to the surface channel potential under the charge transfer gate (VTG), the remaining photo signal charge become slow to move.

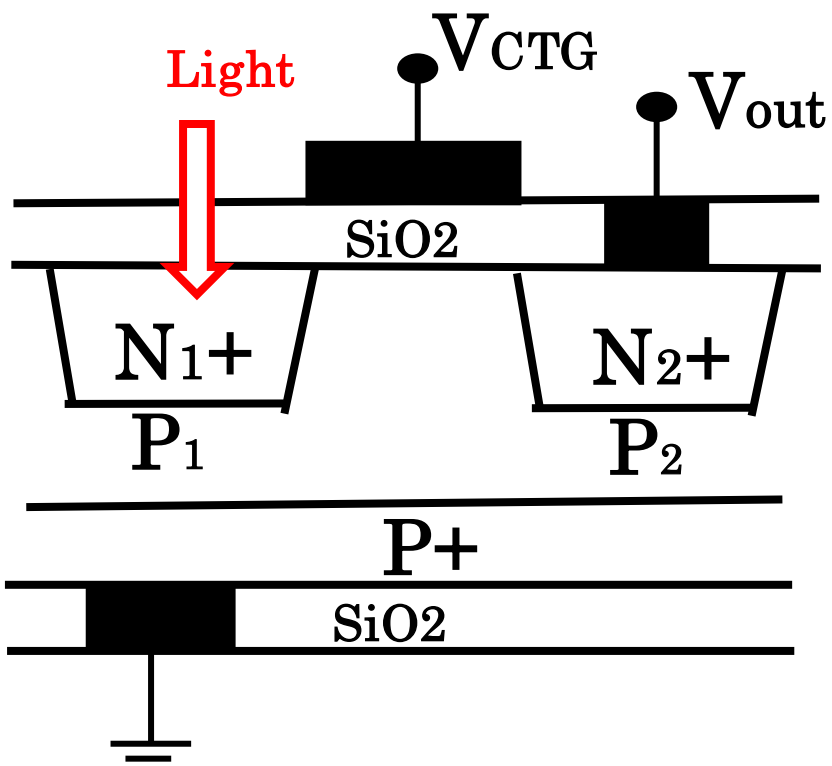


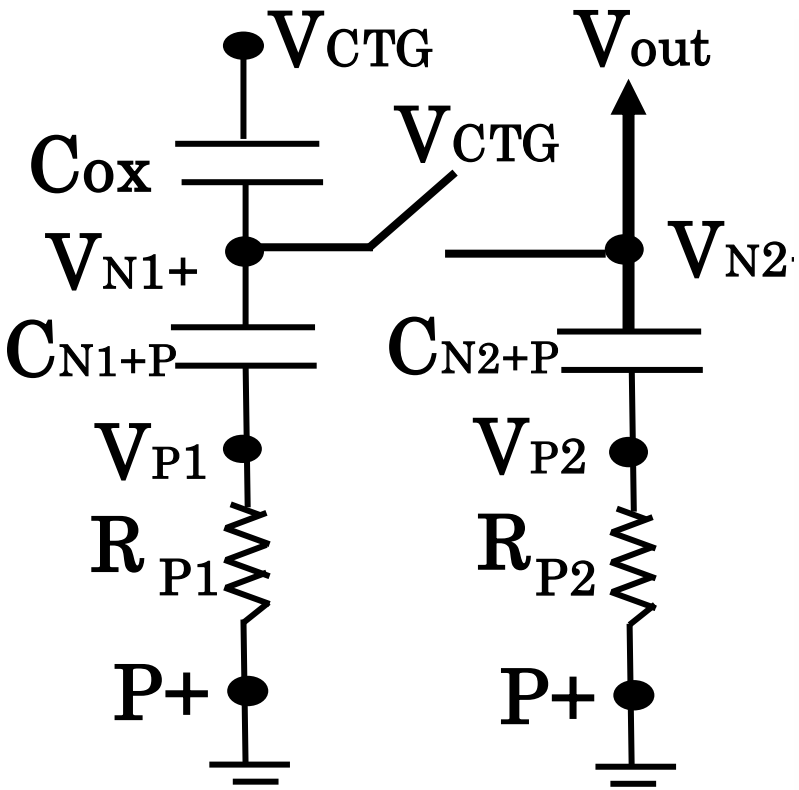


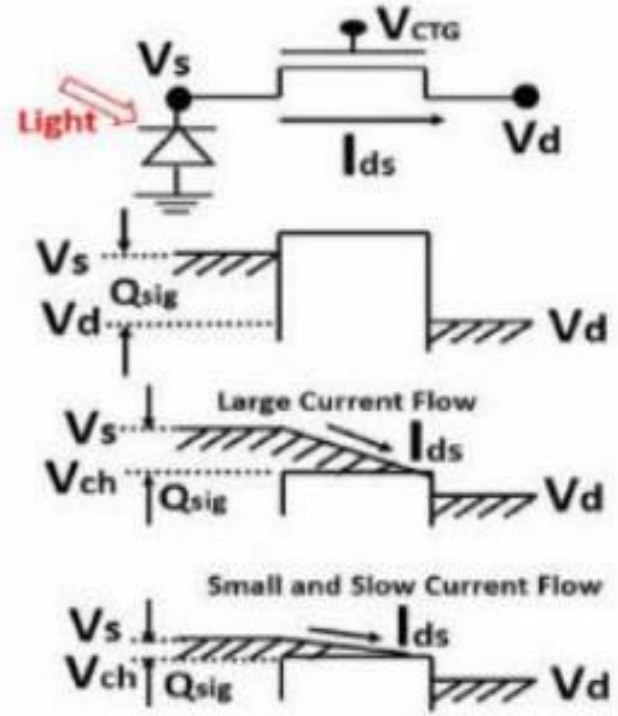


5 Double and Triple junction Dynamic Photo Transistors

Due to the limited short reset switching time, the photo signal charge cannot be transferred completely, and the serious image lag problem occurs.

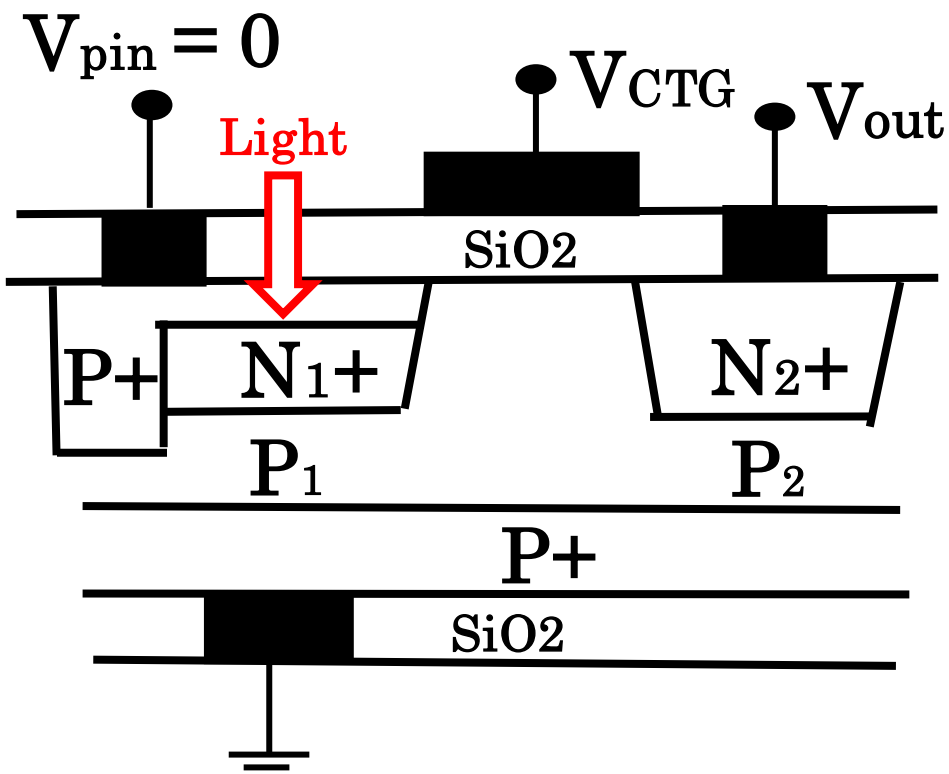


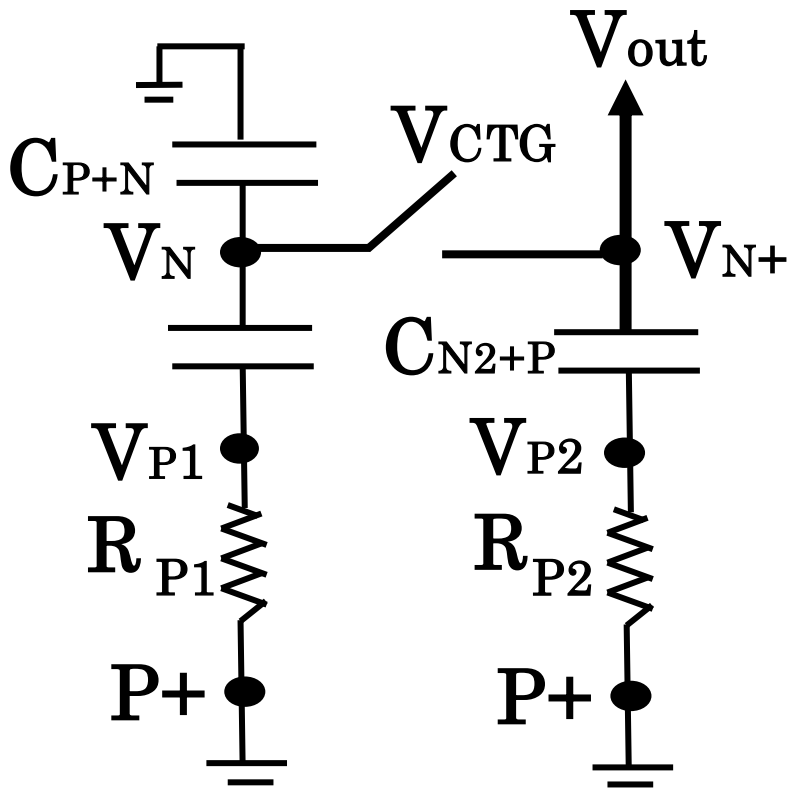


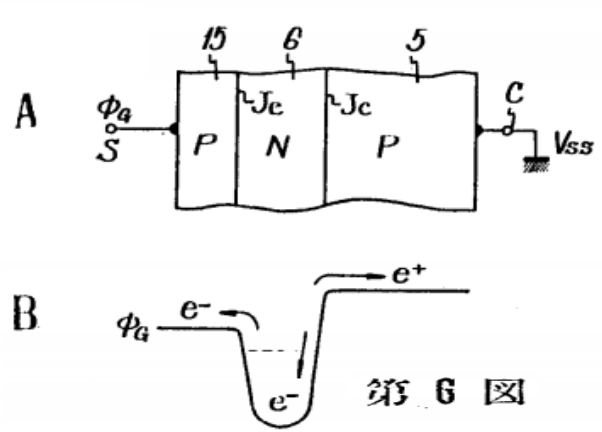


5 Double and Triple junction Dynamic Photo Transistors

Hagiwara at Sony proposed in 1975 the double and triple junction type dynamic photo transistors with the pinned surface majority carrier accumulation region.







The dynamic photo transistor shown in Fig. 6 of JPA 1975-134985

Yoshiaki. Hagiwara, Japanese Patent Applications JPA 1975-127647, JPA 1975-127647 and JPA 1975-134985.

5 Double and Triple junction Dynamic Photo Transistors

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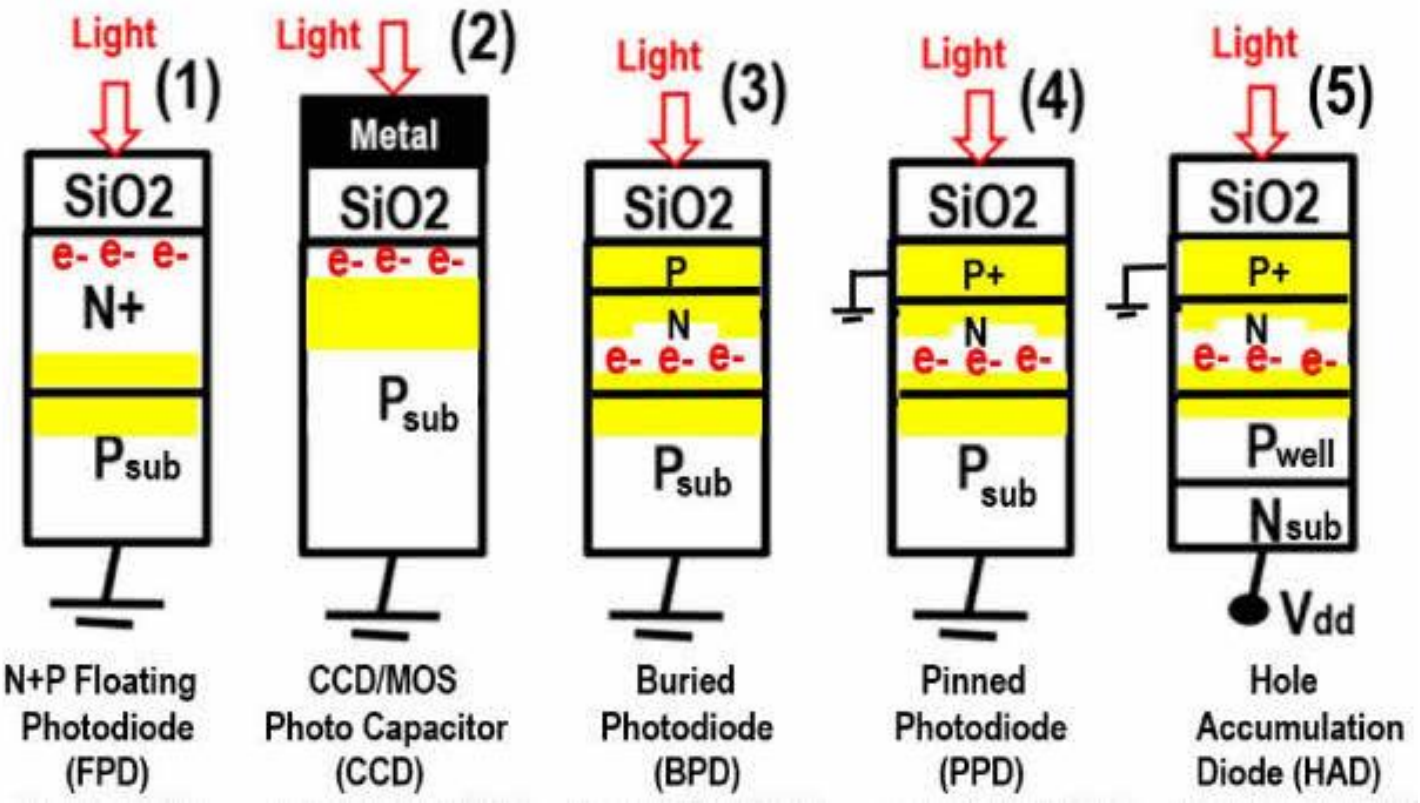
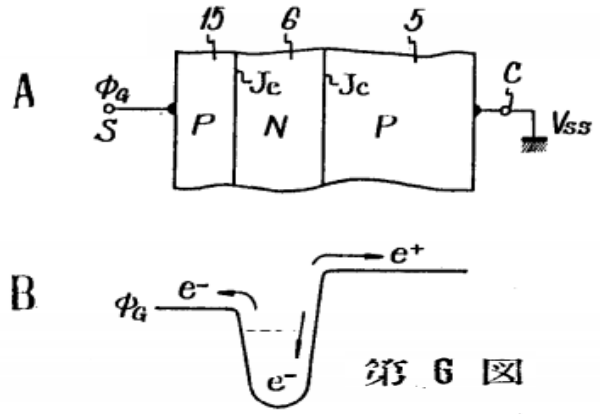
Different kinds of Photon Detecting Device (PDD)





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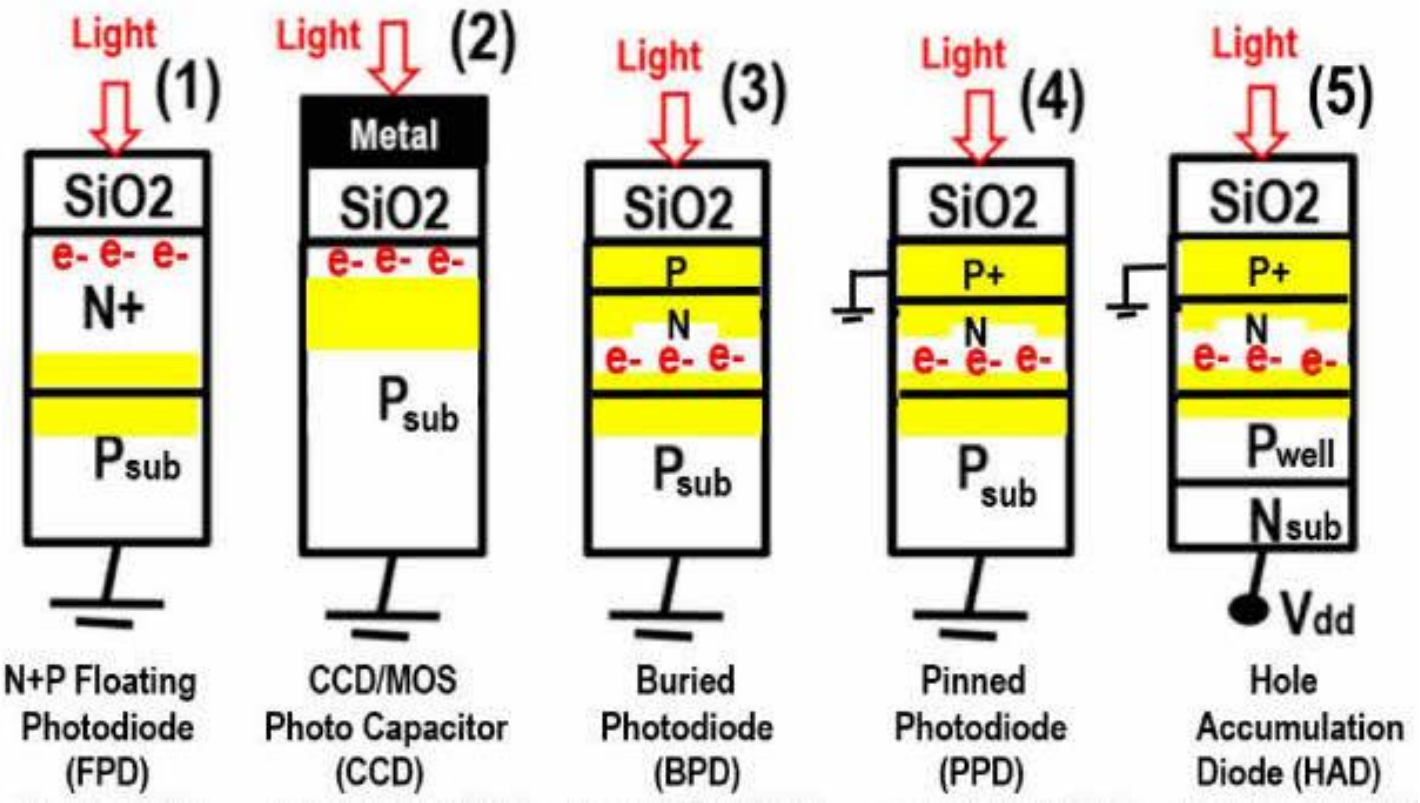
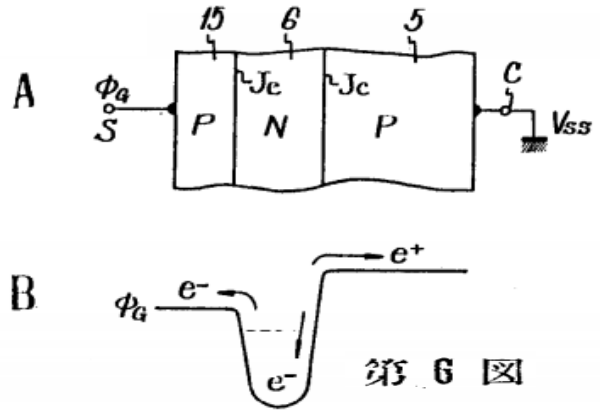
Yoshiaki. Hagiwara, Japanese Patent Applications JPA 1975-127647, JPA 1975-127647 and JPA 1975-134985.

5 Double and Triple junction Dynamic Photo Transistors

The P+ surface hole accumulation region is pinned by the adjacent heavily doped channel stops or by the adjacent metal contact as an option.

Different kinds of Photon Detecting Device (PDD)





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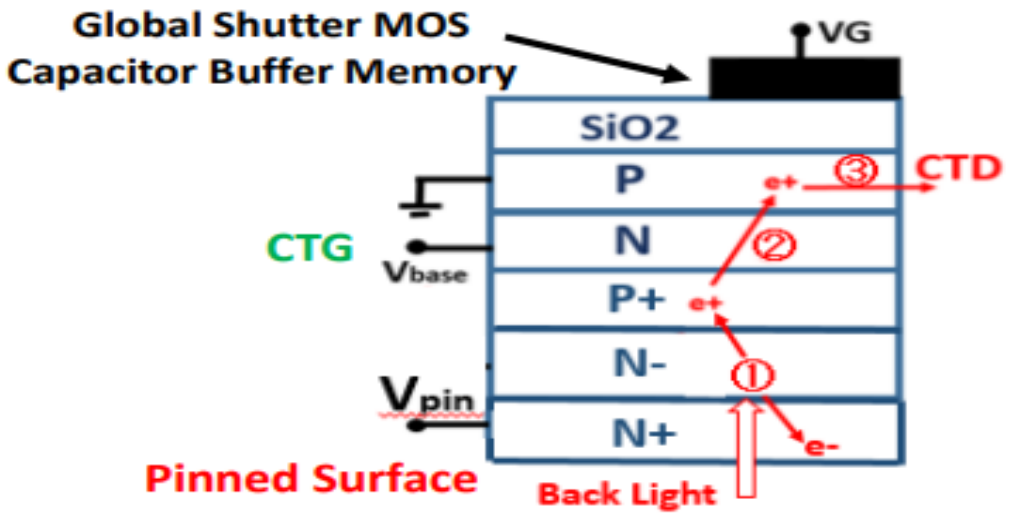
Yoshiaki. Hagiwara, Japanese Patent Applications JPA 1975-127647, JPA 1975-127647 and JPA 1975-134985.

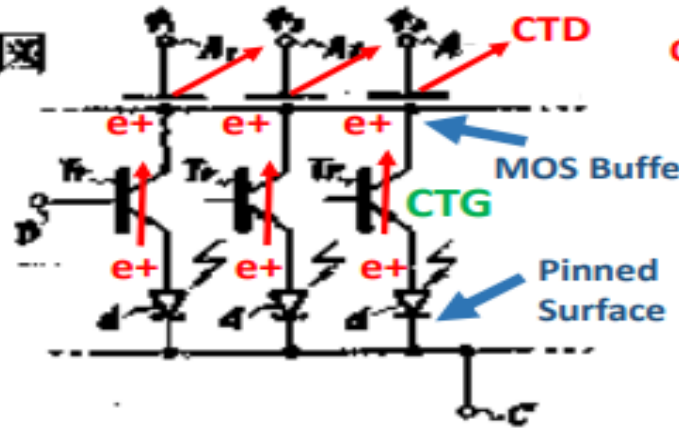
JPA 1975-127646 filed by Yoshiaki Hagiwara, 1975.

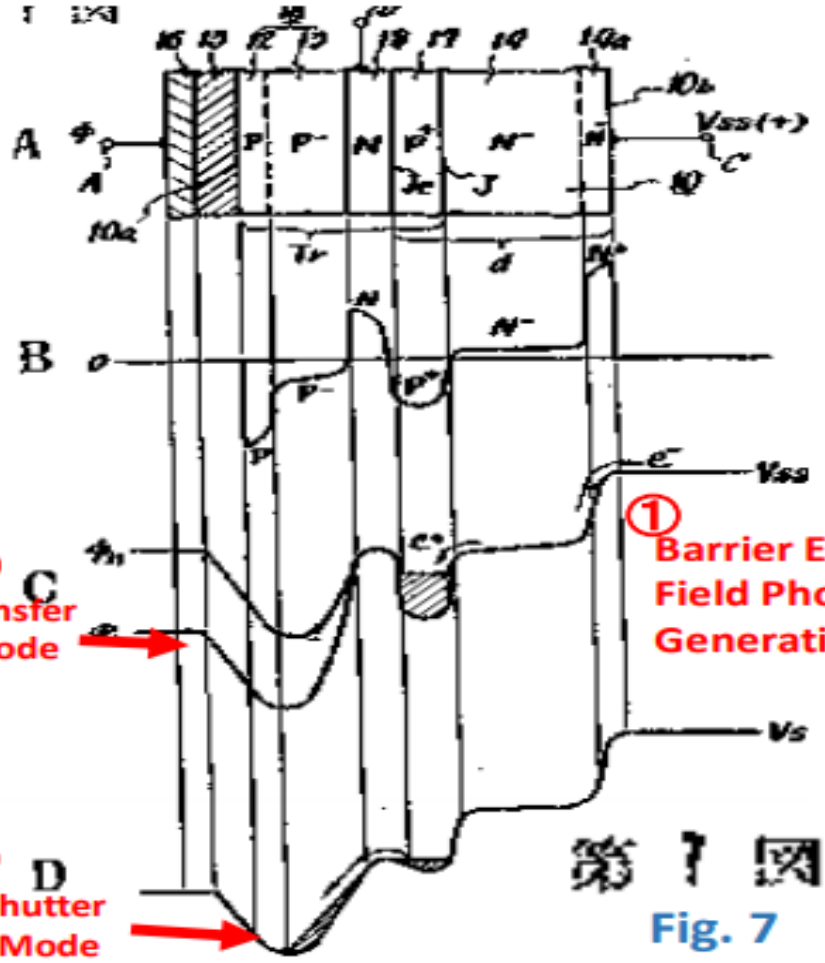
N+NP+NP junction type Buried Pinned Photodiode with Built-in MOS Capacitor Buffer Memory Global Shutter Function and the surface N+N doping slope Barrier Electric Field Photo Pair Generation



第 6 図

Fig. 6





第 7 図

Fig. 7

Japanese Patent Application JPA 1975-127646

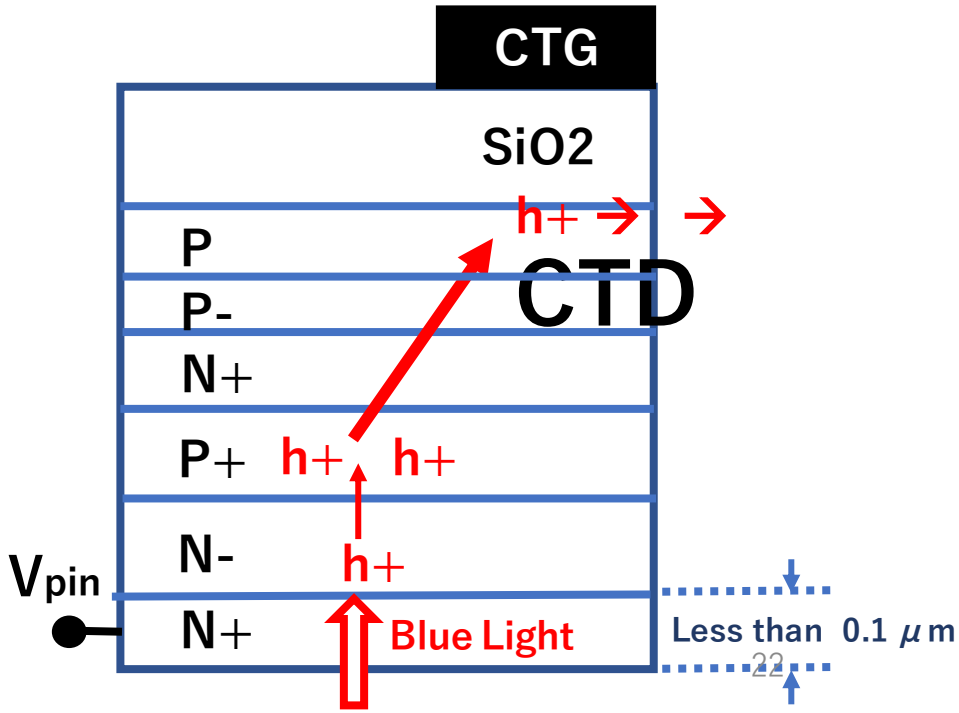
applied by Yoshiaki Hagiwara at Sony on October 23, 1975

Patent Claim in Original Japanese	Patent Claim in English Translation
1) 半導体基体(Nsub)の一方の主面側に、	1) Along the main surface of a semiconductor substrate (Nsub),
2) 絶縁膜(SiO2)を介して電荷転送装置(CTD)が被着される１の導電型の転送領域(P)が形成され、	2) the charge transfer device (CTD) is placed upon the oxide whereby the type 1 charge transfer region (P) is formed,
3) 之(P)に対向して且つ之より上記半導体基体(Nsub)の他方の主面側に上記転送領域(P)との間に他の電導型のベース領域(N)を介して受光領域(P+)が形成され、	3) On the opposite side of the region (P), the light detecting region (P+) is formed on the backside substrate (Nsub), with the base region (N) of another type as a bridge.
4) 上記ベース領域(N)に所定の電圧(A)を印加することにより上記受光領域に蓄積した電荷を上記転送領域に転送し、	4) By applying a voltage pulse (A) to the base region (N), the charge (h+) stored in the charge detecting region (P+) is transferred to the charge transfer region (P).
5) 上記電荷転送領域用領域(CTG(に所定のクロック電圧(B)	5) By applying a proper clock voltage (B) to the charge transfer gate (CTG), the charge (h+) is properly transferred further.

File 1975-127646 Filed 1975/10/23
Public 1977-051815 on 1977/04/26

Buried Pinned Photodiode Patent

the NPNP Triple Junction type
Dynamic Photo Thyristor
with P-type Charge Carrier （h +） Buried Chann
CCD/MOS Dynamic Capacitor type Buffer Memo
used for Instant Photo Charge （h +） Storage
to achieve Global Shutter Function



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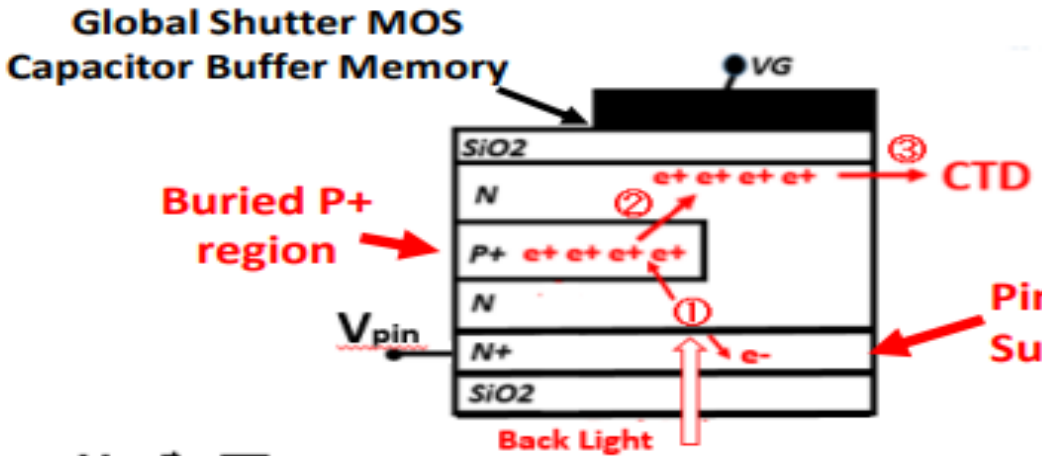

第 6 図

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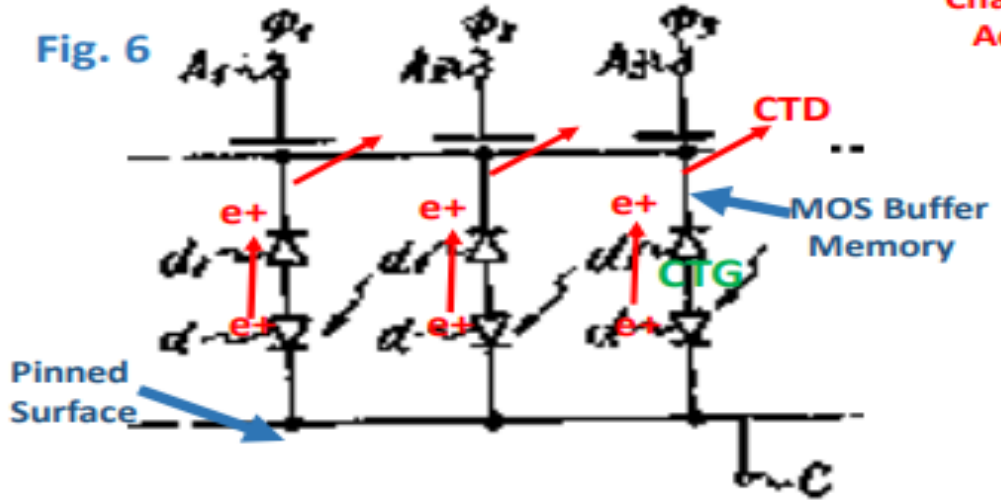

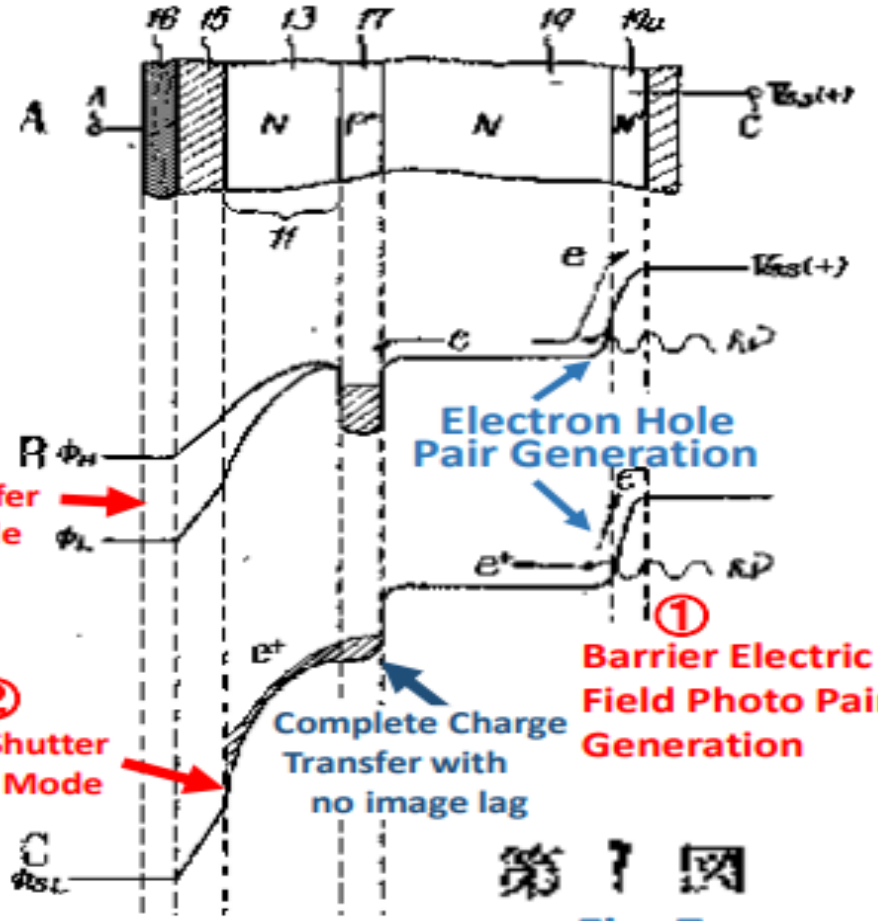

第 7 図

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Japanese Patent Application JPA 1975-127647

applied by Yoshiaki Hagiwara at Sony on October 23, 1975

Patent Claim in Original Japanese

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2) 絶縁膜(SiO2)を介して電荷転送用電極(CTG)が被着配列される１の導電型の転送領域(N)が形成され、

3) 之(N)より上記半導体基体(Nsub)の他方の主面側に上記転送領域(N)に接する他の導電型の領域と該領域に接する１の導電型の領域(N)とより成る受光領域(P+)が形成され、

4) 上記転送用電極(CTG)に所要の電圧(A)を印加することにより、上記受光領域に蓄積した電荷を上記転送領域に転送し、

5) 上記電荷転送用電極に上記所要の電圧（A)とは異なるクロック電圧（B)を印加して上記基体の上記一方の主面に沿って電荷の転送を行うようにしたことを特徴とする個体撮像創装置

Patent Claim in English Translation

1) Along the main surface of a semiconductor substrate (Nsub),

2) the charge transfer gates (CTG) is placed upon the oxide, under which the type 1 charge transfer region (N) is formed.

3) The light detecting region (P+) is formed in the backside of the substrate which is closely placed with both the surface charge transfer region (N) and the back side surface of the substrate (Nsub).

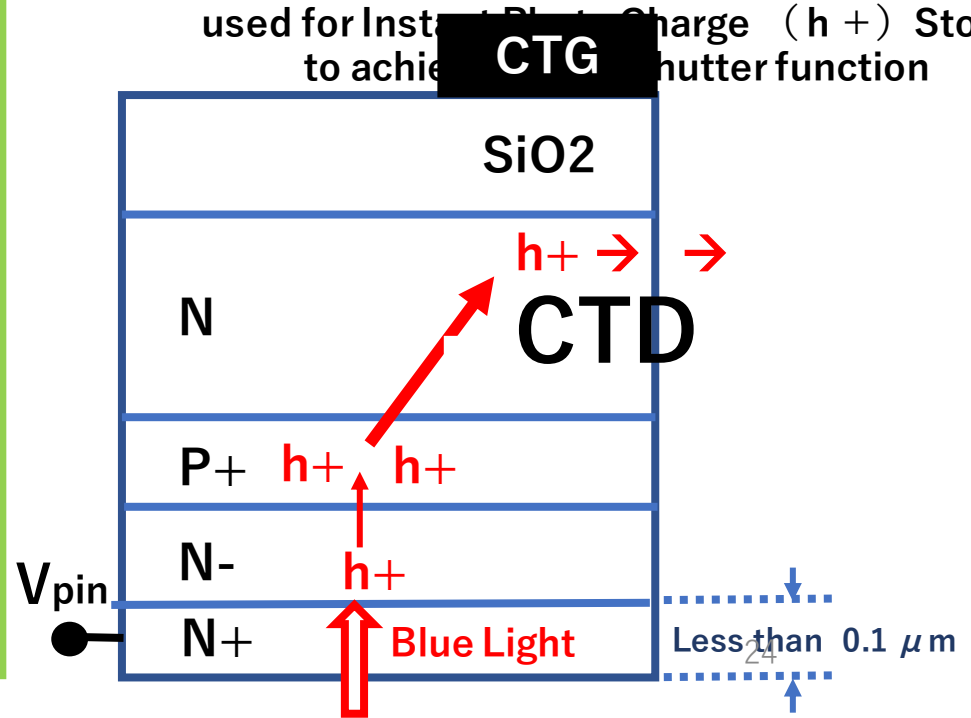
4) By applying a voltage pulse(A) to the Charge Transfer Gate (CTG) the charge (h+) stored in the charge detecting region (P+) is transferred to the surface charge transfer region (N).

5) By applying a another deferent clock voltage (B) to the charge transfer gate (CTG), the charge (h+) is transferred further along the main surface of the substrate.

File 1975-127647 Filed 1975/10/23
Public 1977-051816 on 1977/04/26

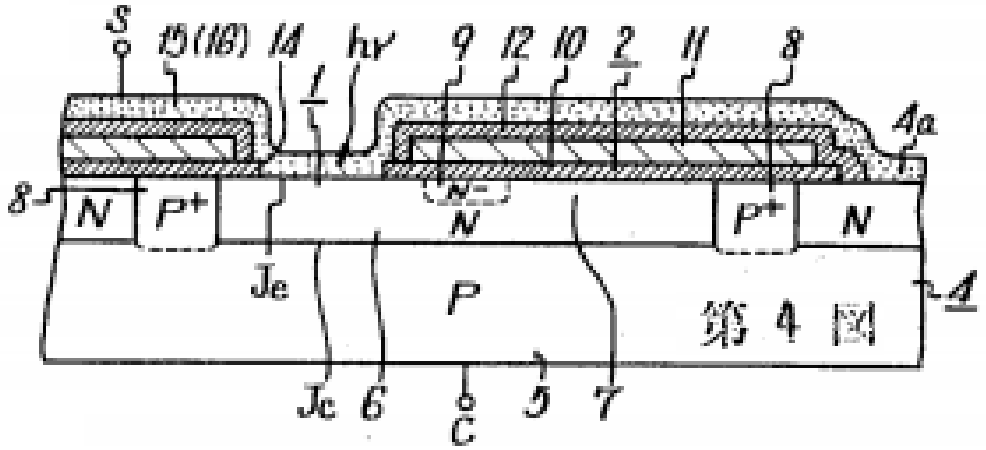
Buried Pinned Photodiode Patent

the NPN Double Junction type Dynamic Photo Transistor with P-type Charge Carrier （h +） Surface Channel CCD/MOS Dynamic Capacitor type Buffer Memory used for Inst harge （h +） Sto to achie utter function



JPA 1975-134985 filed by Yoshiaki Hagiwara, 1975.

An example of Schottky Barrier Photodiode shown in Fig. 4 of JPA 1975-134985



An example of PNP junction Pinned Photodiode shown in Fig. 5 of JPA 1975-134985 with the VOD metal contact as an option.

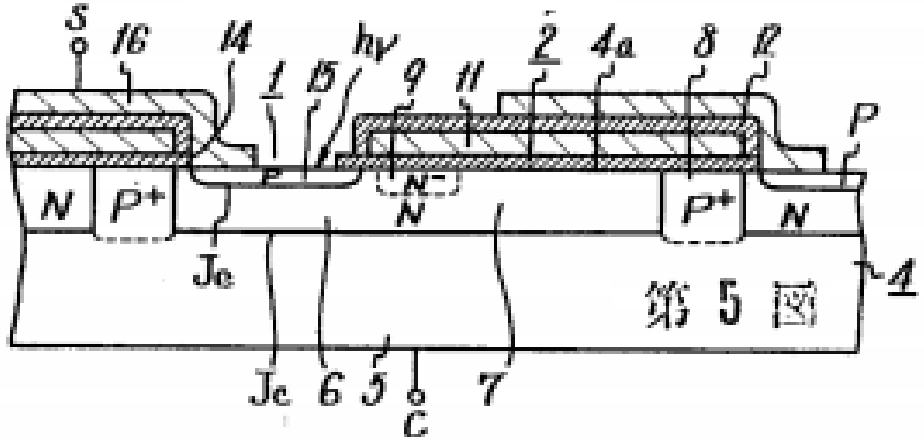
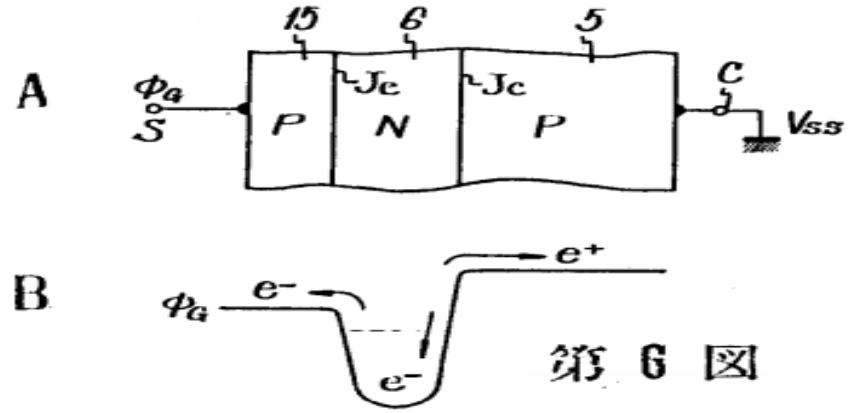
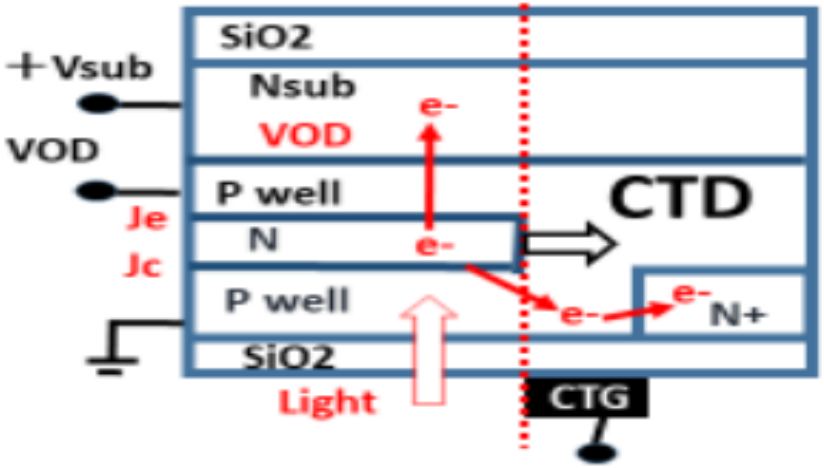


Fig. 6 of JPA 1975-134985





Dynamic Photo Transistor defined by the claim of JPA 1975-121975-134985

Japanese Patent Application JPA 1975-134985

applied by Yoshiaki Hagiwara at Sony on November 10, 1975

Patent Claim in Original Japanese

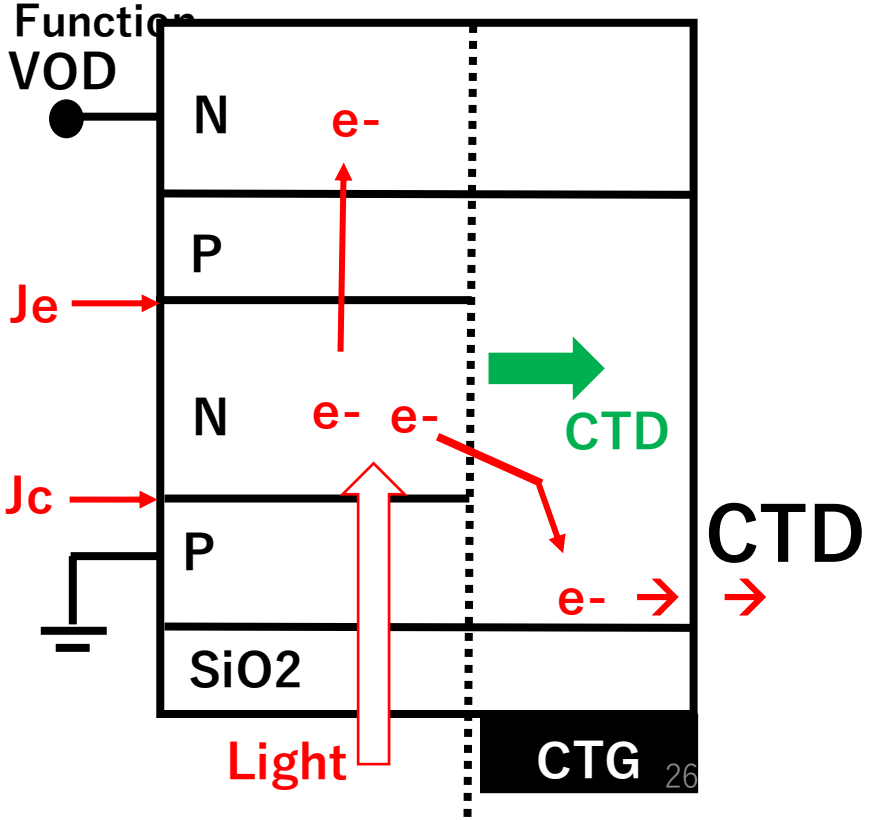
1) 半導体基体(N)に、
2) 第１導電型の第１半導体領域（P)と、之の上に形成された第２導電型の第２半導体領域（N)とが形成されて
3) 光感知部(NP)と之よりの電荷を転送する電荷転送部（CTD)とが上記半導体基体の主面に沿う如く配置されて成る個体撮像装置に於いて
4) 上記光感知部(NP)の上記第２半導体領域（N)に整流性接合が形成され、該接合をエミッタ接合(Je)とし、
5) 上記第１及び第２半導体領域間の接合をコレクタ接合(Jc)とするトランジスタ(PNP)を形成し、
6) 該トランジスタ(PNP)のベースとなる上記第２半導体領域(N)に光学像に応じた電荷を蓄積し
7) ここ(N) に蓄積された電荷を上記転送部に移行させて、その転送を行うようにしたことを特徴とする個体撮像装置

Patent Claim in English Translation

1) In the semiconductor basic body (N),
2) the first region (P) of the first impurity is formed, and on which the second region (N) of the second impurity type is formed.
3) The photo sensor (NP) so defined forms a solid state image sensor with Charge Transfer Device (CTD) placed along the surface of the semiconductor basic body.
4) A rectifying emitter junction (Je) is the second region (N) of the photo sensor (NP).
5) The junction between the first region (P) and the second region (N). being as the collector junction (Jc) of the transistor (PNP),
6) the second region (N) becomes the base region of the transistor (PNP) which stores the photo charge according to the photo image.
7) And the charge stored in this region (N) is transferred to the Charge Transfer Device (CTD).

File 1975-134985 Filed 1975/11/10
Public 1977-058414 on 1977/05/13

Buried Pinned Photodiode Patent
the PNP Double Junction type
Dynamic Photo Transistor
with the Vertical Overflow Drain (VOD)
Function



5 Double and Triple junction Dynamic Photo Transistors

The team of Hagiwara, Ochi and Hashimoto in Sony also invented in 1977 the Electrical Shutter and the Gamma effect clocking schemes using the punch-thru action controlled by the in pixel overflow drain (OFD) voltage with no independently controlled charge transfer gate between the photo charge storage region and the in pixel overflow drain (OFD) region.

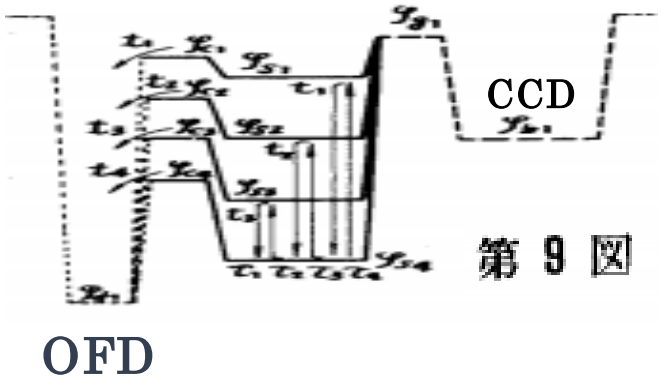


Fig. 9

Gamma Effect Control Mode

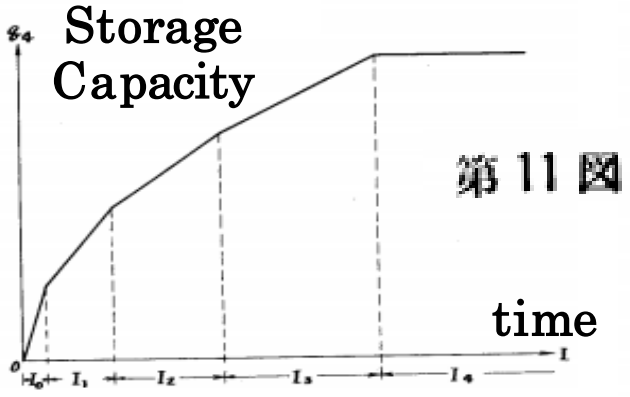


Fig. 11

Gamma Effect Curve

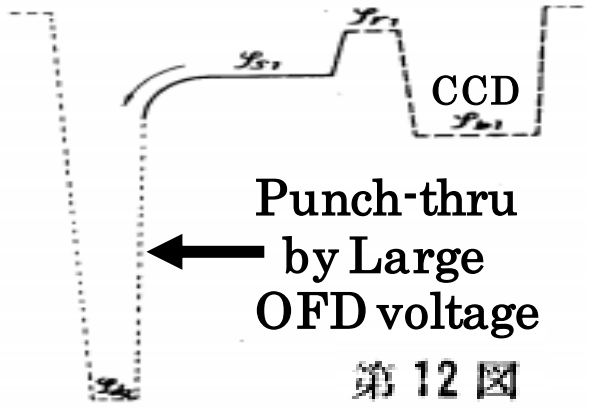


Fig. 12

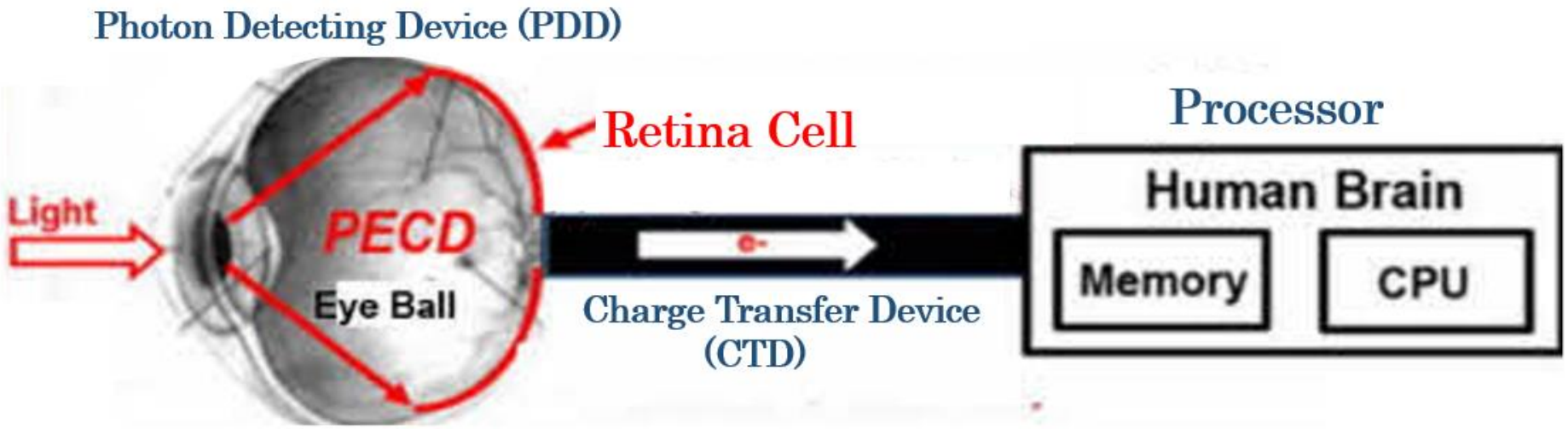
Electric Shutter Mode

Yoshiaki Hagiwara et al, Japanese Patent Application JPA 1977-136885.

5 Double and Triple junction Dynamic Photo Transistors

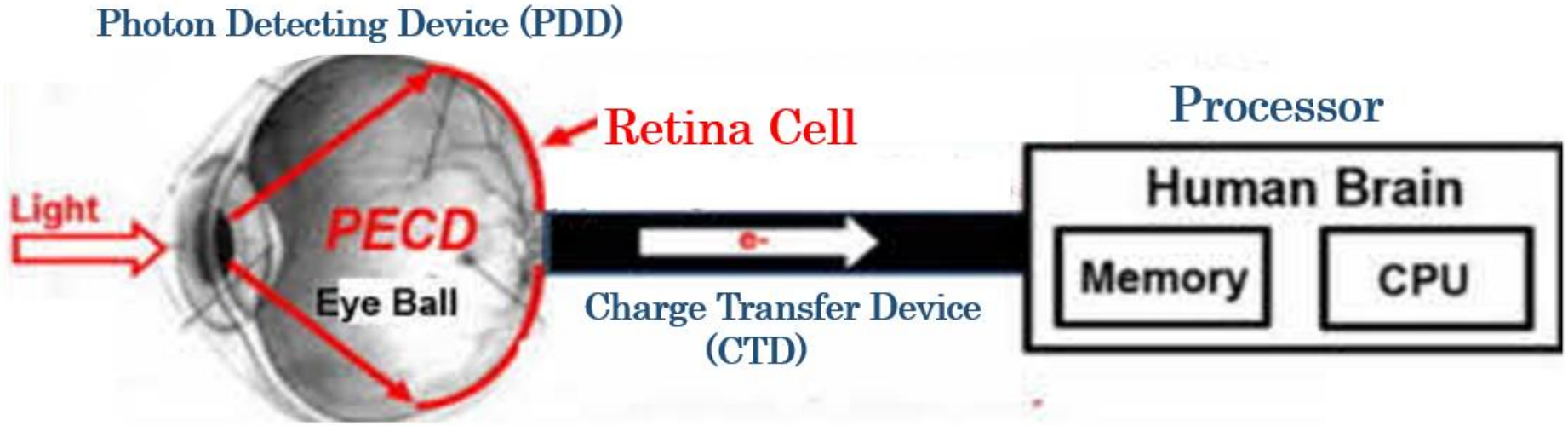
Pinned Photodiode is defined as one special type of Buried Photodiode.

Pinned Photodiode is by necessity always Buried Photodiode.
But Buried Photodiode is not always Pinned Photodiode



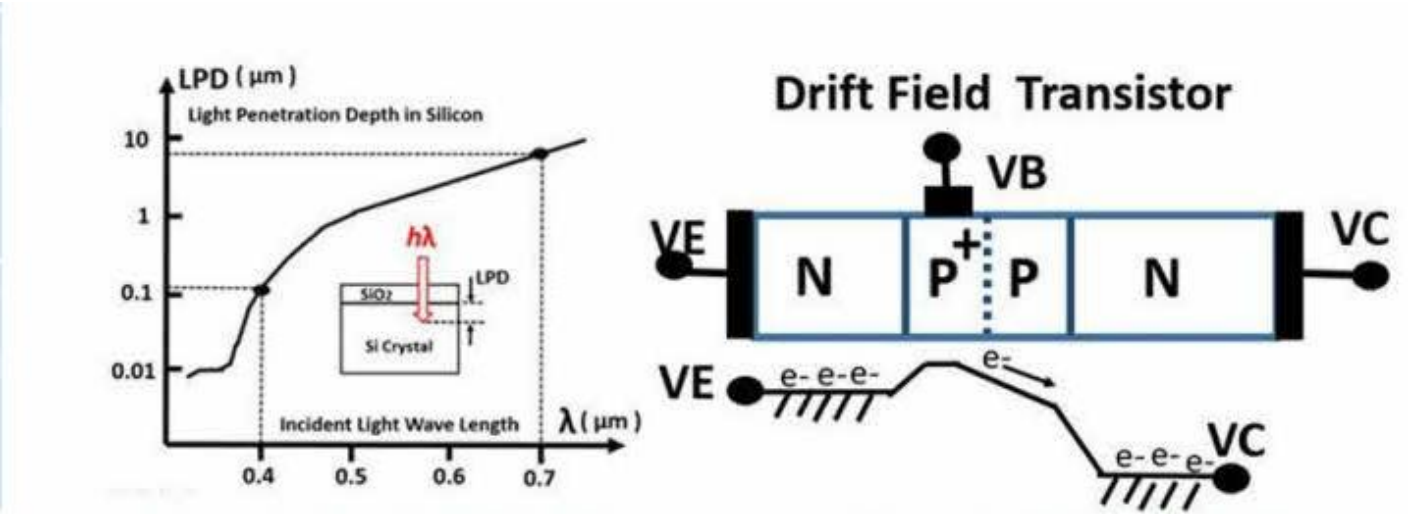
5 Double and Triple junction Dynamic Photo Transistors

Pinned Photodiode must have a flat surface potential with no surface electric field in order to suppress the undesired surface dark current. Pinned Photodiode must have a fixed flat surface potential pinned by an adjacent channel stops or directly connected by an adjacent metal contact nearby. Otherwise, the surface potential would become floating because of the undesired RC delay time.



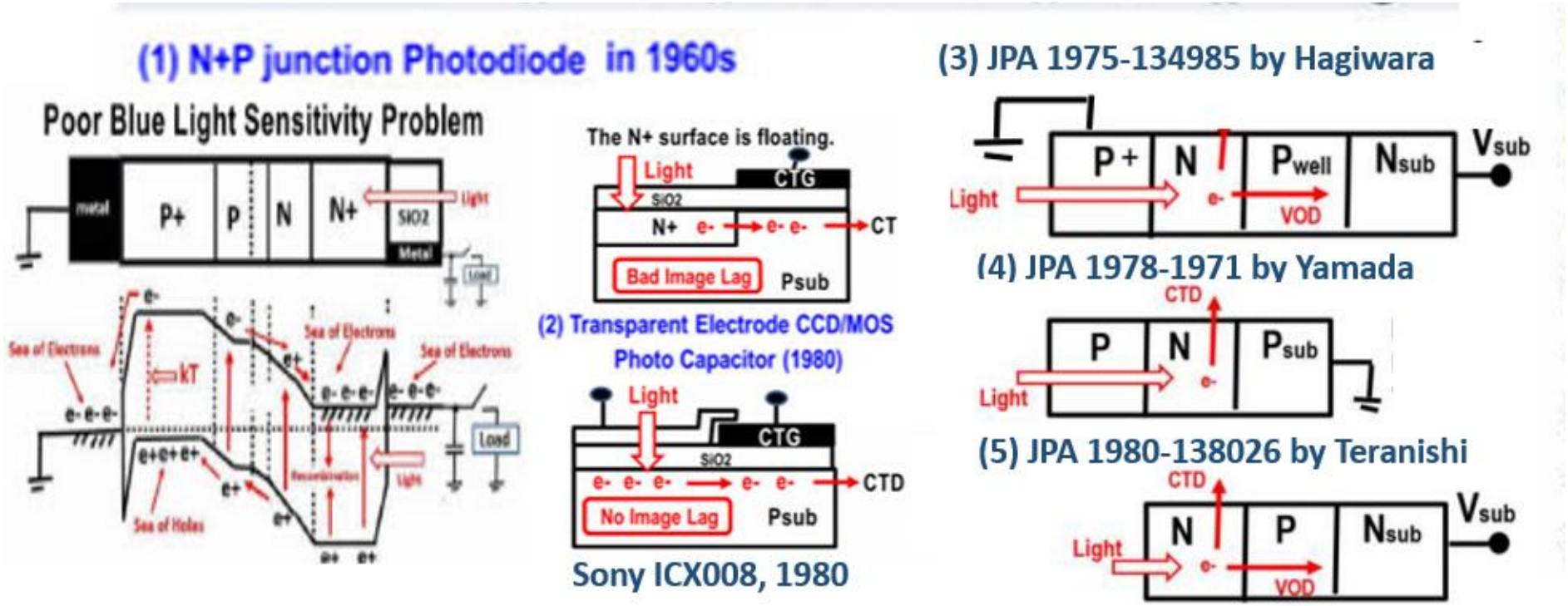
5 Double and Triple junction Dynamic Photo Transistors

Pinned Photodiode must always have the majority carrier accumulation surface layer and also with the minority carriers surface barrier electric field in order to achieve effectively the electron and hole photo pair generation at the majority carrier surface accumulation layer within the depth of less than 0.1 μm, which results in an excellent short wave blue light sensitivity.



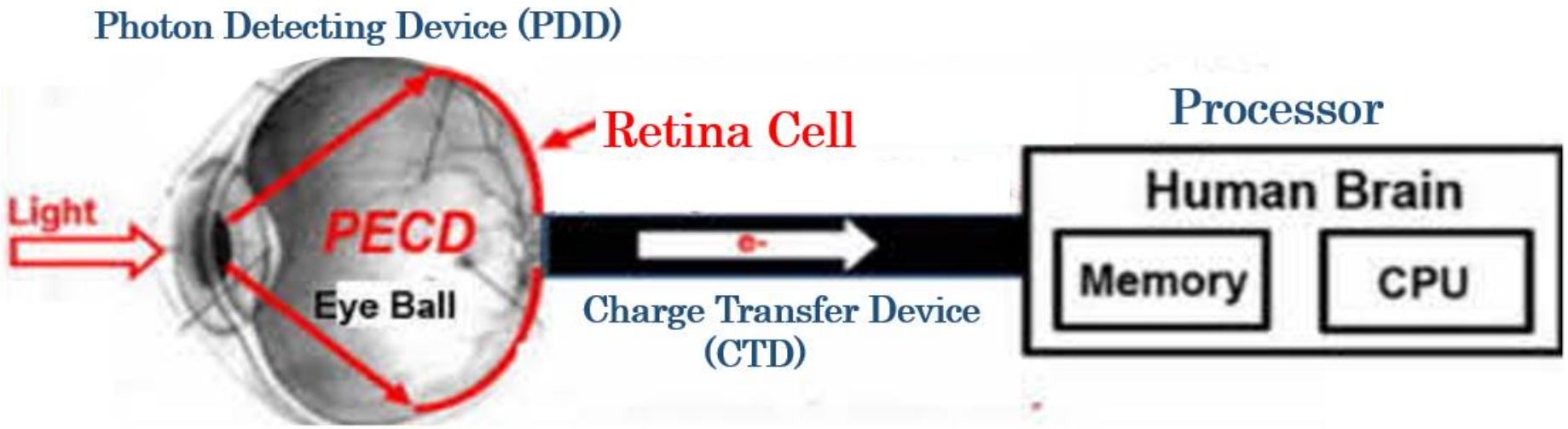
5 Double and Triple junction Dynamic Photo Transistors

Pinned Photodiode always by necessity must have the pinned empty potential well in the buried photo charge collecting and storing region so that when reset the signal photo charge can be drained completely and no image lag feature is achieved.



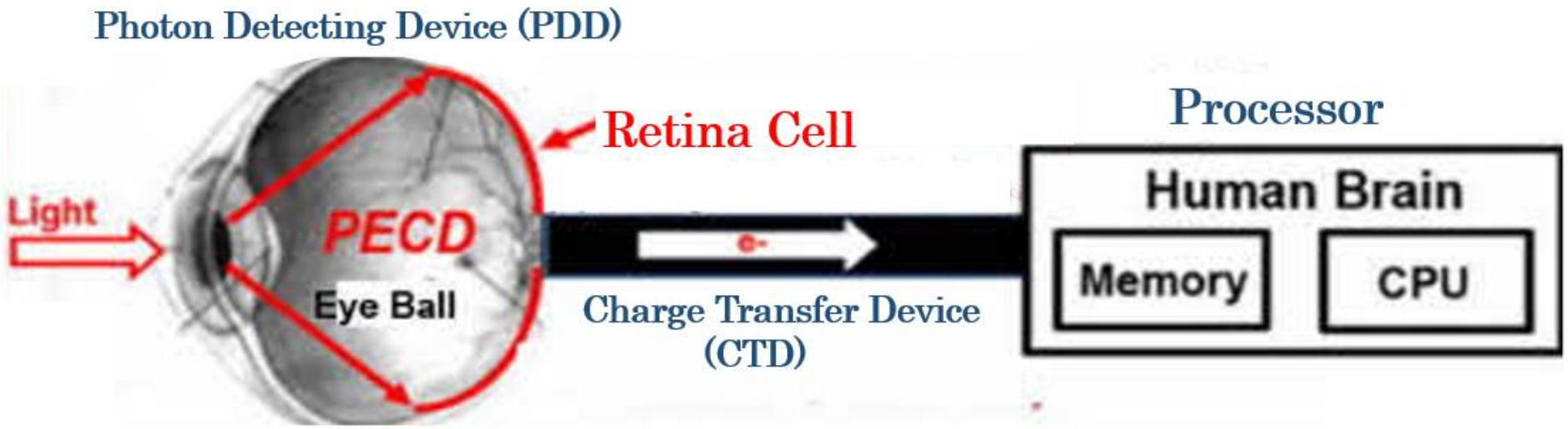
5 Double and Triple junction Dynamic Photo Transistors

Before 1970 when CCD was invented by Boyle and Smith, the N+P single junction type Photodiode was used with the undesired image lag problem. The surface channel type CCD has a serious surface charge trapping noise problem with a very poor charge transfer efficiency.



5 Double and Triple junction Dynamic Photo Transistors

However, the buried channel type CCD has an excellent charge transfer efficiency of about 99.999%. The picture size of the NTSC Format is about 800H x 500V. And at most the charge transfer of 800+500 = 1300 is needed in the NTSC TV system.



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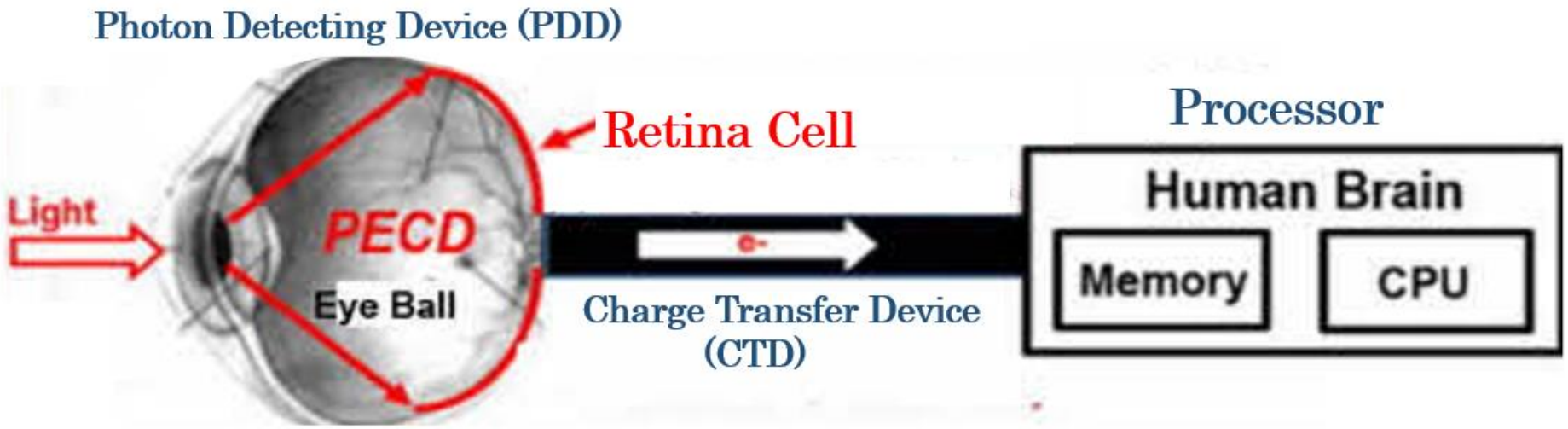
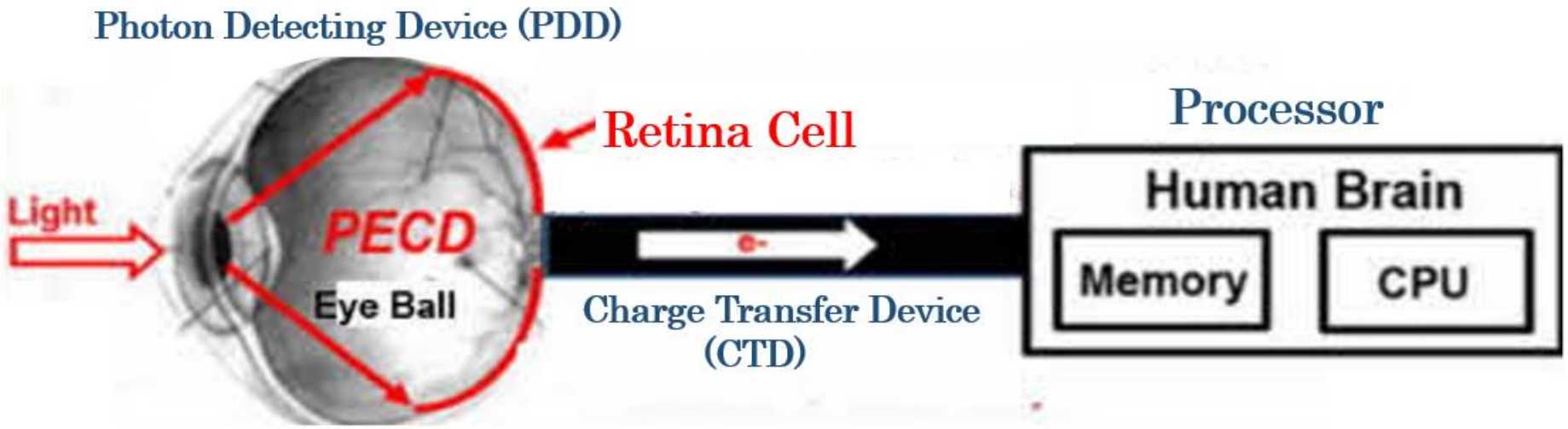


5 Double and Triple junction Dynamic Photo Transistors

This observation gives the image information loss of 0.001 % x 13000 = 1.3 % which is small enough for human eyes since human eyes cannot recognize the picture noise of less than 3 %. CCD became a super star in the Image sensor world in the analog TV era from 1980 to 2000.



5 Double and Triple junction Dynamic Photo Transistors

The first commercially available two-chip CCD video camera with the CCD/MOS dynamic capacitor type photo detecting device (PDD) was introduced by Sony in 1980 and was used in the cock pit of ANA Jumbo 747 which gave the excellent and clear action pictures of the completely no image lag feature .

Sony ICX-008 CCD chips (1980)

<ICX008>

XC-1 1980
Two-Chip Color Video Camera
on ANA 747 Jumbo Jet

all solid state = robustness

●CCD/MOS Dynamic Photo Capacitor with no image lag for action pictures with Electric Shutter Function

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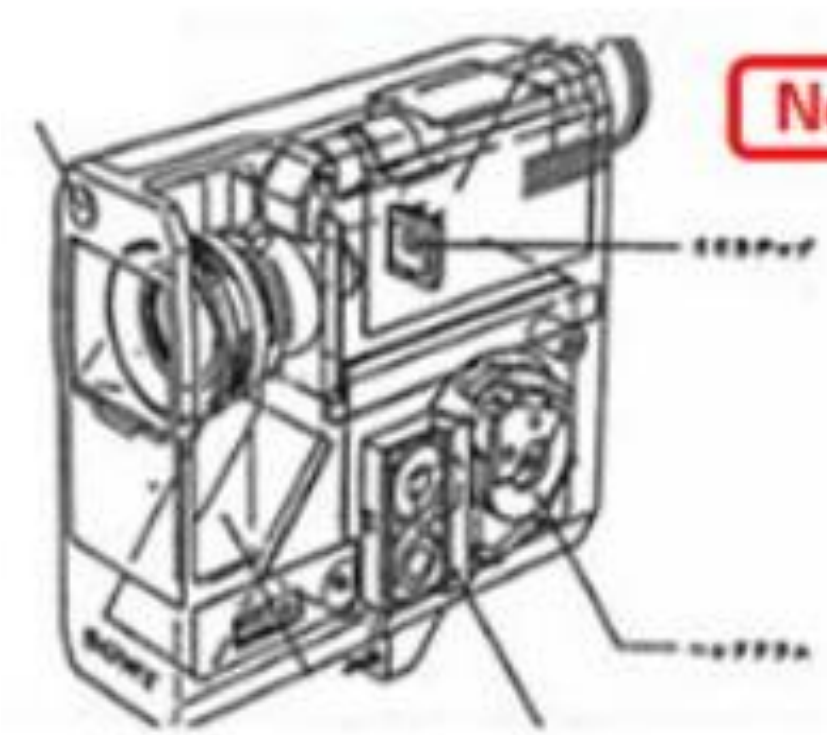
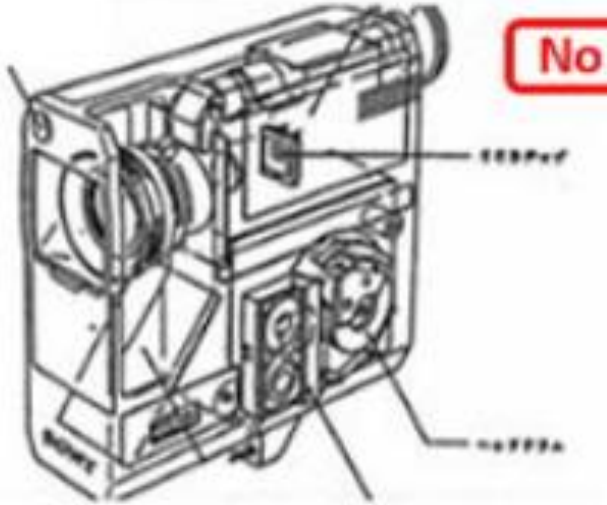
5 Double and Triple junction Dynamic Photo Transistors



The original Pinned Photodiode (PPD) structure was invented by Hagiwara at Sony in 1975. The first one-chip color video camera with a FT CCD image sensor with P+NP junction type Pinned Photodiode (PPD) was reported by Sony in 1980 at Tokyo Press Conference by Iwama Kazuo of Sony president, and at New York Press conference by Morita Akio of Sony chairman.

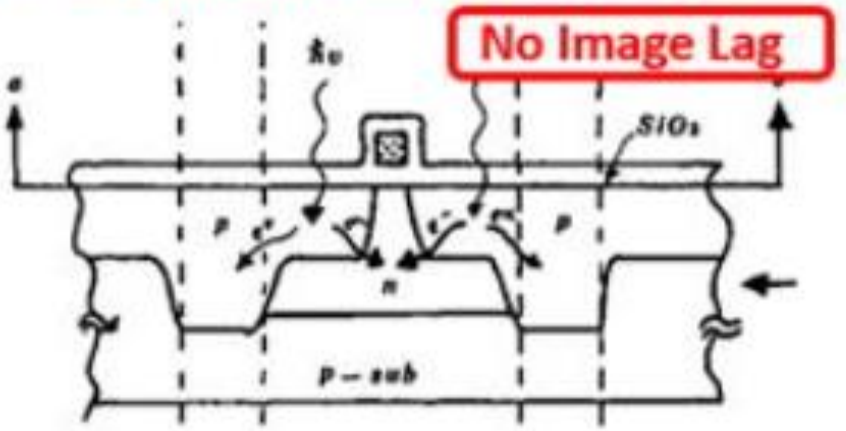
5 Double and Triple junction Dynamic Photo Transistors

Sony original 570H x 498 V one-chip FT CCD Image Sensor with Pinned Photodiode, July 1980



No Image Lag

P+NP Junction Pinned Photodiode



On July 1980, Iwama Kazuo at Sony Tokyo Press Conference and Morita Akio at New York Press Conference announced the one chip CCD video camera with the 8 mm VTR in one box.

See the Original 1978 Publication of the Pinned Photodiode Sensor

Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488V CCD imager with narrow channel transfer gates," Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Appllied Physics , vol. 18, supplement 18–1, pp. 335–340, 1979

5 Double and Triple junction Dynamic Photo Transistors

Japanese patent applications, JPA 1975-127646, JPA 1975-127647 and JPA 1975-134985 are the evidence that Yoshiaki Hagiwara invented the buried photodiode (BPD) with the pinned surface, the Pinned Photodiode (PPD) and Hole Accumulation Diode (HAD).

feature \ type	Classical N+Psub Photodiode	Surface Channel CCD	Buried Channel CCD	Yamada 1978 NPNsub	Teranishi 1980 PNPsub	Hagiwara 1975 PNPNsub
Blue Light Sensitivity	△	X	X	○	○	○
Low Image Lag	X	○	○	X	○	○
Surface Dark Current	○	X	X	X	○	○
Surface Trap Noise	○	X	○	X	○	○
Vertical OFD (VOD)	X	X	X	○	X	○
Electrical Shutter	X	X	X	X	X	○

5 Double and Triple junction Dynamic Photo Transistors

It is also evident that Hagiwara invented the global shutter of the three clocking voltage level scheme with the MOS buffer memory, as shown in JPA 1975-127646 and JPA 1975-127647.

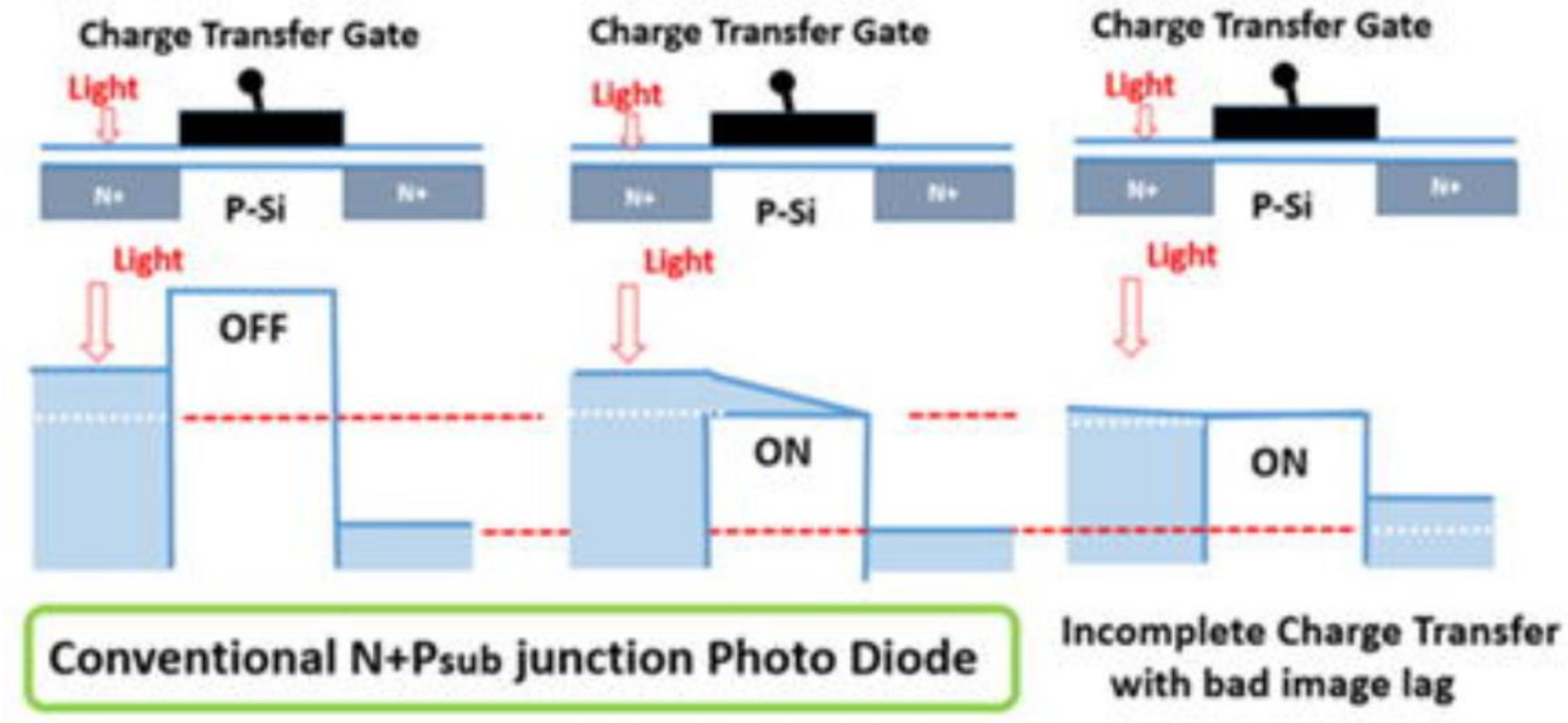
feature \ type	Classical N+Psub Photodiode	Surface Channel CCD	Buried Channel CCD	Yamada 1978 NPNsub	Teranishi 1980 PNPsub	Hagiwara 1975 PNPNsub
Blue Light Sensitivity	△	X	X	○	○	○
Low Image Lag	X	○	○	X	○	○
Surface Dark Current	○	X	X	X	○	○
Surface Trap Noise	○	X	○	X	○	○
Vertical OFD (VOD)	X	X	X	○	X	○
Electrical Shutter	X	X	X	X	X	○

5 Double and Triple junction Dynamic Photo Transistors

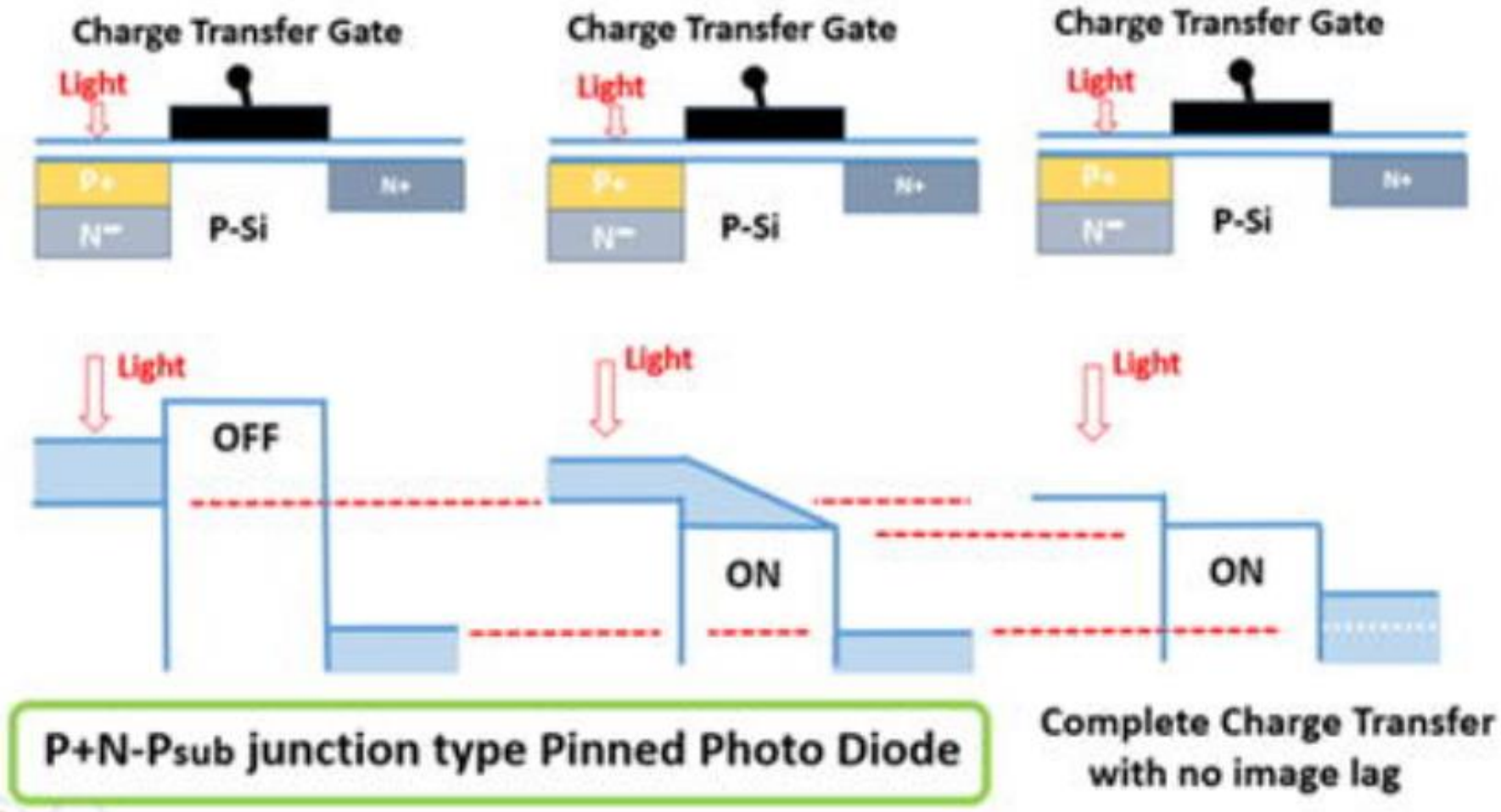
It is also evident that Hagiwara et al invented the electrical shutter clocking scheme by controlling the punch-thru action of the in-pixel overflow drain voltage in JPA 1977-136885.

feature \ type	Classical N+Psub Photodiode	Surface Channel CCD	Buried Channel CCD	Yamada 1978 NPNsub	Teranishi 1980 PNPsub	Hagiwara 1975 PNPNsub
Blue Light Sensitivity	△	X	X	○	○	○
Low Image Lag	X	○	○	X	○	○
Surface Dark Current	○	X	X	X	○	○
Surface Trap Noise	○	X	○	X	○	○
Vertical OFD (VOD)	X	X	X	○	X	○
Electrical Shutter	X	X	X	X	X	○

5 Double and Triple junction Dynamic Photo Transistors

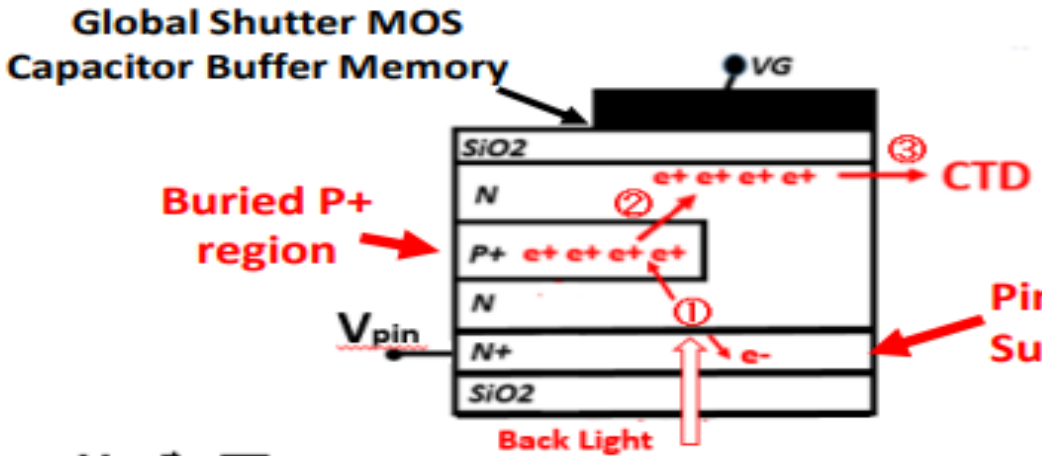


5 Double and Triple junction Dynamic Photo Transistors



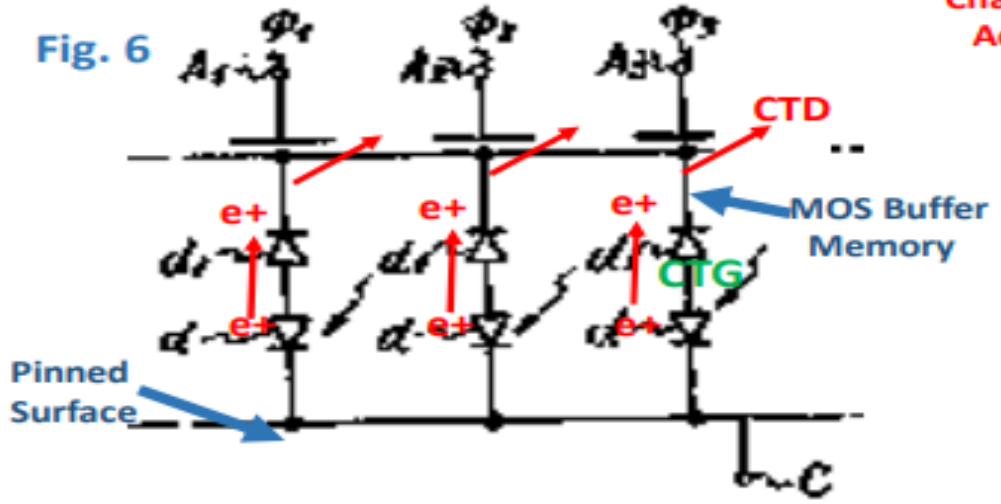
JPA 1975-127647 filed by Yoshiaki Hagiwara, 1975.

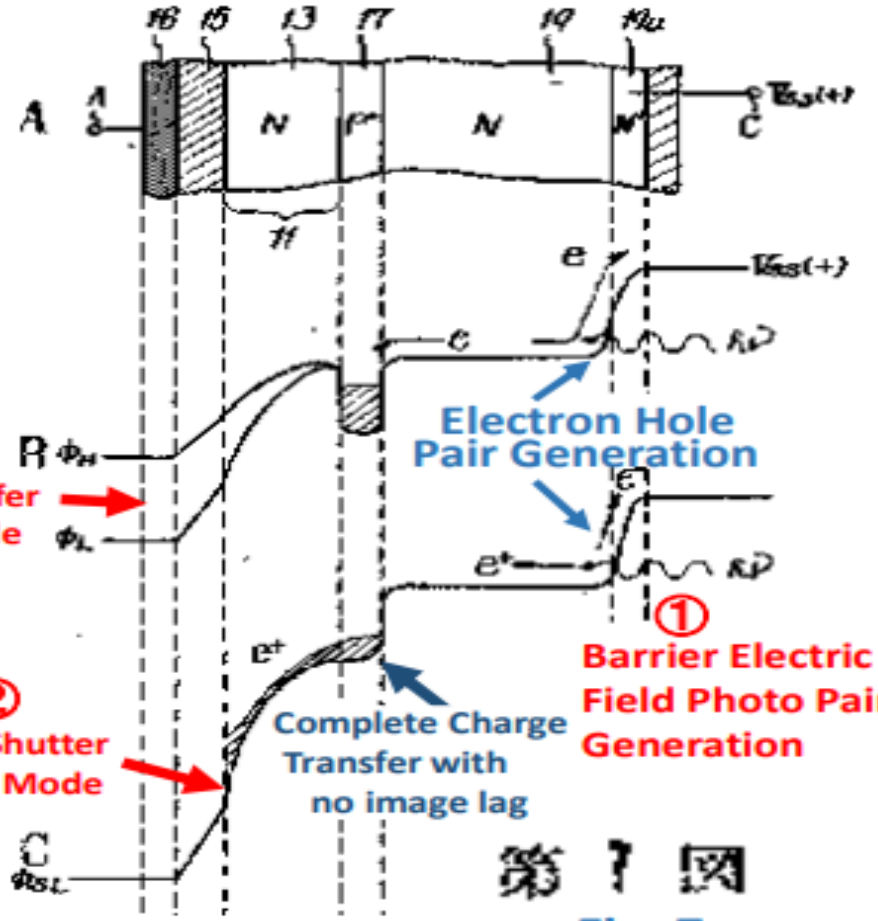
N+NP+N junction Dynamic Photo Transistor type Buried Pinned Photodiode with Built-in MOS Capacitor Buffer Memory Global Shutter Function and the surface N+N doping slope Barrier Electric Filed Photo Pair Generation



第 6 図

Fig. 6





第 7 図

Fig. 7

JPA 1975-134985 filed by Yoshiaki Hagiwara, 1975.

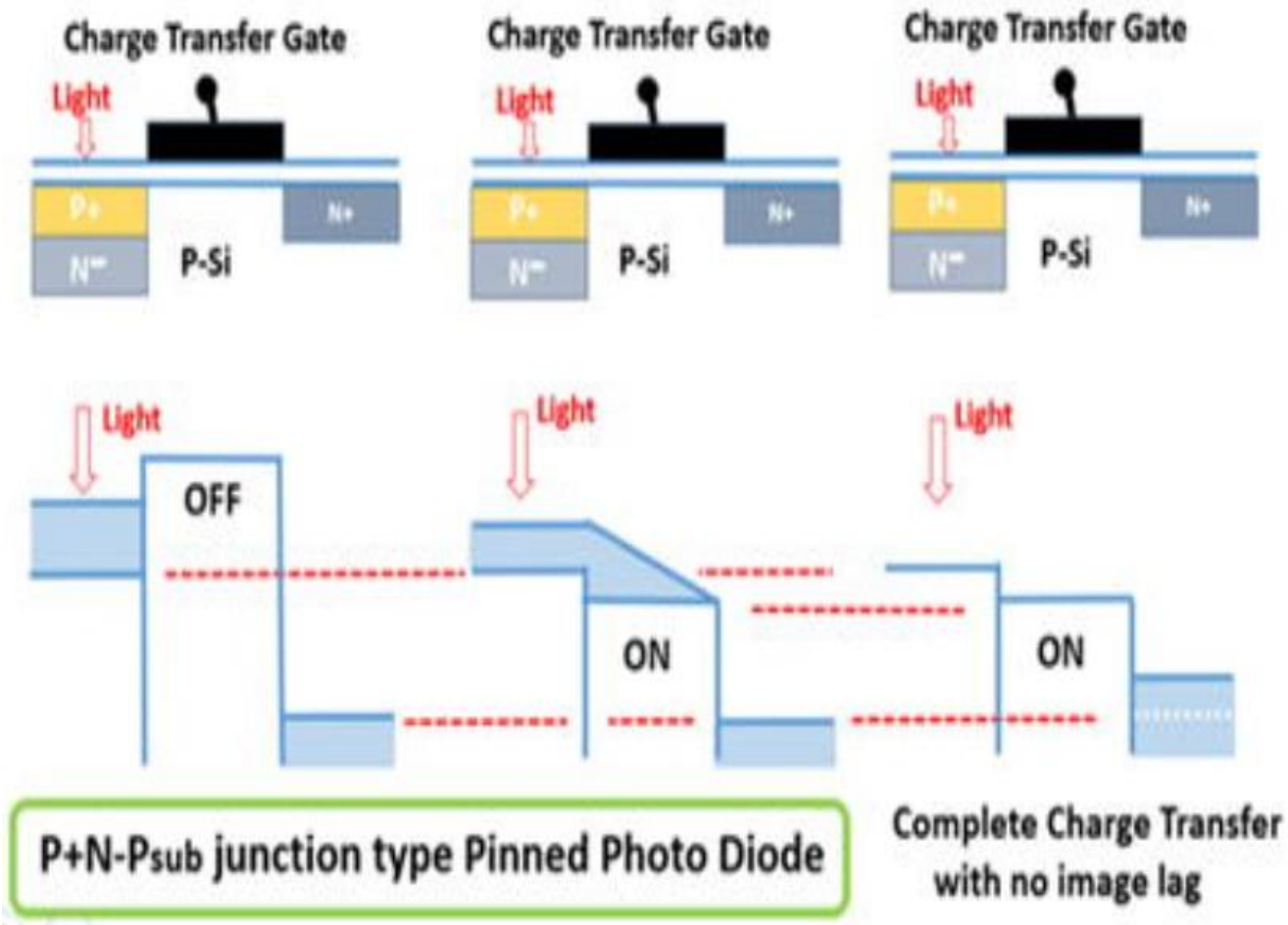
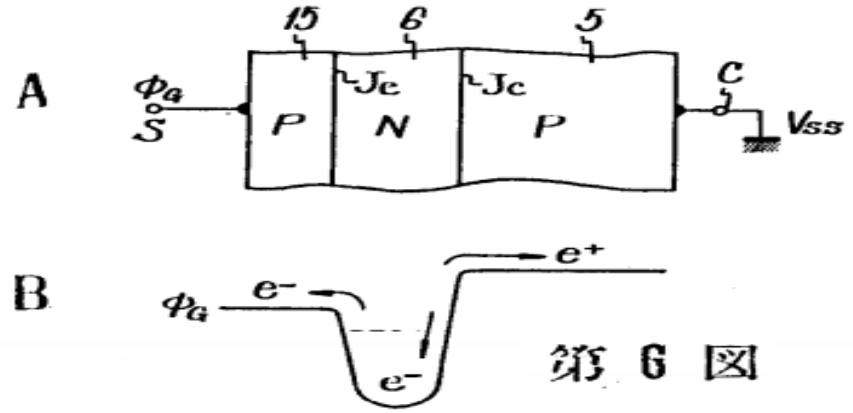
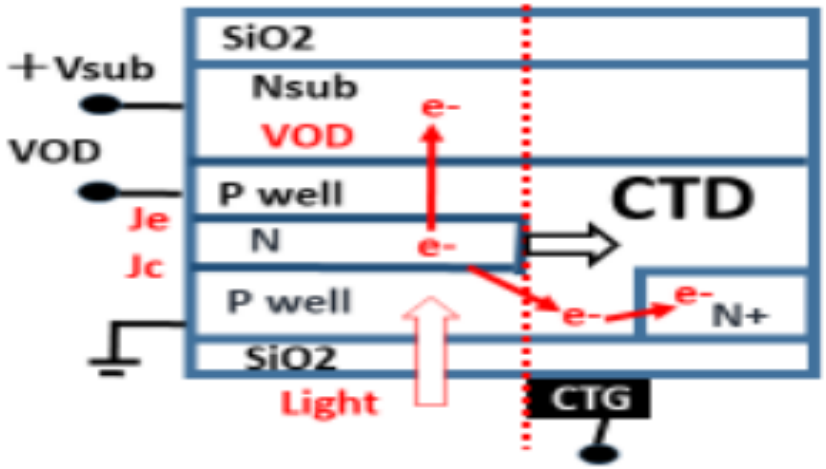


Fig. 6 of JPA 1975-134985





Dynamic Photo Transistor defined by the claim of JPA 1975-121975-134985

5 Double and Triple junction Dynamic Photo Transistors

Photo Detecting Sensor Structures with the No Image Lag Feature
and with the Very High Short Wave Blue Light Sensitivity
were developed by Sony (Hagiwara) Team in 1978 thru 1980.
However, only the P+NP double junction type Pinned Photodiode
invented in 1975 by Hagiwara at Sony survived
because the CCD/MOS type Photo Capacitors have the large surface dark current.
See Japanese Patent Applications 1975-127646, 1975-127647 and 1975-134985.

1 ——— The P+NP Junction type Pinned Photodiode reported SSDM1978 paper by Hagiwara in 1978.
2 — — The 50 nm Thin Polysilicon MOS Gate Photo Capacitor used in Sony ILT CCD Image Sensor in 1980
3 ▬·▬ The 150 nm Polysilicon MOS Gate Photo Capacitor used in Sony ILT CCD Image Sensor in 1980