===Who invented Pinned photodiode? === edited by YoshiakiHagiwara19480704 on Feb 3, 2022

Pinned photodiode[edit source]

Please visit the following three important notices on the WEB site.

(1) for the invention and development efforts of Pinned Photodiode by Yoshiaki Hagiwara at Sony in 1975 thru 1978.

http://www.aiplab.com/

(2) Also please visit and read the details of Hagiwara 1975 invention and 1978 R/D efforts of Pinned Photodiode, which was also named as Sony Hole Accumulation Diode (HAD) in 1987 by Sony. Sony kept silent till 1987 since it took so long for Sony to achieve mass production technology and to commercialize the Pinned Photodiode with the Electrical Shutter Function for consumer video camera applications. PPD was originally conceived and invented by Hagiwara at Sony in 1975.

https://20201128200256965733O.onamaeweb.jp/AIPS_Library/Who_invented_Pinned_Photodiode_Hagiwara_in_Japanesee.pdf

(3) Sony also quoted Hagiwara's 1975 Pinned Photodiode Patents JPA1975-127646, JPA1975-127647 and JPA1975-134985 which is the evidence that Yoshiaki Hagiwara at Sony was the true inventor of Pinned Photodiode.

https://www.sony.com/en/SonyInfo/News/notice/20200626/

which explains the details of Sony's Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became

the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

The first pinned photodiode (PPD) was originally invented by Yoshiaki Hagiwara at Sony in 1975 to use for the interline CCD image sensors. Hagiwara at Sony invented PPD also with the antiblooming function in 1975.The evidence are given by the three Japanese patent application, JPA 1975-127646, JPA 1975-137647 and JPA 1975-134985. Hagiwara team also developed the first PPD and reported at SSDM1978 conference at Tokyo. The first pinned photodiode reported at SSDM1978 has a shallow P+ implant in the buried N type diffusion layer over a P-type substrate with the adjacent pinning heavily doped P+ channel stop regions formed by high ion implantation technology>Sony first PPD process did not used any epitaxial process and the convention LOCOS isolation which are known to induce the undesired dark current and white spots degrading the chip yields as reported in Sony 1978 SSDM paper published by Hagiwara team at Sony.

Sony PPD also had the unique surface P+P doping profile to create barrier potential to enhance the surface photo electron and separation to achieve a very high quantum efficiency for short wave blue light sensitivity.

This led to their invention of the pinned photodiode, a photodetector structure with low lag, low (electronics) noise, high quantum efficiency and low dark current.

It is not to be confused with the PIN photodiode. The PPD is used in CMOS Active sensors

http://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode Difference between Buried Photodiode and Pinned Photodiode. stackexchange.com, which also explained the difference of Buried Photodiode and Pinned Photodiode. Pinned Photodiode is a buried photodiode with the Pinned Surface to the external controlled fix voltage. But Buried photodiode is NOT always Pinned Photodiode. Buried Photodiode with the floating P+ surface is NOT Pinned Photodiode.

http://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode Difference between Buried Photodiode and Pinned Photodiode. stackexchange.com, which also said

that the first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's,

and also the it has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)"

The following the full text:

First off these are not PIN Photodiodes - which stands for P - Intrinsic- N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though.

Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space.

You can get surface state pinning from the dangling Si/SiO2 bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The Si/SiO2 surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface.

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise qn=sqrt(KTC) also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)"

http://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode Difference between Buried Photodiode and Pinned Photodiode. stackexchange.com, which clearly explained clearly stated the diffeence of Buried Photodiode and Pinned Photodiode and Hagiwara at Sony was the inventer of Pinned Buried Photodiode.

Early charge-coupled device type image sensors with the single N+P junction photodiode with the floating surface N+ charge storage region suffered from shutter lag. The image lag problem was completed resolved by Sony 1975 invention and development efforts as explained in details in the question 83018 quoted as above.

Independently Buried Photodiode with the floating surface P+ region was also proposed and developed by Nobukazu Teranishi, Hiromitsu Shiraki and Yasuo Ishihara at NEC in 1980.

Fossum2014:US patent|4484210|U.S. Patent 4,484,210:

Solid-state imaging device having a reduced image lag.

However, their actual photodiode photodiode they produces had the serious image lag since it has the floating P+ surface with the buried N+ storage region.

They explained that lag can be eliminated if the signal carriers could be transferred from the photodiode to the CCD. But that was impossible since the NEC buried photodiode had a floating P+ surface without the adjacent P+ channel stops region needed to pin and fix the P+ surface potential to the substrate GND level.

NEC 1982 IEDM did not quote Sony original 1975 patents and 1978 works on Pinned Photodiode, that led to their invention of the pinned photodiode, a photodetector structure with low lag, low noise (electronics noise), high efficiency and low dark current (physics) dark current.

Fossum Paper was misleading and claimed that Hagiwara did not show the image lag feature in Hagiwara 1975 patent but it was not true. Fossum wrote a mislaading paper

[21]

Hagiwara at Sony invented PPD with the antiblooming function in 1975.

However, in English speaking IEEE Community, the PPD was in 1982 publicly reported by Teranishi and Ishihara with A. Kohono, E. Oda and K. Arai in 1982, with the addition of an anti-blooming structure.

[21][22]

The buried photodiode with the serious image lag developed and reported at NEC was very different from the buried photodiode with the pinned surface developed and reported by KOAK in 1984. Pinned Photodiode (PPD) was named by B.C. Burkey at Kodak in 1984. In 1987, the PPD began to be incorporated into most CCD sensors, becoming a fixture in consumer electronic video cameras and then digital still cameras.

Teranishi team at NEC reported PPD for the first time in English speaking IEEE Community.

However Hagiwara team at Sony already published PPD in the SSDM1978 conference in Tokyo 1978, which is the first and original PPD with the P+ adjacent channel stops region formed by high energy ion implantation technology, instead of the LOCS isolation process, which enhanced the chip yields drastically.

In 1994, Eric Fossum, while working at NASA's Jet Propulsion Laboratory (JPL), proposed an improvement to the CMOS sensor: the integration of the pinned photodiode. Fossum was not fair: Fossum did not quite the Peter Noble's 1969 invention of in-pixel active sensor which is now the basis for the CMOS image sensor. A CMOS sensor with PPD technology was first fabricated in 1995 by a joint JPL and Kodak team that included Fossum along with P.P.K. Lee, R.C. Gee, R.M. Guidash and T.H. Lee. Since then, the PPD has been used in nearly all CMOS sensors. The CMOS sensor with PPD technology was further advanced and refined by R.M. Guidash in 1997, K. Yonemoto and H. Sumi in 2000, and I. Inoue in 2003. This led to CMOS sensors achieve imaging performance on par with CCD sensors, and later exceeding CCD sensors.