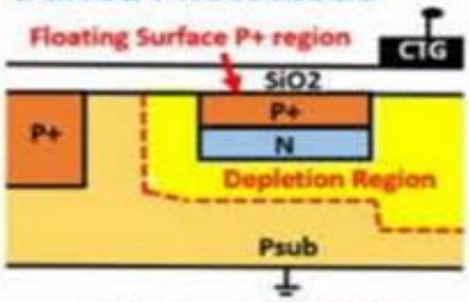
NEC IEDM1982 paper was not Pinned Photodiode by definition.

Difference of Buried Photodiode and Pinned Photodiode

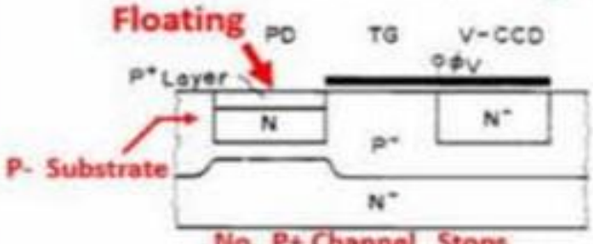
Figure 5 does not have the P+ channel stop nearby.

Buried Photodiode



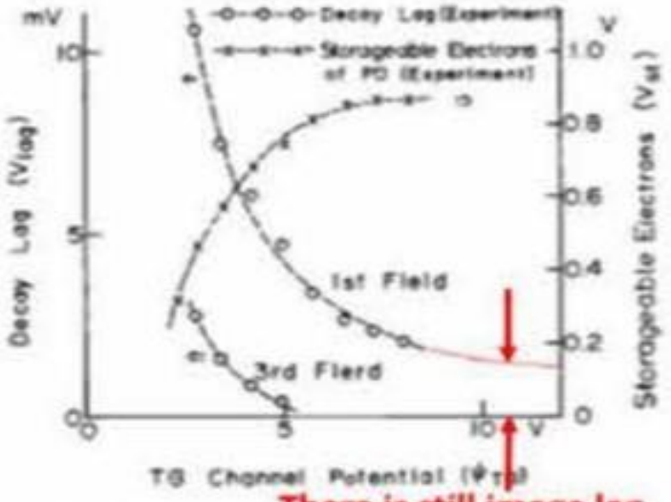
Serious Image Lag Problem

NEC IEDM1982 Paper



No P+ Channel Stops

Fig.5. P+NP- structure photodiode
(a) Unit cell cross sectional view



There is still image lag
at the CTD gate voltage more than 10 volt.

Fig.6. Storageable electrons vs. transfer gate channel potential, and decay lag vs. transfer gate channel potential in the P+NP- structure photodiode

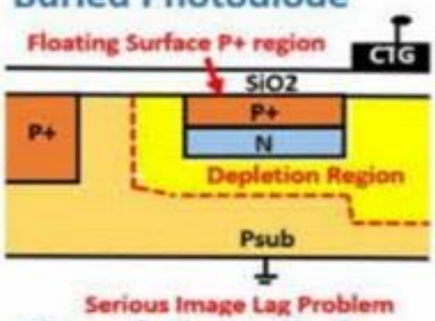
NEC IEDM1982 Paper reported Image Lag

Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 volt.

A long P+ Surface Stripe also has a serious RC delay.

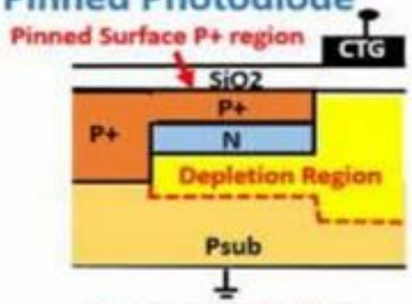
Pinned Photodiode Must Have the Grounded P+ Channel Stops Nearby.

Buried Photodiode



Serious Image Lag Problem

Pinned Photodiode



No Image Lag Problem

The resistivity ρ of the P+ hole accumulation layer is given by

$$\rho = R * W * d / L$$

In the 2/3 inch optical lens system, we have the optical image size of 8.8 mm (H) x 6.6 mm (V) which was a common size in 1980s. Hence, we then have L = 6.6 mm = 6600 μm

The short wave blue light cannot penetrate more than d = 0.2 μm into the silicon crystal in depth. Hagiwara reported in SSDM1978 paper $Qd = 2 \times 10^{13} cm^{-2}$ which gives $Nd = Qd/d = 1 \times 10^{18} cm^{-3}$

For $Nd = 1 \times 10^{18} cm^{-3}$ we have ρ = 0.04 ohm cm = 400 ohm μm

$$RC = \{ L\rho / (W*d) \} \{ \varepsilon W*L / Xo \} = \varepsilon \rho L^2 / (d\, Xo)$$

We have ε = 216 e/volt μm for silicon oxide and $e = 1.6 \times 10^{-19}$ Coulomb

$$RC = (216)(1.6 \times 10^{-19})(400)(6600)(6600) / (0.2)/(0.1) \text{ sec}$$

RC = 30.1 μsec while one frame is 1/60 sec = 16.7 msec and the Vertical CCD register clock period is 16.7/500 = 33.4 μsec

Hence RC delay time may not be ignored and surface P+ may be floating ?