

Hagiwara reported the Pinned Windows and Pinning Surface Potential in 1978 based on his 1975 invention of the P+NPNsub junction type Pinned Photo diode.

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The Hole Role in Solid-State Imagers

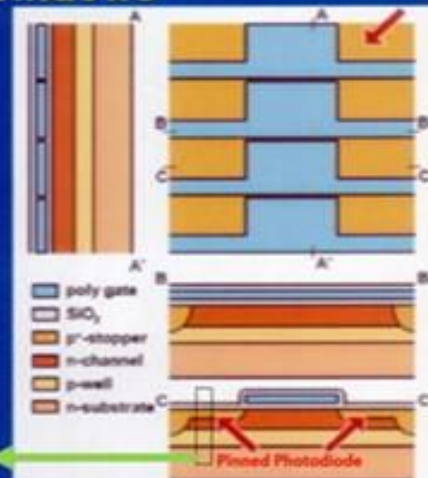
Albert J. P. Theuwissen, Fellow, IEEE

Despite these advantages, notice that parts of the depleted n-type CCD channels are not covered by gate material. In this way, their electrostatic potential is not defined! Such a structure will suffer from serious charge transport issues during its operation, because charge can and will be trapped in local potential pockets. The effect can simply be solved by defining the potential in the open areas through an extension of the p⁺-channel stopper. A simple self-aligned p-implant of $2 \cdot 10^{13}/\text{cm}^2$ B-ions after the gate construction is sufficient to extend the channel stop area to the gate edge and, consequently, fix the potential in the open areas. The result after this self-aligned implant is shown in Fig. 4. The presence of enough holes plays a crucial role in fixing the potential for the regions normally "beyond control" of the gates. [Is this structure the mother of the PPD or buried diode or hole-accumulation device (HAD)?]

CCD with Pinned Windows

Pinning surface potential by:

- self-aligned, shallow B implant,
- e.g. $2 \cdot 10^{13}/\text{cm}^2$,
- 1978 : Hagiwara (Sony),
- 1982 : Beck (Philips).



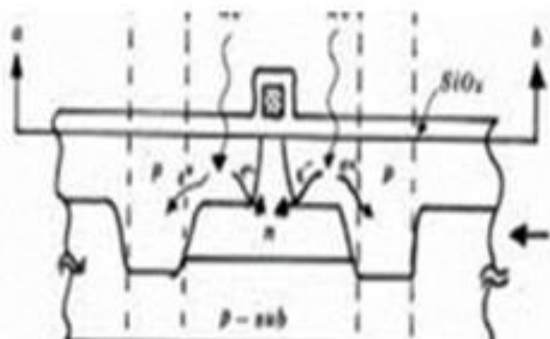
Albert Theuwissen quoted Hagiwara 1978 paper and explained the importance of hole role in image sensors @ Workshop on CMOS Imaging, Duisburg May 16, 2006

Direct Quotation

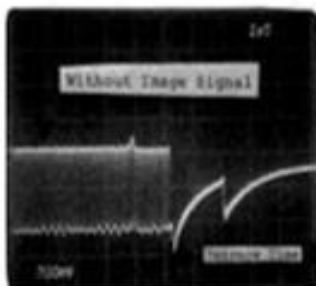
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Quoted directly from IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL.53, No.12, DEC 2006

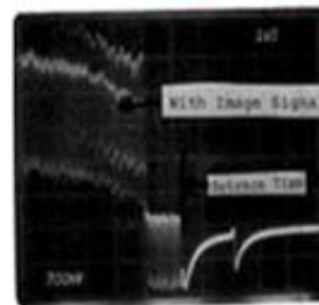
Hagiwara SSDM1978 Conference paper



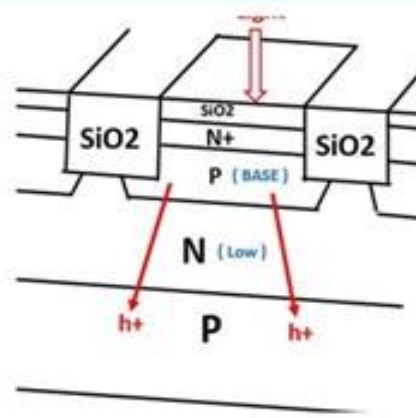
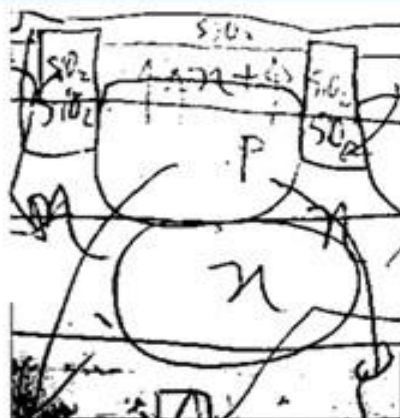
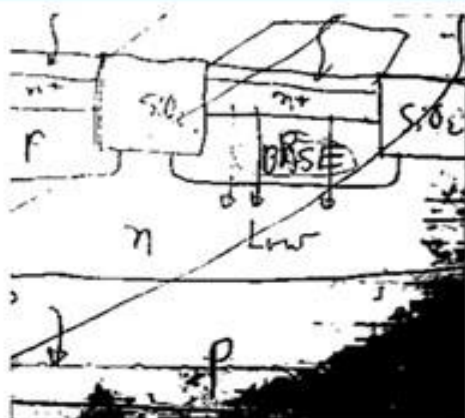
Low Dark Current



**Complete Charge Transfer
No Image Lag**



Proceeding of the 10th Conference on Solid State Devices, Tokyo, 1978;



Hagiwara 1975 Lab Note shows Pinned Photodiode Structure.