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The_First_Pinned_Photodiode_was_invented_in_1975_by_Yoshiaki_Hagiwara_at_Sony_001

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The details of explanations are given below regarding the 1975 invention of the Fisrt Pinned Photodiode proposed by Yoshiaki Hagiwara at Sony in 1975.

In his 1975 Japanese patents Hagiwara proposed a double junction and a triple junction type photodiodes with the pinned silicon surface hole accumulation region with the excellent short wave blue light sensitivity and also the complete charge transfer capability resulting in the no-image-lag high performance photodiode.

As Prof. Albert Theuwissen wrote in his IEDM2005 paper, the structure that Hagiwara proposed in 1975 , that Hagiwara developed in 1978 and that Hagiwara reported in the SSDM1978 conference can be considered as the "mother" of of NEC Buried Photodiode, KODAK Pinned Photodiode and Sony Hole accumulation Diode.

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Albert J.P. Theuwissen, Jan T.J. Bosiers, Edwin Roks, " The Hole Role ", an invited paper at IEDM2005, Washington DC, Techn. Dig. , 2005.

But in the case that parts of the depleted n-type CCD channels are not covered by gate material, their surface potential is undefined ! Such a structure will suffer from charge transport issues during operation, because charge can be trapped in local potential pockets. The effect can be solved by defining the potential in the open areas through an extension of the p^+ channel stopper. A simple self-aligned implant of 2×10^{13} /cm^2 boron ions is sufficient to extend the channel stop areas to the gate edge and consequently fix the potential in the open areas [2]. The result after this self-aligned implant is shown in Figure 3. The presence of enough holes plays a crucial role in fixing the potential for the regions "beyond control" of the gates. (Is this structure the mother of the pinned-photodiode or buried diode or hole-accumulation device ?)

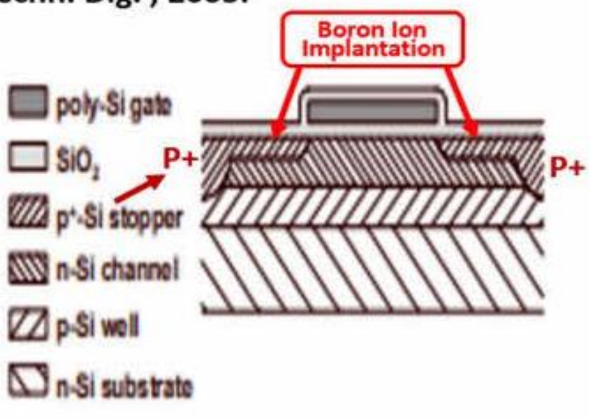

Figure 3. Cross section of a buried-channel CCD on n-Si substrate including light windows and pinned interface potential in the non-covered CCD channels (the cross section is made perpendicular to the CCD channel).

[2] Y. Daimon-Hagiwara et.al., Proc. 10th Conf. on Solid-State Devices, Tokyo, 1978, pp.335-340,

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The_First_Pinned_Photodiode_was_invented_in_1975_by_Yoshiaki_Hagiwara_at_Sony_002
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At that time Prof. Albert Theuwissen did not know the details of Hagiwara1975 Japanese patents, yet.

Hagiwara did not explain in the past till 2019 his 1975 PPD inventions in details to the English speaking community.

The Hagiwara 1975 Japanese patents, proposing the Buried Pinned Hole Accumulation Photodiode, had never been exposed in details in the English speaking community until in September, 2019.

Hagiwara published a paper in the 3DIC2019 Conference sponsored by IEEE EDS and held in Sendai, Japan.

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Yoshiaki Hagiwara, "Multichip CMOS Image Sensor Structure for Flash Image Acquisition", 2019 International 3D Systems integration Conference (3DIC), Paper 2DIC2019.4017, Sendai Japan, September 2019

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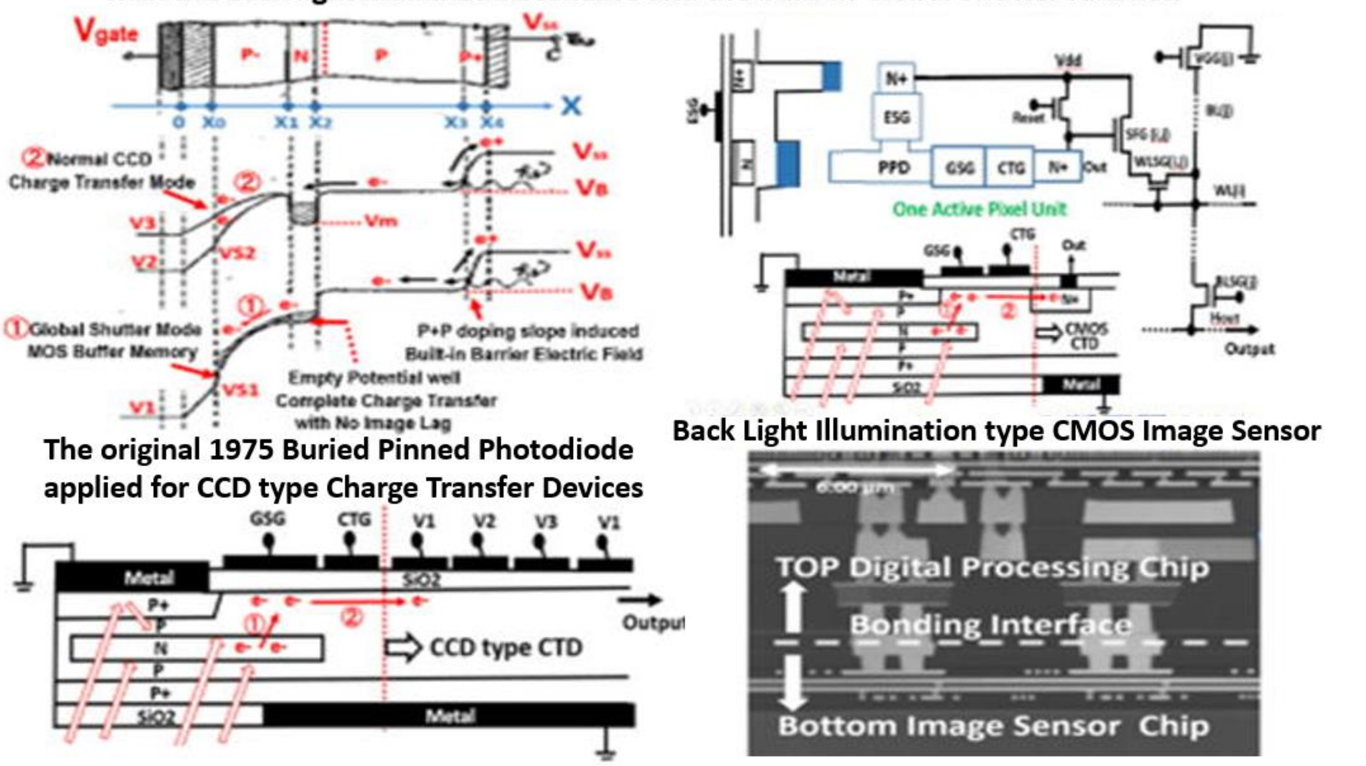
The P+PNP double junction type Buried Pinned Photodiode (HAD) used in the back light illumination type Modern CMOS Image Sensors

Japanese Patent Application JPA1975-127647 invented by Yoshiaki Hagiwara at Sony in 1975 with the back light illumination scheme and the built-in Global Shutter function



The original 1975 Buried Pinned Photodiode applied for CCD type Charge Transfer Devices

Back Light Illumination type CMOS Image Sensor

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The_First_Pinned_Photodiode_was_invented_in_1975_by_Yoshiaki_Hagiwara_at_Sony_003
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Hagiwara also proposed in 1977 the electrical shutter clocking scheme by controlling the punch-thru overflow drain voltage.

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http://www.aiplab.com/JP1977-126885.jpg
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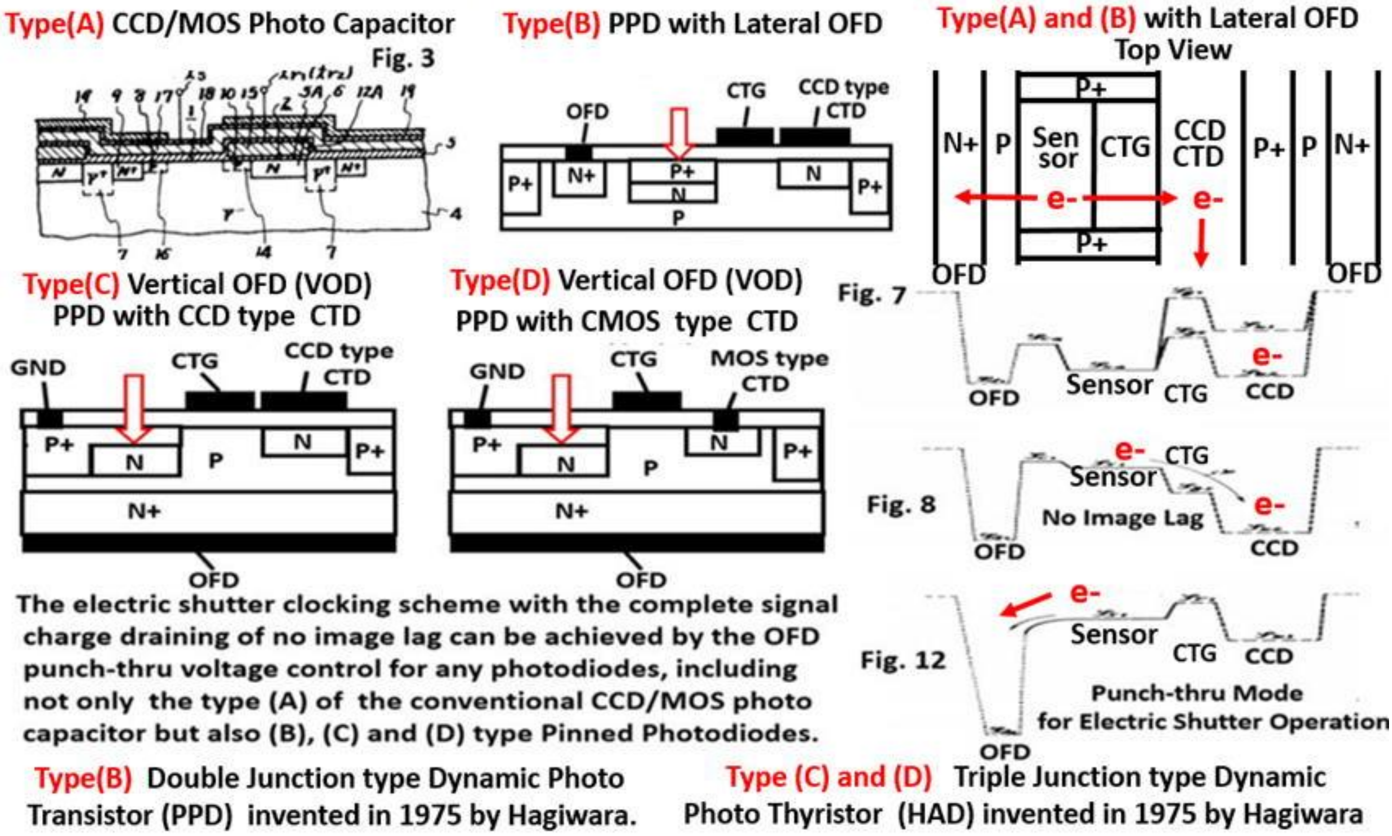
Hagiwara realized that we don't need the control gate over the p-region which bridges the photo charge collecting storage region and the overflow drain (VOD).

Hagiwara realized that the strong overflow drain (VOD) voltage can induce the punch-thru action to transfer all the signal photo charge completely to the VOD.

With these technology, we now can enjoy ourselves in the world of the mechanical free and filmless image sensors.

Japanese Patent 1977-126885

Japanese Patent JPA 1977-126885 on Electrical Shutter Clocking Scheme invented by Y. Hagiwara, S. Ochi and T. Hashimoto in 1977.



See Japanese Patent Application JPA 1975-127646, 1975-127647 and 1975-134985

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The_First_Pinned_Photodiode_was_invented_in_1975_by_Yoshiaki_Hagiwara_at_Sony_004
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In March 2019, the History Museum of Japan sponsored by the SSIS community said that Hagiwara at Sony proposed the PPD structure in 1975 and developed in 1978.

Semiconductor History Museum of Japan

To search page

1975-80

Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

~ Discrete Semiconductor/Others ~

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

Photodiodes are used for photodetectors of image sensors. In 1987, Sony introduced a 2 / 3-inch, 380,000-pixel CCD image sensor (ICX022) using a new type of photodetector, now called a Pinned Photodiode (Sony named it HAD: Hole Accumulation Diode)[1].

The Pinned Photodiode is a photodiode in which the entire N layer is covered with a P layer. The part of the P layer on the light incident surface is heavily doped P+ (Fig-1). Kodak named this structure Pinned Photodiode in 1984 because the P + surface of the light incident surface was pinned to the substrate potential. This device has features such as high light sensitivity, wide dynamic range, image lag free, much smaller dark current due to reduced influence of GR center on the light receiving surface, and no white scars.

In 1975, Sony proposed using a PNP transistor as the photodetector[3]. By providing a P + layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated, greatly improving the light sensitivity. This P + layer was also a proposal to reduce the dark current and image lag which became the basis of the pinned photodiode.

In 1978, Sony presented a 93,000-pixel FT (Frame Transfer) -CCD image sensor compliant with the Analog TV Broadcasting Standard (SDTV) for the first time in the world[5], using the photodiode with the same structure as above. Sony succeeded in 1981 in trial production of a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor by further improvement of this technology[6].

References:

【1】M. Hamasaki, T. Suzuki, Y. Kagawa, K. Ishikawa, K. Miyata and H. Kambe, "An IT-CCD imager with electronically variable shutter speed" , Technical Report of The Institute of Image Information and Television Engineers. vol. 12, no. 12, pp. 31-36, (1988)

【3】Y. Hagiwara, Japanese Patent JP1975—134985

【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

【6】I. Kajino, M. Shimada, Y. Nakada, Y. Hirata and Y. Hagiwara, "Single Chip Color Camera Using Narrow channel CCD Imager with Over Flow Drain"、Technical Report of The Institute of Image Information and Television Engineers、vol. 5, no. 29, pp.

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The_First_Pinned_Photodiode_was_invented_in_1975_by_Yoshiaki_Hagiwara_at_Sony_005
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In June 2019, Sony also said Hagiwara at Sony invented in 1975 the Pinned Photodiode with the VOD function, which is identical to the Sony PNPN junction type Hole Accumulation Diode (HAD)

https://www.sony.net/SonyInfo/Newa/notice/20200626/

Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

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The_First_Pinned_Photodiode_was_invented_in_1975_by_Yoshiaki_Hagiwara_at_Sony_006

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In September 1978, at the International Solid State Device Meeting (SSDM1978), Y. Hagiwara, M. Abe, and C. Okada reported a technical paper which is titled as "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, 1978.

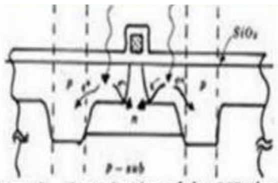


Figure 2 Cross Section of the CCD charge Transfer Region with the P+NP junction type Pinned Photodiode (PPD)

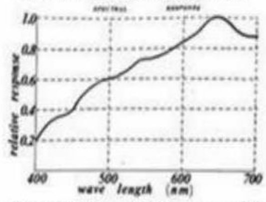


Figure 13 Spectral Response of the P+NP junction Pinned Photodiode (PPD) with the excellent blue light sensitivity

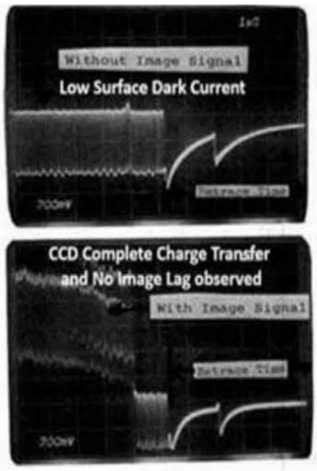


Figure 14 Comparison of CCD image sensor output signals with and without image signal.

See the Original 1978 Publication of the Pinned Photodiode Sensor

Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488V CCD imager with narrow channel transfer gates," Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Apllied Physics, vol. 18, supplement 18-1, pp. 335-340, 1979

The oxide exposed surface P+ hole accumulation region of Pinned Photodiode must have the adjacent heavily doped P+ channel stops nearby. The reason can be explained by the observation that, if covered by the surrounding depletion region extended by the strongly reverse biased buried N charge storage region, the surface P+ region would be isolated from the substrate grounded voltage and would become floating.

Consequently the electron potential of the empty potential well would also be floating, being coupled by the adjacent parasitic charge transfer gate (CTG) oxide capacitance. The situation is similar to the case of the classical N+P single junction photodiode with the floating surface N+ charge storage region, being coupled by the adjacent parasitic charge transfer gate (CTG) oxide capacitance, which is well known to have the serious image lag problem due to the incomplete charge transfer operation mode.

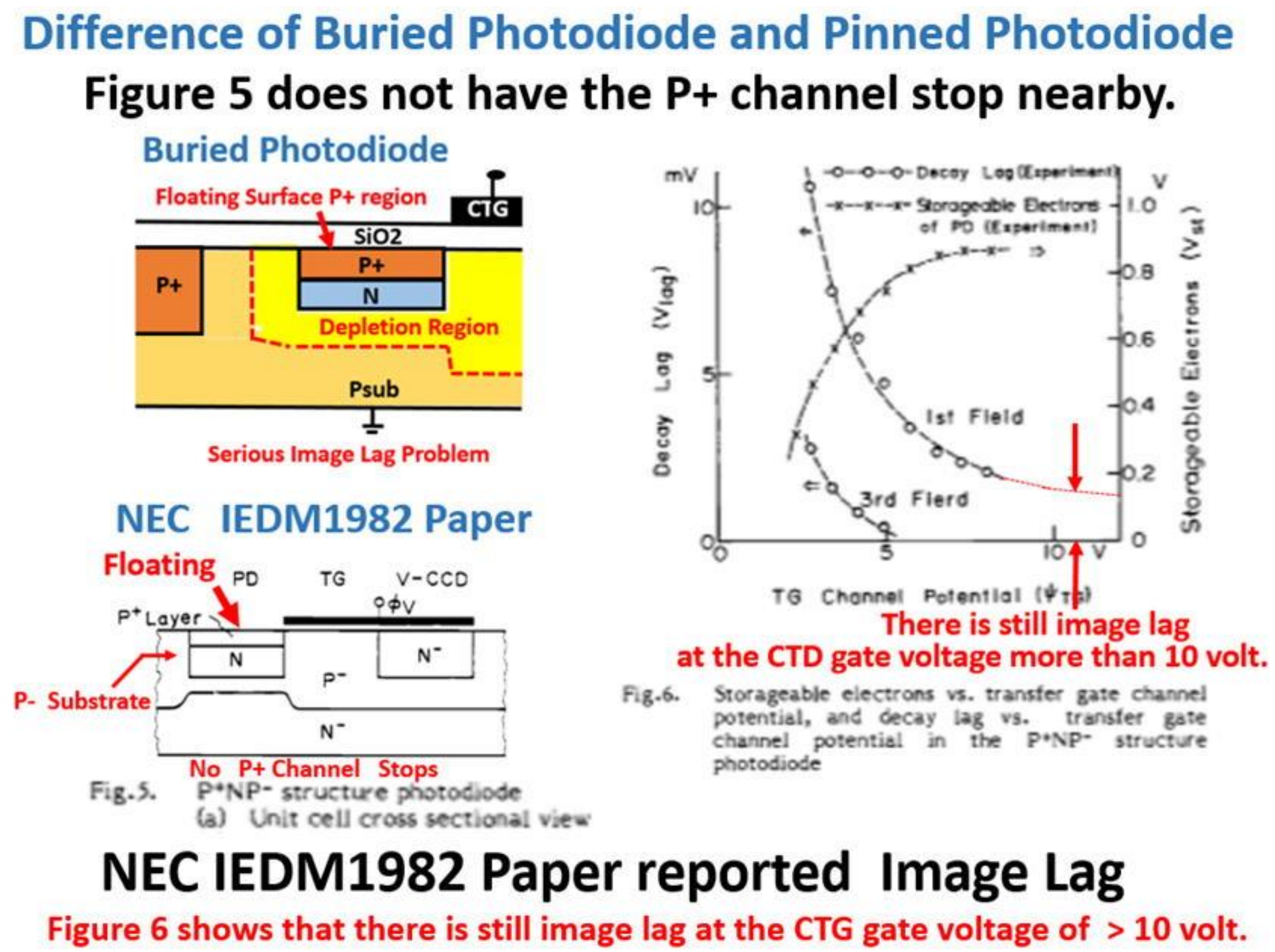
The empty potential well of the buried charge storage region must also be pinned to have the complete charge transfer operation mode of the no image lag feature. The adjacent P+ channel stops is a must for Pinned Photodiode to have the no image lag feature. Hagiwara Team developed in 1978 the First Pinned Photodiode with the adjacent P+ channel stops, formed by the high energy ion implantation technology without the conventional LOCOS device isolation technology which induces the serious silicon crystal stress.

Hagiwara reported in the SSDM1978 conference the CCD image sensor signal output data with the excellent short wave blue light sensitivity, the no image lag feature and the very low surface dark current feature. The choice of the high energy ion implantation technology was the key to form the P+ heavily doped adjacent channel stops for the Pinned Photodiode.

In SSDM1978 Hagiwara reported the excellent performance of the P+NP double junction type dynamic photo transistor which was later called as Pinned Photodiode by the IEDM1984 KODAK paper and also as Hole Accumulation Diode (HAD) by Sony in 1987.

However, Buried Photodiode reported by NEC in the IEDM1982 paper had the serious image lag problem and was not Pinned Photodiode by definition because the surface P+ hole accumulation region is not completely pinned. Apparently there was no heavily doped P+ channel stops adjacent to the Buried Photodiode reported by NEC at the IEDM1982.

The IEDM1982 NEC paper indeed reported the serious image lag problem.

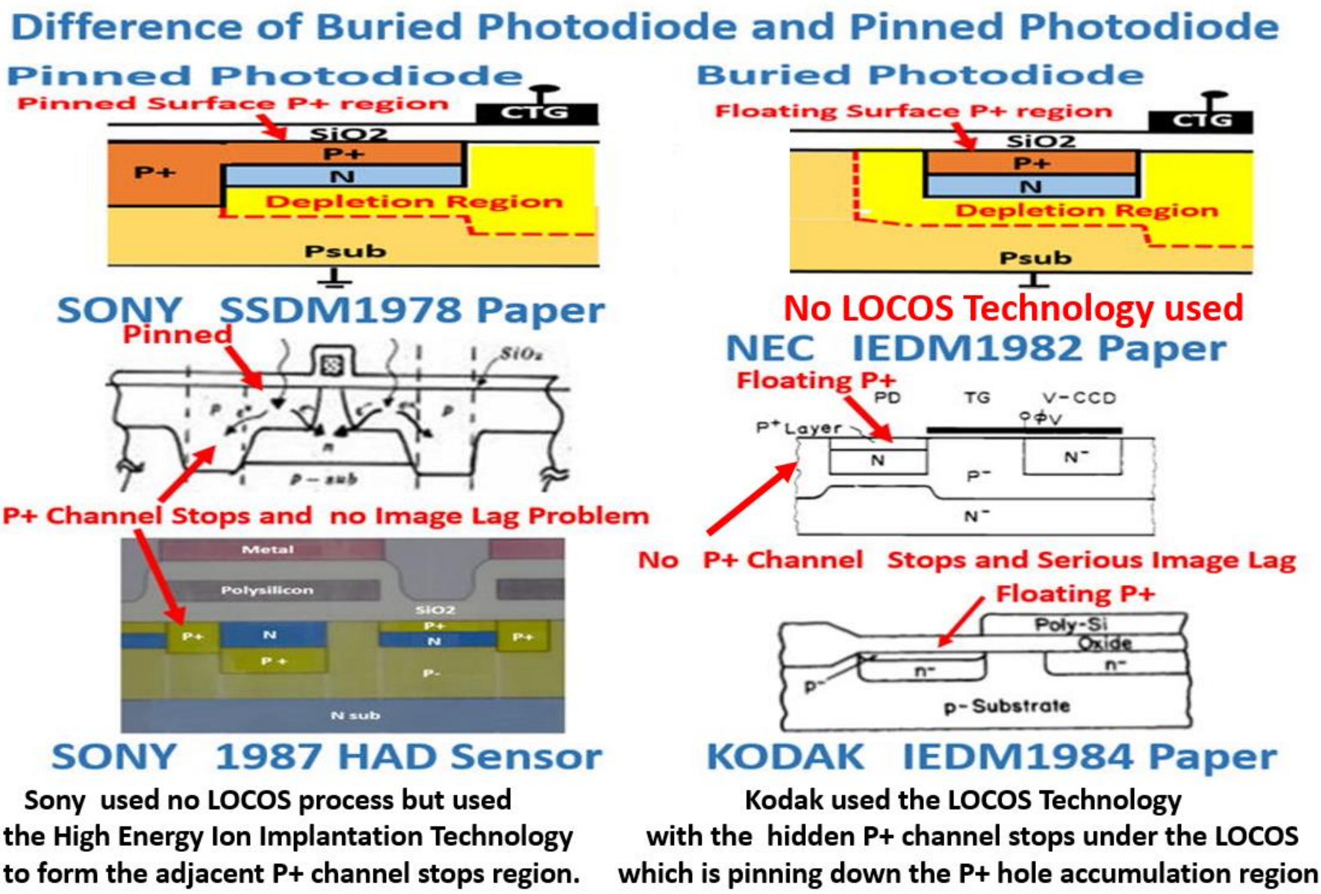


So by definition, the photodiode reported in IEDM1984 KODAK paper was Pinned Photodiode while the buried photodiode reported in IEDM1982 NEC paper was not a Pinned Photodiode.

The reason can be explained by the observation that the surface P+ region in the IEDM1982 NEC paper may be isolated from the grounded substrate voltage by the surrounding depletion region extended by the deeply biased buried N charge storage region. The result is the floating P+ surface and the floating empty potential of the buried charge collecting storage region.

Hagiwara reported in the SSDM1978 conference the CCD image sensor signal output data with the excellent short wave blue light sensitivity, the no image lag feature and the very low surface dark current feature. The choice of the high energy ion implantation for the formation of the P+ heavily doped adjacent channel stops was the key technology. Hagiwara Team developed in 1978 the First Pinned Photodiode with the adjacent P+ channel stops, formed by the high energy ion implantation technology. Sony did not used the conventional LOCOS device isolation technology which induces the serious silicon crystal stress.

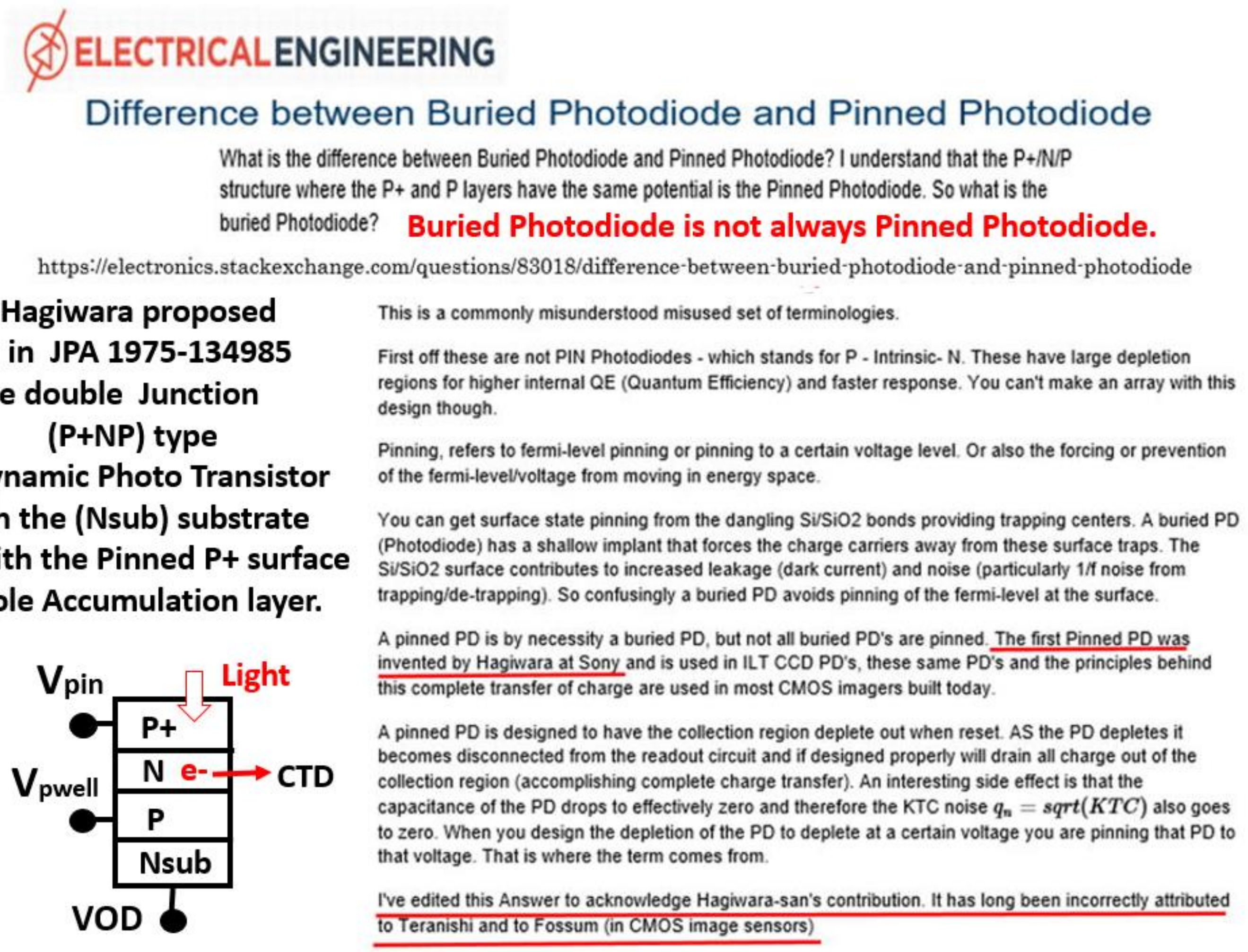
NEC apparently understood by 1982 that the LOCOS device isolation technology induces the serious silicon crystal stress and is not suited for the image sensor processing. NEC did not use the LOCOS device isolation technology for the buried photodiode process formation. NEC 1982 photodiode was not Pinned Photodiode while KODAK 1984 photodiode was Pinned Photodiode.



NEC in the IEDM1982 paper did not apparently use the high energy ion implantation and had no heavily doped surface P+ channel stops adjacent to the buried photodiode. This may be the reason why the P+ surface becomes floating and causing the serious image lag problem in the NEC IEDM1982 buried photodiode. On the other hand, the IEDM1984 KODAK paper used the LOCOS isolation technology which has the hidden P+ channel stops under the LOCOS region that would pin down the adjacent P+ surface potential. Hence the KODAK Photodiode is Pinned Photodiode, for the first time used in the Interline Transfer CCD image sensor.

Pinned Photodiode is by necessity Buried Photodiode, but not all Buried Photodiodes are pinned.

The first Pinned Photodiode was invented by Hagiwara at Sony and is used in ILT CCD Pinned Photodiodes, these same Pinned Photodiodes and the principles behind this complete transfer of charge are used in most CMOS imagers built today.


ELECTRICALENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode? **Buried Photodiode is not always Pinned Photodiode.**

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

Hagiwara proposed in JPA 1975-134985 the double Junction (P+NP) type dynamic Photo Transistor in the (Nsub) substrate with the Pinned P+ surface Hole Accumulation layer.

This is a commonly misunderstood misused set of terminologies.

First off these are not PIN Photodiodes - which stands for P - Intrinsic- N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though.

Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space.

You can get surface state pinning from the dangling Si/SiO2 bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The Si/SiO2 surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface.

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

Edited this Answer to acknowledge Hagiwara-san's contribution, it has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors).

Teranishi did not invent the Pinned Photodiode. The NEC IEDM1982 paper had the serious image lag problem. It was NOT Pinned Photodiode. It was just a Buried Photodiode with the serious image lag problem. Fossum did not invent the in-Pixel source follower amplifier circuit for the Active Amp CMOS image sensors. Peter Noble invented the in-Pixel Amp in 1968. Fossum wrote a fake paper in 2016 in which Fossum insulted SONY and Hagiwara by making a false statement, saying that Hagiwara 1975 patent application had no description on the image lag feature, which is not true. Hagiwara 1975 PPD patents indeed had clear descriptions of the complete charge transfer and no image lag feature.

The First PPD was invented by Hagiwara in 1975. Teranishi did not invent PPD.

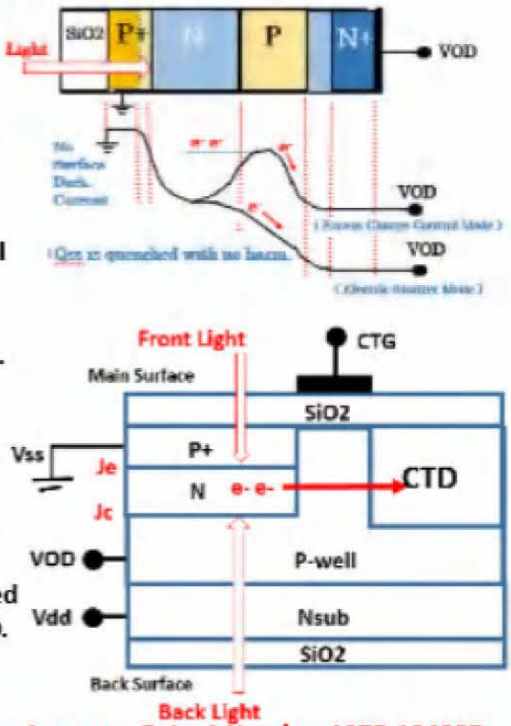
P+NP/Sub junction type Pinned Photo Diode

invented by Hagiwara at Sony in Japanese Patent 1975-134985.

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

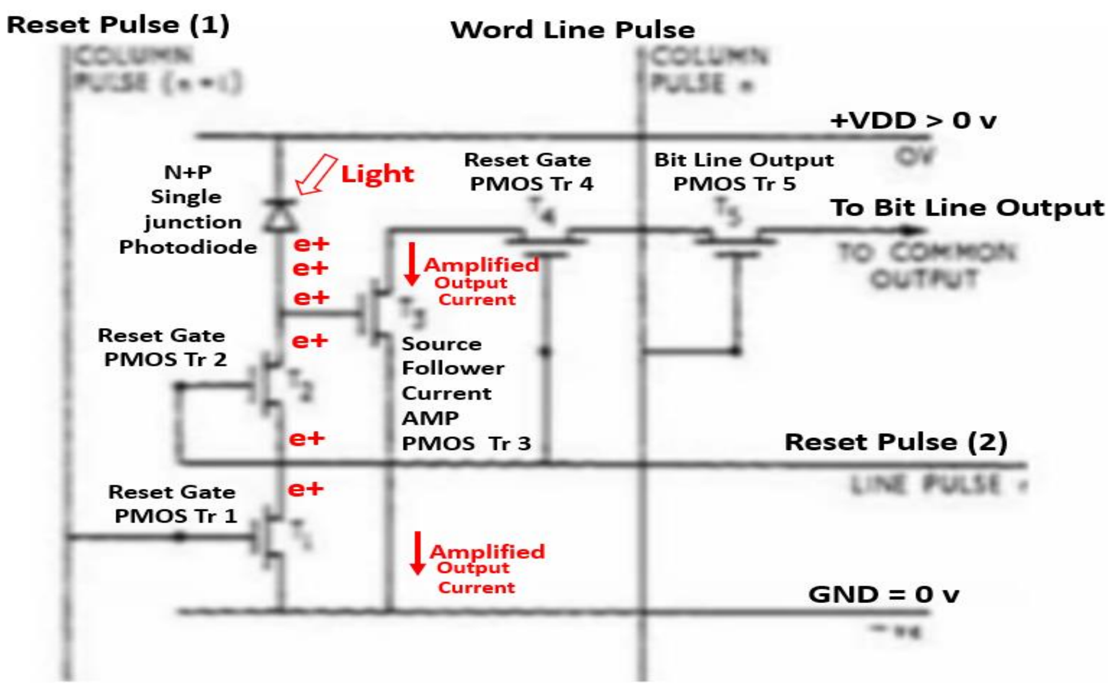
Patent Claim in English Translation

(1) In the semiconductor substrate (Nsub), the first region(Pwell) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N/Pwell Junction) is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N/Pwell) , (6) forming a P+NP Junction type transistor structure with the N/Pwell junction as Collector junction (Jc). (7) The charge, stored in the Base region (N) according to the illuminated light intensity, is transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.



Visit https://www.j-platpat.inpit.go.jp/ and type Japanese Patent Number 1975-134985

Peter Noble invented the in-Pixel Amp MOS Image Sensor in 1968.
See IEEE Transaction Electron devices 15-4 (1968) pp.202-209.
Fossum did not invent the in-Pixel Amp Active CMOS Image Sensor.

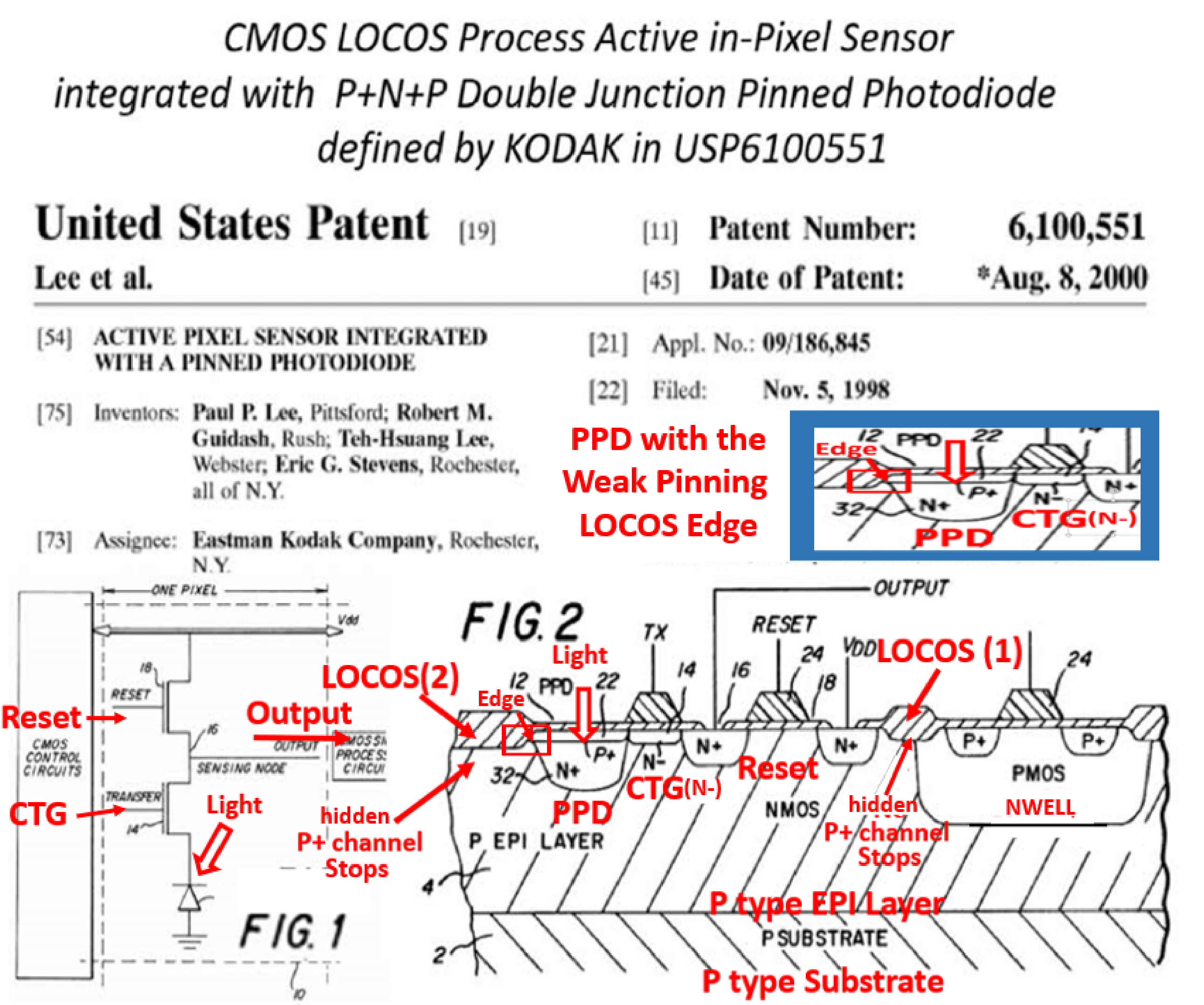


Active Pixel Sensor (APS) with a photodiode and buffer amplifier as proposed by Peter Noble in 1968

NHK scientists developed the active MOS image sensor in 1989 already. See "Amplified MOS Intelligent Imager (AMI)", Japanese TV Journal,41, 11, pp.1075-1081, (1987). Fossum did not invent the Active Amp CMOS Image Sensors.

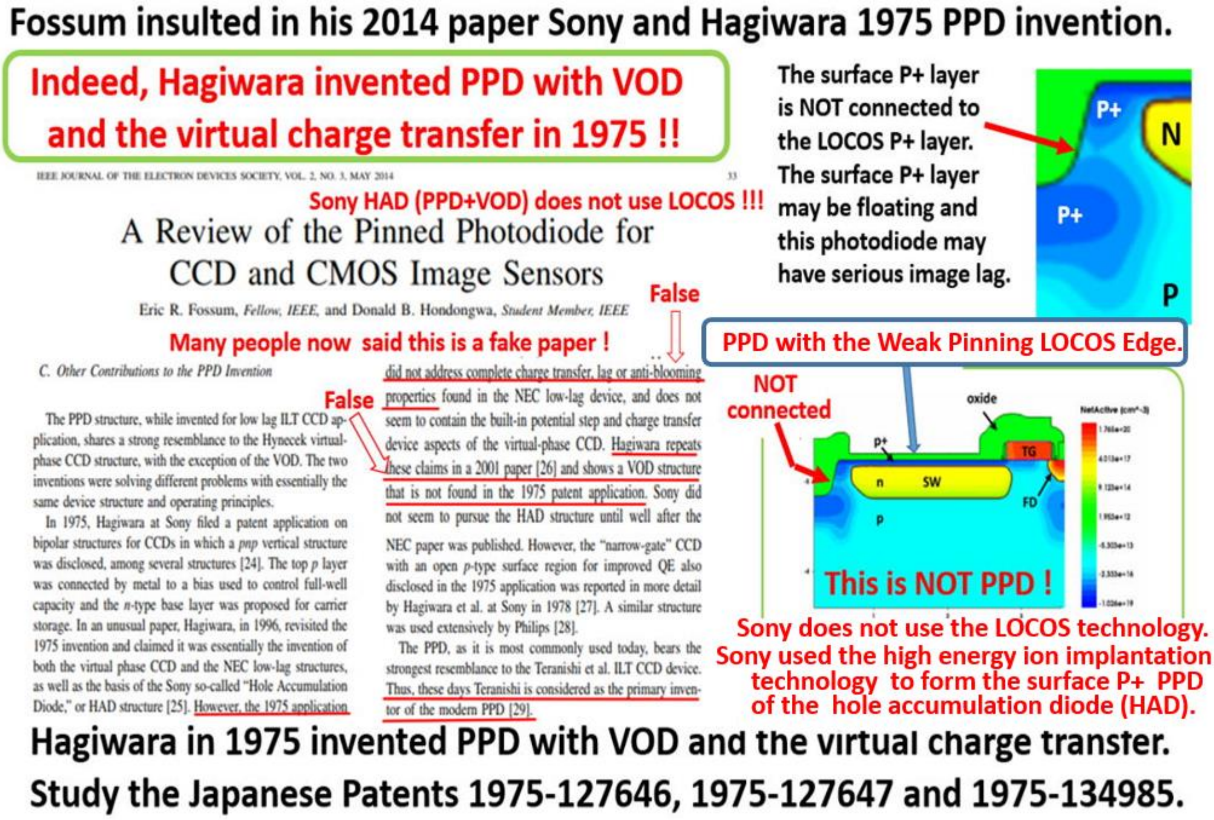
Also see E. Oba, K. Mabuchi, U. Ida, N. Nakamura, and H. Mimura, "A 1/4 Inch 330K Square Pixel Progressive Scan CMOS Active Pixel Image Sensor", ISSCC Digest of Technical Papers, pp. 180-181 (1997).

KODAK also had the USP patent on the CMOS process
applied to the In Pixel Source Follower Amplifier circuit
for modern CMOS Image Sensors.

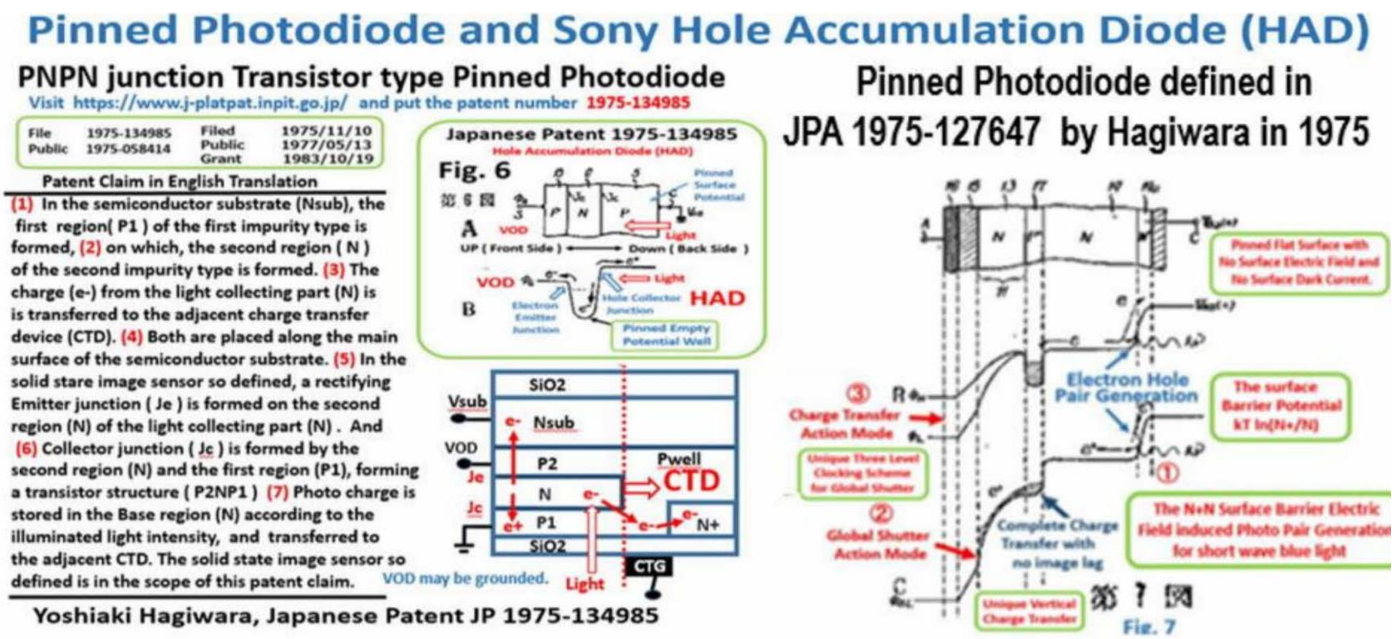


Kodak still used the LOCOS technology for the image sensor process.
Yes, there is possibly hidden P+ channel stops for pinning
under the LOCOS (1) Area Edge and also at the boundary LOCOS (2).

Fossum wrote a fake paper in 2016 in which Fossum insulted SONY and Hagiwara by making a false statement, saying that Hagiwara 1975 patent application had no description on the image lag feature, which is not true.



Sony does not use the LOCOS technology which may have the serious trouble of the silicon crystal stress and also the possible disconnection between the heavily dope P+ channel stops under the LOCOS and the P+ surface hole accumulation layer. Hagiwara 1975 PPD patents indeed had clear description of the empty potential well, the evidence of complete charge transfer and no image lag feature.

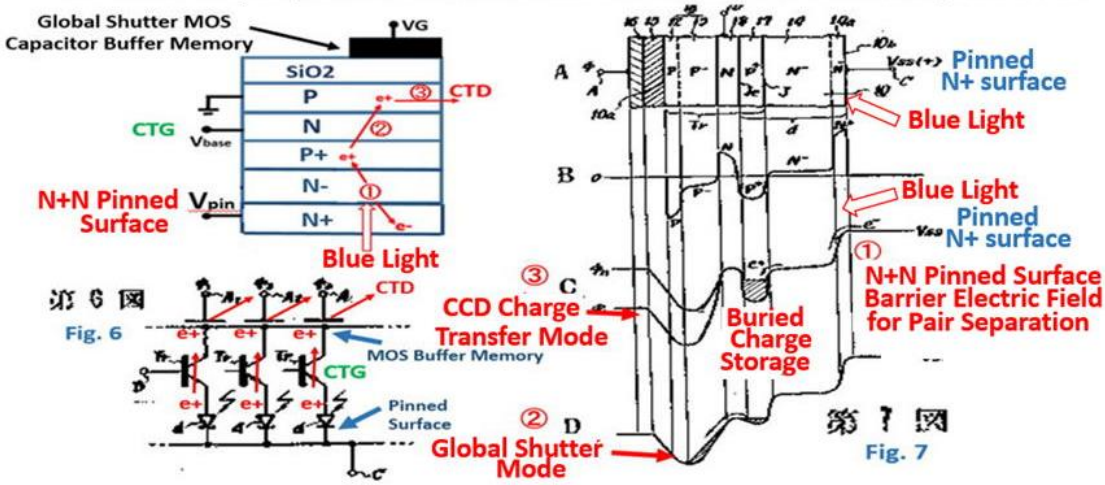


Hagiwara applied two Japanese Patents JPA1975-127646, and JPA1975-127647 for the back light illumination type Pinned Photodiode with Global Shutter Function which is a very important feature needed for the modern CMOS image sensors. The complete charge transfer mode and the no image lag feature is also shown and implied by the empty potential well of the buried charge storage region.

Japanese Patent 1975-127646

N+NP+NP junction type Buried Pinned Photodiode
with Built-in MOS Capacitor Buffer Memory Global Shutter Function
and the surface N+N doping slope Barrier Electric Field Photo Pair Generation

The First Japanese PPD Patent Application JPA 1975-127646 was applied for the back light illumination type Pinned Photodiode (PPD) image sensors with the CCD/MOS capacitor type buffer memory for Global Shutter Function which is a very important function needed for Modern CMOS Image Sensors.



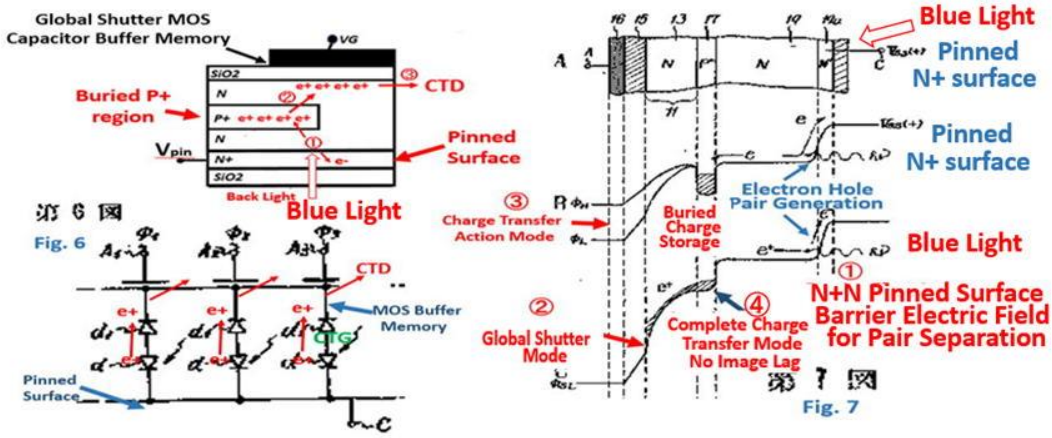
Japanese Patent 1975-127647

Global Shutter Mode

Complete Charge Transfer Mode No Image Lag

N+NP+N junction type Buried Pinned Photodiode
with Built-in MOS Capacitor Buffer Memory Global Shutter Function
and the surface N+N doping slope Barrier Electric Field Photo Pair Generation

This Japanese PPD Patent Application JPA 1975-127647 was also applied for the back light illumination type Pinned Photodiode (PPD) image sensors with the CCD/MOS capacitor type buffer memory for Global Shutter Function which is a very important function needed for Modern CMOS Image Sensors.



Hagiwara also applied two Japanese Patents JPA1975-134985 for the PPD structure with the VOD and also JPA1977-126885 on the electrical shutter clocking scheme controlling the overflow drain voltage in the punch-thru mode.

Japanese Patent 1975-134985

Pinned Photodiode and Sony Hole Accumulation Diode (HAD)

Pinned Surface Double Junction P+NP Dynamic Photo Transistor in the silicon substrate (Nsub)
Pinned Photodiode with the vertical overflow drain (VOD) function in the silicon substrate (Nsub)

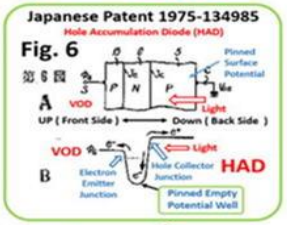
PNPN junction Transistor type Pinned Photodiode

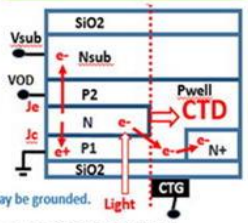
Visit https://www.j-platpat.inpit.go.jp/ and put the patent number 1975-134985

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

Patent Claim in English Translation

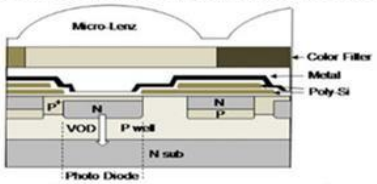
(1) In the semiconductor substrate (Nsub), the first region(P1) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N) is is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N) . And (6) Collector junction (Jc) is formed by the second region (N) and the first region (P1), forming a transistor structure (P2NP1) (7) Photo charge is stored in the Base region (N) according to the illuminated light intensity, and transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.





Yoshiaki Hagiwara, Japanese Patent JP 1975-134985

Most CCD Image sensors and CMOS Image sensors today are applied with the combination of the vertical overflow drain (VOD) and Pinned Photodiode.



In 1975 Yoshiaki Hagiwara at Sony proposed using a PNP transistor as the photodetector which is the combination of the VOD and Pinned Photodiode.

By providing a P + layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated, greatly improving the light sensitivity. This P + layer was also a proposal to reduce the dark current and image lag which became the basis of the pinned photodiode

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

Double Junction Dynamic Photo Transistor (PPD) invented in 1975 by Hagiwara at Sony.

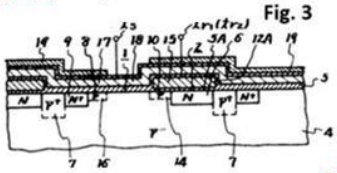
Triple Junction Dynamic Photo Thyristor (HAD) invented in 1975 by Hagiwara at Sony.

See Japanese Patent Application JPA 1975-127646, 1975-127647 and 1975-134985

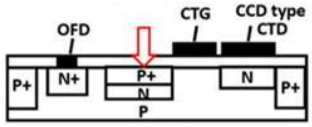
Japanese Patent 1977-126885

Japanese Patent JPA 1977-126885 on Electrical Shutter Clocking Scheme invented by Y. Hagiwara, S. Ochi and T. Hashimoto in 1977.

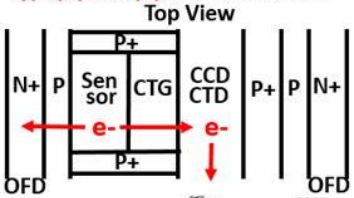
Type(A) CCD/MOS Photo Capacitor



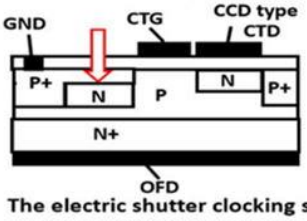
Type(B) PPD with Lateral OFD



Type(A) and (B) with Lateral OFD Top View



Type(C) Vertical OFD (VOD) PPD with CCD type CTD



Type(D) Vertical OFD (VOD) PPD with CMOS type CTD

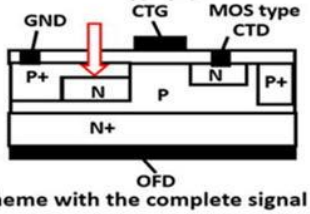


Fig. 7

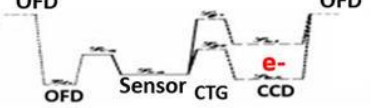
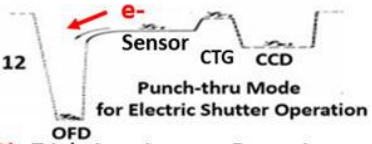


Fig. 8

Fig. 12



The electric shutter clocking scheme with the complete signal charge draining of no image lag can be achieved by the OFD punch-thru voltage control for any photodiodes, including not only the type (A) of the conventional CCD/MOS photo capacitor but also (B), (C) and (D) type Pinned Photodiodes.

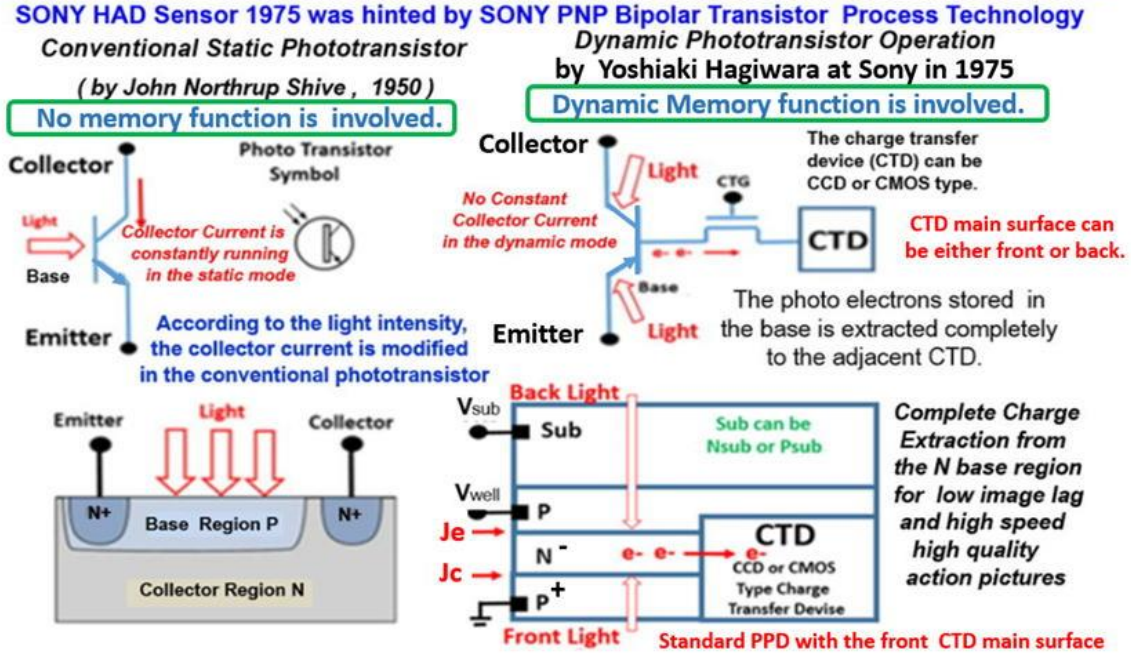
Type(B) Double Junction type Dynamic Photo Transistor (PPD) invented in 1975 by Hagiwara.

Type (C) and (D) Triple Junction type Dynamic Photo Thyristor (HAD) invented in 1975 by Hagiwara

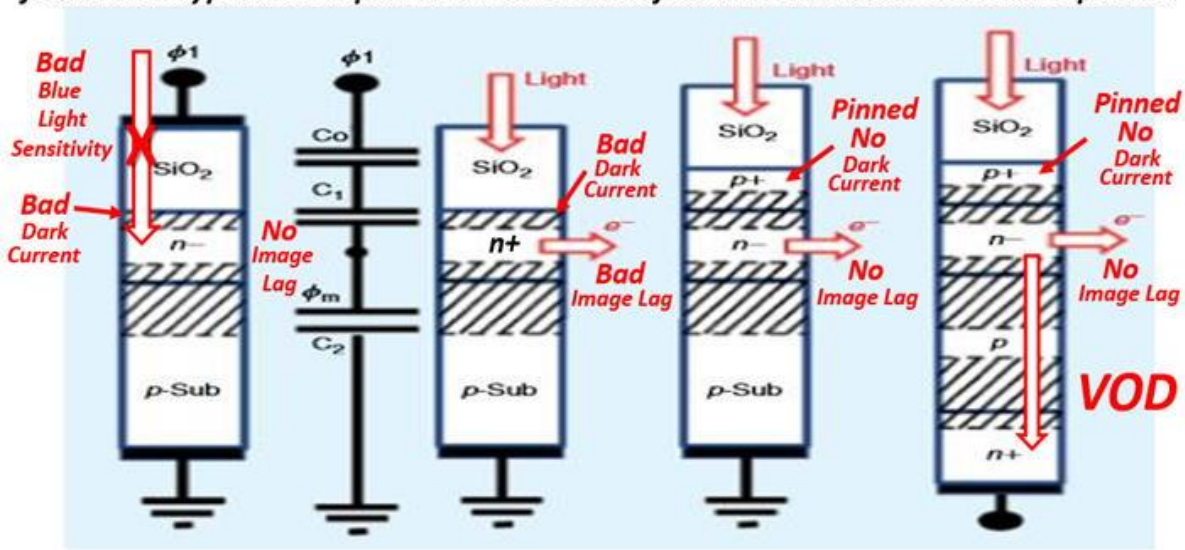
See Japanese Patent Application JPA 1975-127646, 1975-127647 and 1975-134985

Difference of the static and dynamic photo transistors are illustrated in these figures.
Sony Hole Accumulation Diode (HAD) is the P+NPNsub junction dynamic photo transistor with the surface P+ hole collecting and accumulation region is pinned and grounded, which is now widely called as Pinned Photodiode with the vertical overflow drain (VOD) function. Only Pinned Photodiode with the VOD function can realize the electrical shutter function.

SONY HAD Sensor 1975 was hinted by SONY PNP Bipolar Transistor Process Technology



History of dynamic Solid State image sensing structure
from BCCD type MOS capacitor to the P+NPN junction Pinned Photodiode capacitor



(1) CCD type
invented by Bell Lab in 1968

(2) N+P type
The classical photodiode with serious image lag

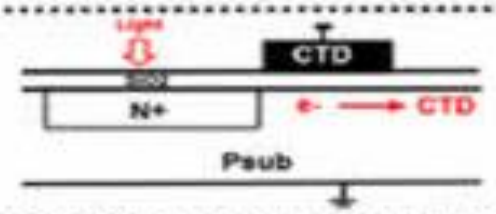
(3) P+NP type (4) P+NPN type
(3) and (4) are the P+NP junction type Pinned Photodiode invented by Yoshiaki Hagiwara, 1975

In Japanese patent 1975-134985, Hagiwara at Sony invented the Pinned photodiode with very low dark current, which is also the completely depleted Buried Photodiode with image lag free picture quality, and also with the built-in vertical overflow drain (VOD) function.

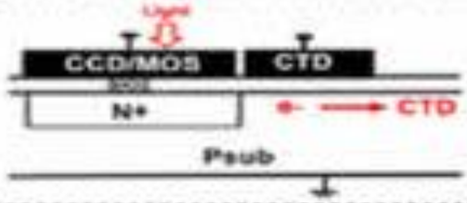
Reference: IEEE Solid-STATE CIRCUITS MAGAZINE, SUMMER 2013 issue pp. 6 ~

Four Types of Image Sensor Structure

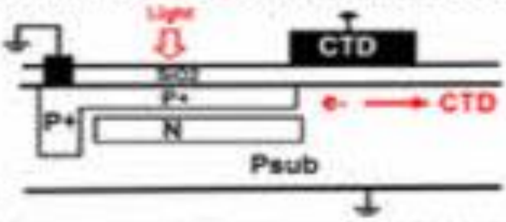
(1) the N+P Single Junction type
Classical Floating Surface
Dynamic Photodiode



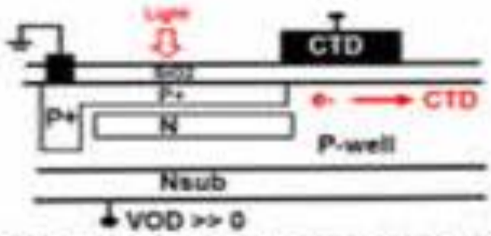
(2) the CCD/MOS Metal Oxide Gate
Dynamic Photo Capacitor
invented and developed
by Boyle/Smith in 1969

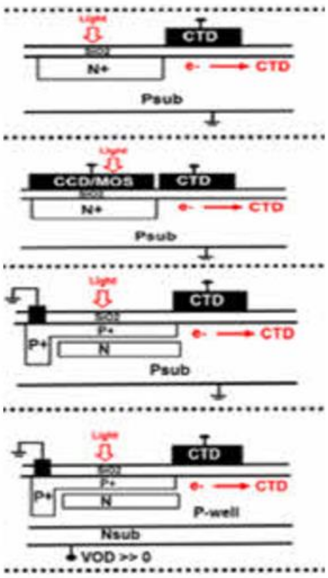


(3) the P+NPsub Double Junction type
Pinned Photodiode
invented by Hagiwara in 1975
and developed in 1978
by Hagiwara Team in Sony
with Excellent Blue Light Sensitivity
No Image Lag and No Surface Dark Current



(4) the P+NPNsub Triple Junction type
Pinned Photodiode
invented by Hagiwara in 1975
and developed in 1987
by Hamazaki Team in Sony
with Completely Mechanical-Parts Free
No Image Lag Electrica Shutter

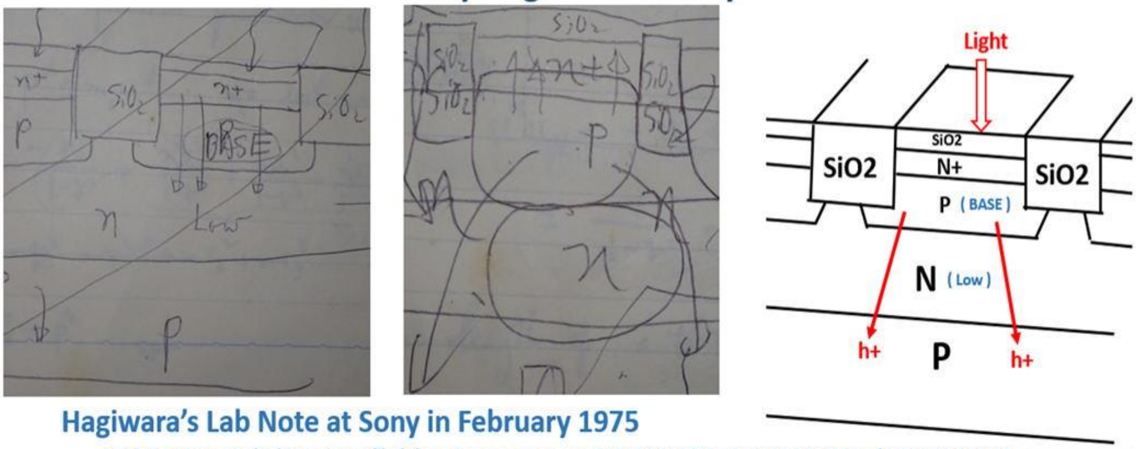




	Blue Light Sensitivity	Image Lag	Surface Dark Current	Electric Shutter
(1)	△	×	○	×
(2)	×	○	×	×
(3)	○	○	○	×
(4)	○	○	○	○

Four Types of Image Sensor Structure

The N+PNP junction type Dynamic Photo Transistor Structure
Pinned Photodiode and Sony Hole Accumulation Diode (HAD)
with the vertical overflow drain (VOD) function
invented by Hagiwara at Sony in 1975

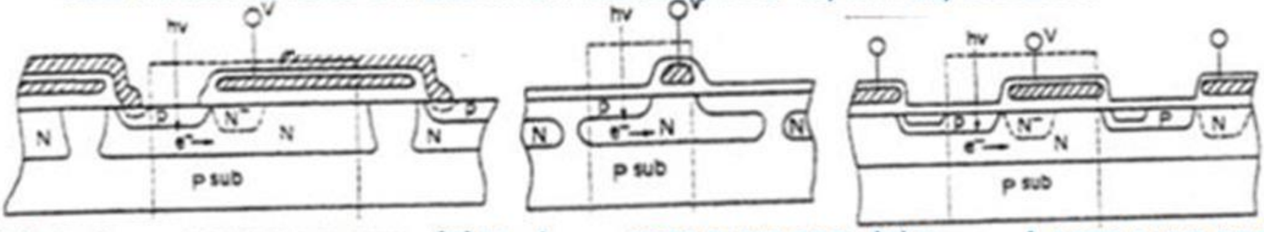


Hagiwara's Lab Note at Sony in February 1975

In 1975 at Sony, Yoshiaki Hagiwara filed three Japanese patents JPA1975-127646, JPA1975-127647 and JPA1975-134985 on the Pinned Surface Photodiode with the VOD function which is later called as Sony Hole Accumulation Diode (HAD). Hagiwara did not file a patent on the SiO2 device isolation but this lab note shows that Hagiwara had an idea of forming the Shallow Trench Isolation by the Local Oxidation Method, which was hinted by the LOCOS isolation in 1970s.

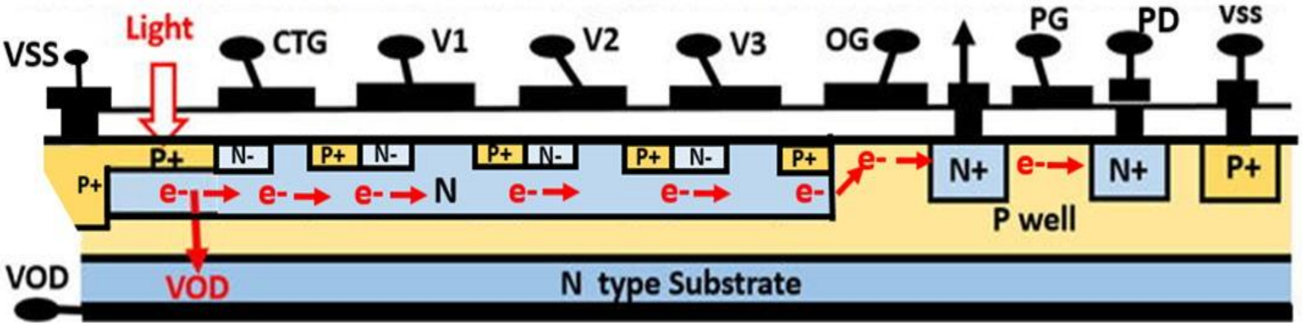
Since PPD also has the complete charge transfer capability, a single polysilicon electrode type CCD delay line becomes possible with the complete charge transfer, by creating the pinned potential wells of PPD at the polysilicon electrode gaps.

See the Japanese Patent 1975-134985 for the original invention of the Pinned Photodiode
High-Density and High-Quality Frame Transfer CCD Imager with
Vey Low Smear, Low Dark Current, and Very High Blue Sensitivity
Yoshiaki Hagiwara
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 43, NO. 12, DEC 1996



(1) Hagiwara 1975 P+NP PPD (2) Hagiwara 1978 P+NP PPD (3) Henecek 1979 P+NP PPD

The most important idea of the P+NP Double Junction Buried Pinned Photodiode proposed by Hagiwara in the 1975-134985 Japanese Patent Application is the virtual complete charge transfer operation with no image lag which does not need the conventional double polysilicon overlapping CCD process with very poor productivity.



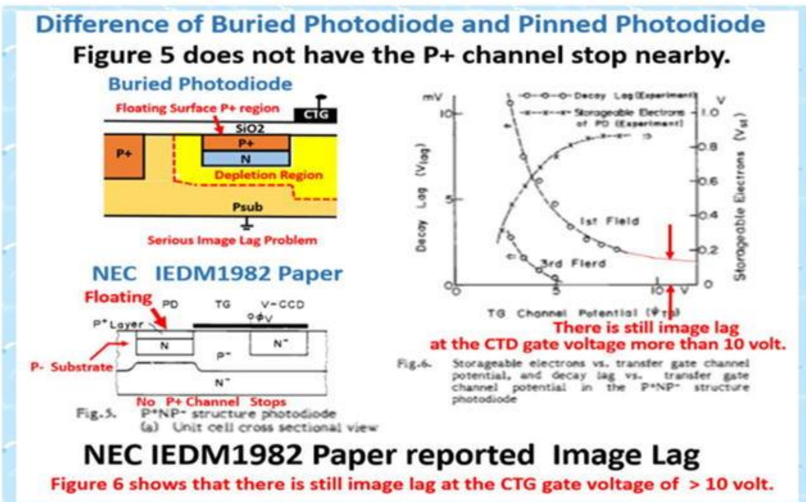
The electric shutter function becomes possible only in the CCD/MOS type photo capacitor sensor and Pinned Photodiode (PPD), both of which have the complete charge transfer capability of no image lag. However, Buried Photodiode (BPD) is not always Pinned Photodiode (PPD). But, Pinned Photodiode (PPD) is always Buried Photodiode (BPD). Buried Photodiode (BPD) and Pinned Photodiode (PPD) are both the same double junction type PNP dynamic photo transistors invented by Yoshiaki Hagiwara in 1975.

Hagiwara applied two Japanese Patents JPA1975-127646, and JPA1975-127647 for the back light illumination type Pinned Photodiode with Global Shutter Function which is a very important feature needed for the modern CMOS image sensors. The complete charge transfer mode and the no image lag feature is also shown and implied by the empty potential well of the buried charge storage region.

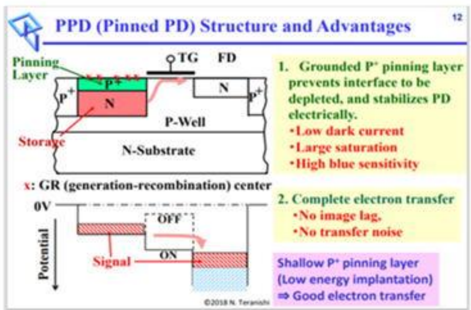
Hagiwara also applied two Japanese Patents JPA1975-134985 for the PPD structure with the VOD and also JPA1977-126885 on the electrical shutter clocking scheme controlling the overflow drain voltage in the punch thru mode.

Teranishi did not invent Pinned Photodiode. The NEC IEDM1982 paper had the serious image lag problem. It was NOT Pinned Photodiode. It was just a Buried Photodiode with the serious image lag problem. We cannot not obtain the empty potential well unless the surface P+ hole accumulation layer is completely pinned.

Hagiwara invented PPD in 1975 and developed PPD in 1978 and reported in the SSDM1978 conference.
See JPA 1975-127646, 1975-127647 and 1975-134985. Also see the SSDM1978 paper by Hagiwara.



Teranishi added the P+ channel stops in his recent report as if he invented PPD with the P+ channel stops nearby. Teranishi was not honest at all.



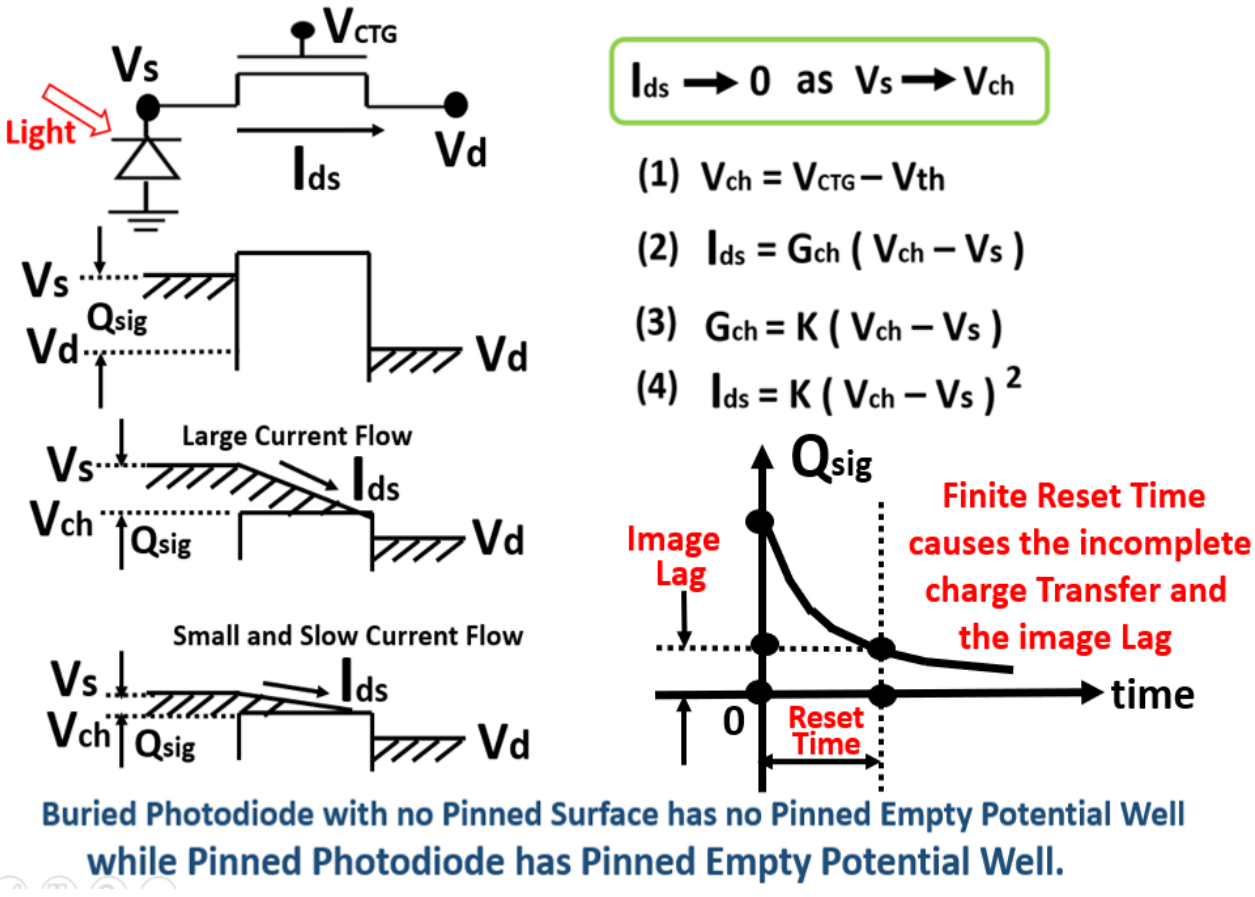
The photodiode reported in IEDM1982 by Teranishi did not have the P+ channel stops nearby , and it had a serious image lag as seen in Fig. 6. Any Photodiode with a serious image lag is not Pinned Photodiode. Teranishi did not develop Pinned Photodiode.
Teranishi added the P+ channel stops in his recent paper dishonestly.

https://indico.cern.ch/event/706286/attachments/1601588/2547606/20180223CERN_ver2.pdf

The simple analysis of the saturation mode MOS transistor Current and Voltage Relationship can be used to explain why the classical floating N+P junction type photodiode has the serious image lag problem. The limited time allowed for reset is the cause of the serous image lag problem since it would take a long time for transferring the signal charge Qsig thru the adjacent charge transfer gate (CTG).

The floating N+P junction type photodiode has the serious Image Lag Problem.

Buried Photodiode with no Pinned Surface also has the serious Image Lag problem.



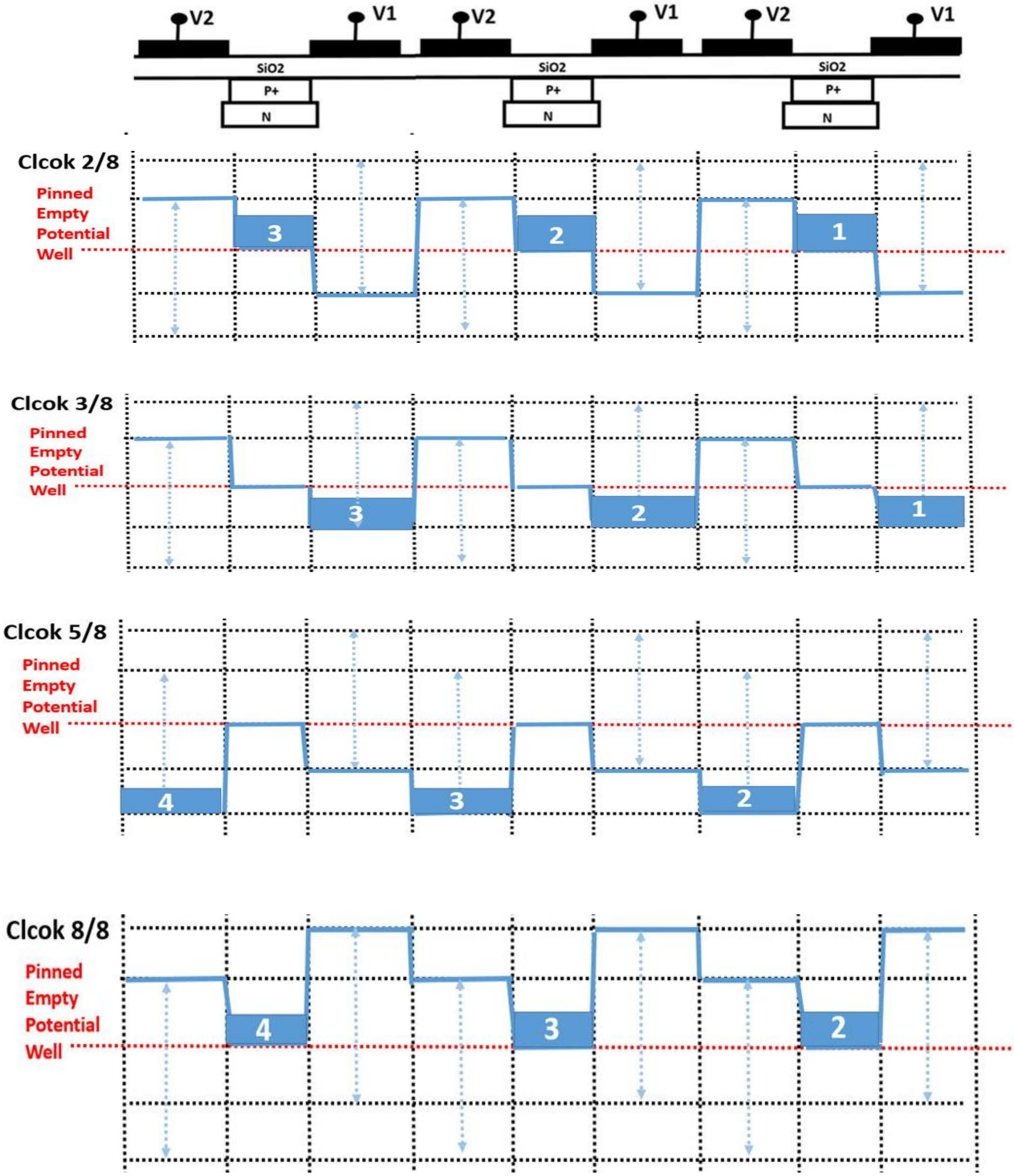
Buried Photodiode with no Pinned Surface has no Pinned Empty Potential Well while Pinned Photodiode has Pinned Empty Potential Well.

Enen the P+NPNsub junction type Sony Hole Accumulation Diode (HAD) would have the serioous image lag and would not have been operated in the complate image lag free mode with the electrical shutter capability unless the surface P+ hole accumulation layer is pinned by the adjacent heavily doped P+ channel stops.

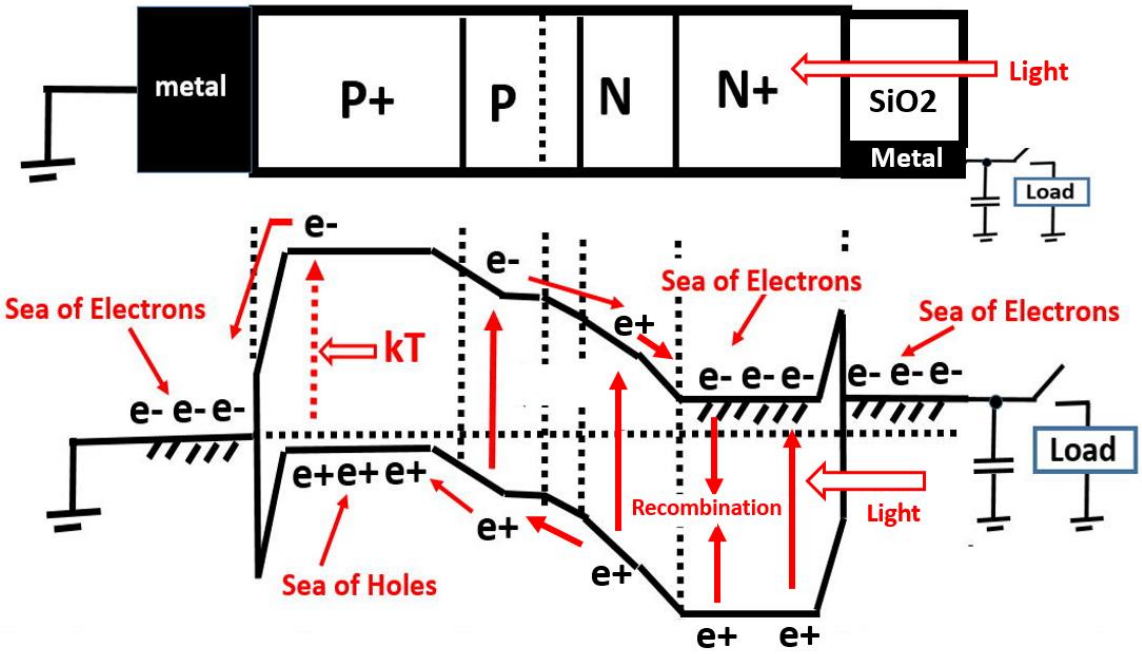
If the surface P+ hole accumuation layer is floating, it may be at some positive value potential and would have no enough voltage drop between the surface P+ hole accumualtion layer and the buried N type signal charge storage region. The buried N type signal charge storage potential would stay at a strong positive potential and the signal charge would not be transferred completely to the charge transfer gate (CTG) nearby and would suffer the serious image lag problem.

Hagiwara_invented_PPD_and_Virtual_Charge_Transfer_in_1975

Hagiwara in 1975 proposed the PPD Charge Transfer which is later called as Virtual Phase Charge Transfer.
Hagiwara in 1975 proposed also the NEC Buried Photodiode, the KODAK PPD and the Sony HAD.
Study Japanese Patent 1975-127646, 1975-127647 and 1975-134985 for the details.

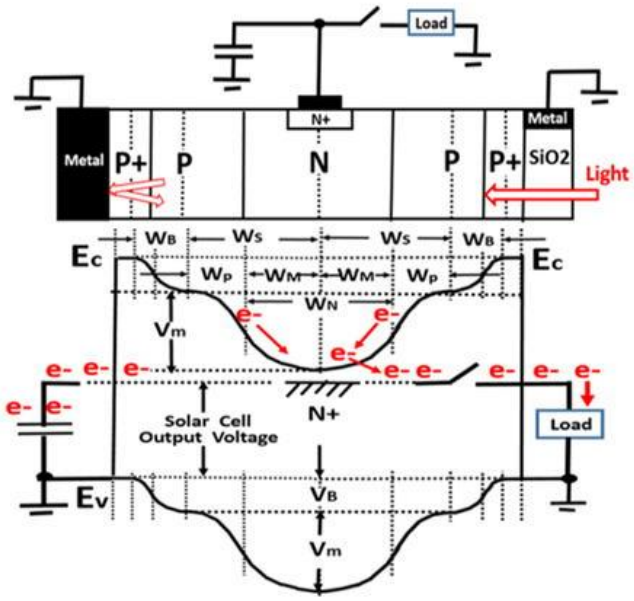


The conventional single N+P junction type solar cell has a very poor efficiency of the photon to electron energy conversion.



Pinned Photodiode (PPD) has the excellent short wave blue light sensitivity, the very low surface dark leakage current feature and the complete charge transfer capability for the excellent image lag free picture quality needed for the electric shutter. Now this double junction type PPD is proposed to apply for solar cells.

Minimum Potential V_m and Width W_{cell} of Solar Cell



$$W_{cell} = 2\,(W_B + W_s)$$

W_B can be controlled by the Surface P+P Gaussian doping slope.

Set $V_m = E_G/2$

$$V_m = \frac{1}{2\varepsilon_{si}}\left(N_p W_p^2 + N_d W_M^2\right)$$

$$N_p W_p = N_d W_M$$

$$W_s = W_p + W_M$$

$$\frac{1}{N} = \frac{1}{N_p} + \frac{1}{N_d}$$

N type 500 Ω cm Silicon Wafer

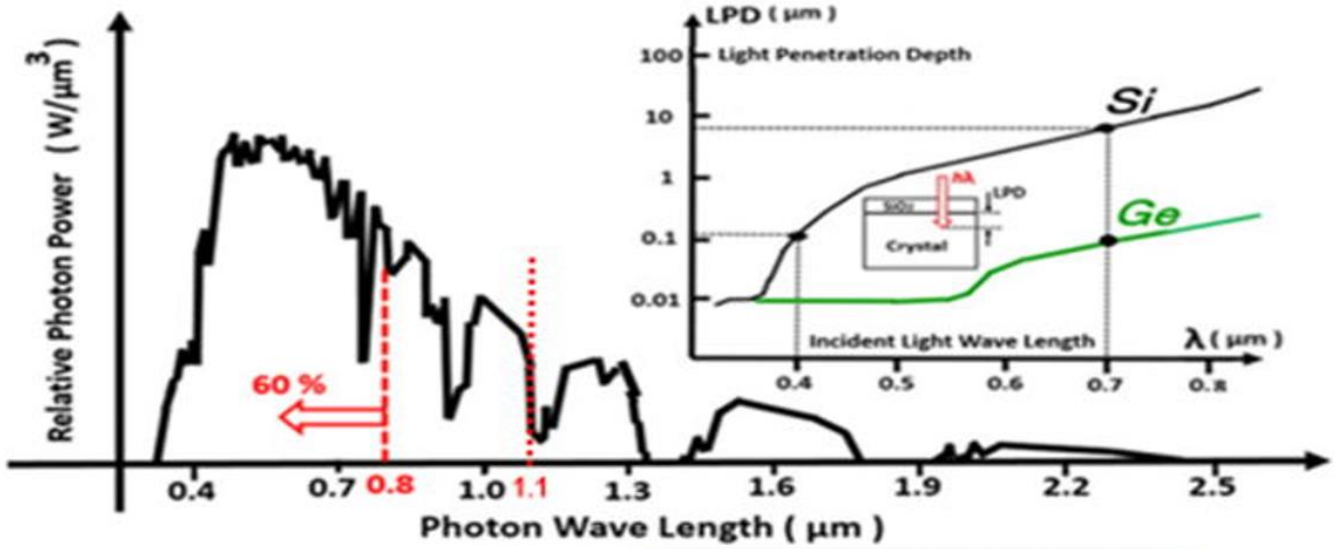
$\varepsilon_{si} = 648$ e / volt·μm

$E_G = 1.1$ volt

$N = 7.128$ e / μm^3

$$W_{cell} = 2\left(W_B + \sqrt{\frac{\varepsilon_{si} E_G}{N}}\right)$$

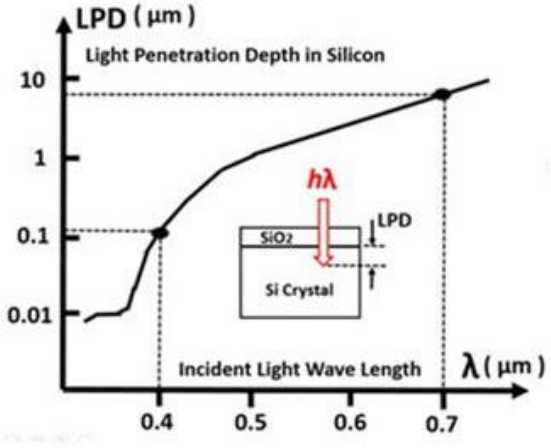
gives $W_s = 10$ μm.



For Silicon, E_G = 1.10 eV and λ = 1.12 μm

$$E = \hbar\omega = h f = h c / \lambda$$
$$E\ (eV) = 1.24 / \lambda\ (\mu m)$$

Silicon Based Solar Cells of the Enery Gap = 1.10 eV cannot convert photon energy of the wave length more than λ = 1.12 μm.



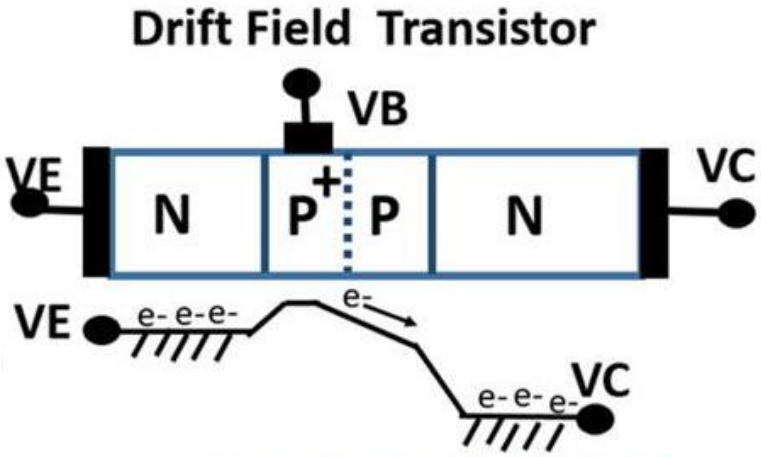


Figure 7 of JAP 1975-127647

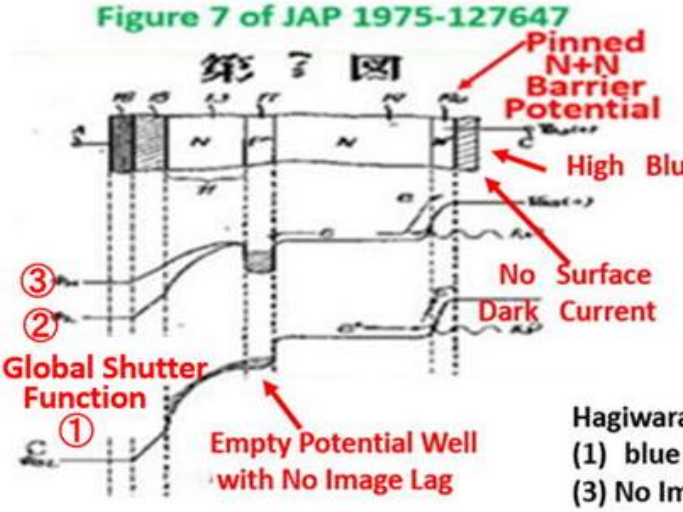
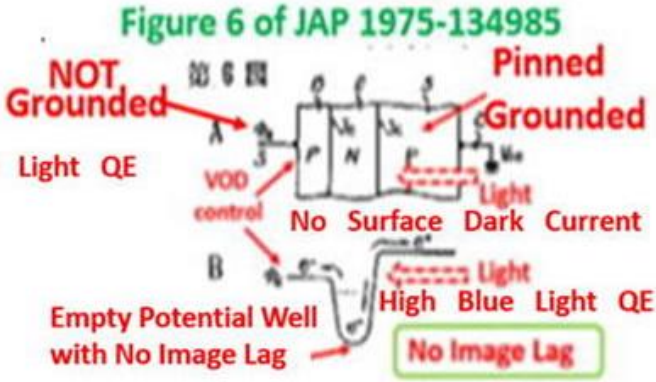
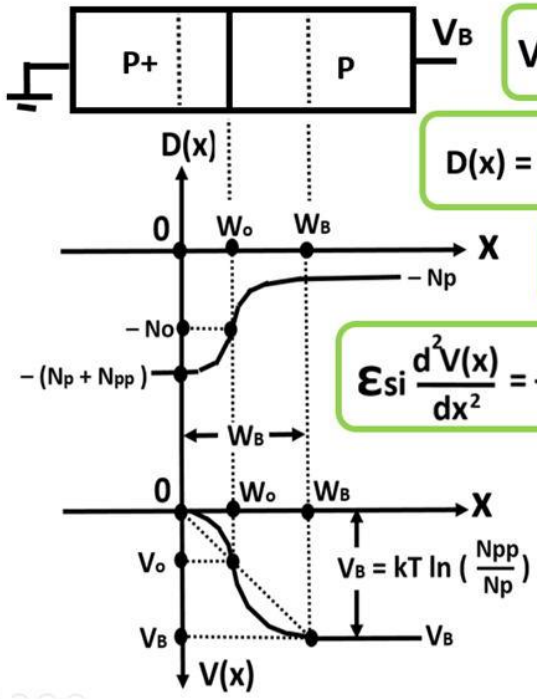


Figure 6 of JAP 1975-134985



Hagiwara invented PNP junction type PPD in 1975 with (1) blue light 100% QE, (2) No Surface Dark Current and (3) No Image Lag, Complete Charge Transfer features.

The Barrier Potential V_B and the Width W_B



$$V_B = kT \ln\left(\frac{N_{pp}}{N_p}\right) \qquad W_B = W_o \frac{V_B}{V_o}$$

$$D(x) = -N_p - N_{pp} \exp\left(-\frac{x^2}{R^2}\right) \quad \text{for } x > 0$$

$$\frac{d^2 D(x)}{dx^2} = 0 \quad \text{at } x = W_o \qquad W_o = \frac{R}{\sqrt{2}}$$

$$\varepsilon_{si} \frac{d^2 V(x)}{dx^2} = -D(x) - (N_p + N_{pp}) \exp\left(-\frac{V(x)}{kT}\right)$$

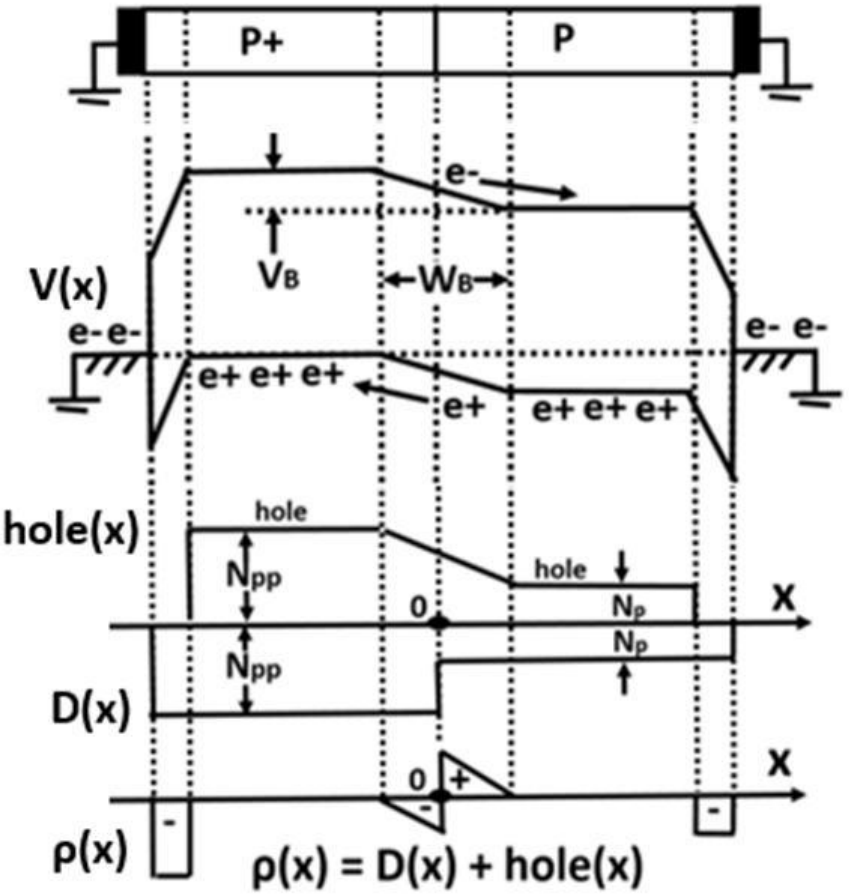
$$V(x) = 0 \quad \text{at } x = 0$$

$$V(x) = V_B \quad \text{at } x = W_B$$

$$N_o = N_p + N_{pp} \exp\left(-\frac{W_o^2}{R^2}\right)$$

$$N_o = (N_p + N_{pp}) \exp\left(-\frac{V_o}{kT}\right)$$

P+P Doping Slope Barrier Potential V_B

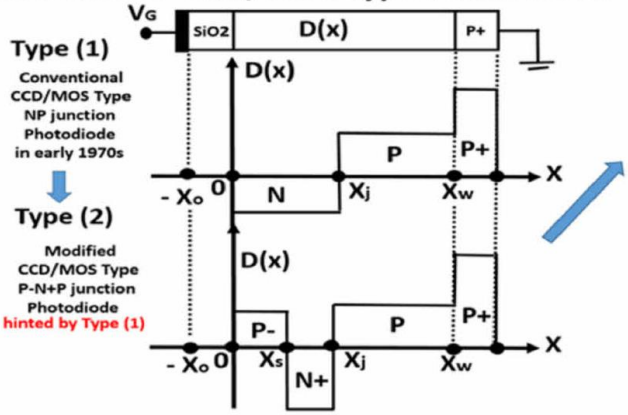


Origin of 1975 Pinned Photodiode Concept was hinted by CCD/MOS type Buried Photodiode

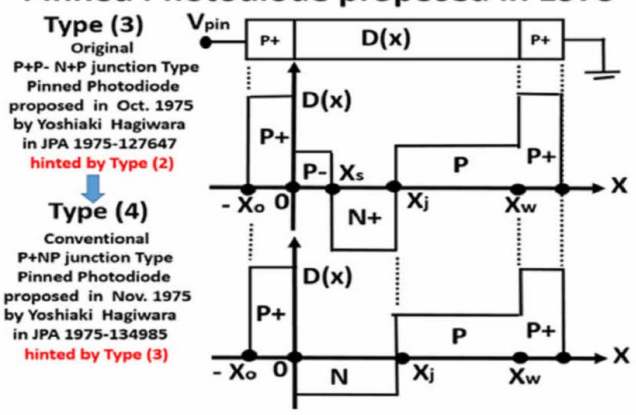
See JPA 1975-127646, JPA 1975-127647 and JPA 1975-134985 by Yoshiaki Hagiwara in 1975

Numerical Computation of Potential V(x) of Arbitrary Doping Profile D(x) from x = 0 to x = Xw with the given boundary condition V(x) = Vs and dV(x)/dx = Es at x = 0 .
Find the proper value of V(x) = Vs so that we have V(x) = Vw and dV(x)/dx = Ew at x = Xw.

Conventional CCD/MOS type Photodiode



Pinned Photodiode proposed in 1975



For x < 0 in Type(1) and Type(2)

$$\frac{d^2V(x)}{dx^2} = 0$$

gives at x = 0

$$E_s = C_{ox}\,(\,V_s - V_G + V_{mo} - V_{os}\,)\,/\varepsilon_{si}$$

For x < 0 in Type(3) and Type(4)

$$\varepsilon_{Si}\frac{d^2V(x)}{dx^2} = N_{pp} - N_{pp}\exp(\,(\,V_{pin} - V(x)\,)\,/\,kT\,)$$

gives at x = 0

$$E_s = \sqrt{\frac{2\,N_{pp}\,kT}{\varepsilon_{si}}\left\{\left(\frac{V_s}{kT}\right) - 1 + \exp\left(-\frac{V_s}{kT}\right)\right\}}$$

For 0 < x < Xw in all types (1) thru (4)

$$\varepsilon_{Si}\frac{d^2V(x)}{dx^2} = D(x) - N_{pp}\exp(\,-V(x)\,/\,kT\,)$$

needs to be solved numerically for any arbitrary doping function D(x).

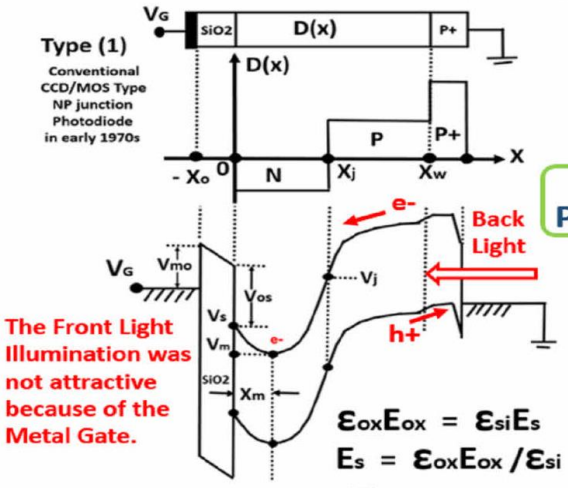
For Xw < x in all types (1) thru (4)

$$\varepsilon_{Si}\frac{d^2V(x)}{dx^2} = N_{pp} - N_{pp}\exp(\,-V(x)\,/\,kT\,)$$

gives at x = Xw

$$E_w = -\sqrt{\frac{2\,N_{pp}\,kT}{\varepsilon_{si}}\left\{\left(\frac{V_w}{kT}\right) - 1 + \exp\left(-\frac{V_w}{kT}\right)\right\}}$$

The conventional Buried Channel CCD/MOS type photodiode has a very large surface electric field Es.



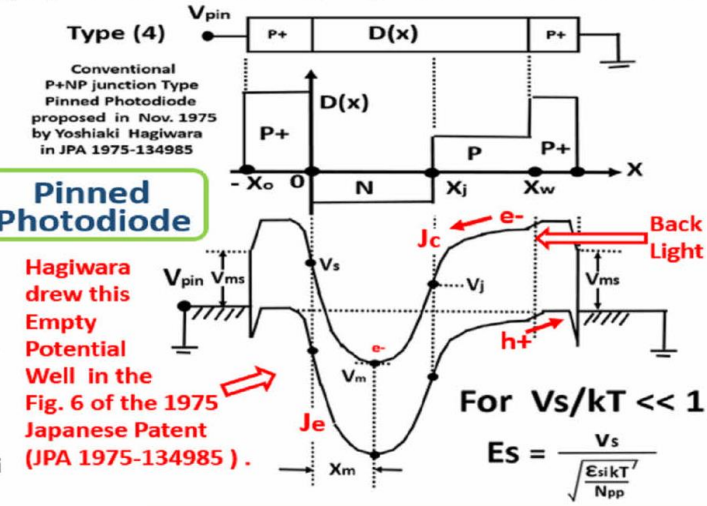
The Front Light Illumination was not attractive because of the Metal Gate.

$$\varepsilon_{ox}E_{ox} = \varepsilon_{si}E_s$$

$$E_s = \varepsilon_{ox}E_{ox}\,/\varepsilon_{si}$$

$$V_s = V_G - V_{mo} + E_{ox}\,X_o + V_{os}$$

$$E_s = C_{ox}\,(\,V_s - V_G + V_{mo} - V_{os}\,)\,/\varepsilon_{si}$$



Pinned Photodiode

Hagiwara drew this Empty Potential Well in the Fig. 6 of the 1975 Japanese Patent (JPA 1975-134985).

For $V_s/kT \ll 1$,

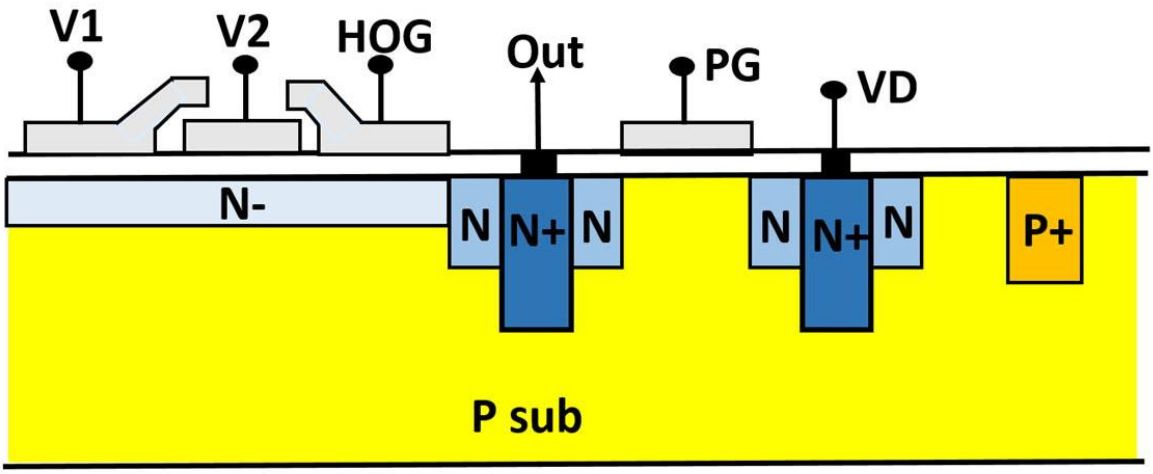
$$E_s = \frac{V_s}{\sqrt{\frac{\varepsilon_{si}kT}{N_{pp}}}}$$

$$E_s = \sqrt{\frac{2\,N_{pp}\,kT}{\varepsilon_{si}}\left\{\left(\frac{V_s}{kT}\right) - 1 + \exp\left(-\frac{V_s}{kT}\right)\right\}}$$

The surface electric field Es of the P+NP junction type Pinned Photodiode is also very large which is worse since the surface electric field depends also on the surface P+ doping level Npp. Type (2) and Type (3) modifications may help reducing the surface electric field Es.

Hagiwara had the idea of the lightly doped drain (LDD) concept and used for the CCD output of Sony FT (FCX018) and ILT (ICX008) CCD image sensors that Hagiwara designed and developed with other Sony engineers in 1978. But Hagiwara did not disclose the details of CCD design knowhows to the public. Hagiwara did not file any patent on the LDD concept in 1978.

Lowly Doped Drain (LDD) MOS used in Sony CCD Image sensors in SSDM1978 paper by Hagiwara at Sony.



For ONE chip Image sensor in NTSC system, Sony(Hagiwara) needed the CCD clock frequency of 14.31818 MHz.
Sony (Haiwara) used the thermal diffusion N+ for the metal contact with the lightly doped drain for the prcharge (PG) gate.

Sony used already in early 1970s the correlated double sampling (CDS) technique intensively for the clock noise reduction for CCD image sensors. This CDS technique reduced the clock noise of MOS image sensors much more drastically.

M.M. White et al, "Characterization of Surface Channel CCD Image Arrays at Low Light Levels", IEEE J. Solid State Circuits, SC-9, pp.410-414 (1974)

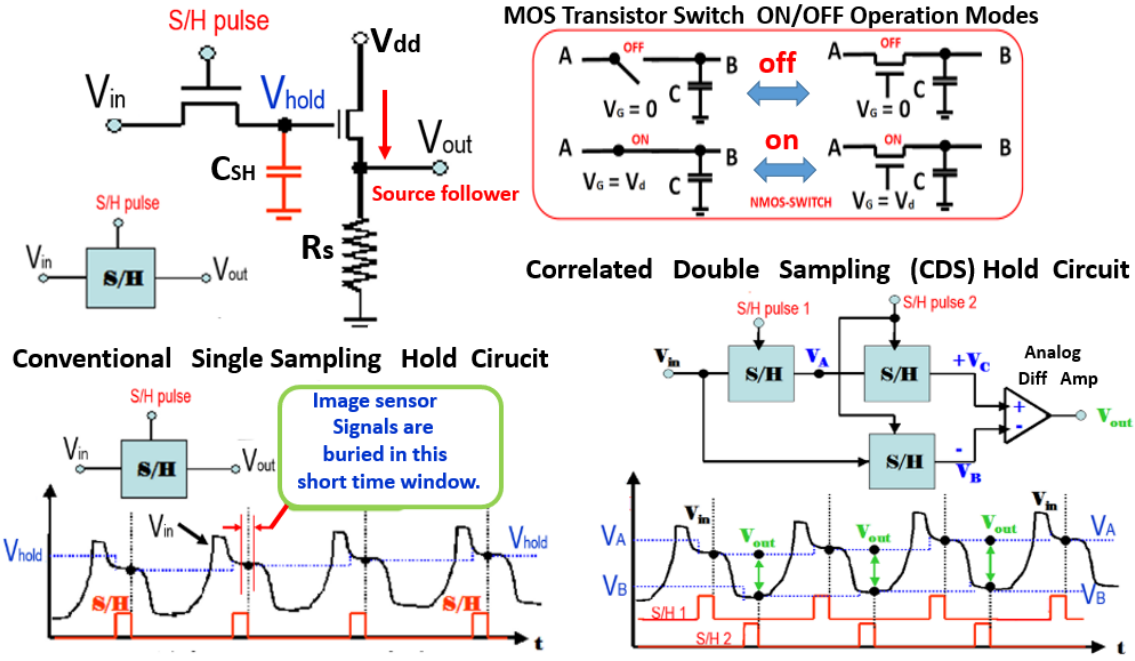


Image sensor Signals are buried in the large clock noises.

Sony reported "High Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor" in ISSCC2006.

ISSCC 2006 / SESSION 27 / IMAGE SENSORS / 27.5

Modern CMOS Image Sensors have (1) HAD (2) APS and (3) CDS.

(1) HAD (PPD) was invented by Y. Hagiwara in 1975.
(2) APS was invented by Peter Noble in 1968.
(3) CDS was invented by M. White in 1972.
(4) Sony engineers perfected these technologies in 2006.

27.5 High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor

Yoshikazu Nitta, Yoshinori Muramatsu, Kiyotaka Amano, Takayuki Toyama, JunYamamoto, Koji Mishina, Atsushi Suzuki, Tadayuki Taura, Akihiko Kato, Masaru Kikuchi, Yukihiro Yasui, Hideo Nomura, Noriyuki Fukushima
Sony, Atsugi, Japan

Traditionally, the advantages of compact image sensors (CISs) over CCDs have been low power consumption and the capability for system integration. Additionally, the image quality of CISs has recently begun to rival and even surpass that of CCDs in the area of high-speed imaging [1]. Compared to high-speed CCDs, CISs utilize the advantage of a column-parallel pixel readout.

The pixels are conventional 4T active pixel sensor (APS) pixels that use hole accumulation diodes (HADs). HADs enable image sensors such as CCDs and CISs to realize ideal properties of low dark current, no kTC noise, and no image lag [2]

Digital double-sampling architecture is proposed to remove device variation and circuit offset that cause vertical FPN [3]. Our column-inline dual-CDS architecture (Fig. 27.5.2) implements digital double-sampling (digital CDS) and analog CDS in parallel columns. A high-speed 297MHz clock is utilized to reduce the double digital sampling period. Additionally, an analog CDS is used to reduce the ADC period for the reset signal V_{RST} by eliminating the analog offset of the pixel and the comparator output.

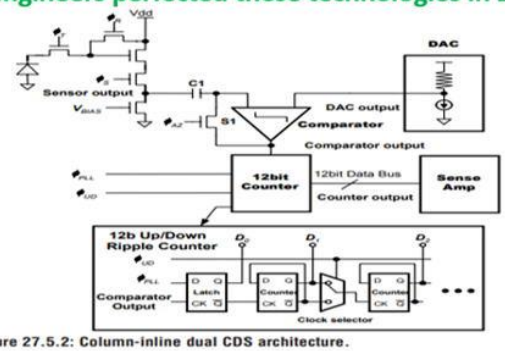
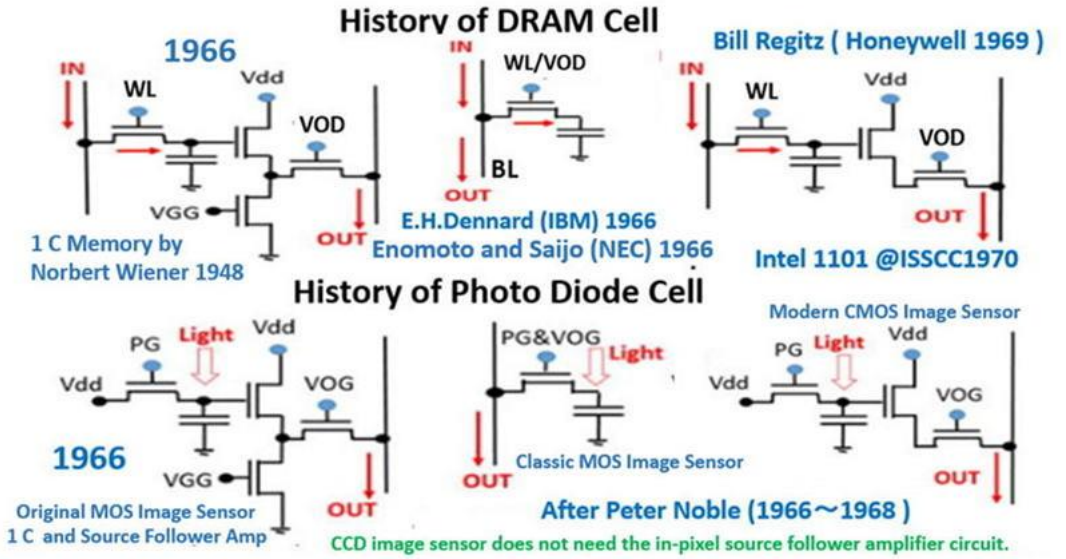


Figure 27.5.2: Column-inline dual CDS architecture.

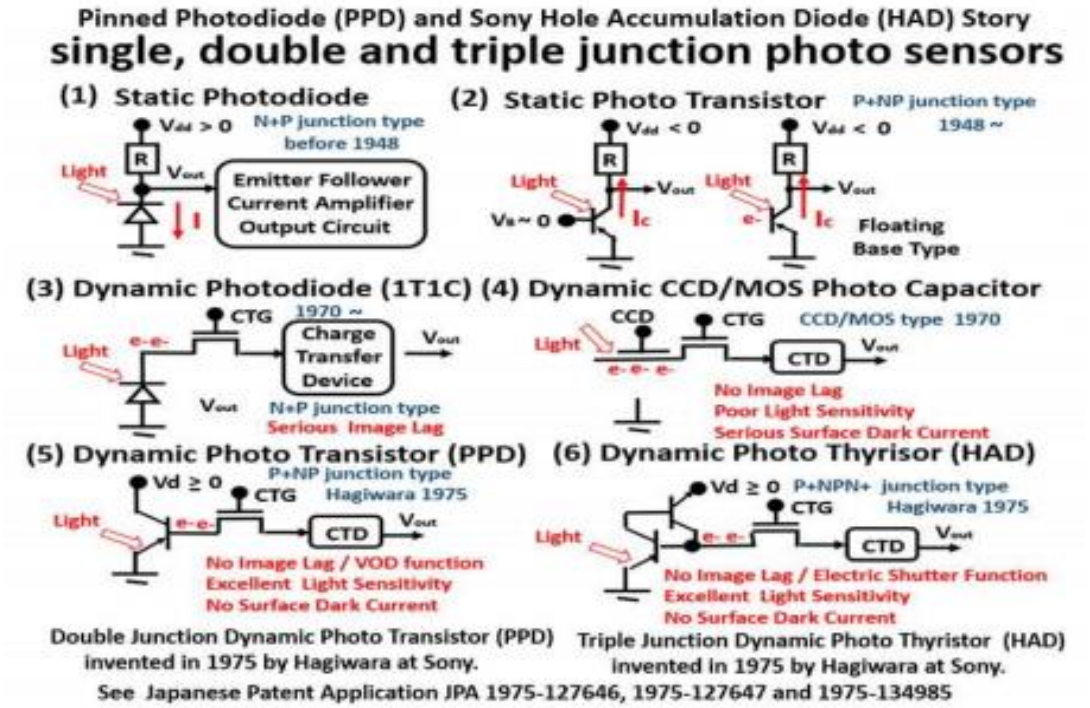
References:
[1] A. I. Krymski, N. E. Bock, N. Tu, D. Van Blerkom, E. R. Fossum, "A High Speed, 240frames/s, 4.1-Megapixel CMOS Sensor," *IEEE Trans. Electron Devices*, vol. 50, no. 1, pp. 130-135, Jan., 2003.
[2] K. Mabuchi, N. Nakamura, E. Funatsu, T. Abe, T. Umeda, T. Hoshino, R. Suzuki, H. Sumi, "CMOS Image Sensor Using a Floating Diffusion Driving Buried Photodiode," *ISSCC Dig. Tech. Papers*, pp. 102-103, Feb., 2004.
Hagiwara 1975 invention (JPA 1975-134985)
[3] W. Yang, O. Kwon, J. Lee, G. Hwang, S. Lee, "Integrated 800×600 CMOS Imaging System," *ISSCC Dig. Tech. Papers*, pp.304-305, Feb., 1999.

We all came to a long way since Peter Noble invented the Active Amp in 1968. Modern CMOS Image Sensors used the technology of CDS, Active Amp and PPD.

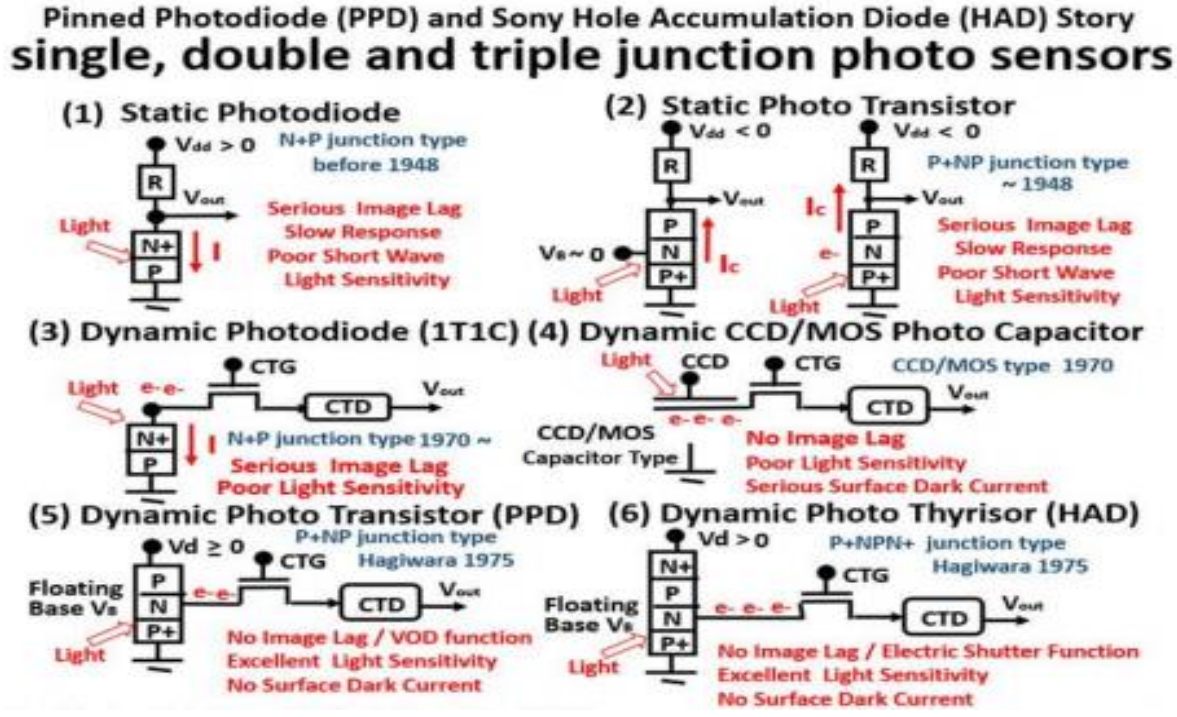


**CMOS Inverter and Source Follower circuits are basics for digital circuit design.
But we had to wait, till the advancement of CMOS process scaling rule,
in order to place the source follower active circuit in each small picture cell area.
Meanwhile CCD had a great role in the advancement of image sensors in 1980s.
For modern high definition TV image sensor applications, CCD has the power issue
and also the limit in charge transfer efficiency of 99.999%, which is not enough now.**

In classical image sensors, the single junction type N+P dynamic photodiode was used with the floating surface charge collecting storage N+ region, which suffered the incomplete charge transfer that created the serious image lag problem.



Hagiwara at Sony proposed in 1975 the double junction type P+NP dynamic photo transistor, Pinned Photodiode (PPD), with the pinned surface hole accumulation P+ layer with no image lag feature and the extremely low surface dark current feature. Hagiwara also proposed at the same time in 1975 the triple junction type P+NPNsub dynamic photo thyristor, Sony Hole Accumulation Diode (HAD), with the in-pixel Vertical Overflow Drain (VOD) function with no image lag feature which made possible to achieve the electrical shutter function.



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The_First_Pinned_Phtodiode_was_invented_in_1975_by_Yoshiaki_Hagiwara_at_Sony_028

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In Japanese Patent Application JPA 1975-124676, Yoshiaki Hagiwara at Sony in 1975 invented the First Pinned Phtodiode in the form of a triple junction N+NP+NP dynamic photo thyristor with the electron-accumulation pinned N+ surface layer and which has the surface N+N barrier electric field that can separate effectively the photo electron and hole pairs generated within the 0.2 μm in the vicinity of the pinned N+ Si surface.

Japanese Patent Application JPA 1975-127646 on the triple junction N+N-P+NP-P type Dynamic Photo Thyristor
< the first Pinned Photodiod >
with the in-pixel built-in vertical charge draining and overflow draining (VOD) capability and the MOS buffer memory for the Global Shutter function with the N+N Pinned Surface.

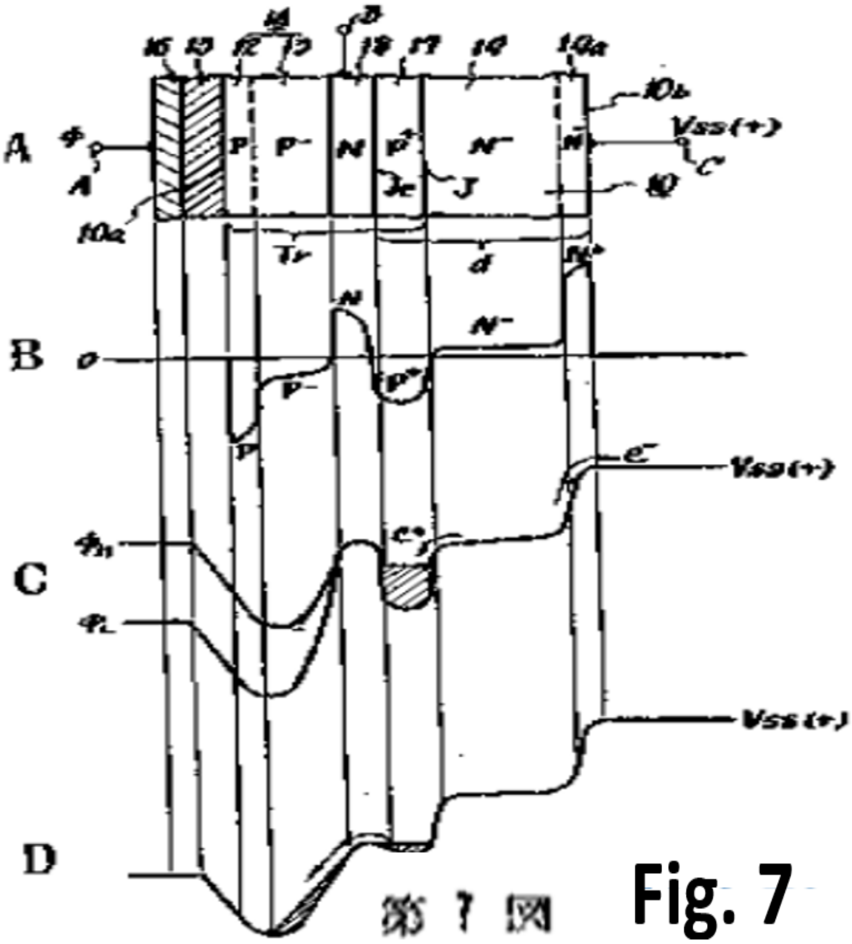

Fig. 7

It is well known that the short wave blue light cannot penetrate more than 0.2 μm in depth into the silicon crystal. However, the surface N+N barrier electric field can be created at the silicon surface within the 0.2 μm in depth and can be used effectively to separate photo electron and hole pairs generated in the vicinity of the Si surface.

On the other hand it is very difficult to create, within the silicon surface of the 0.2μm in depth, the N+P jucnion depletion region for the photo electron hole pair separation.

In conventional single junction type N+P photodiodes, the floating surface N+ region has a flat surface potential of no surface elecric field. The pairs cannot be separated effectively in the surface floating N+ region. Eventually, the pairs in the floating N+ surface will be recombined, not contributing the photo electron and hole generations.

This is why the classical single junction type N+P dynamic photodiode has the poor short wave blue light sensitivity. Conventional solar cells also use the classical N+P single junction type photodiode with the floating N+ surface of poor short wave blue light sensitivity. This is why the current solar cell has a poor efficiency of about 20%.

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The_First_Pinned_Phtodiode_was_invented_in_1975_by_Yoshiaki_Hagiwara_at_Sony_029

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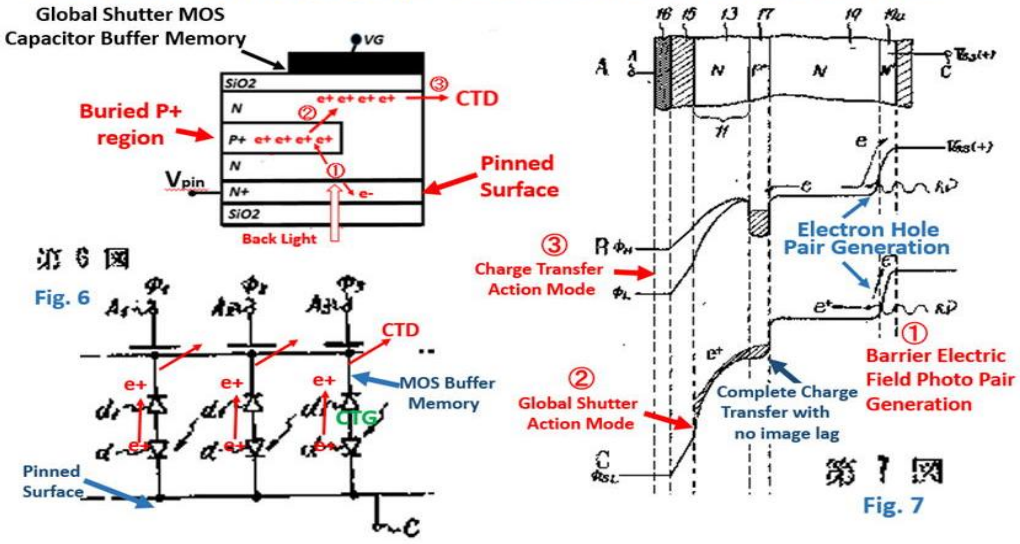
Hagiwara proposed the MOS capacior type buffer memory for the Global Shutter function function abosolutely needed for the modern CMOS image sensors. See JPA 1975-124647.

Hagiwara also proposed the double juncion type Dynamic Photo Transistor with the complete charge transfer operation capability of no image lag feature to achieve the electrical shutter function for digital cameras, completely free from mechanical parts.

Japanese Patent 1975-127647

N+NP+N junction type Buried Pinned Photodiode
with Built-in MOS Capacitor Buffer Memory Global Shutter Function
and the surface N+N doping slope Barrier Electric Filed Photo Pair Generation



Hagiwara also proposed in JPA 1975-134985, the double juncion P+NP type Dynamic Photo Transistor on the silicon substrate (Nsub), which was later called as Sony Hole Accumulation Diode (HAD) in 1987 with the vertical overflow drain (VOD) function. It has also the complete charge transfer operation capability of no image lag feature with the pinned P+ surface potential, which is needed absolutely in order to achieve the electrical shutter function for digital cameras, completely free from mechanical parts. Hagiwara also proposed in JPA 1977-126885 the basic clocking scheme of the electrical shutter operation using the punch thru operation mode of the in-pixel overflow drain voltage control scheme.

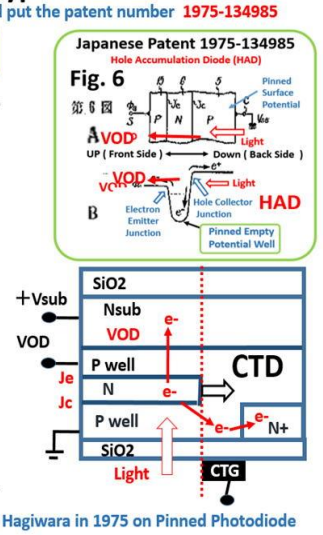
PNPN junction Transistor type Pinned Photodiode

Visit https://www.j-platpat.inpit.go.jp/ and put the patent number 1975-134985

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

Patent Claim in English Translation

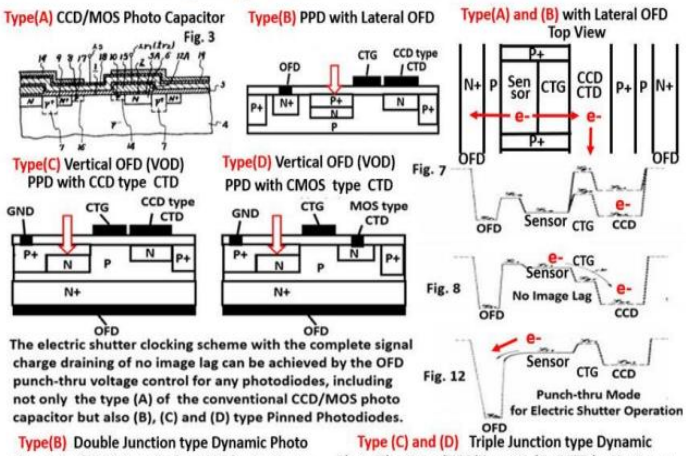
(1) In the semiconductor substrate (Nsub), the first region(P well) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N) is is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N) . And (6) Collector junction (Jc) is formed by the second region (N) and the first region (P well), forming a (PNP) transistor structure, (7) Photo charge is stored in the Base (N) according to illuminated light intensity and transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.



Japanese Patent Application 1975-134985 by Hagiwara in 1975 on Pinned Photodiode

Japanese Patent 1977-126885

Japanese Patent JPA 1977-126885 on Electrical Shutter Clocking Scheme
invented by Y. Hagiwara, S. Ochi and T. Hashimoto in 1977.



The electric shutter clocking scheme with the complete signal charge draining of no image lag can be achieved by the OFD punch-thru voltage control for any photodiodes, including not only the type (A) of the conventional CCD/MOS photo capacitor but also (B), (C) and (D) type Pinned Photodiodes.

Type(B) Double Junction type Dynamic Photo Transistor (PPD) invented in 1975 by Hagiwara.

Type (C) and (D) Triple Junction type Dynamic Photo Thyristor (HAD) invented in 1975 by Hagiwara