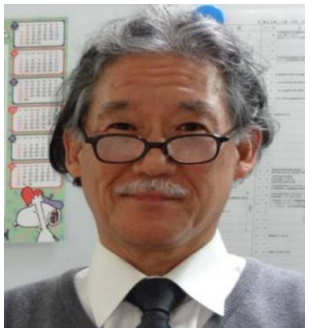
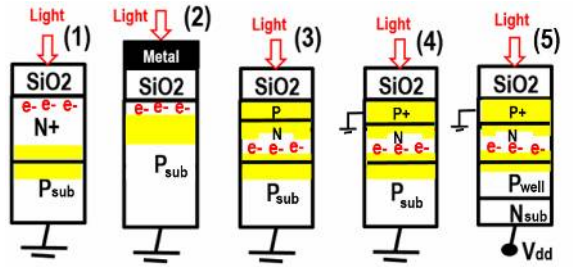
Image Sensor Story

Yoshiaki Hagiwara

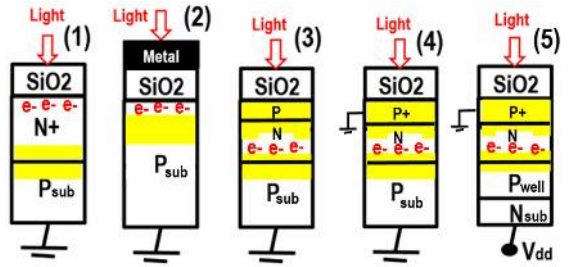
AIPS





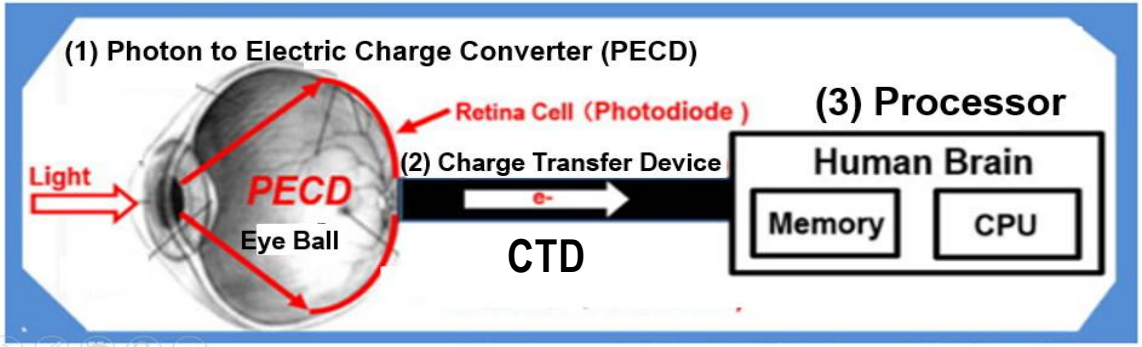
Front-illuminated CIS

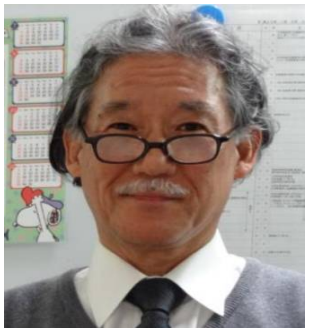
Back-illuminated CIS

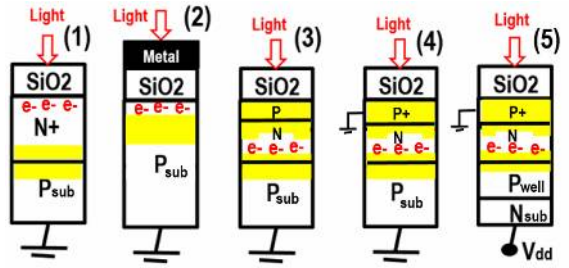


Front-illuminated CIS

Back-illuminated CIS

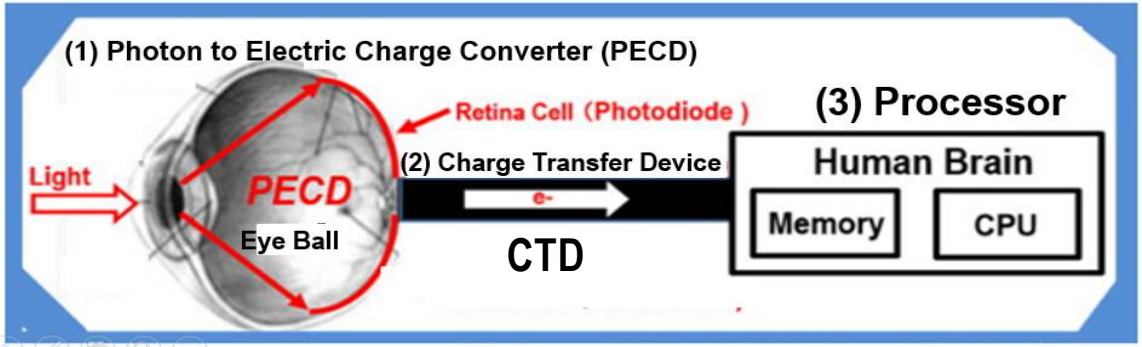


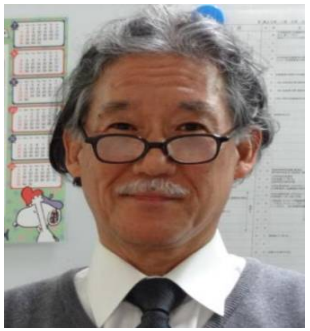




Front-illuminated CIS

Back-illuminated CIS



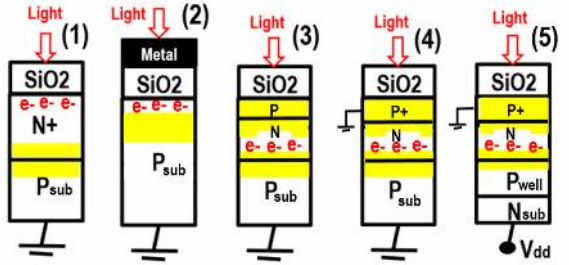


(1) Photon to Electric Charge Converter (PECD)

●N+P single junction ●P+NP double junction ●P+NPN triple junction

(2) Charge Transfer Device (CTD)

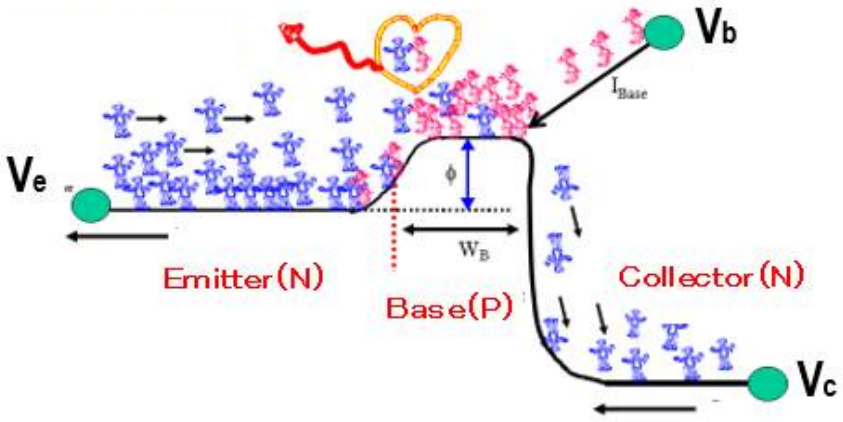
●MOS type ●CCD type ●Active Pixel (In Pixel Current Amp + CDS + ADC) CMOS



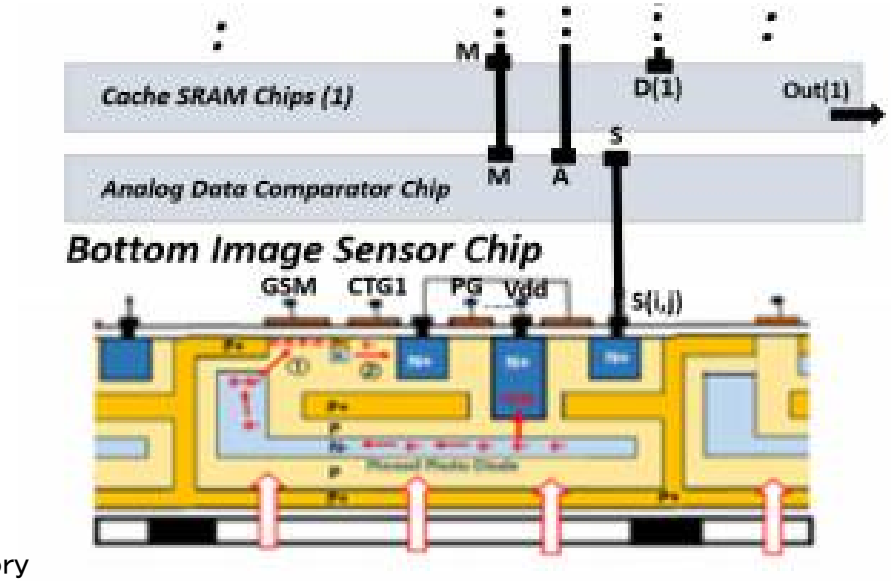
Front-illuminated CIS

Back-illuminated CIS

●NPN transistor Current Amplification

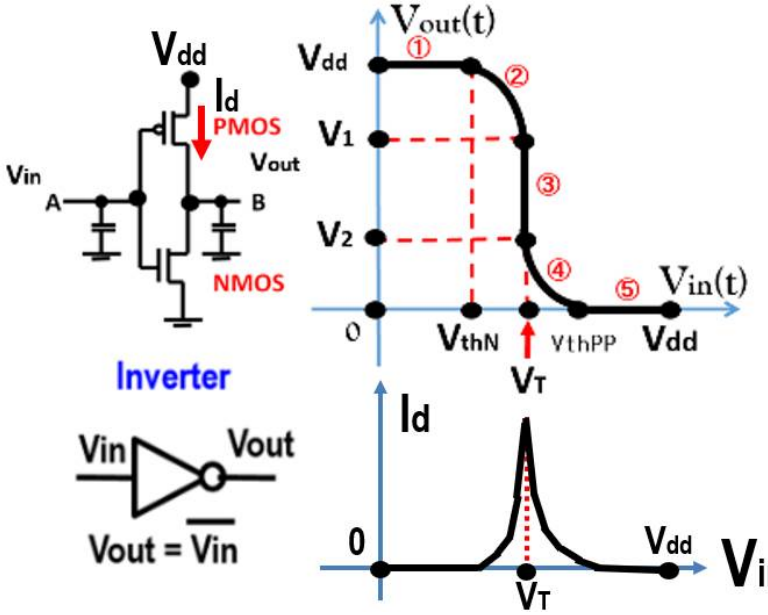


3-D Multi-chips Intelligent CMOS Image Sensor System

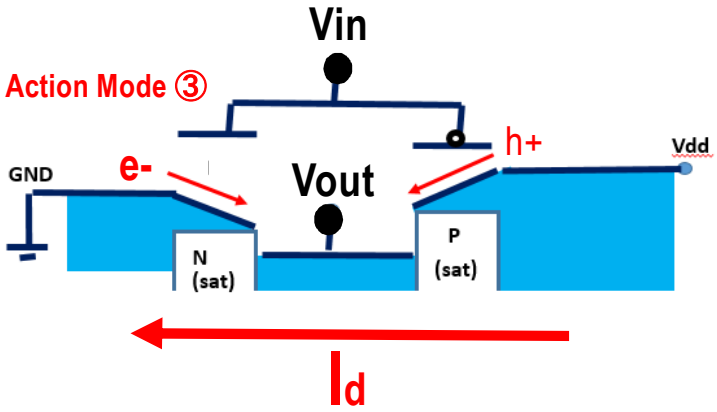


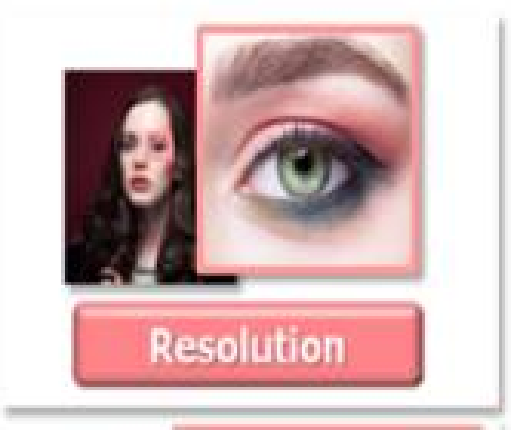
●Why CMOS is so strong ?

●Low Power CMOS inverter

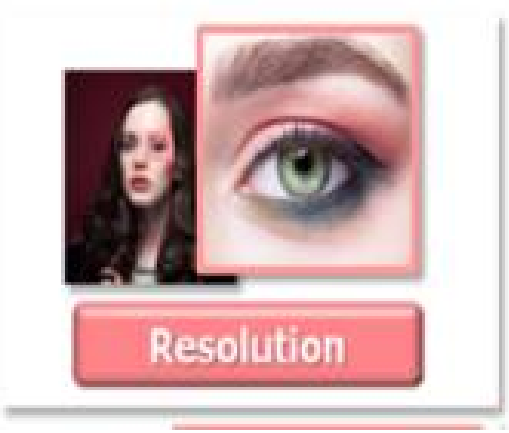


●Water Gate Model for CMOS Inverter





Resolution



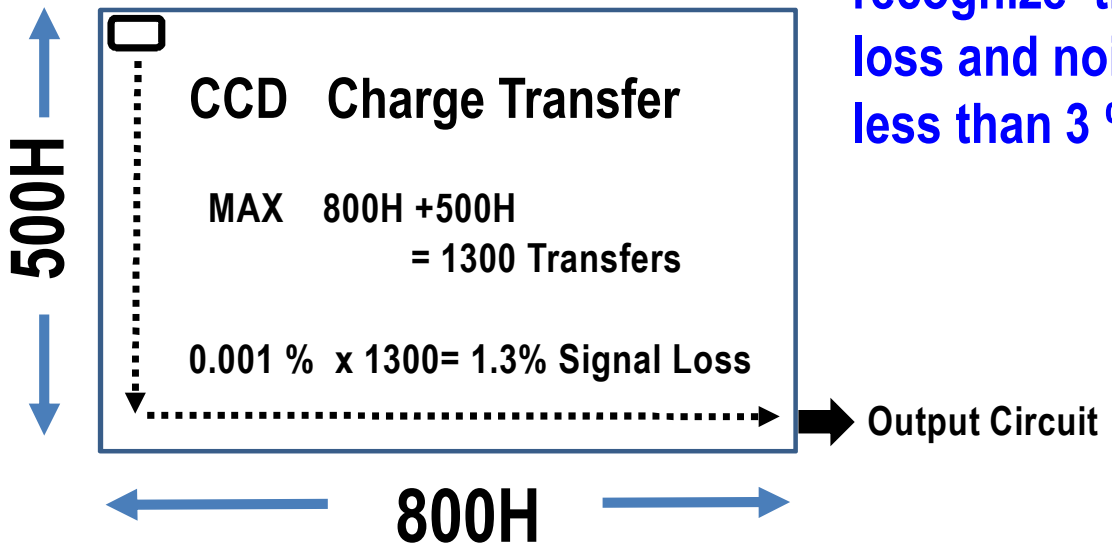
Resolution

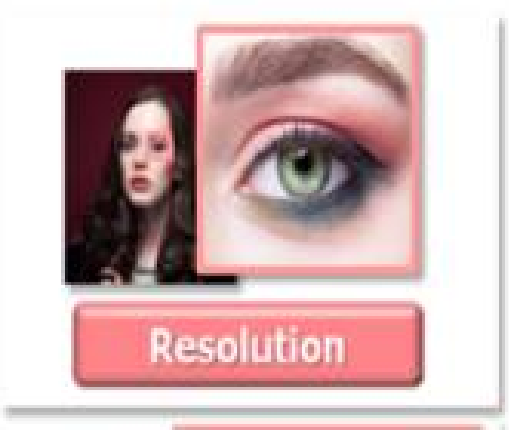
●Analog TV

800H x 500 V = 400,000 pixels

CCD Charge Transfer Efficiency < 99.999%

Human Eyes cannot recognize the signal loss and noise of less than 3 % .





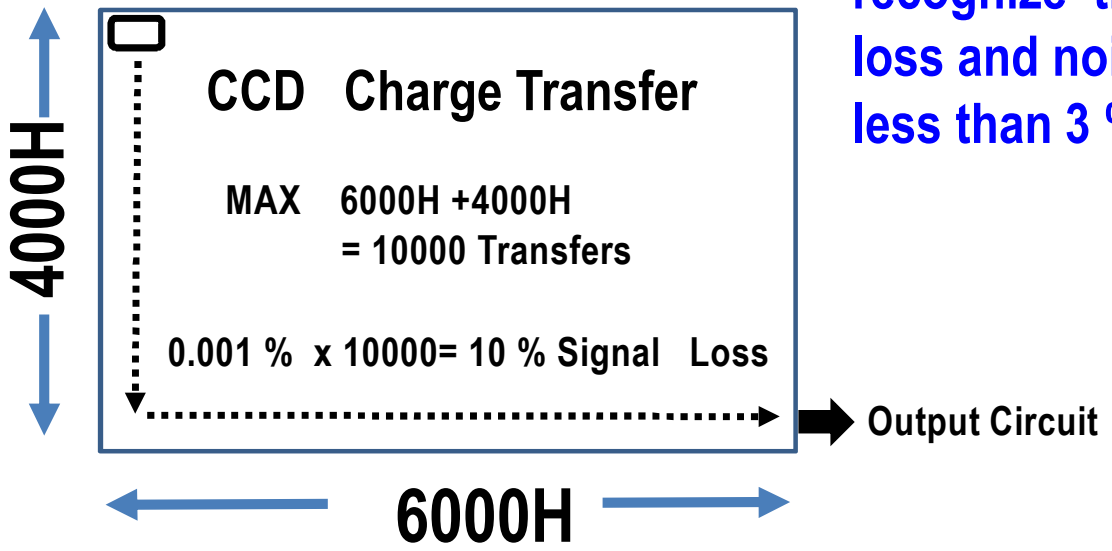
Resolution

●Digital TV

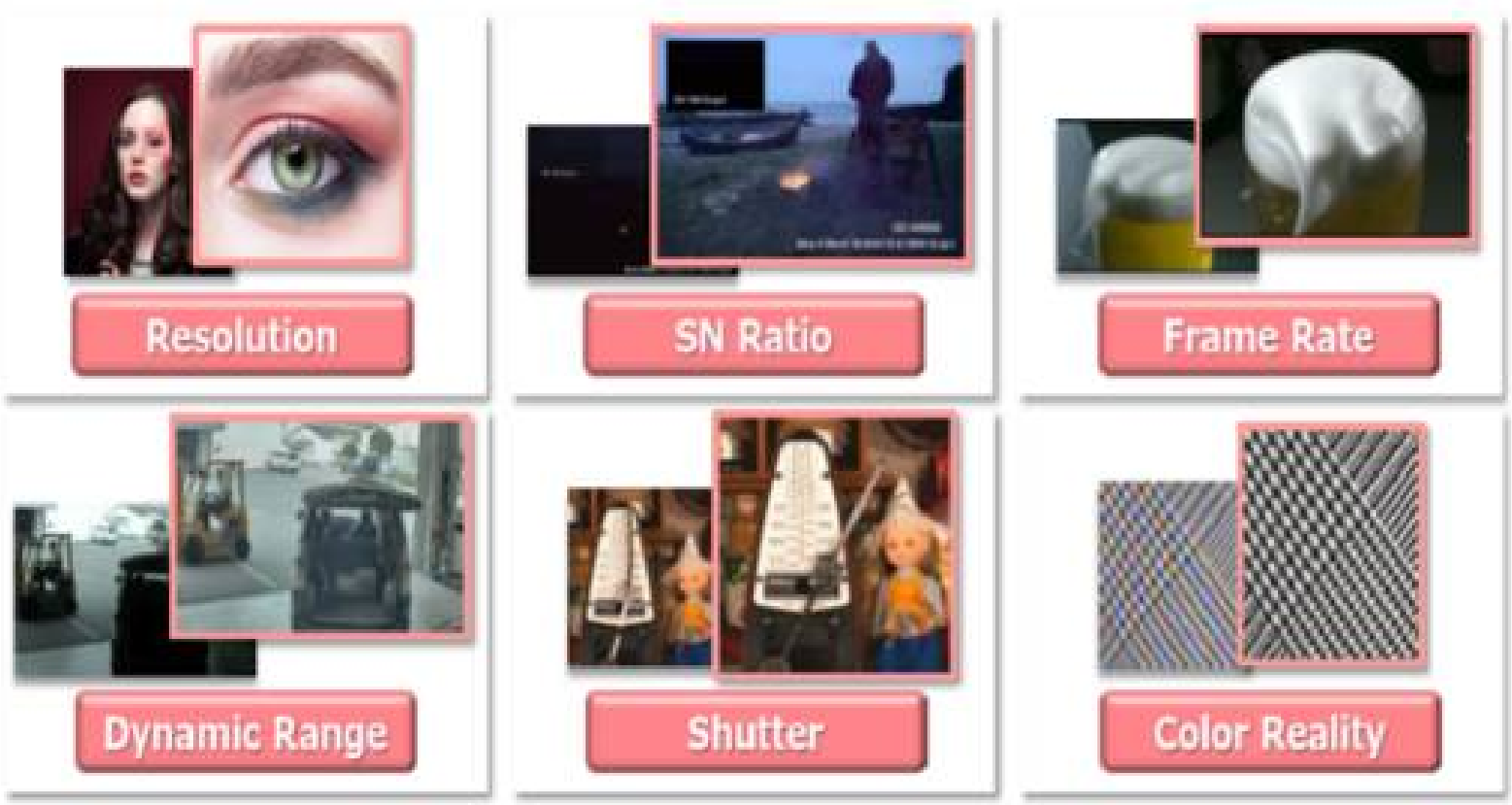
6000H x 4000 V = 24,000,000 pixels

CCD Charge Transfer Efficiency < 99.999%

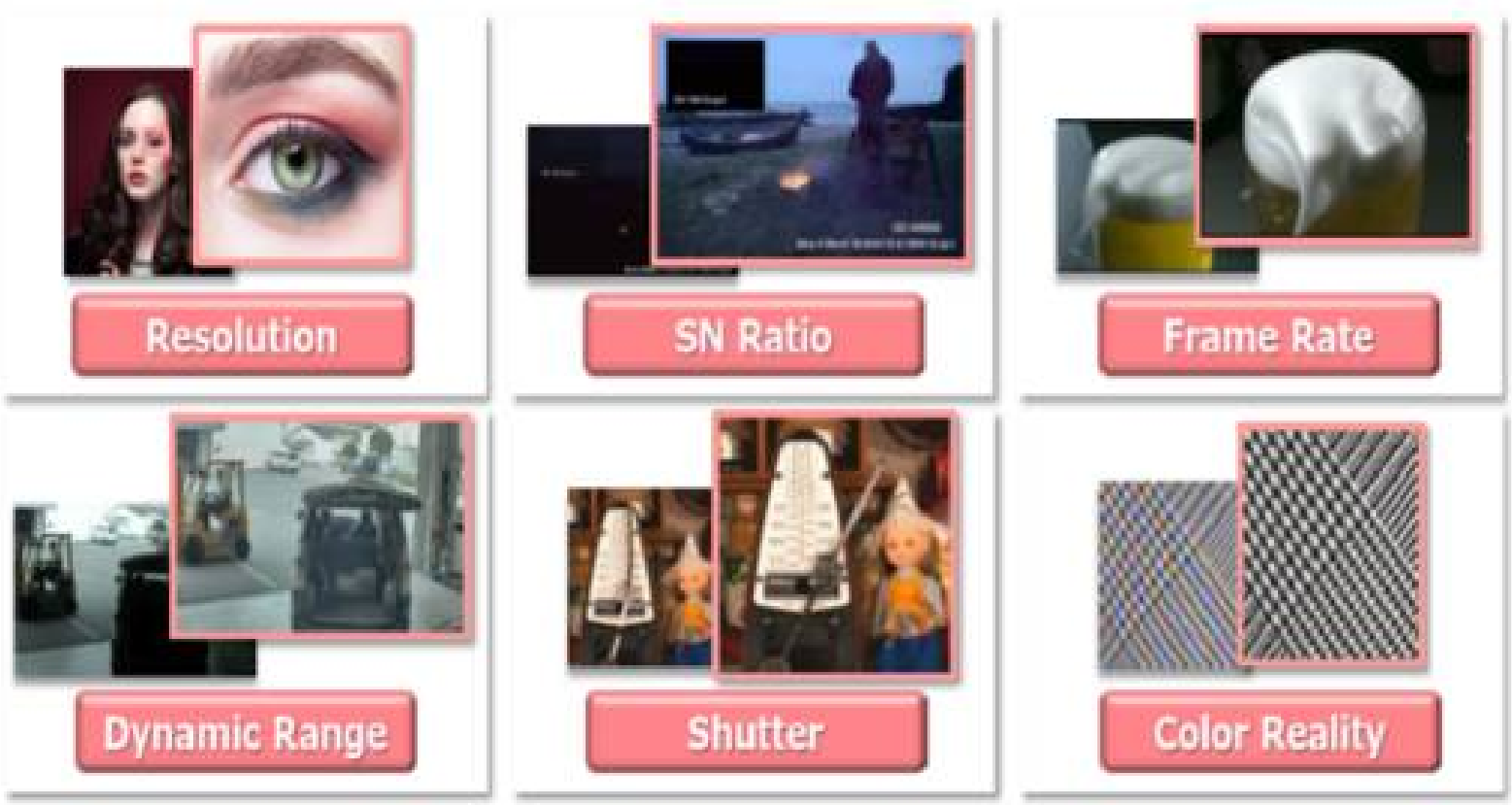
Human Eyes cannot recognize the signal loss and noise of less than 3 % .



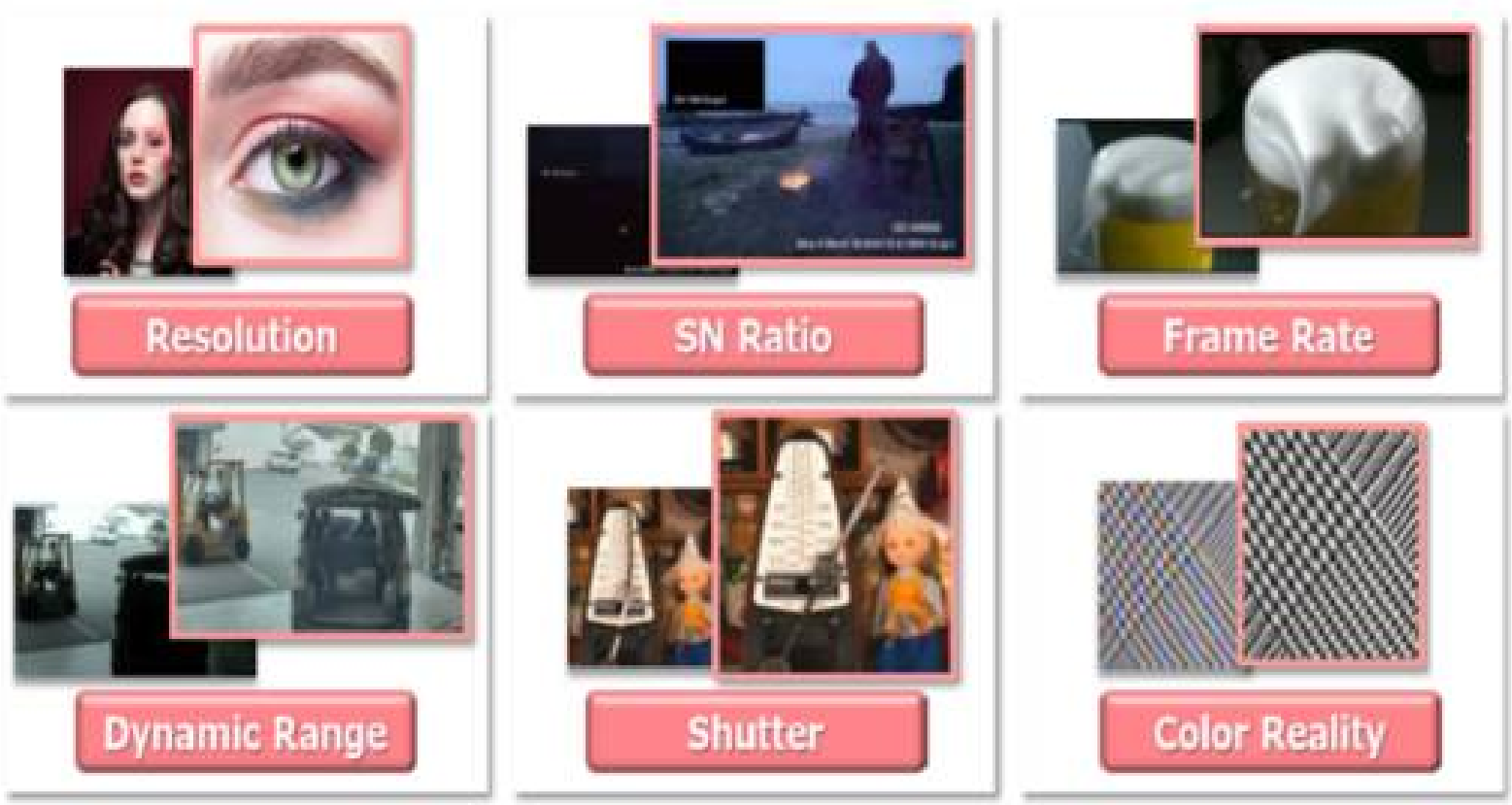
Resolution


Resolution
SN Ratio
Frame Rate
Dynamic Range
Shutter
Color Reality

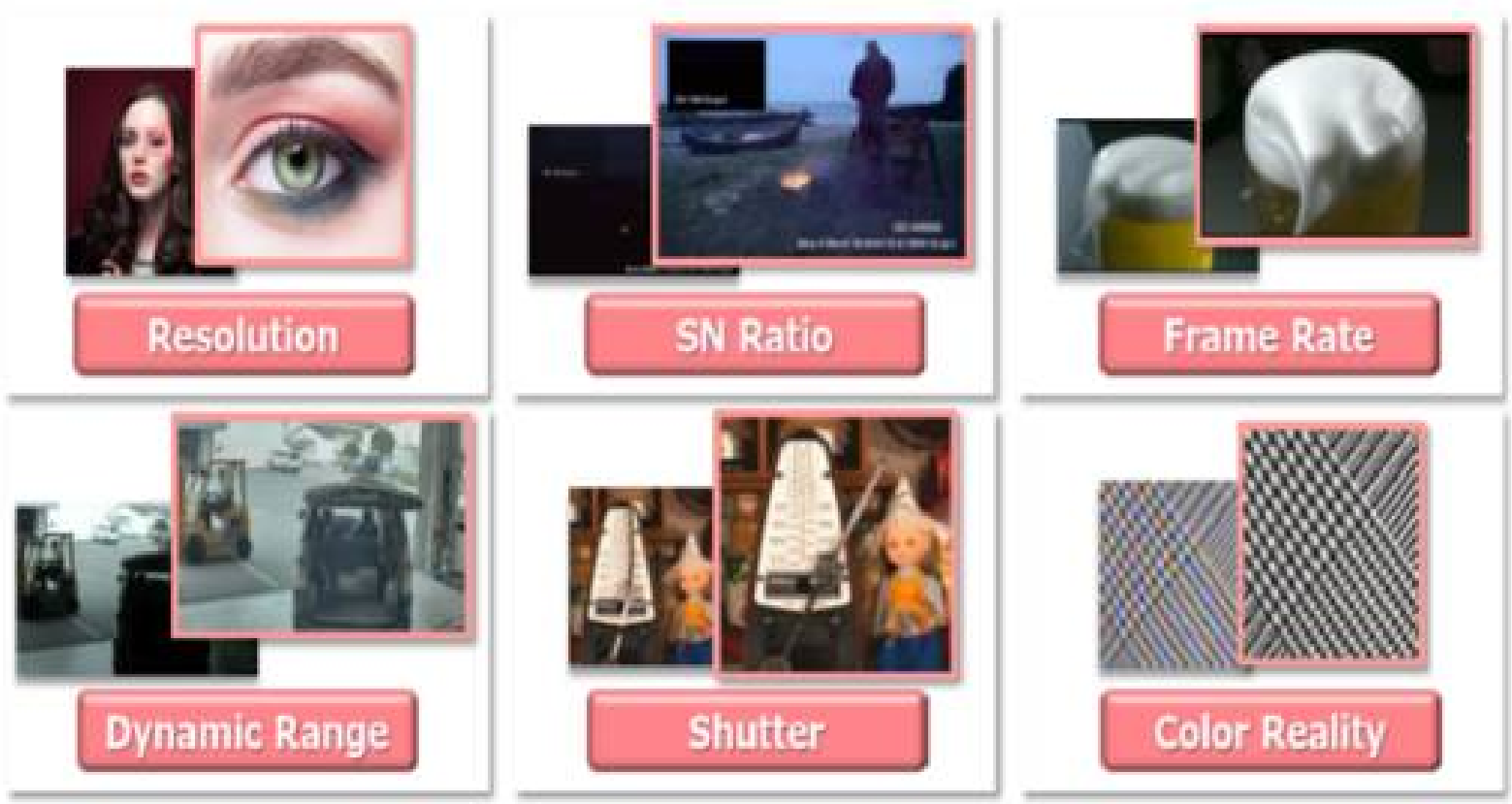
S/N Ratio


Resolution
SN Ratio
Frame Rate
Dynamic Range
Shutter
Color Reality

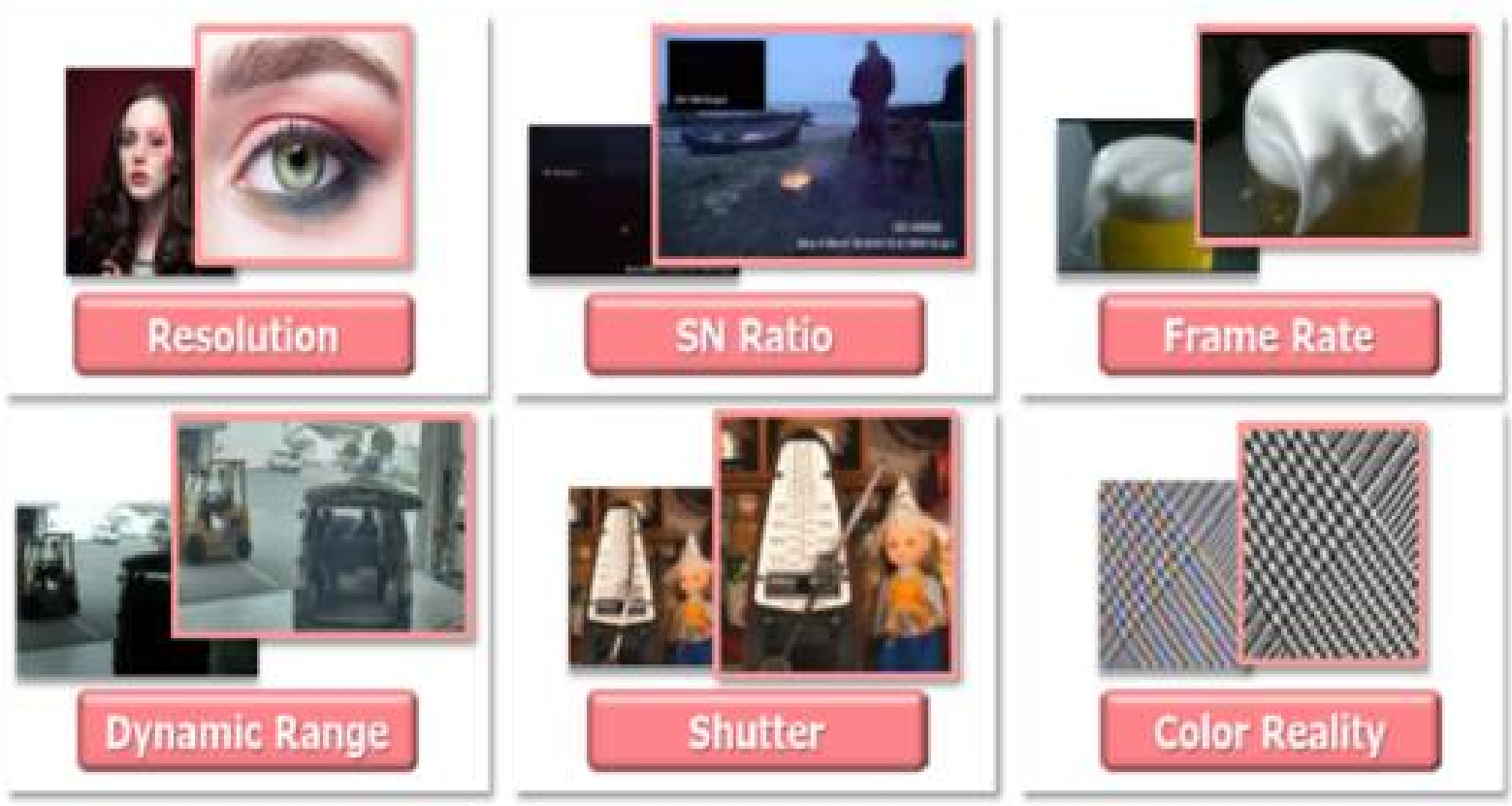
Frame Rate


Resolution
SN Ratio
Frame Rate
Dynamic Range
Shutter
Color Reality

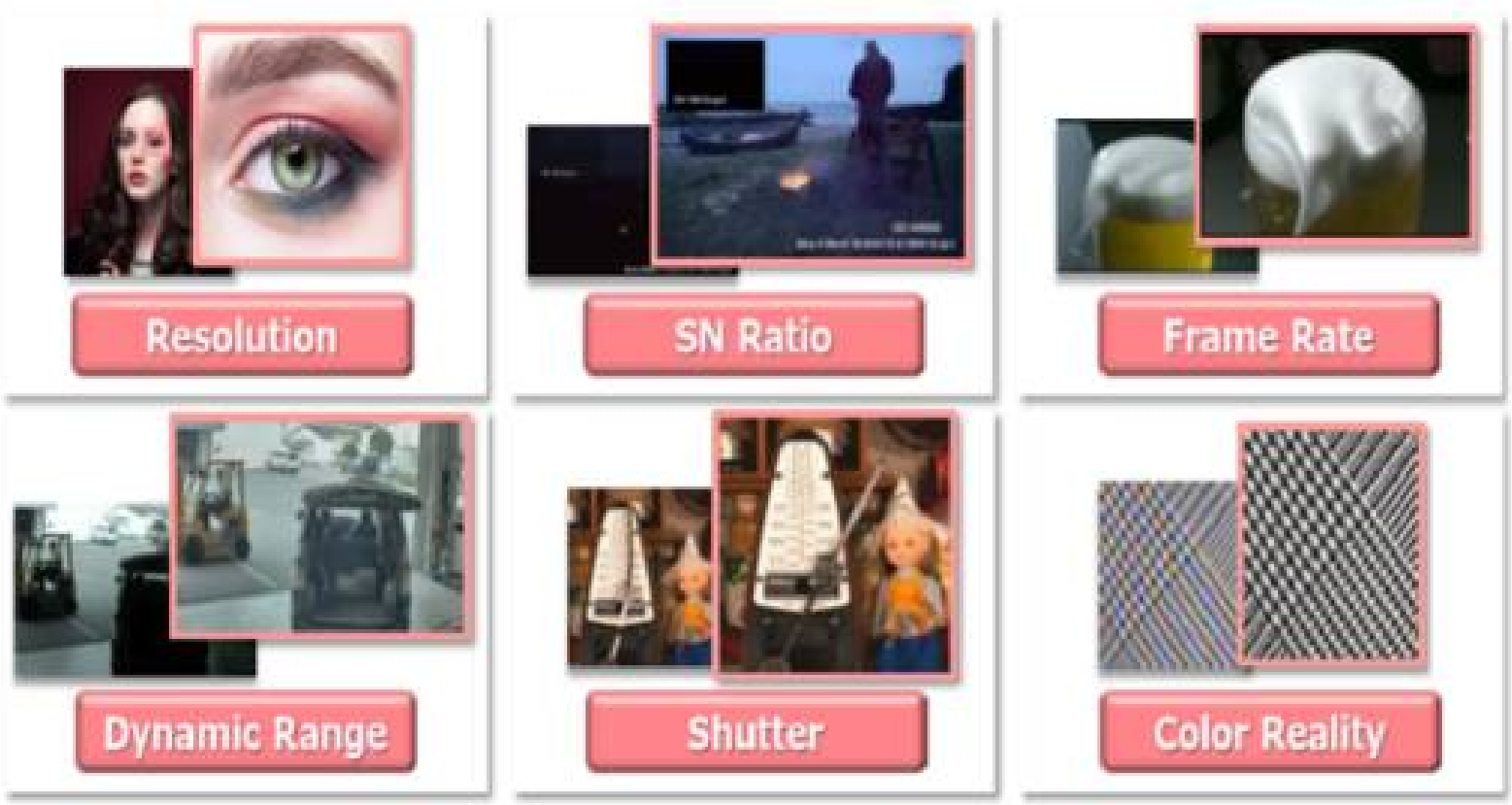
Dynamic Range



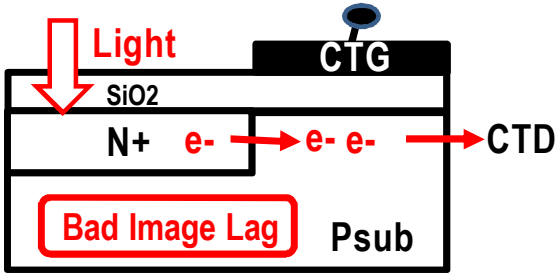
Shutter


Resolution
SN Ratio
Frame Rate
Dynamic Range
Shutter
Color Reality

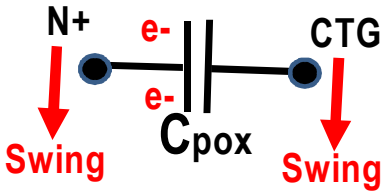
Color Reality



(1) N+P junction Photodiode in 1960s



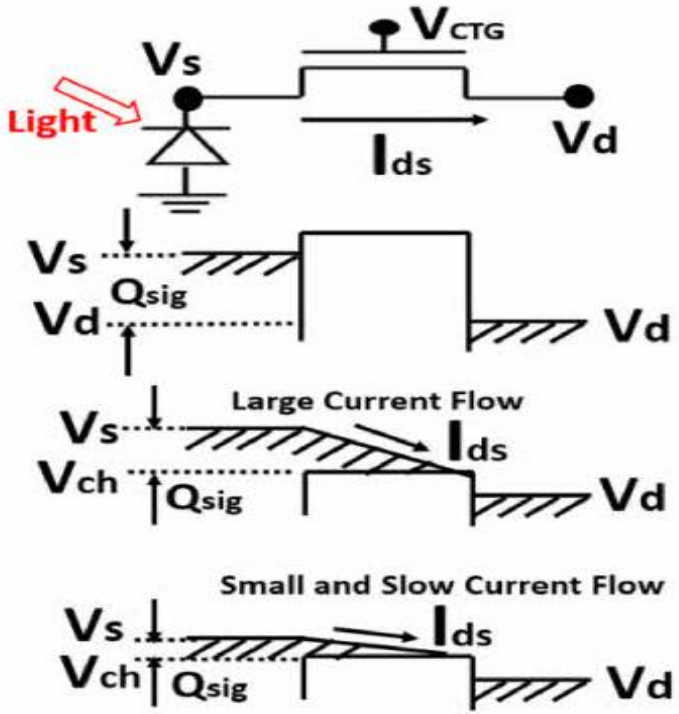
Parasitic Oxide Capacitor C_{pox}

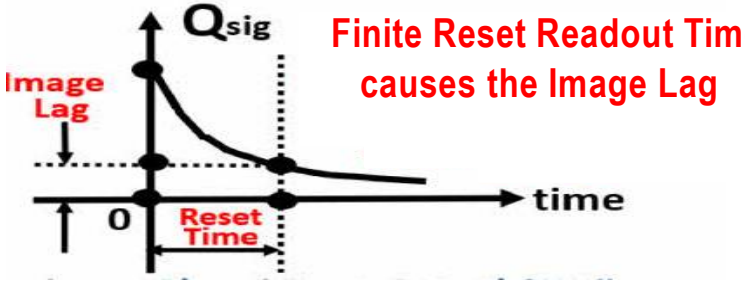


$$I_{ds} = K\,(V_s - V_{ch})^2$$

As $(V_s - V_{ch}) \rightarrow 0$

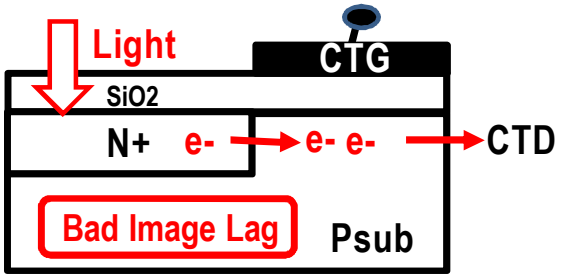
$I_{ds} \rightarrow 0$





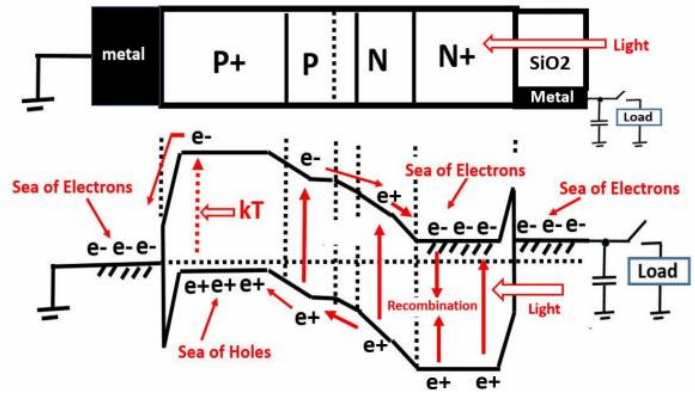
Finite Reset Readout Time causes the Image Lag

(1) N+P junction Photodiode in 1960s

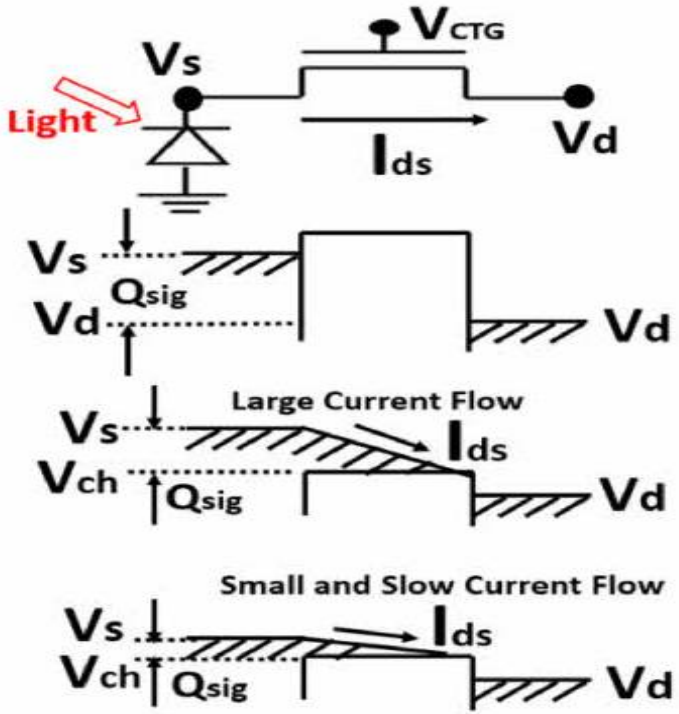


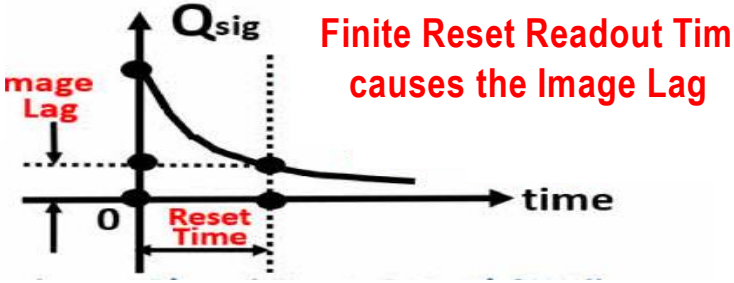
More Problem

Poor Blue Light Sensitivity Problem



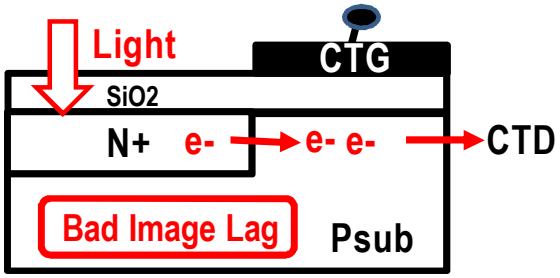
Single Junction N+P type Solar Cell also has a very poor short wave blue light sensitivity.



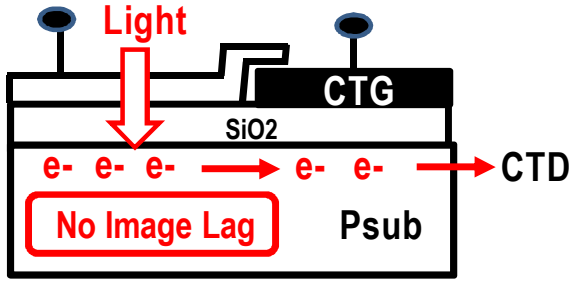


Finite Reset Readout Time causes the Image Lag

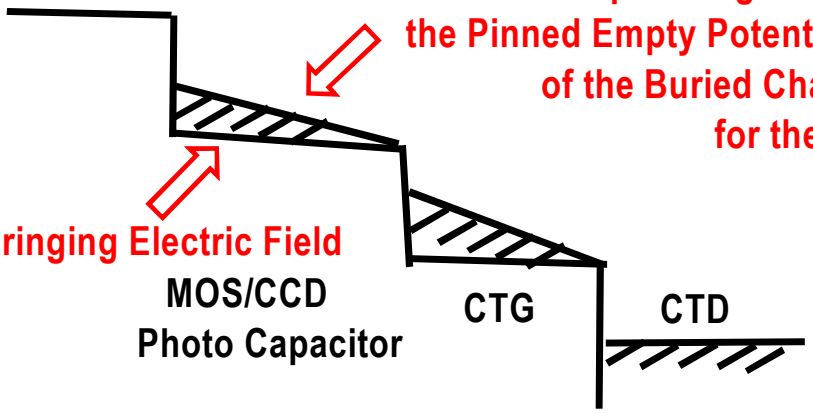
(1) N+P junction Photodiode
in 1960s



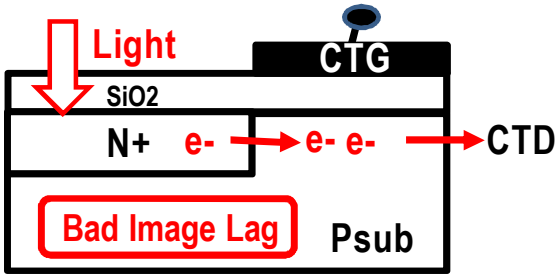
(2) Transparent Electrode CCD/MOS Photo Capacitor (1980)



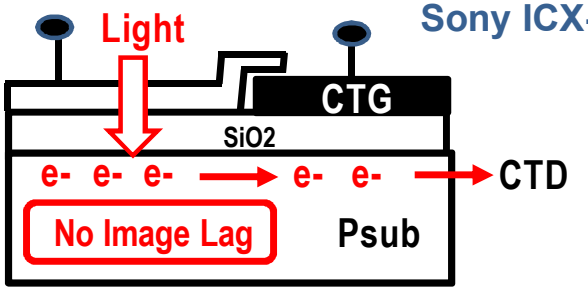
The CCD/MOS capacitor gives
the Pinned Empty Potential Well
of the Buried Channel Region
for the (2) case.



(1) N+P junction Photodiode in 1960s



(2) Transparent Electrode CCD/MOS Photo Capacitor (1980)



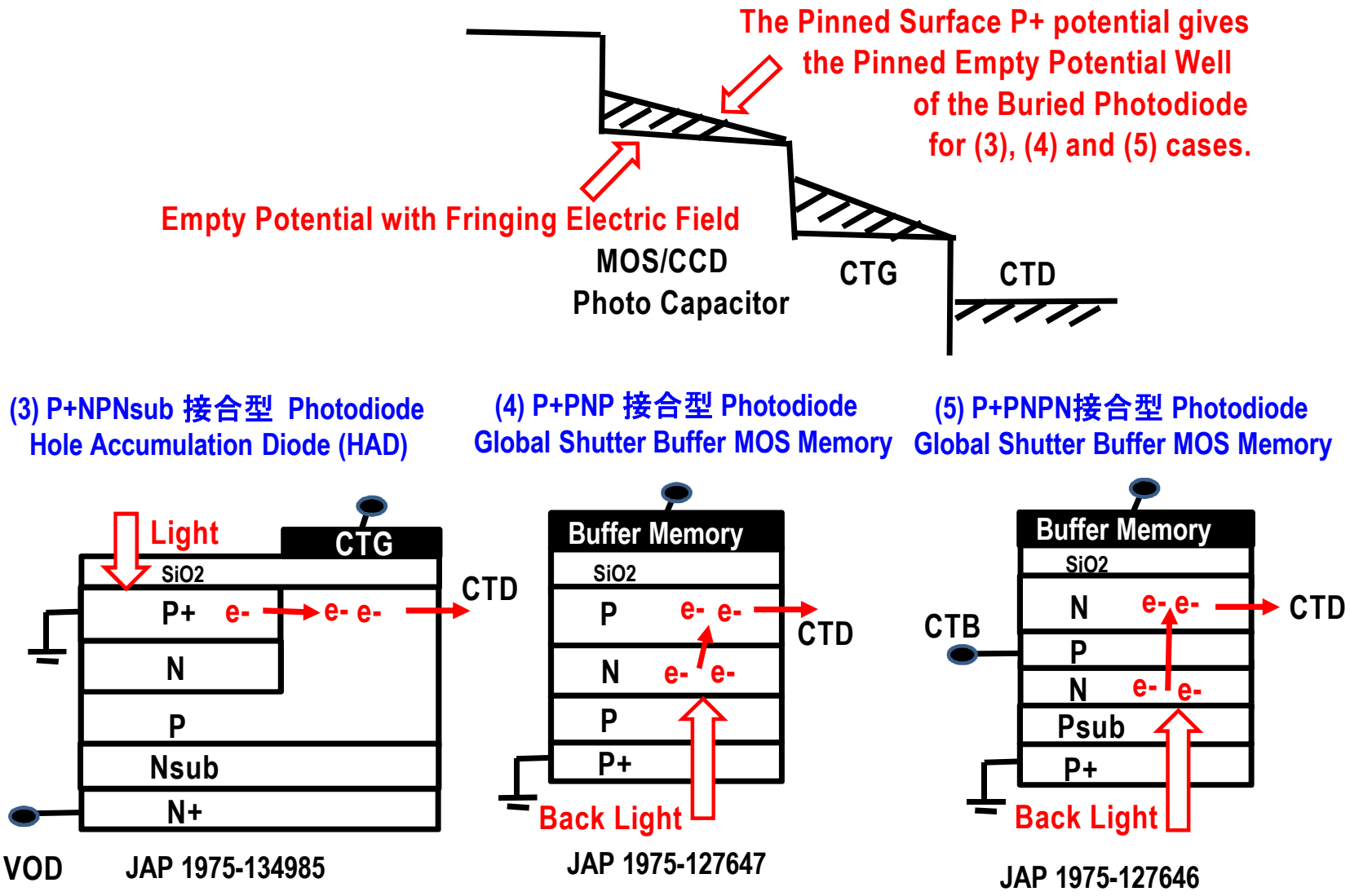
Sony ICX-008 CCD chips (1980)

<ICX008>

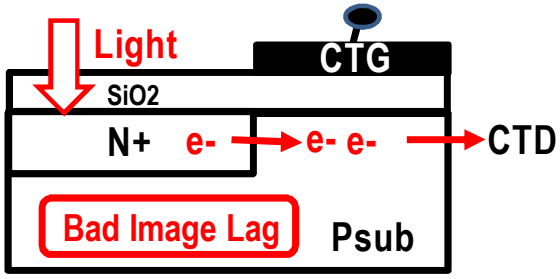
XC-1 1980
Two-Chip Color Video Camera
on ANA 747 Jumbo Jet

all solid state = robustness

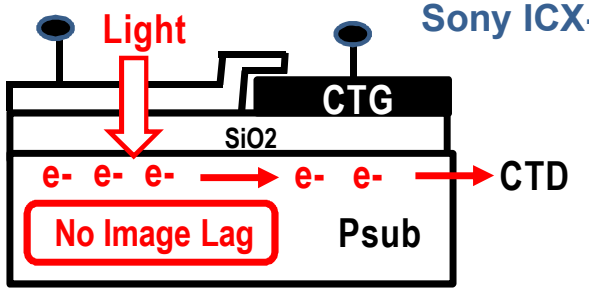
- CCD/MOS Dynamic Photo Capacitor with no image lag for action pictures with Electric Shutter Function


The Pinned Surface P+ potential gives
the Pinned Empty Potential Well
of the Buried Photodiode
for (3), (4) and (5) cases.
Empty Potential with Fringing Electric Field
MOS/CCD
Photo Capacitor
CTG
CTD
(3) P+NPNsub 接合型 Photodiode
Hole Accumulation Diode (HAD)
Light
CTG
SiO2
P+
e-
e- e-
CTD
N
P
Nsub
N+
VOD
JAP 1975-134985
(4) P+PNP 接合型 Photodiode
Global Shutter Buffer MOS Memory
Buffer Memory
SiO2
P
e- e-
CTD
N
e- e-
P
P+
Back Light
JAP 1975-127647
(5) P+PNPN接合型 Photodiode
Global Shutter Buffer MOS Memory
Buffer Memory
SiO2
N
e- e-
CTD
CTB
P
N
e- e-
Psub
P+
Back Light
JAP 1975-127646

(1) N+P junction Photodiode
in 1960s



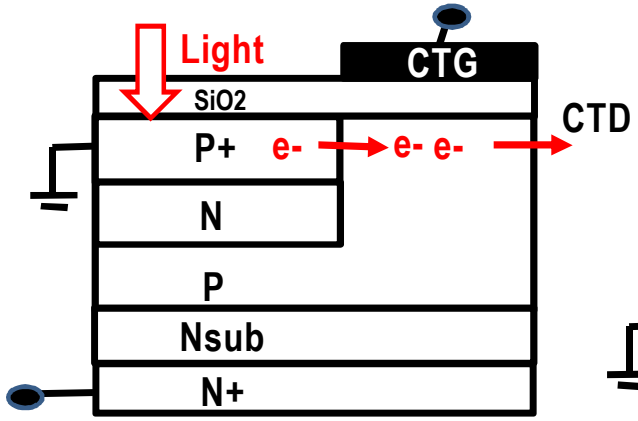
(2) Transparent Electrode CCD/MOS Photo Capacitor (1980)



Sony ICX-008 CCD chips (1980)

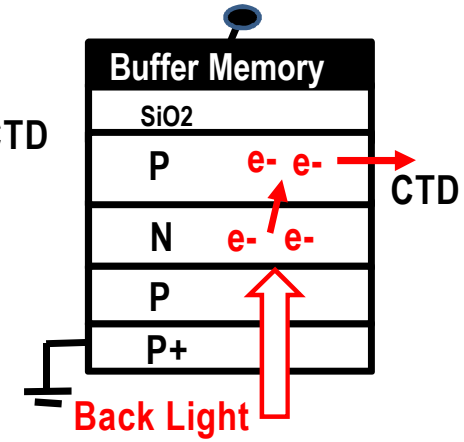
<ICX008>

(3) P+NPNsub 接合型 Photodiode
Hole Accumulation Diode (HAD)



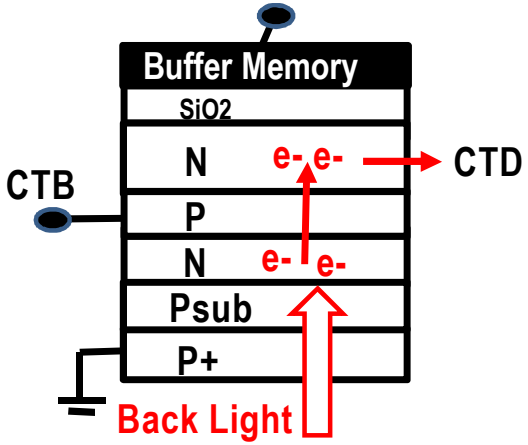
JAP 1975-134985

(4) P+PNP 接合型 Photodiode
Global Shutter Buffer MOS Memory



JAP 1975-127647

(5) P+PNPN接合型 Photodiode
Global Shutter Buffer MOS Memory



JAP 1975-127646

●P+NPNsub Pinned Photodiode (JAP 1975-134985)

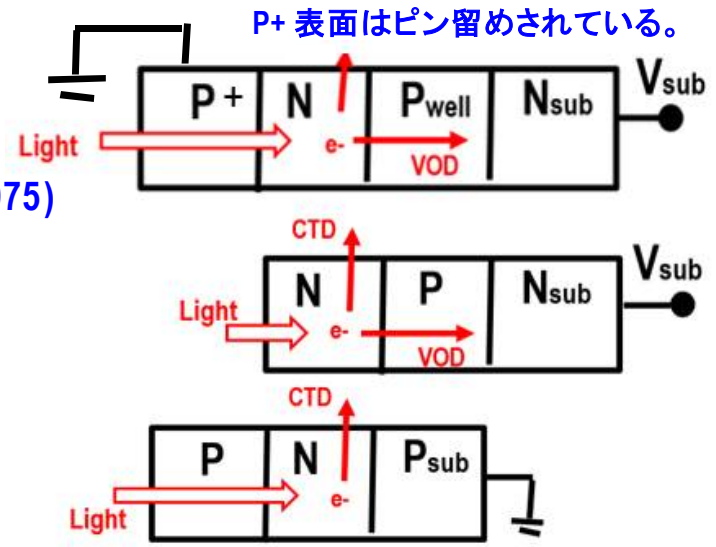
with VOD function and No Image Lag by Hagiwara (1975)

●NPNsub with VOD function (JAP 1978-1971)

by Yamada at Toshiba (1978)

●PNPsub Buried Photodiode (JAP 1980-138026)

by Teranish at Toshiba (1978)



Comparison of Various Light Detecting Photo Sensor Structures

feature \ type	Classical N+Psub Photodiode	Surface Channel CCD	Buried Channel CCD	Yamada 1978 NPNsub	Teranishi 1980 PNPsub	Hagiwara 1975 PNPNsub
Blue Light Sensitivity	△	X	X	○	○	○
Low Image Lag	X	○	○	X	○	○
Surface Dark Current	○	X	X	X	○	○
Surface Trap Noise	○	X	○	X	○	○
Vertical OFD (VOD)	X	X	X	○	X	○
Electrical Shutter	X	X	X	X	X	○

The actual 1978 Sony HAD sensor has the P+PN+Psub Junction type Pinned Photodiode (PPD) sensor structure for the excellent short wave blue light sensitivity.

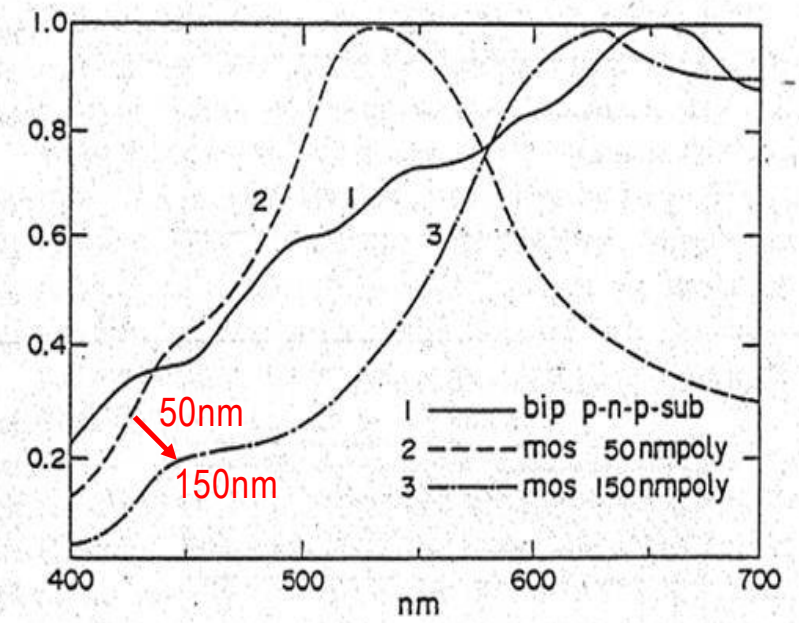
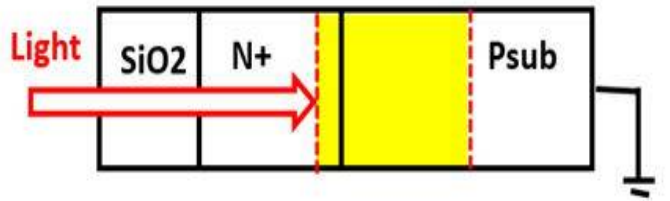
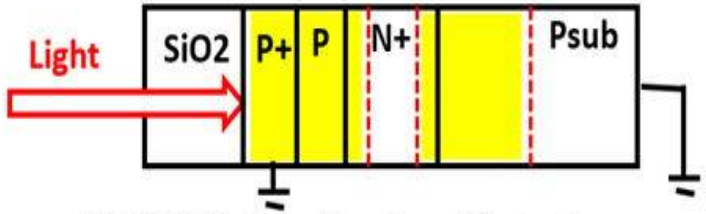


Fig. 7. Relative spectrum response. The relative response of the bipolar-type SiO_2–P2–N1–P1–SUB structure is compared with poly–SiO_2–N2–P(SUB) structures of the polysilicon thickness of 50 and 150 nm.

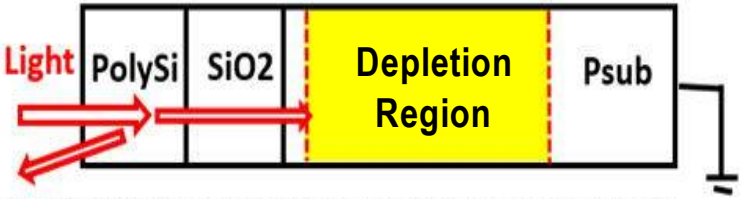
(0) Original N+P junction type Photo Sensor with very poor short wave blue light sensitivity



(1) Bip PNPsub junction type Photo Sensor with excellent short wave blue light sensitivity

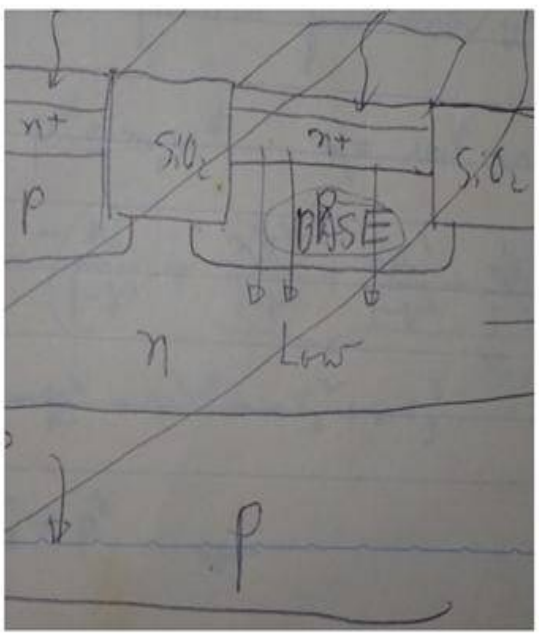


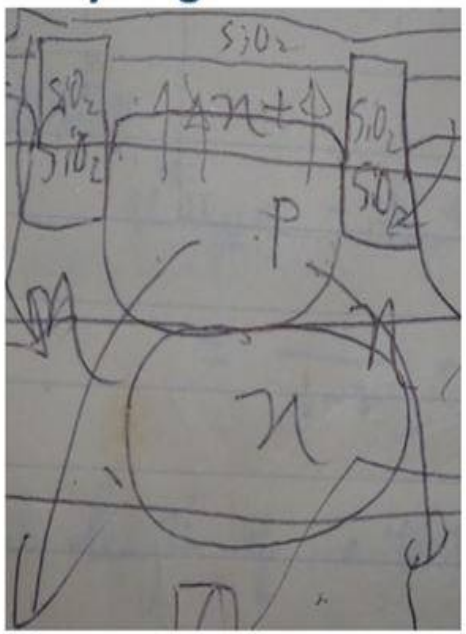
(2,3) MOS Capacitor type Photo Sensor with fairly good short wave blue light sensitivity

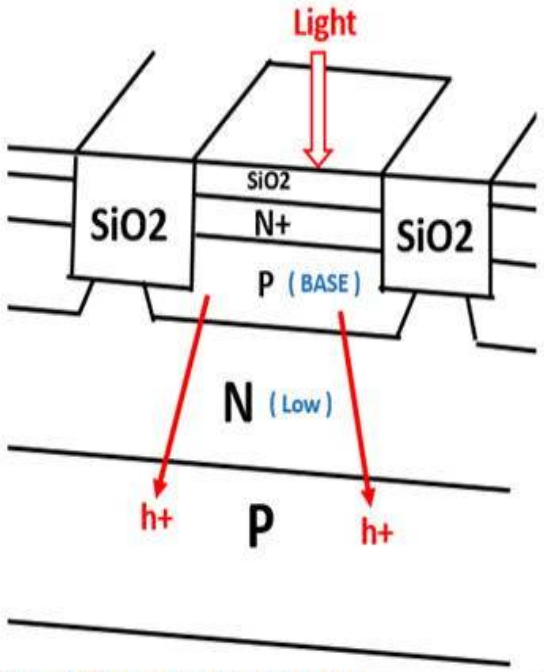


Yoshiaki Hagiwara,"High Density and High Quality Frame Transfer CCD Imager with Very Low Smear, Low Dark Current and Very High Blue Sensitivity", IEEE Transaction on Electron Devices, Vol 43, no. 12, December 1996
http://www.aiplab.com/P1996_Pinned_Photodidoe_used_in_Sony_1980_FT_CCD_Image_Sensor.pdf

The N+PNP junction type Dynamic Photo Transistor Structure Pinned Photodiode and Sony Hole Accumulation Diode (HAD) with the vertical overflow drain (VOD) function invented by Hagiwara at Sony in 1975



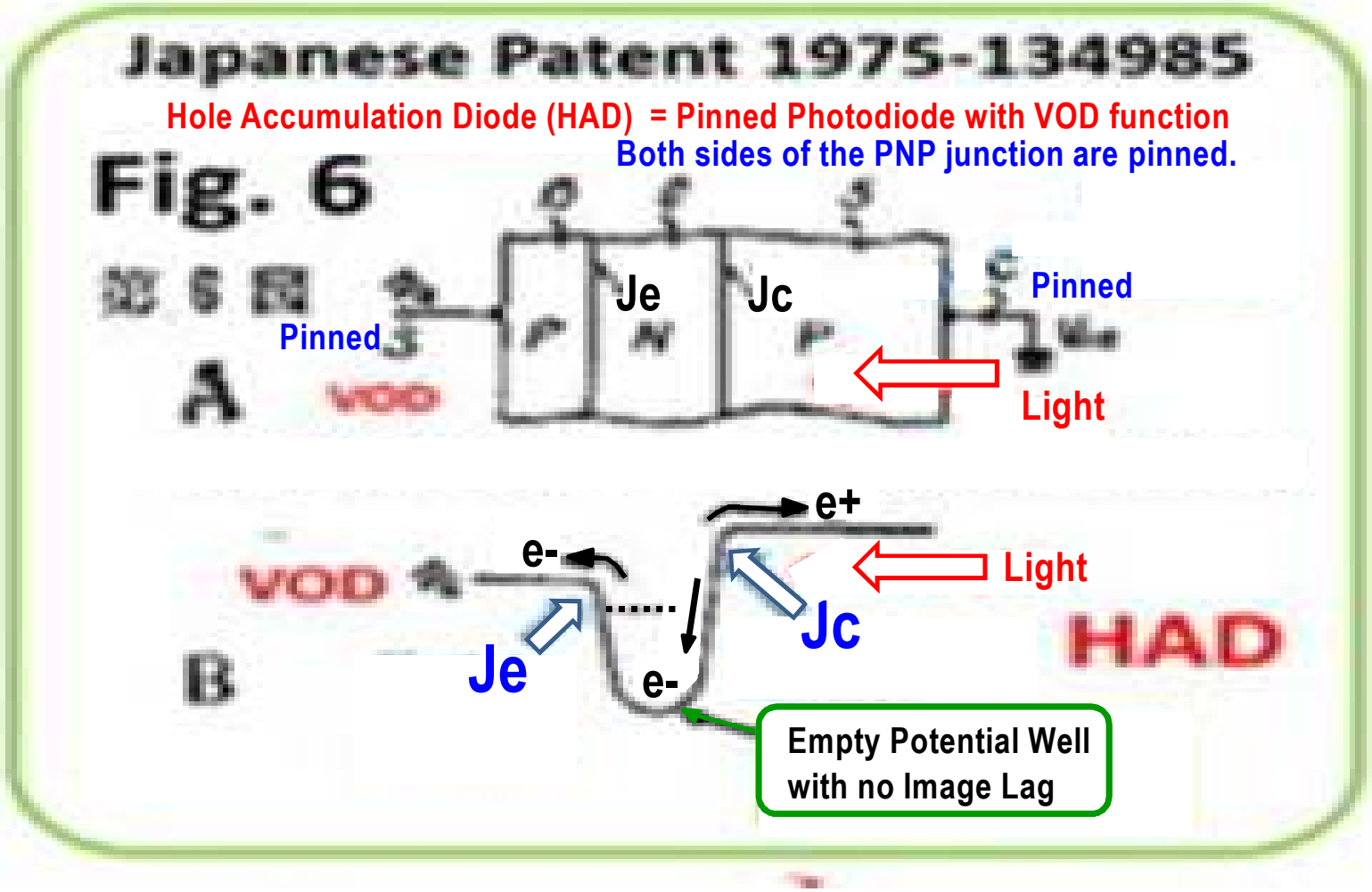




Hagiwara's Lab Note at Sony in February 1975

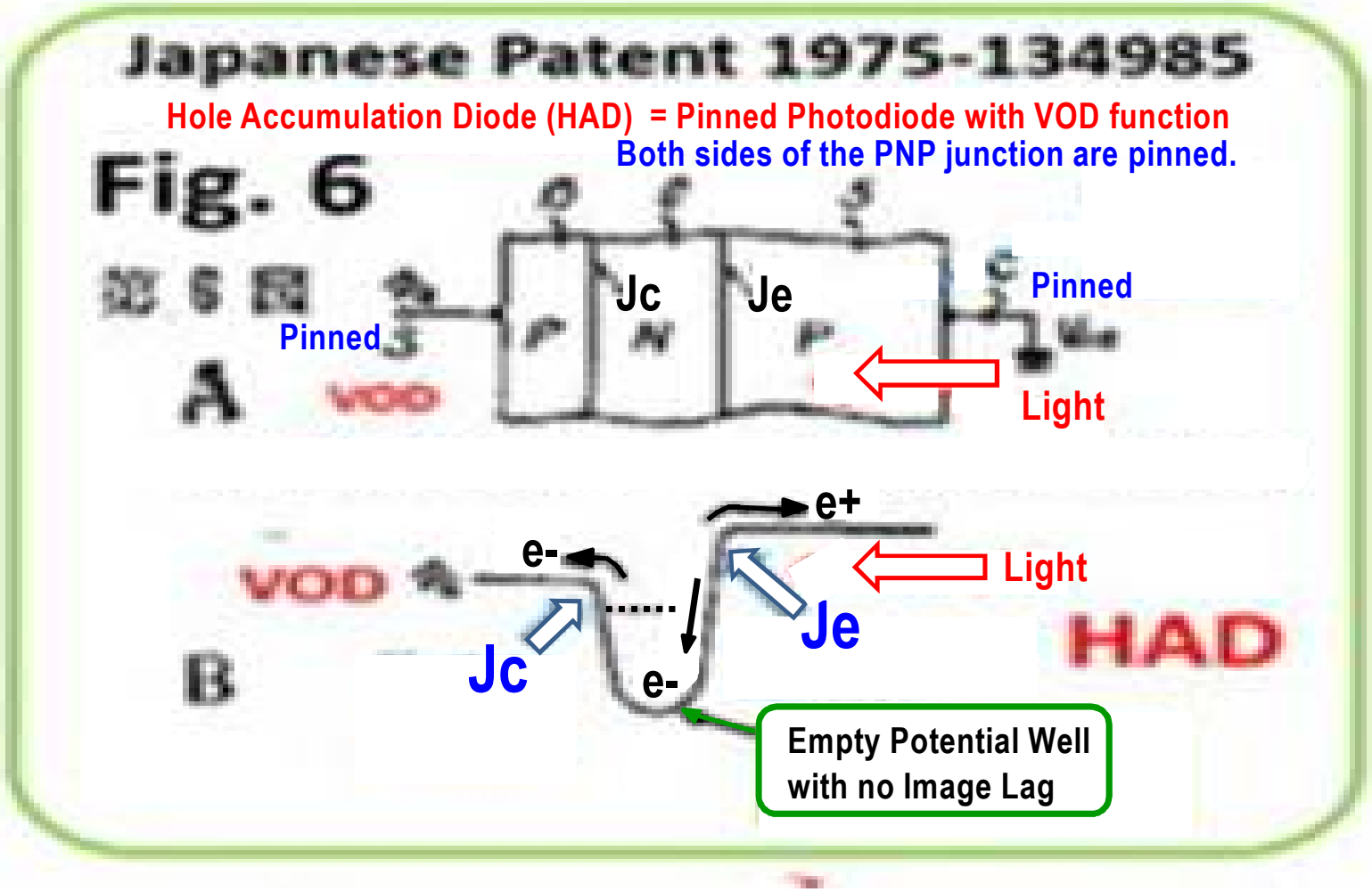
In 1975 at Sony, Yoshiaki Hagiwara filed three Japanese patents JPA1975-127646, JPA1975-127647 and JPA1975-134985 on the Pinned Surface Photodiode with the VOD function which is later called as Sony Hole Accumulation Diode (HAD). Hagiwara did not file a patent on the SiO2 device isolation but this lab note shows that Hagiwara had an idea of forming the Shallow Trench Isolation by the Local Oxidation Method, which was hinted by the LOCOS isolation in 1970s.

(1) Light (Jc) VOD (Je) type Pinned Photodiode



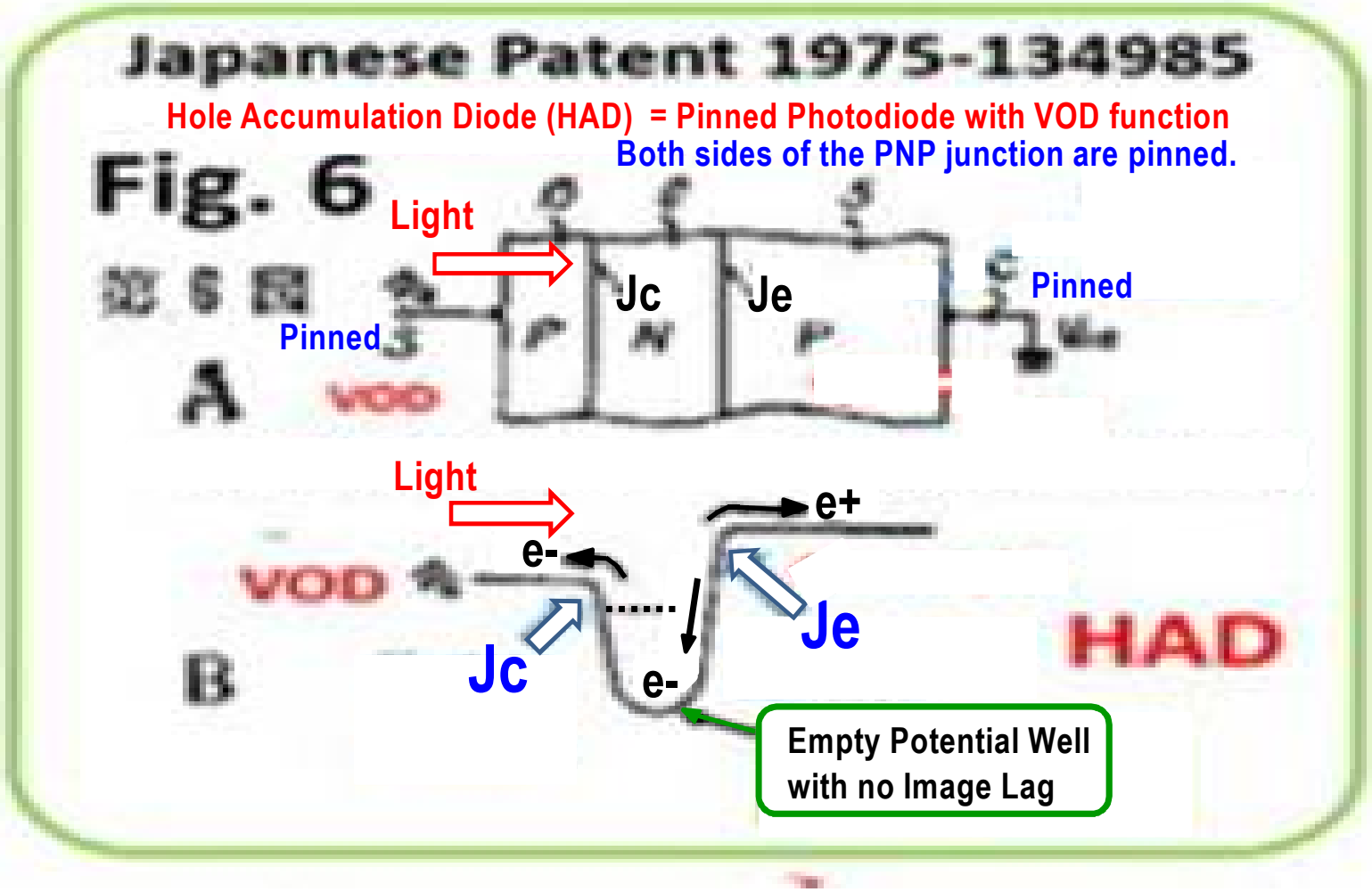
Hagiwara invented in 1975 the in-pixel vertical overflow drain (VOD) in PNP Pinned Photodiode.

(2) Light (Je) VOD (Jc) type Pinned Photodiode



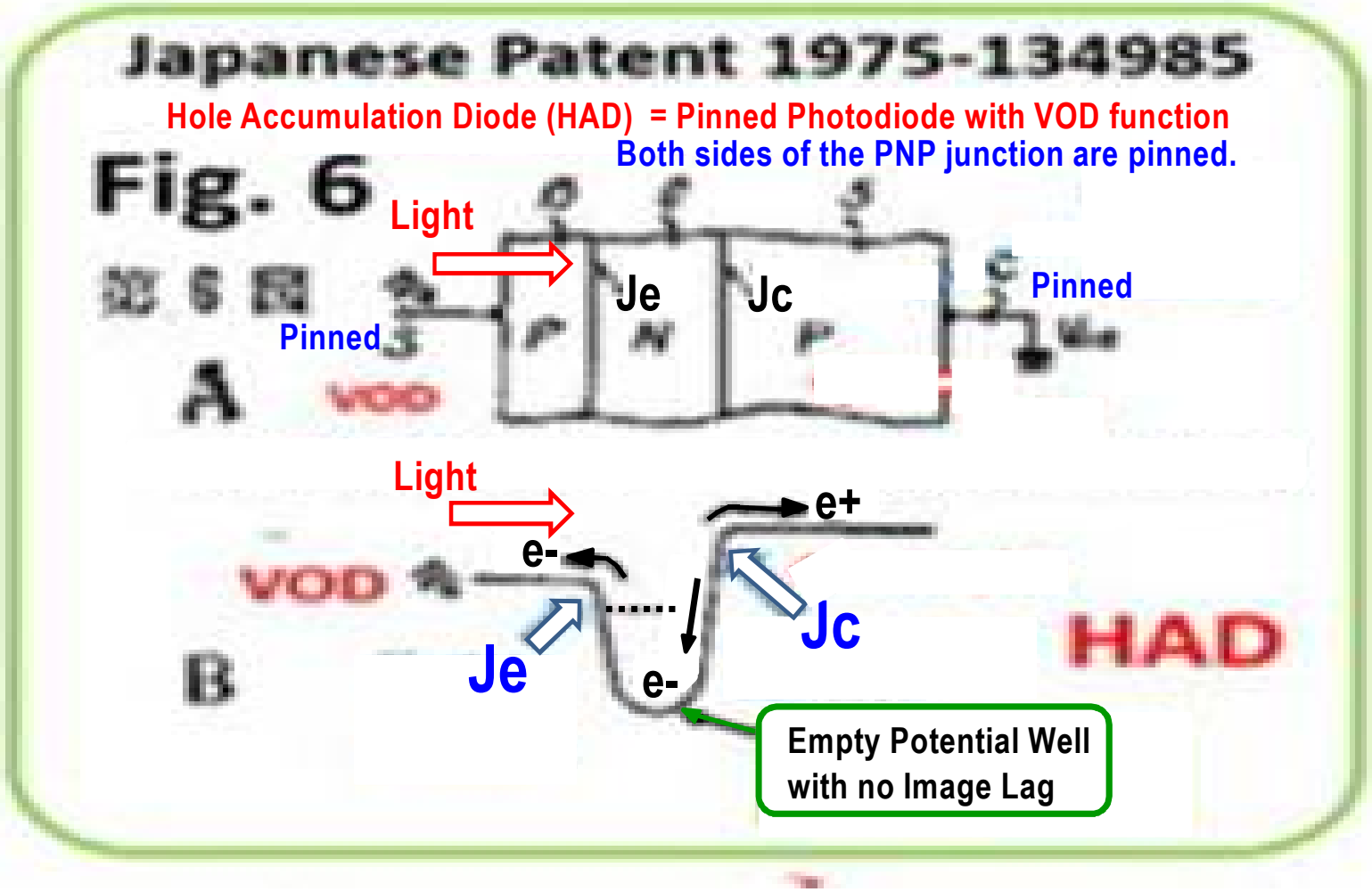
Hagiwara invented in 1975 the in-pixel vertical overflow drain (VOD) in PNP Pinned Photodiode.

(3) Light (Jc) VOD (Jc) type Pinned Photodiode



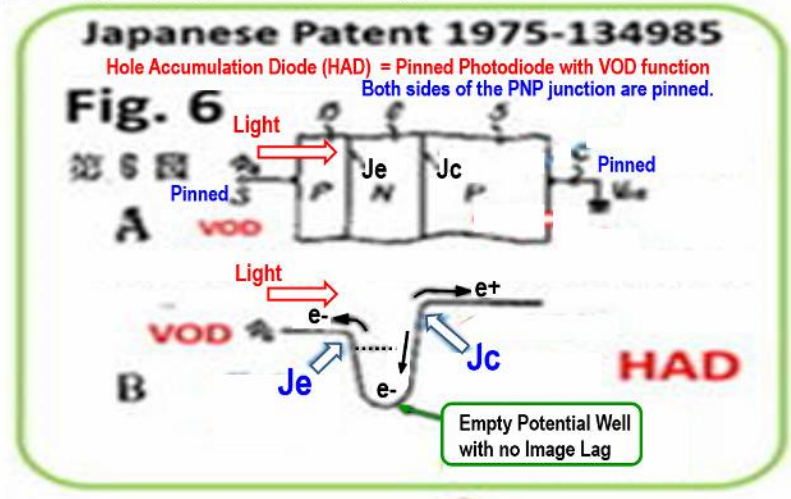
Hagiwara invented in 1975 the in-pixel vertical overflow drain (VOD) in PNP Pinned Photodiode.

(4) Light (Je) VOD (Je) type Pinned Photodiode



Hagiwara invented in 1975 the in-pixel vertical overflow drain (VOD) in PNP Pinned Photodiode.

(4) Light (Je) VOD (Je) type Pinned Photodiode



Light(Je) type Pinned Photodiode

Je side is used for light illumination

VOD(Je) type Pinned Photodiode

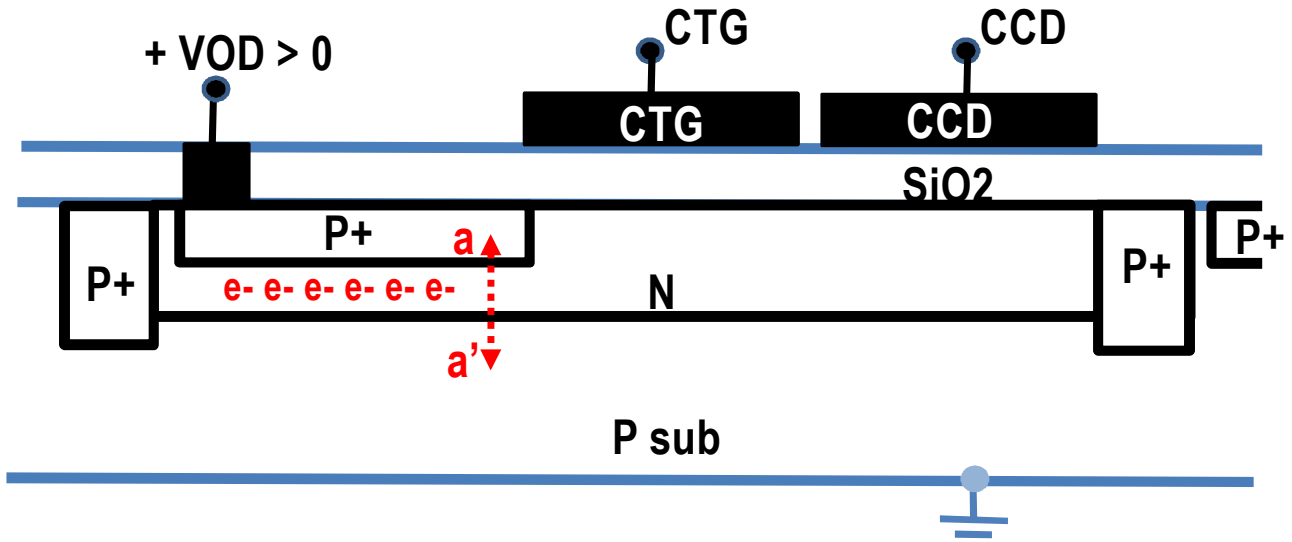
Je side is used for VOD action

PPD needs P+ Channel Stops.

VOD metal contact is optional. If the surface VOD is not needed, the VOD metal contact can be deleted and the surface P+ can be connected to the adjacent P+ channel stops.

PPD needs P+ Channel Stops.

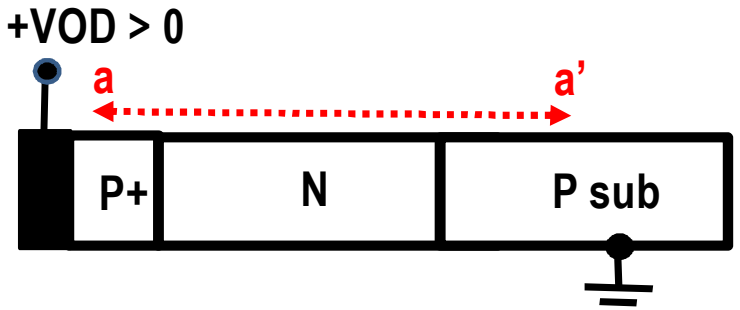
Fig. 5 of the Japanese Patent Application JPA 1975-134985 shows the P+NP double junction type Pinned Photodiode with the VOD function

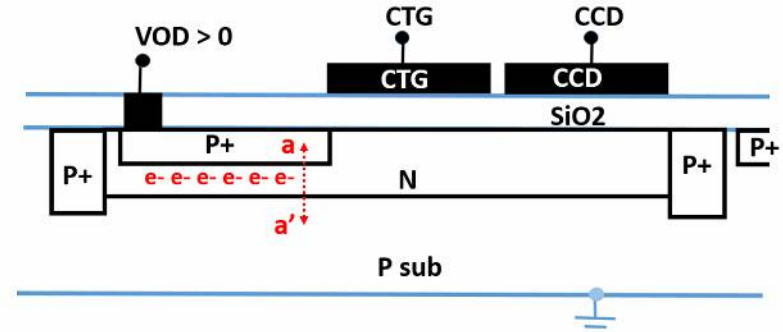


VOD metal contact is optional. If the surface VOD is not needed, the VOD metal contact can be deleted and the surface P+ can be connected to the adjacent P+ channel stops.

PPD needs P+ Channel Stops.

Fig. 5 of the Japanese Patent Application JPA 1975-134985 shows the P+NP double junction type Pinned Photodiode with the VOD function

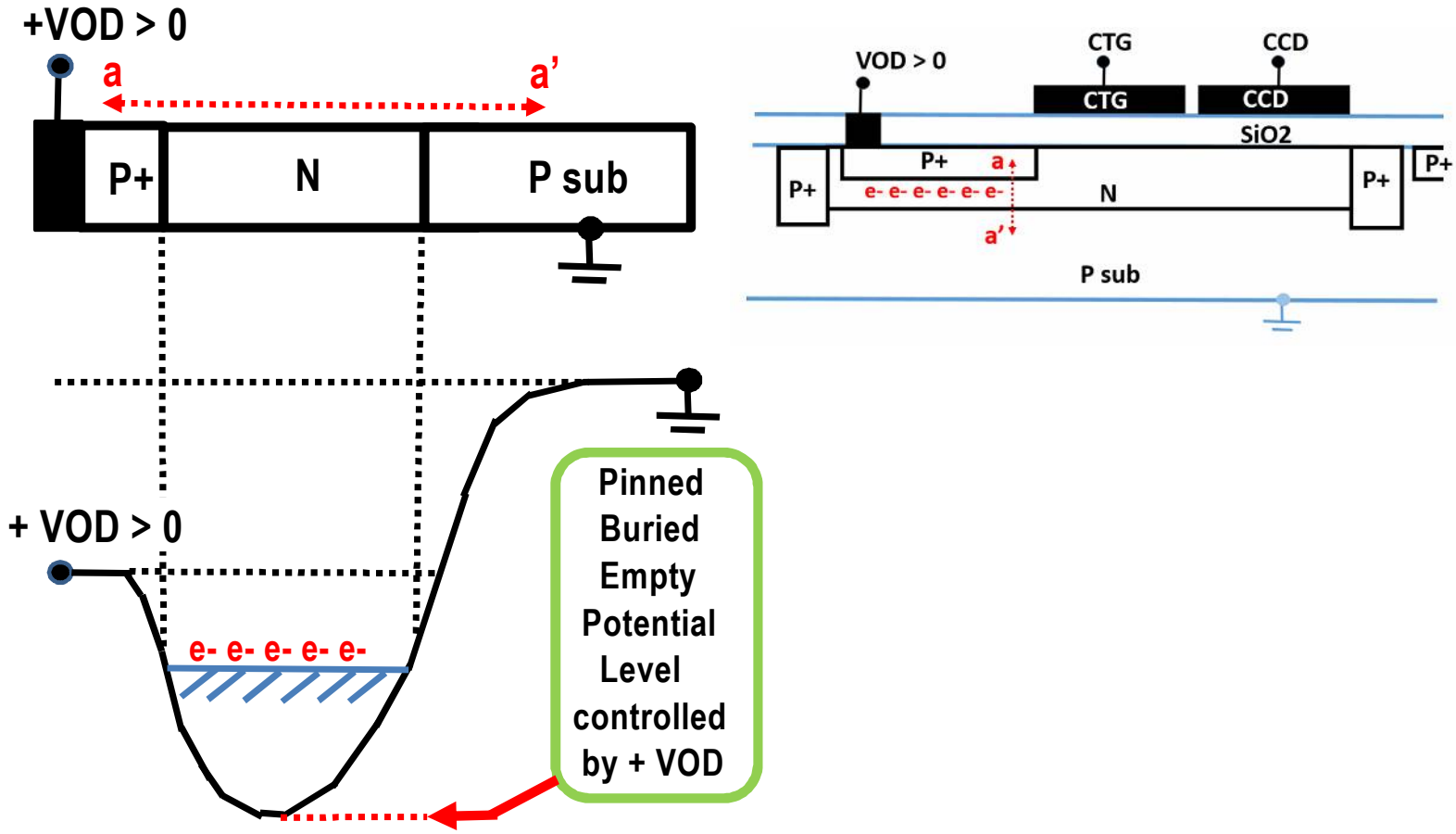




VOD metal contact is optional. If the surface VOD is not needed, the VOD metal contact can be deleted and the surface P+ can be connected to the adjacent P+ channel stops.

PPD needs P+ Channel Stops.

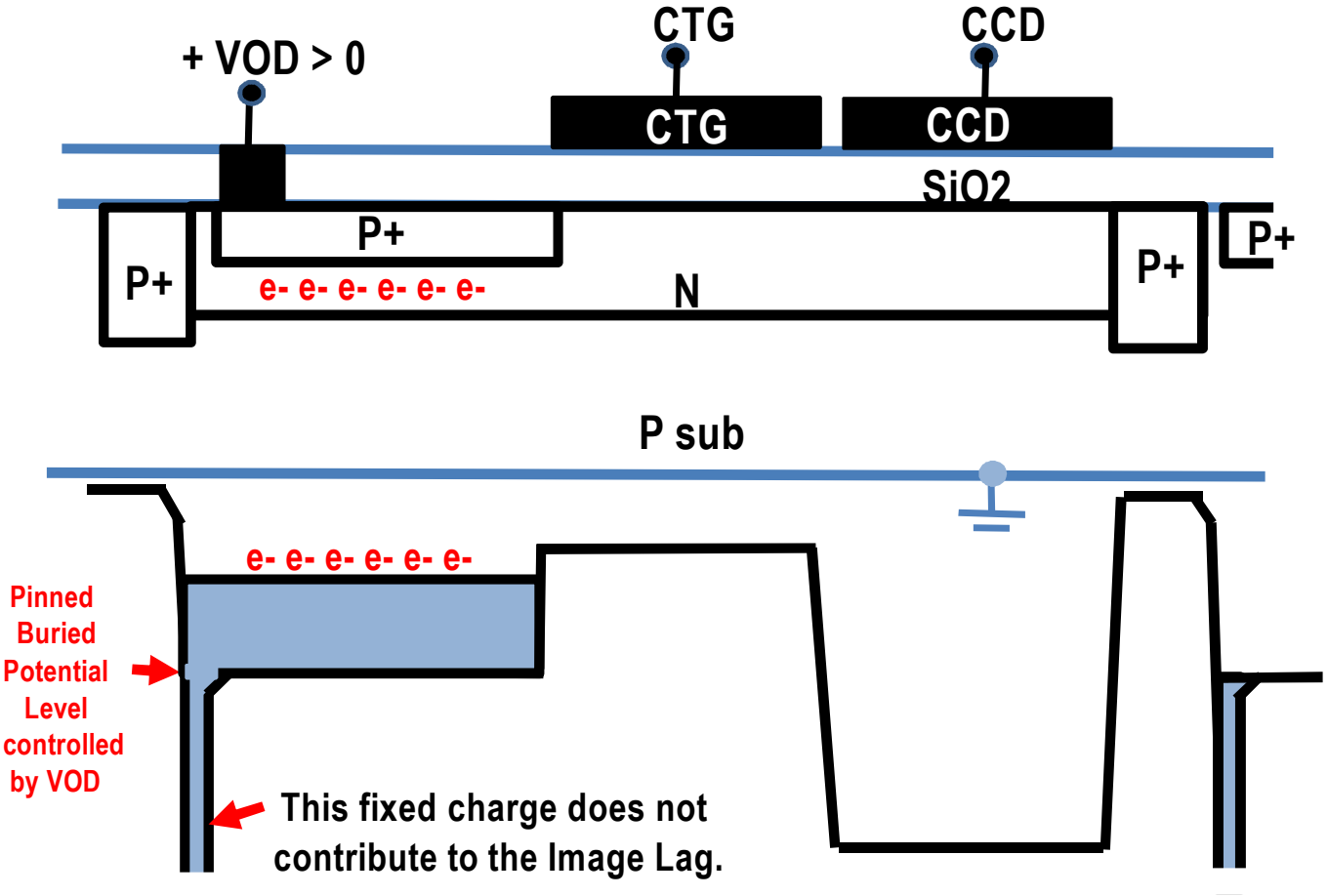
Fig. 5 of the Japanese Patent Application JPA 1975-134985 shows the P+NP double junction type Pinned Photodiode with the VOD function



VOD metal contact is optional. If the surface VOD is not needed, the VOD metal contact can be deleted and the surface P+ can be connected to the adjacent P+ channel stops.

PPD needs P+ Channel Stops.

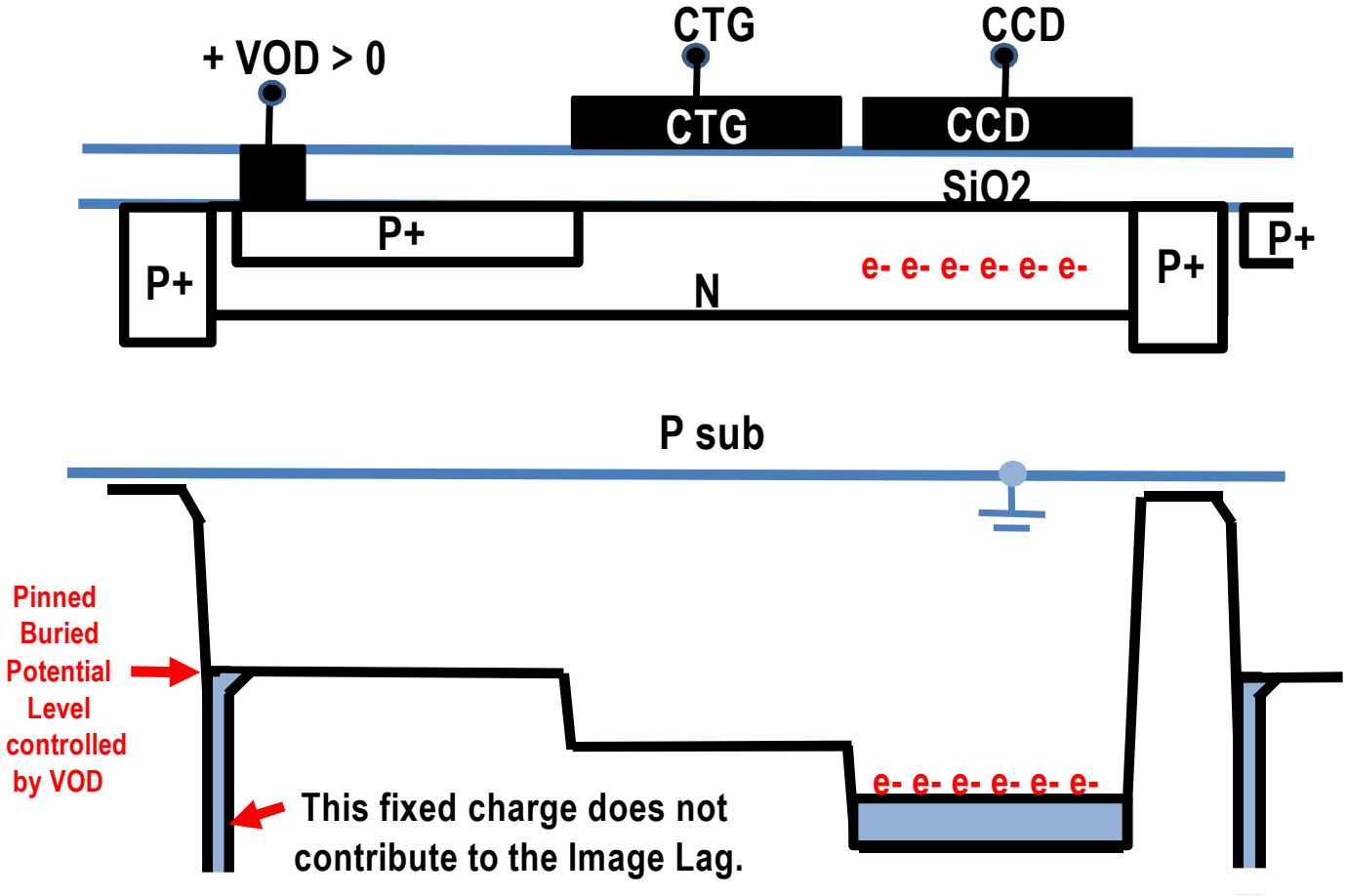
Fig. 5 of the Japanese Patent Application JPA 1975-134985 shows the P+NP double junction type Pinned Photodiode with the VOD function



VOD metal contact is optional. If the surface VOD is not needed, the VOD metal contact can be deleted and the surface P+ can be connected to the adjacent P+ channel stops.

PPD needs P+ Channel Stops.

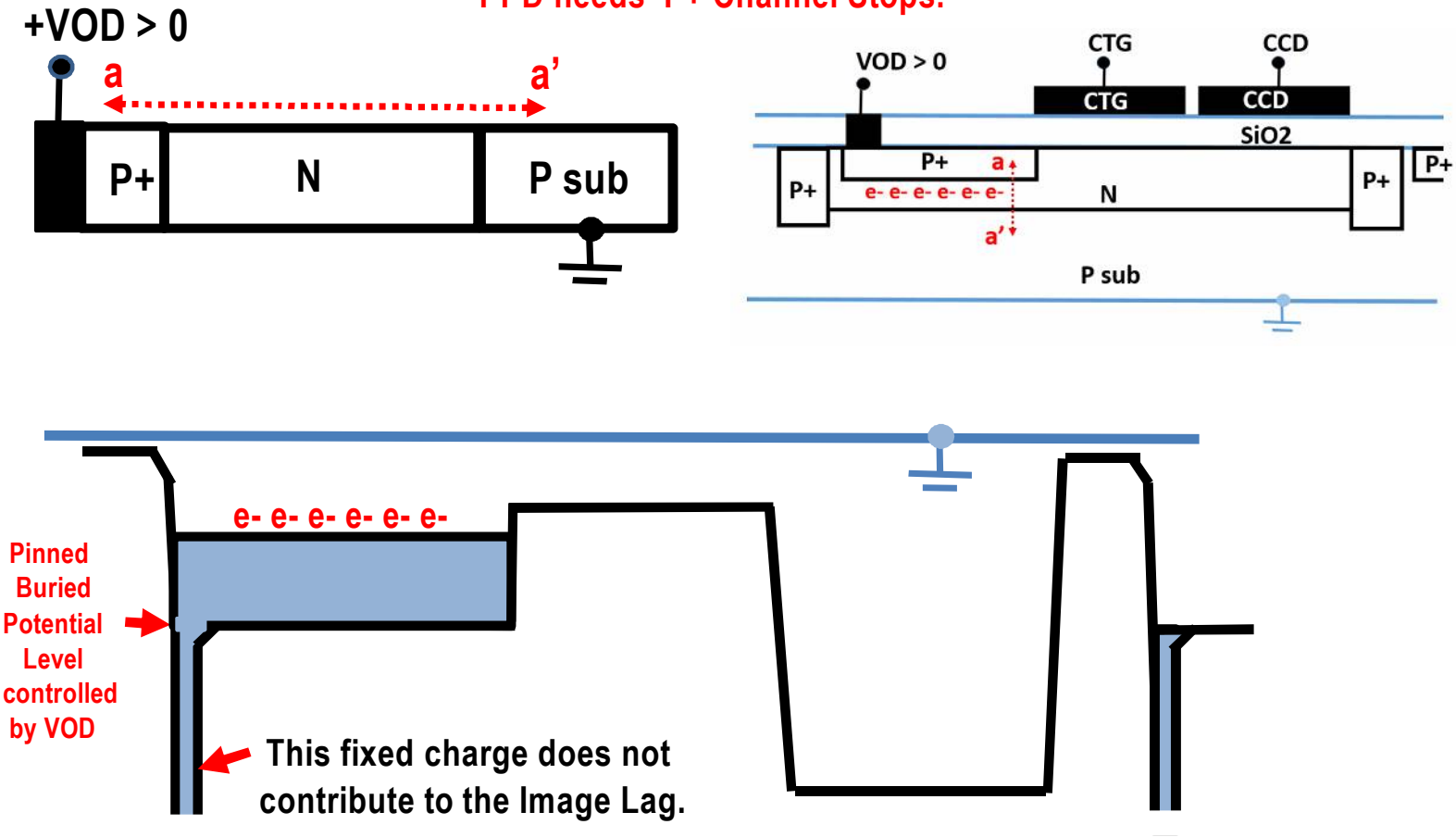
Fig. 5 of the Japanese Patent Application JPA 1975-134985 shows the P+NP double junction type Pinned Photodiode with the VOD function



VOD metal contact is optional. If the surface VOD is not needed, the VOD metal contact can be deleted and the surface P+ can be connected to the adjacent P+ channel stops.

Fig. 5 of the Japanese Patent Application JPA 1975-134985 shows the P+NP double junction type Pinned Photodiode with the VOD function

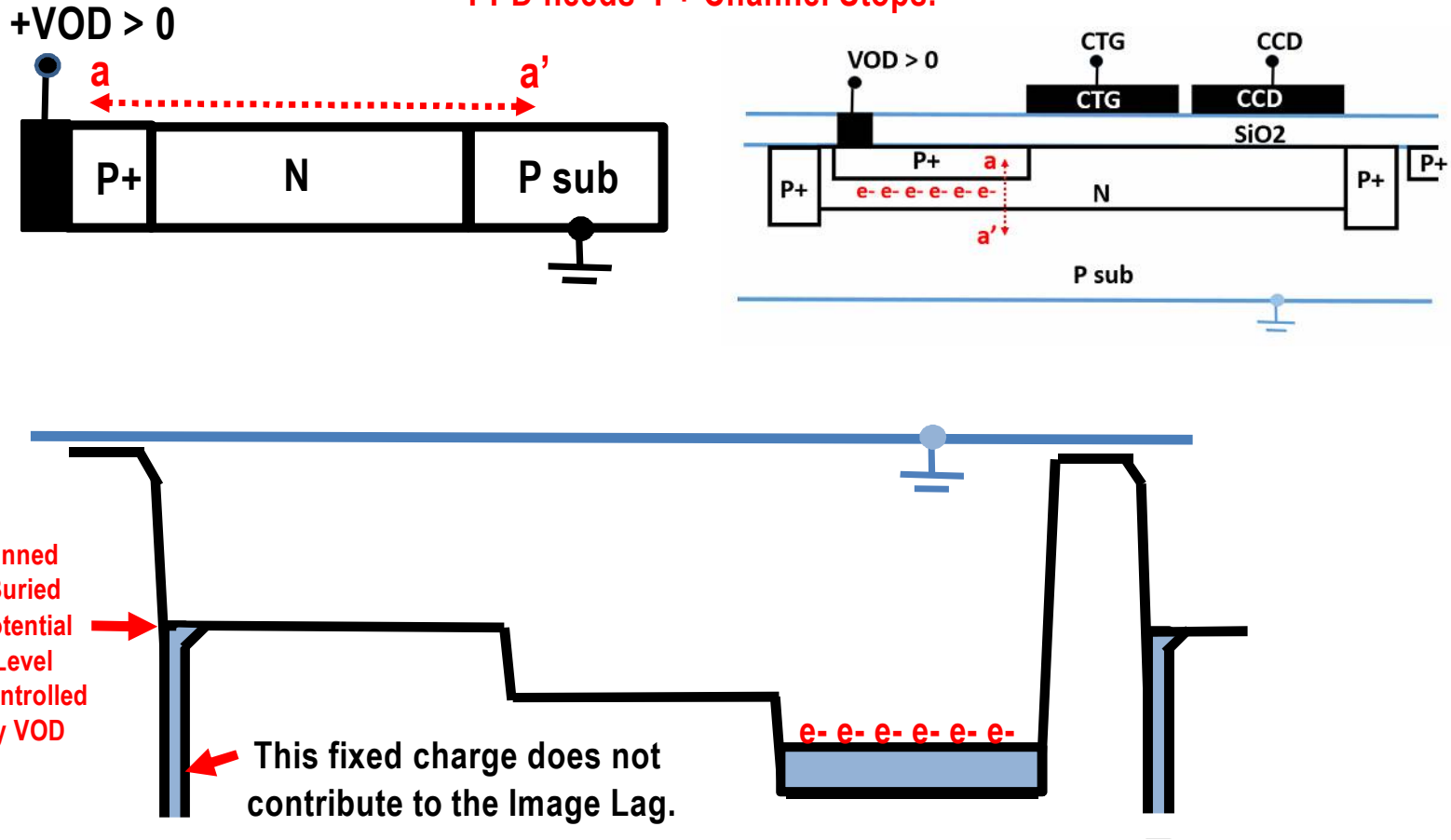
PPD needs P+ Channel Stops.



VOD metal contact is optional. If the surface VOD is not needed, the VOD metal contact can be deleted and the surface P+ can be connected to the adjacent P+ channel stops.

Fig. 5 of the Japanese Patent Application JPA 1975-134985 shows the P+NP double junction type Pinned Photodiode with the VOD function

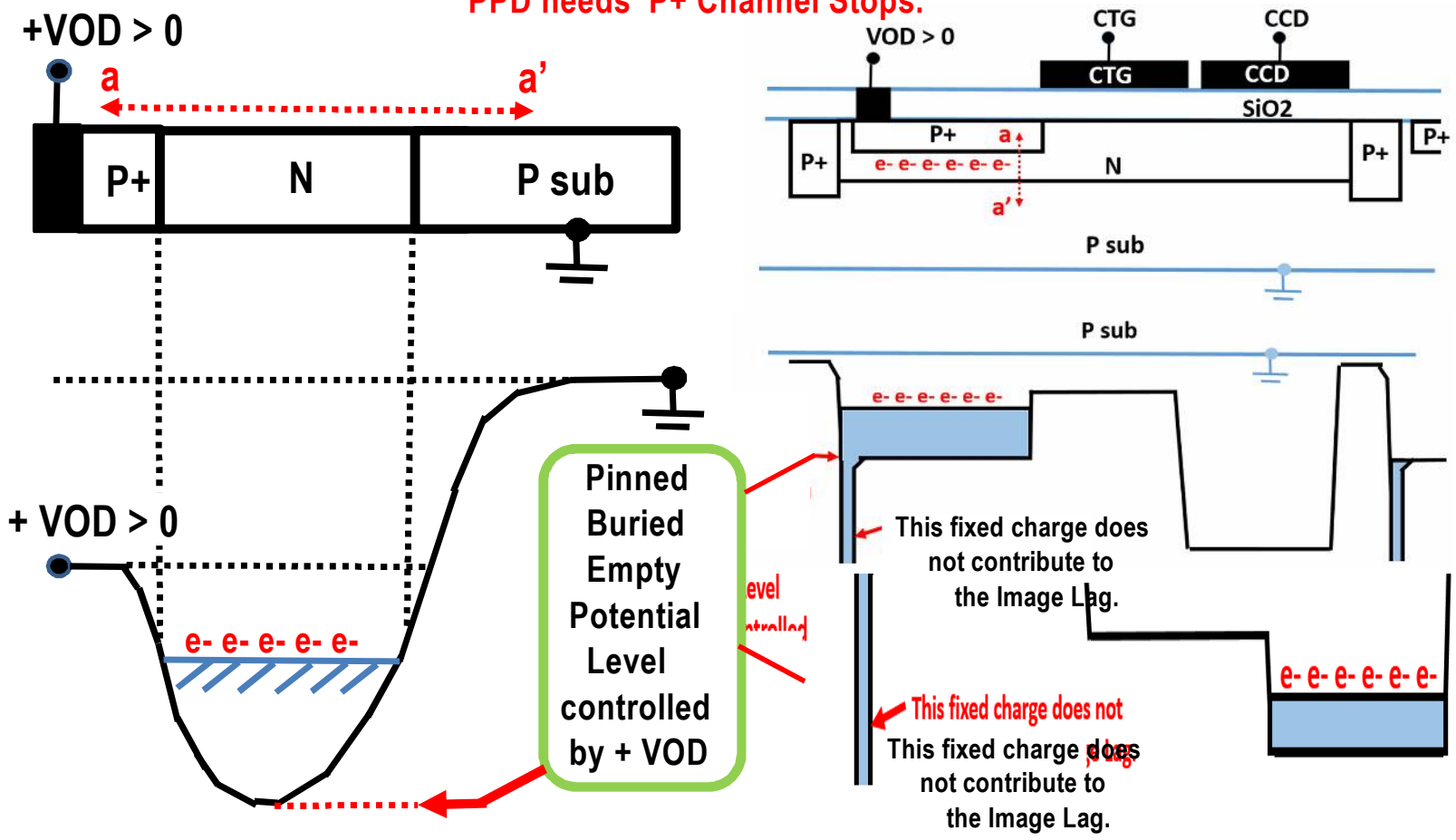
PPD needs P+ Channel Stops.



VOD metal contact is optional. If the surface VOD is not needed, the VOD metal contact can be deleted and the surface P+ can be connected to the adjacent P+ channel stops.

Fig. 5 of the Japanese Patent Application JPA 1975-134985 shows the P+NP double junction type Pinned Photodiode with the VOD function

PPD needs P+ Channel Stops.

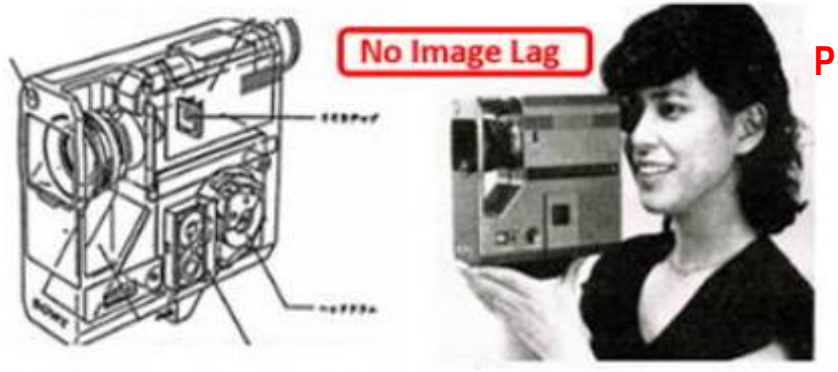


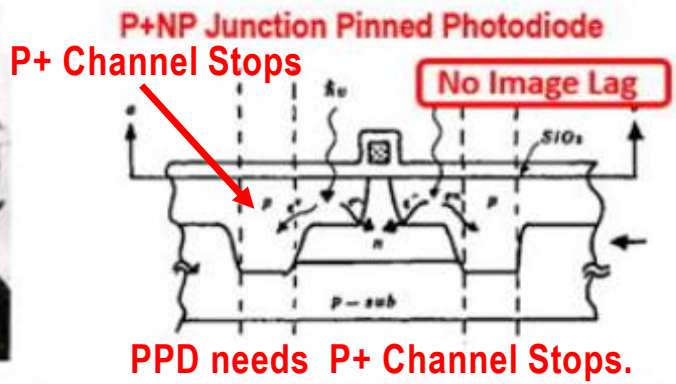
VOD metal contact is optional. If the surface VOD is not needed, the VOD metal contact can be deleted and the surface P+ can be connected to the adjacent P+ channel stops.

SONY HAD (Pinned Photodiode) Publications at the International Solid State Device Conference in 1978 and the Tokyo & New York SONY Press Conference in 1980

The original Pinned Photodiode (PPD) structure was invented by Hagiwara at Sony in 1975. The first one-chip color video camera with a FT CCD image sensor with P+NP junction type Pinned Photodiode (PPD) was reported by Sony in 1980 at Tokyo Press Conference by Iwama Kazuo of Sony president, and at New York Press conference by Morita Akio of Sony chairman.

Sony original 570H x 498 V one-chip FT CCD Image Sensor with Pinned Photodiode, July 1980





On July 1980, Iwama Kazuo at Sony Tokyo Press Conference and Morita Akio at New York Press Conference announced the one chip CCD video camera with the 8 mm VTR in one box.

See the Original 1978 Publication of the Pinned Photodiode Sensor

Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488V CCD imager with narrow channel transfer gates," Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Appllied Physics , vol. 18, supplement 18–1, pp. 335–340, 1979

High quality picture of SONY CMOS Imager is also based on SONY HAD (Pinned Photodiode).

P+NP/Sub junction type Pinned Photo Diode

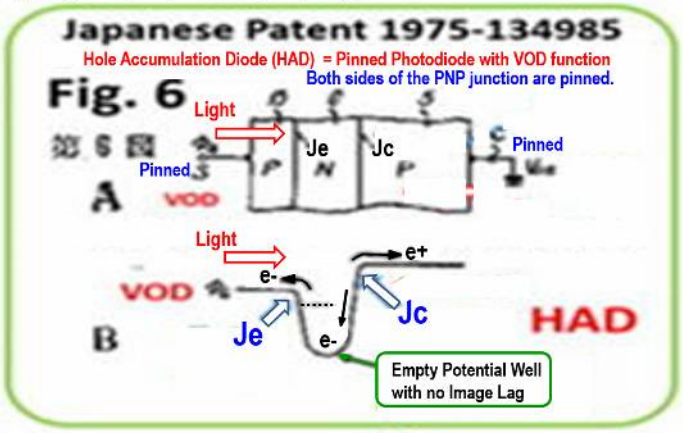
invented by Hagiwara at Sony in Japanese Patent 1975-134985.

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

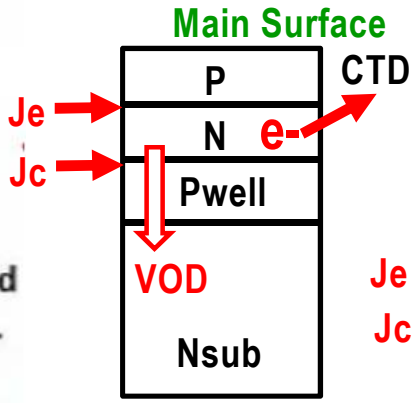
Patent Claim in English Translation

(1) In the semiconductor substrate (Nsub), the first region(Pwell) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N/Pwell Junction) is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N/Pwell) , (6) forming a PNP Junction type transistor structure with the N/Pwell junction as Collector junction (Jc). (7) The charge, stored in the Base region (N) according to the illuminated light intensity, is transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.

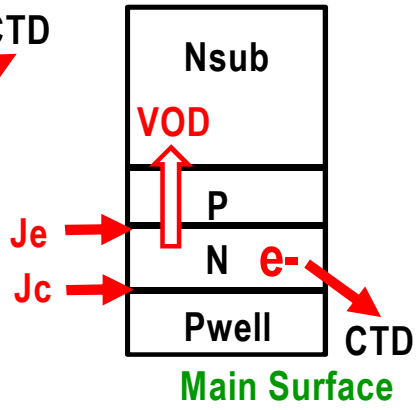
(4) Light (Je) VOD (Je) type Pinned Photodiode



(4) Light(Je)VOD(Jc)



(1) Light(Jc) VOD(Je)



Visit https://www.j-platpat.inpit.go.jp/ and type Japanese Patent Number 1975-134985

P+NP/Sub junction type Pinned Photo Diode

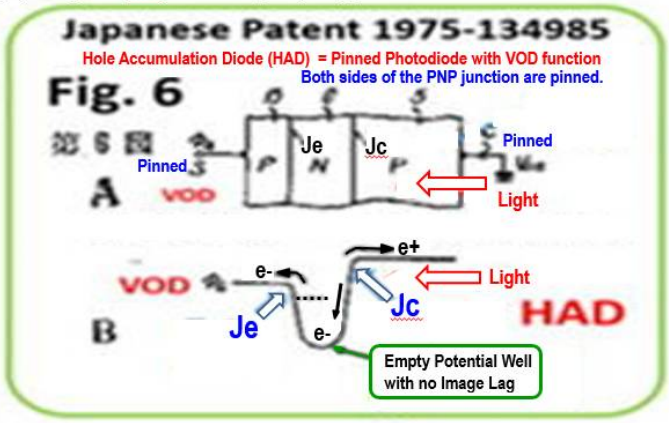
invented by Hagiwara at Sony in Japanese Patent 1975-134985.

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

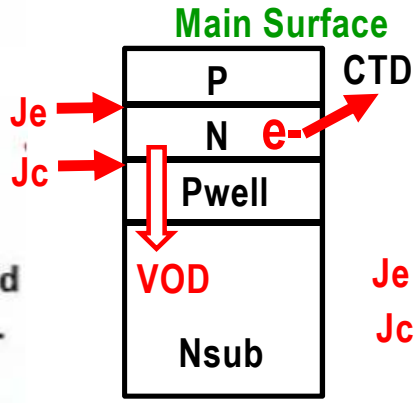
Patent Claim in English Translation

(1) In the semiconductor substrate (Nsub), the first region(Pwell) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N/Pwell Junction) is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N/Pwell) , (6) forming a PNP Junction type transistor structure with the N/Pwell junction as Collector junction (Jc). (7) The charge, stored in the Base region (N) according to the illuminated light intensity, is transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.

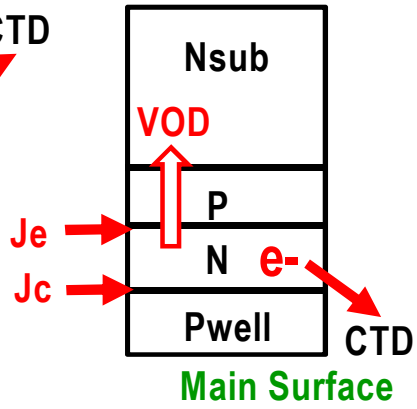
(1) Light (Jc) VOD (Je) type Pinned Photodiode



(4) Light(Je)VOD(Jc)



(1) Light(Jc) VOD(Je)



Visit https://www.j-platpat.inpit.go.jp/ and type Japanese Patent Number 1975-134985

P+NP/Sub junction type Pinned Photo Diode

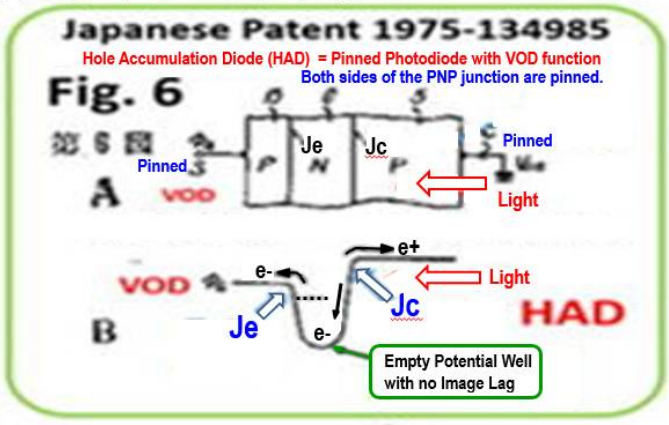
invented by Hagiwara at Sony in Japanese Patent 1975-134985.

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

Patent Claim in English Translation

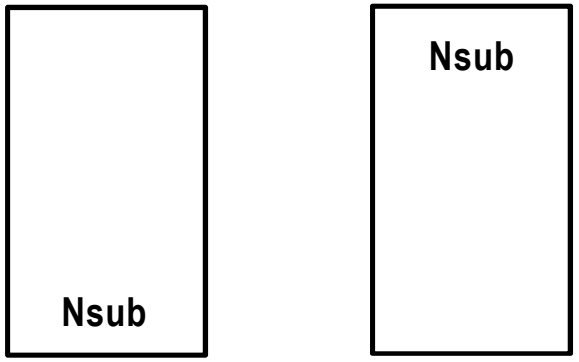
(1) In the semiconductor substrate (Nsub),

(1) Light (Jc) VOD (Je) type Pinned Photodiode



(4) Light(Je)VOD(Jc)

(1) Light(Jc) VOD(Je)



Visit https://www.j-platpat.inpit.go.jp/ and type Japanese Patent Number 1975-134985

P+NP/Sub junction type Pinned Photo Diode

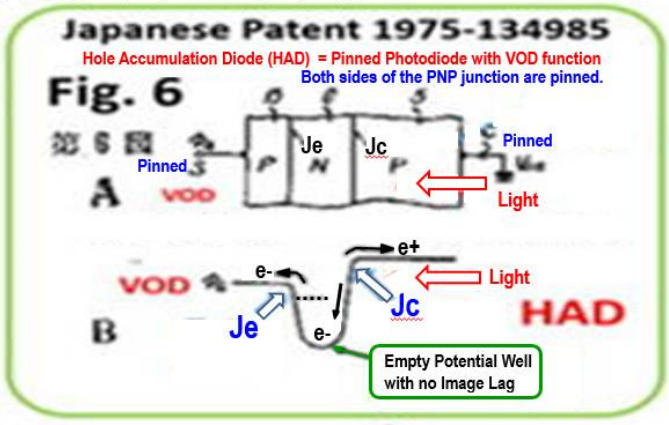
invented by Hagiwara at Sony in Japanese Patent 1975-134985.

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

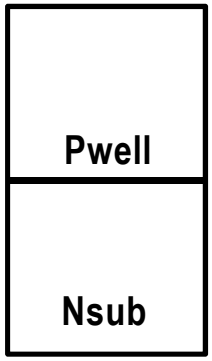
Patent Claim in English Translation

(1) In the semiconductor substrate (Nsub), the first region(Pwell) of the first impurity type is formed,

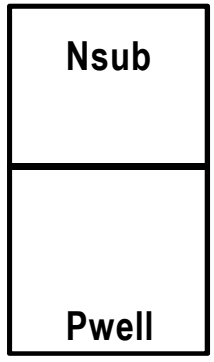
(1) Light (Jc) VOD (Je) type Pinned Photodiode



(4) Light(Je)VOD(Jc)



(1) Light(Jc) VOD(Je)



Visit https://www.j-platpat.inpit.go.jp/ and type Japanese Patent Number 1975-134985

P+NP/Sub junction type Pinned Photo Diode

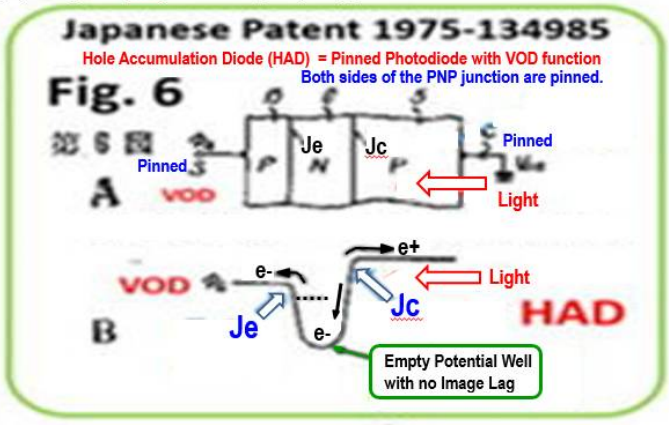
invented by Hagiwara at Sony in Japanese Patent 1975-134985.

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

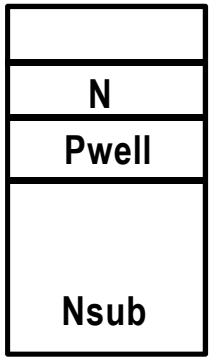
Patent Claim in English Translation

(1) In the semiconductor substrate (Nsub), the first region(Pwell) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed.

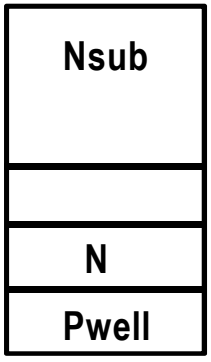
(1) Light (Jc) VOD (Je) type Pinned Photodiode



(4) Light(Je)VOD(Jc)



(1) Light(Jc) VOD(Je)



Visit https://www.j-platpat.inpit.go.jp/ and type Japanese Patent Number 1975-134985

P+NP/Sub junction type Pinned Photo Diode

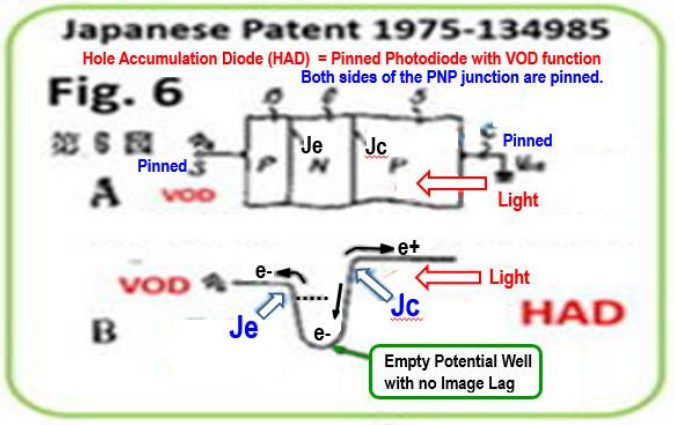
invented by Hagiwara at Sony in Japanese Patent 1975-134985.

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

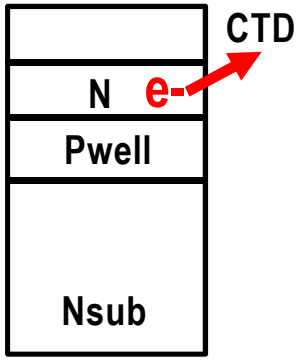
Patent Claim in English Translation

(1) In the semiconductor substrate (Nsub), the first region(Pwell) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N/Pwell Junction) is transferred to the adjacent charge transfer device (CTD).

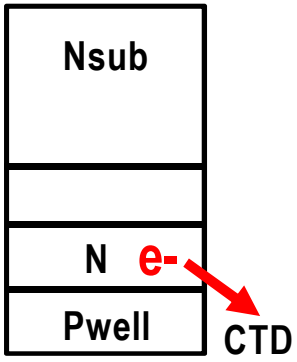
(1) Light (Jc) VOD (Je) type Pinned Photodiode



(4) Light(Je)VOD(Jc)



(1) Light(Jc) VOD(Je)



Visit https://www.j-platpat.inpit.go.jp/ and type Japanese Patent Number 1975-134985

P+NP/Sub junction type Pinned Photo Diode

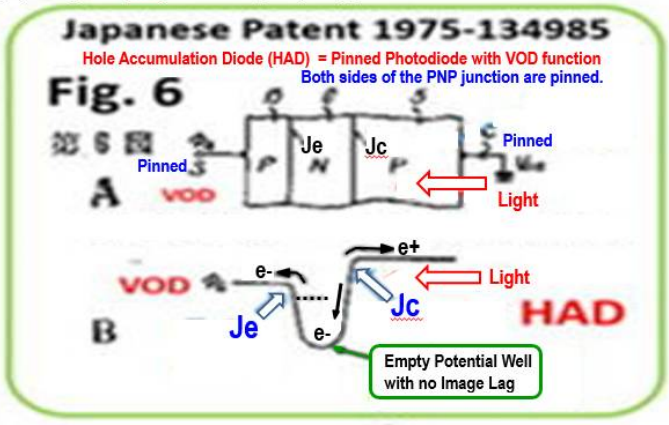
invented by Hagiwara at Sony in Japanese Patent 1975-134985.

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

Patent Claim in English Translation

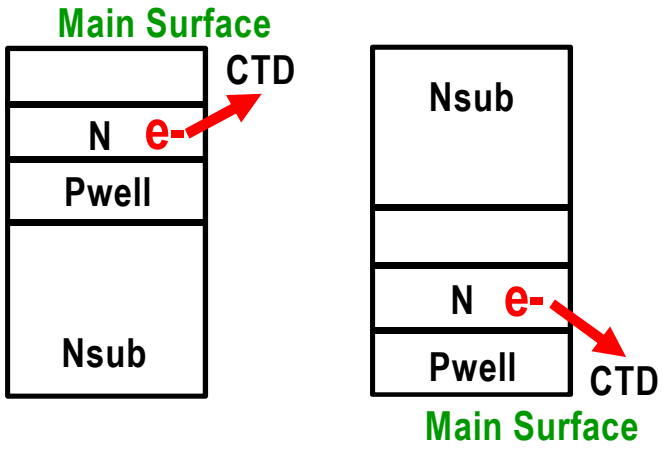
(1) In the semiconductor substrate (Nsub), the first region(Pwell) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N/Pwell Junction) is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate.

(1) Light (Jc) VOD (Je) type Pinned Photodiode



(4) Light(Je)VOD(Jc)

(1) Light(Jc) VOD(Je)



Visit https://www.j-platpat.inpit.go.jp/ and type Japanese Patent Number 1975-134985

P+NP/Sub junction type Pinned Photo Diode

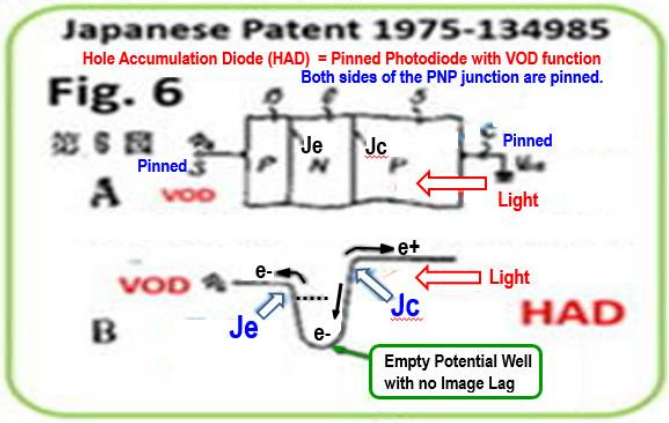
invented by Hagiwara at Sony in Japanese Patent 1975-134985.

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

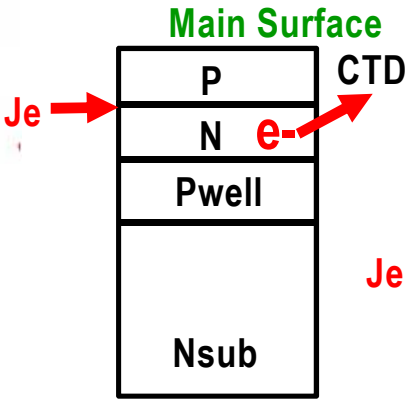
Patent Claim in English Translation

(1) In the semiconductor substrate (Nsub), the first region(Pwell) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N/Pwell Junction) is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N/Pwell) ,

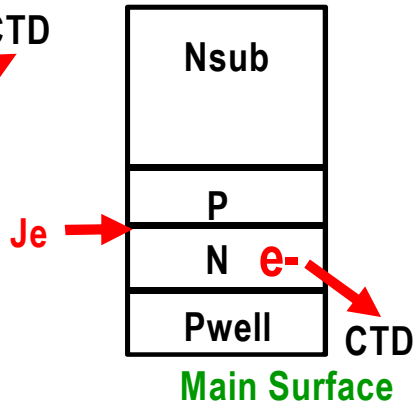
(1) Light (Jc) VOD (Je) type Pinned Photodiode



(4) Light(Je)VOD(Jc)



(1) Light(Jc) VOD(Je)



Visit https://www.j-platpat.inpit.go.jp/ and type Japanese Patent Number 1975-134985

P+NP/Sub junction type Pinned Photo Diode

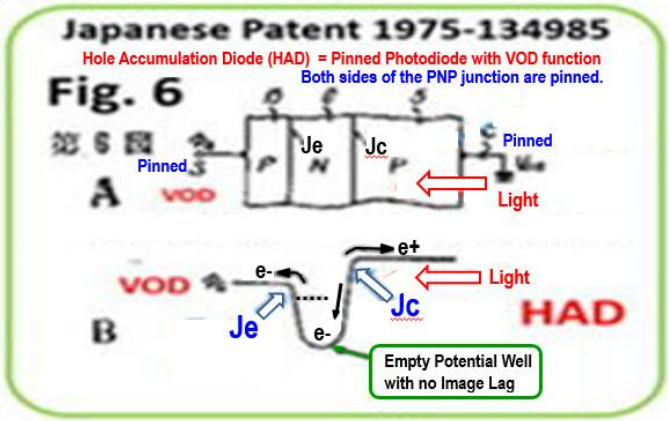
invented by Hagiwara at Sony in Japanese Patent 1975-134985.

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

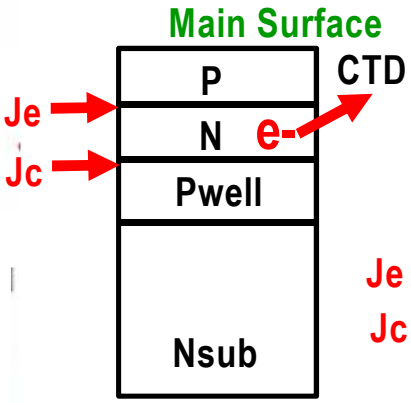
Patent Claim in English Translation

(1) In the semiconductor substrate (Nsub), the first region(Pwell) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N/Pwell Junction) is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N/Pwell) , (6) forming a PNP Junction type transistor structure with the N/Pwell junction as Collector junction (Jc).

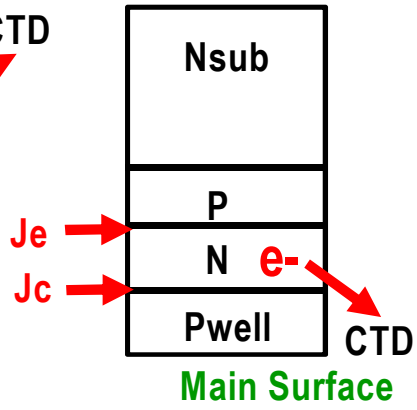
(1) Light (Jc) VOD (Je) type Pinned Photodiode



(4) Light(Je)VOD(Jc)



(1) Light(Jc) VOD(Je)



Visit https://www.j-platpat.inpit.go.jp/ and type Japanese Patent Number 1975-134985

P+NP/Sub junction type Pinned Photo Diode

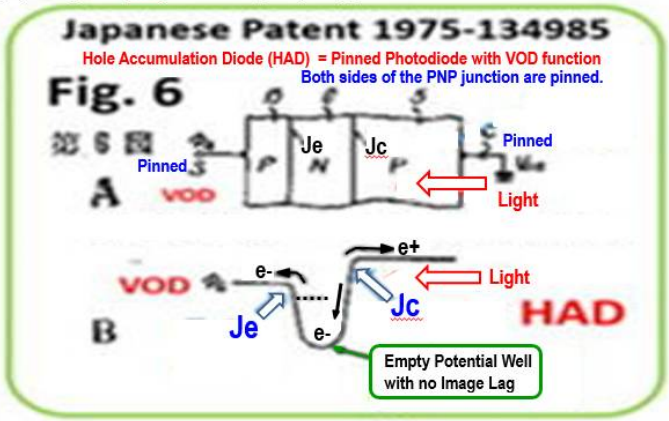
invented by Hagiwara at Sony in Japanese Patent 1975-134985.

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

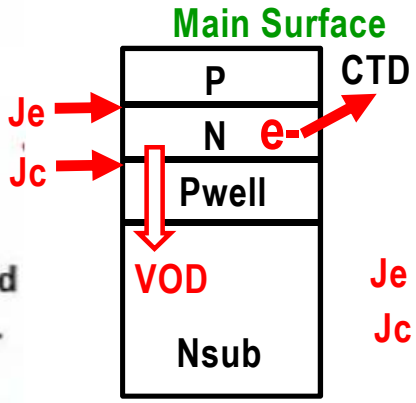
Patent Claim in English Translation

(1) In the semiconductor substrate (Nsub), the first region(Pwell) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N/Pwell Junction) is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N/Pwell) , (6) forming a PNP Junction type transistor structure with the N/Pwell junction as Collector junction (Jc). (7) The charge, stored in the Base region (N) according to the illuminated light intensity, is transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.

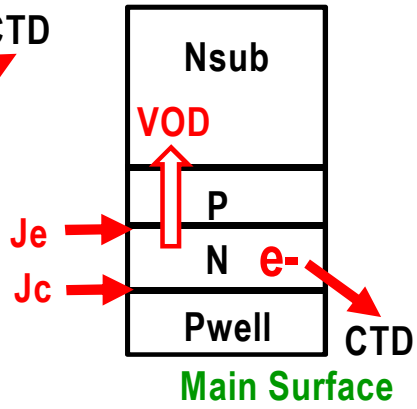
(1) Light (Jc) VOD (Je) type Pinned Photodiode



(4) Light(Je)VOD(Jc)



(1) Light(Jc) VOD(Je)

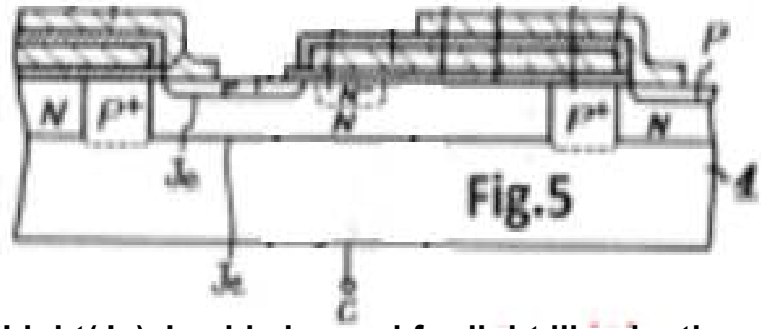


Visit https://www.j-platpat.inpit.go.jp/ and type Japanese Patent Number 1975-134985

P+NP/Sub junction type Pinned Photo Diode

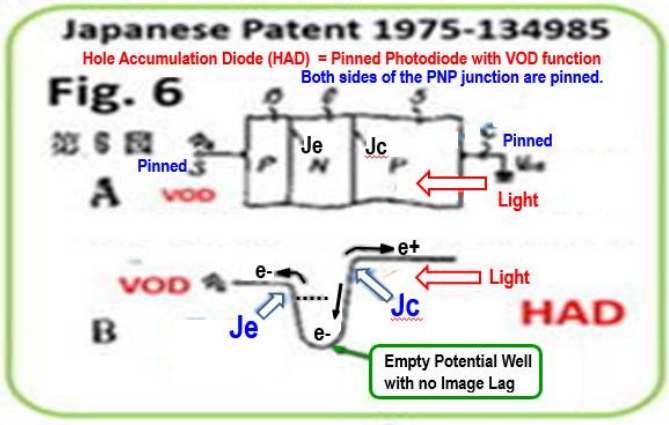
invented by Hagiwara at Sony in Japanese Patent 1975-134985.

(4) Light (Je) / VOD (Je) type

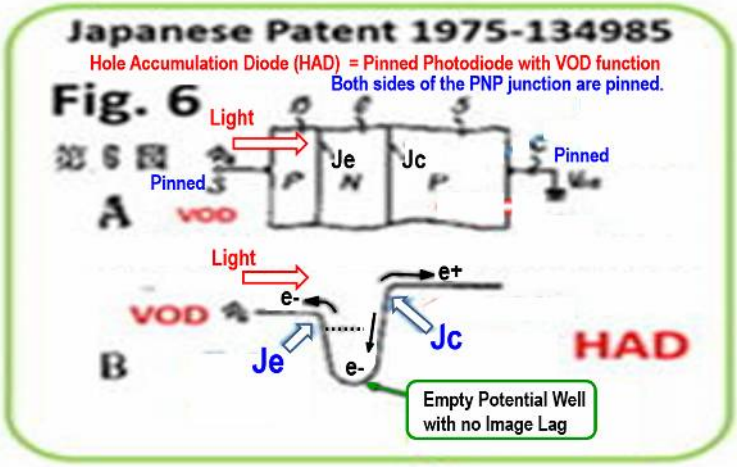


Light(Je) Je side is used for light illumination
VOD(Jc) Jc side is used for VOD action

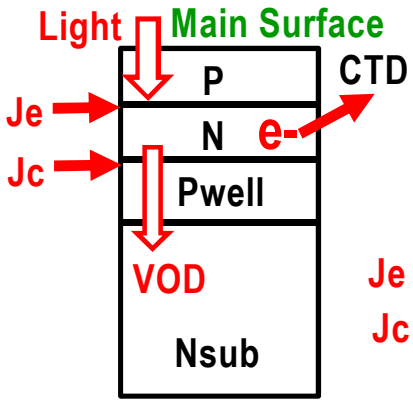
(1) Light (Jc) VOD (Je) type Pinned Photodiode



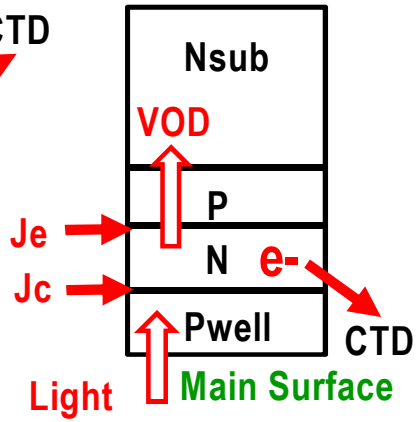
(4) Light (Je) VOD (Je) type Pinned Photodiode



(4) Light(Je)VOD(Jc)



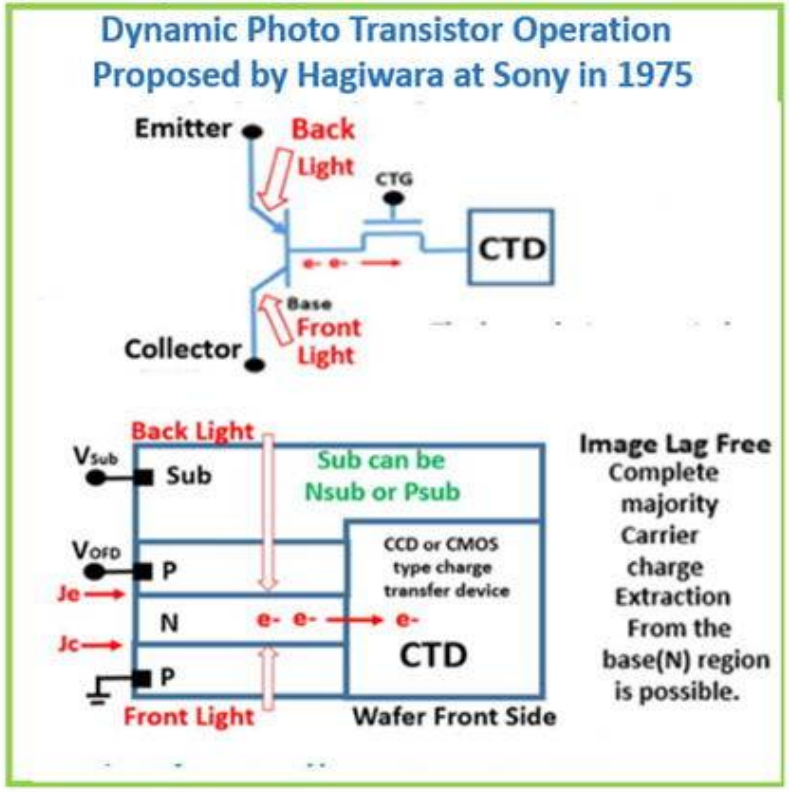
(1) Light(Jc) VOD(Je)



Visit https://www.j-platpat.inpit.go.jp/ and type Japanese Patent Number 1975-134985

Finally the Sony-Fairchild Patent Wat(1991-2000) ended over the Sony HAD Sensor which is identical to the P+NPNsub junction type Pinned Photodiode with Vertical Overflow Drain, originally invented by Hagiwara at Sony in 1975.

And finally Hagiwara received for his 1975-134985 Japanese Patent officially , the First Patent Award from Mr. Ando, Sony president in April, 2001 after more 26 years of struggles since his invention.



Japanese Patent JPA 1977-126885 on Electrical Shutter Clocking Scheme invented by Y. Hagiwara, S. Ochi and T. Hashimoto in 1977.

Fig. 3 CCD/MOS Photo Capacitor

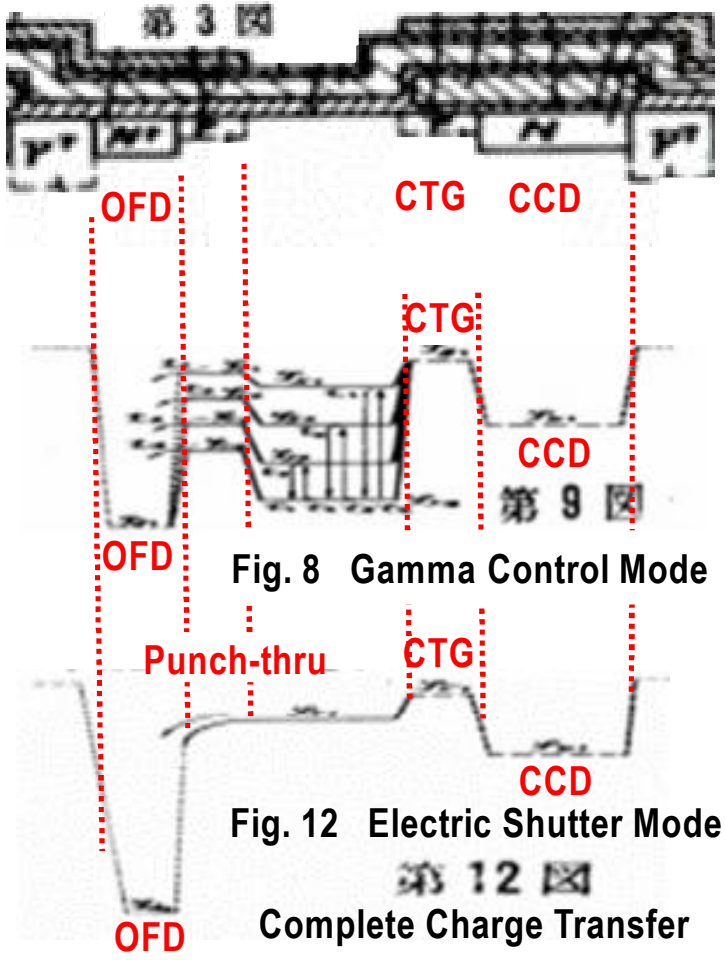


Fig. 8 Gamma Control Mode

Fig. 12 Electric Shutter Mode

Complete Charge Transfer and no image lag

The electric shutter clocking scheme with the complete draining of signal charge with the no image lag feature can be achieved by controlling the overflow drain (OFD) punch-thru voltage.

Pinned Photodiode with VOD function

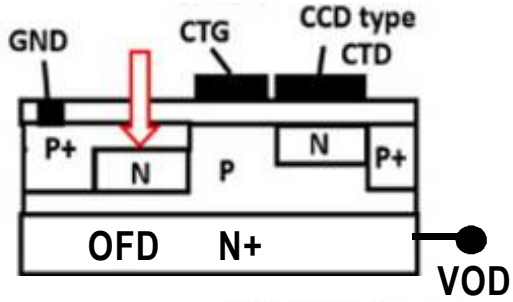


Fig. 7

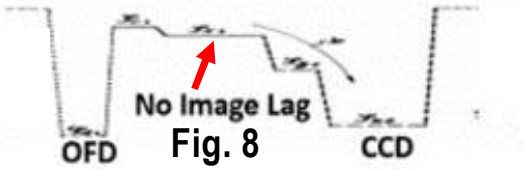
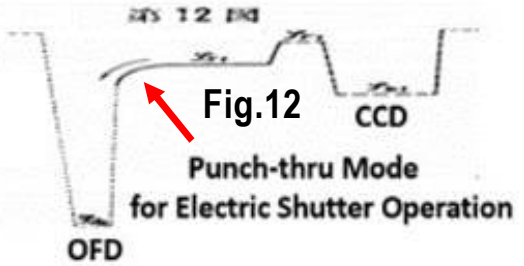
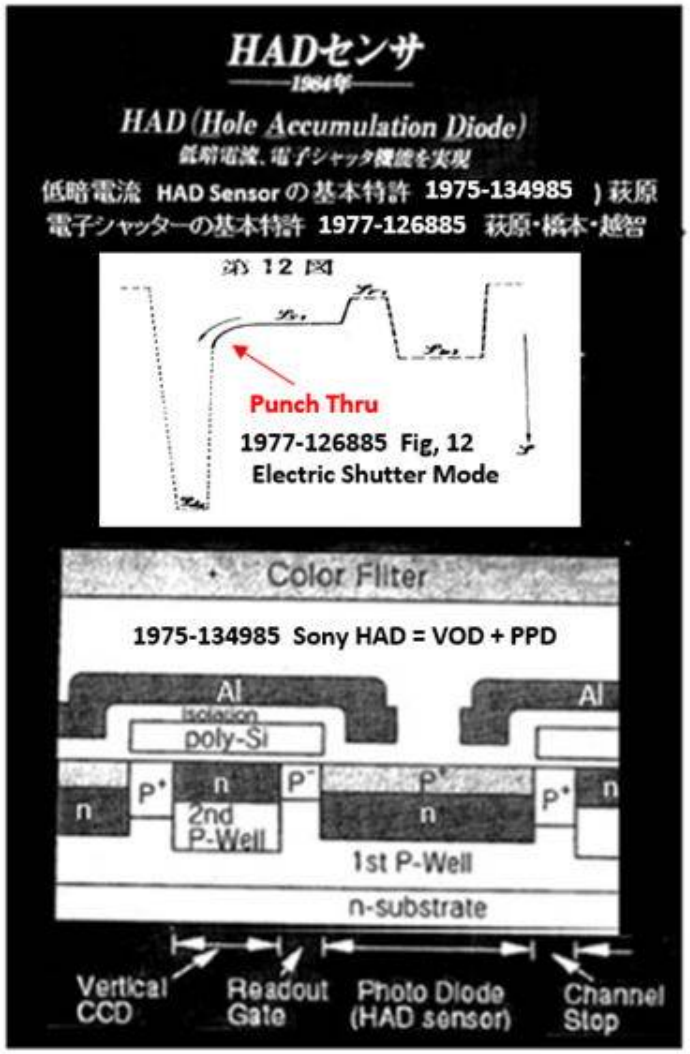


Fig. 8



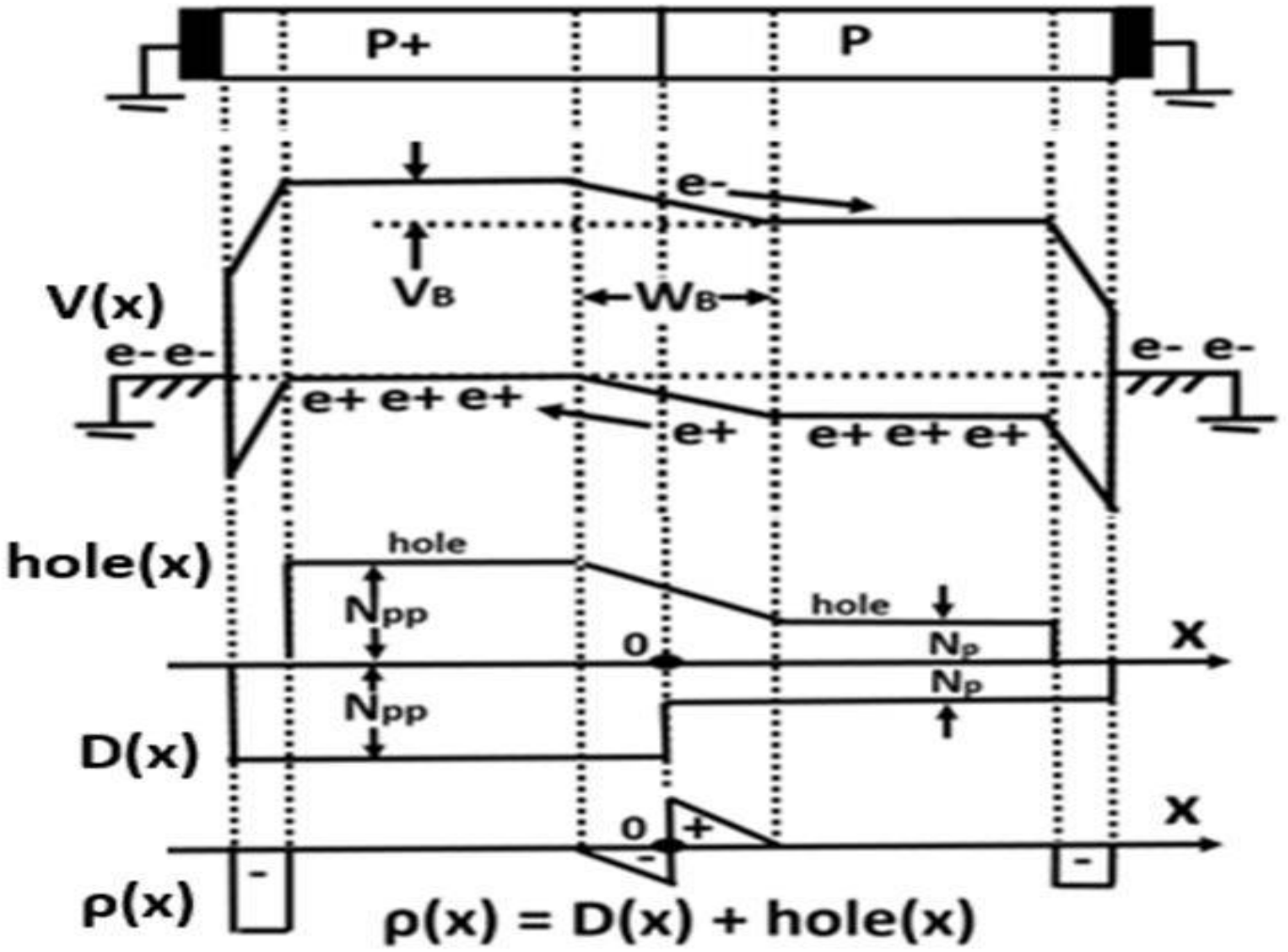
The Pinned Photodiode（Sony Original HAD sensor）Structure

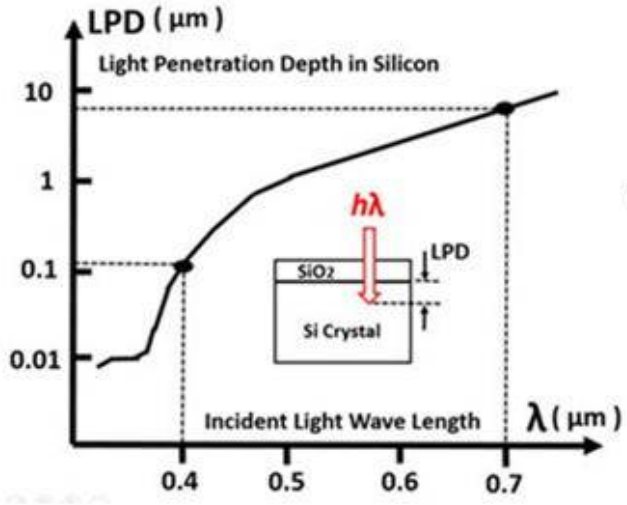


(from SONY Product Catalog)

Electric Shutter Basic Patent Award
from Sony President Idei to Yoshiaki Hagiwara
for Japanese Patent 1977-126885 by Hagiwara

P+P Doping Slope Barrier Potential V_B





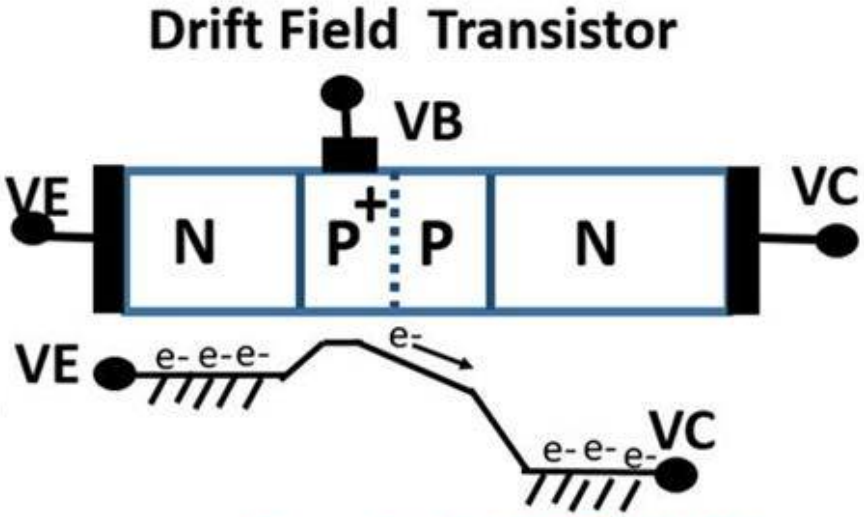


Figure 7 of JAP 1975-127647

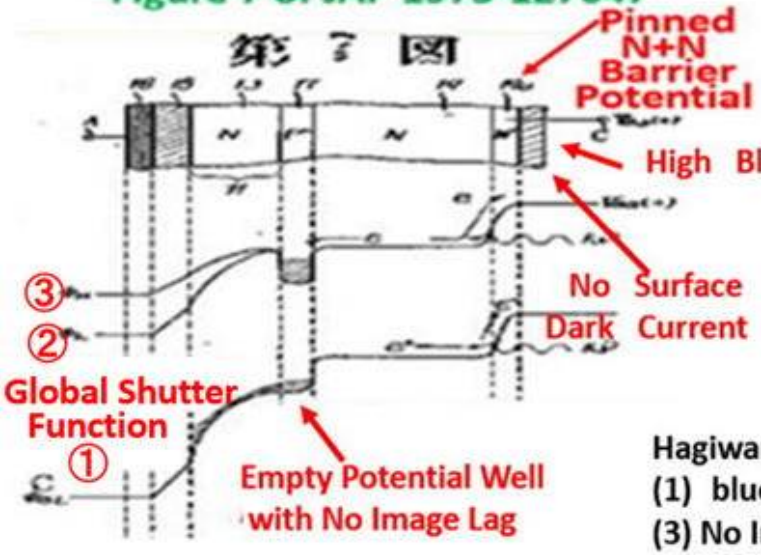
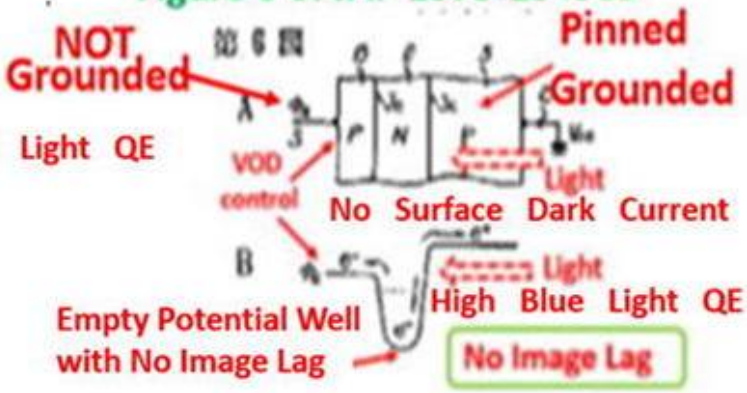


Figure 6 of JAP 1975-134985

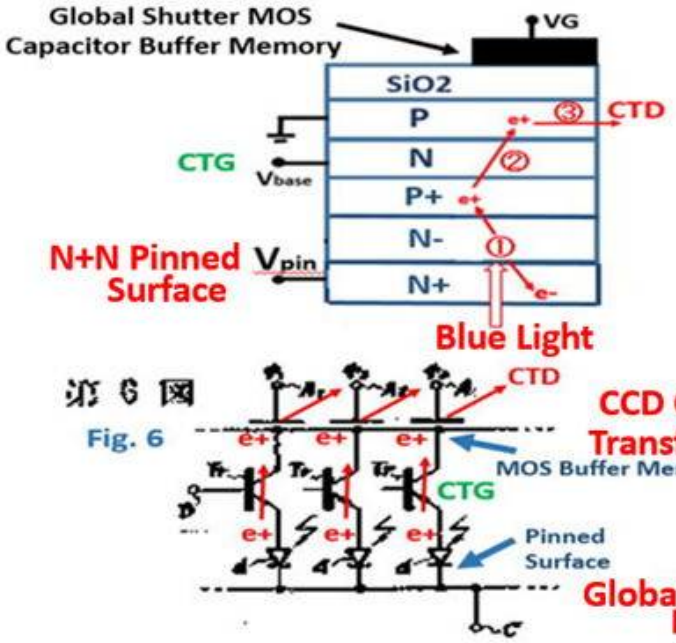


Hagiwara invented PNP junction type PPD in 1975 with
(1) blue light 100% QE, (2) No Surface Dark Current and
(3) No Image Lag, Complete Charge Transfer features.

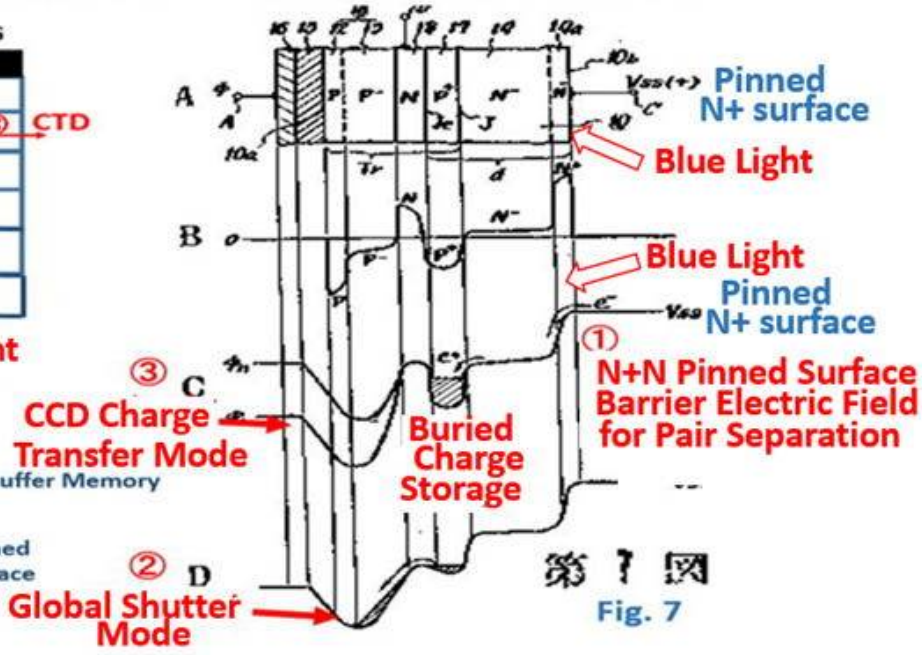
Japanese Patent 1975-127646

N+NP+NP junction type Buried Pinned Photodiode with Built-in MOS Capacitor Buffer Memory Global Shutter Function and the surface N+N doping slope Barrier Electric Field Photo Pair Generation

The First Japanese PPD Patent Application JPA 1975-127646 was applied for the back light illumination type Pinned Photodiode (PPD) image sensors with the CCD/MOS capacitor type buffer memory for Global Shutter Function which is a very important function needed for Modern CMOS Image Sensors.



Double Junction Dynamic Photo Transistor (PPD) invented in 1975 by Hagiwara at Sony.



Triple Junction Dynamic Photo Thyristor (HAD) invented in 1975 by Hagiwara at Sony.

See Japanese Patent Application JPA 1975-127646, 1975-127647 and 1975-134985

Global Shutter Mode

Japanese Patent 1975-127647

Complete Charge Transfer Mode No Image Lag

N+NP+N junction type Buried Pinned Photodiode with Built-in MOS Capacitor Buffer Memory Global Shutter Function and the surface N+N doping slope Barrier Electric Field Photo Pair Generation

This Japanese PPD Patent Application JPA 1975-127647 was also applied for the back light illumination type Pinned Photodiode (PPD) image sensors with the CCD/MOS capacitor type buffer memory for Global Shutter Function which is a very important function needed for Modern CMOS Image Sensors.

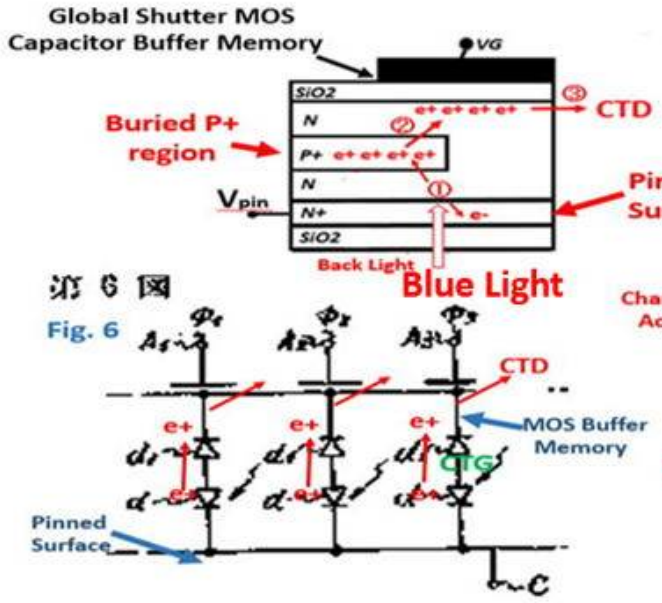


Fig. 6

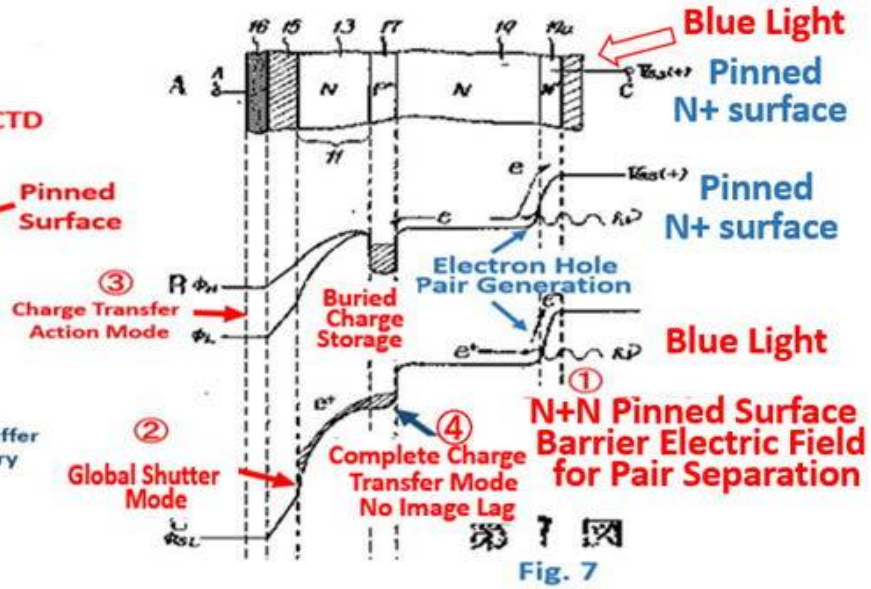


Fig. 7

Double Junction Dynamic Photo Transistor (PPD) invented in 1975 by Hagiwara at Sony.

Triple Junction Dynamic Photo Thyristor (HAD) invented in 1975 by Hagiwara at Sony.

See Japanese Patent Application JPA 1975-127646, 1975-127647 and 1975-134985

Japanese Patent 1975-134985

Pinned Photodiode and Sony Hole Accumulation Diode (HAD)

Pinned Surface Double Junction P+NP Dynamic Photo Transistor in the silicon substrate (Nsub)
Pinned Photodiode with the vertical overflow drain (VOD) function in the silicon substrate (Nsub)

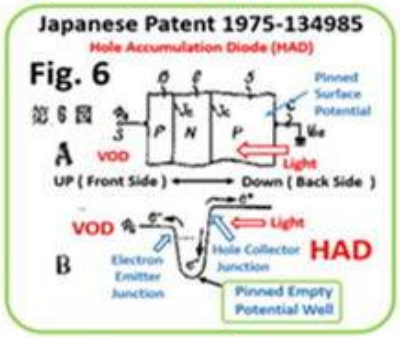
PNPN junction Transistor type Pinned Photodiode

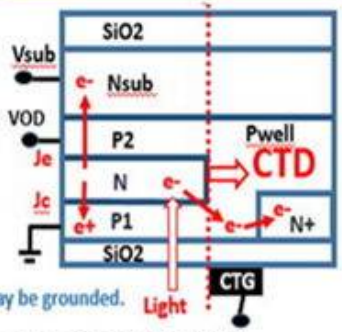
Visit https://www.j-platpat.inpit.go.jp/ and put the patent number 1975-134985

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

Patent Claim in English Translation

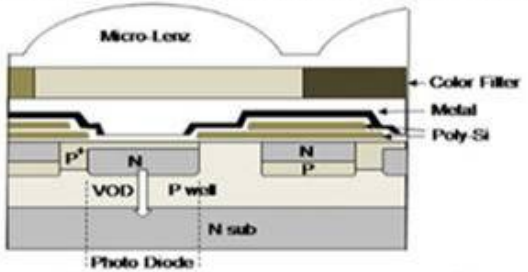
(1) In the semiconductor substrate (Nsub), the first region(P1) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N) is is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N) . And (6) Collector junction (Jc) is formed by the second region (N) and the first region (P1), forming a transistor structure (P2NP1) (7) Photo charge is stored in the Base region (N) according to the illuminated light intensity, and transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.





Yoshiaki Hagiwara, Japanese Patent JP 1975-134985

Most CCD Image sensors and CMOS Image sensors today are applied with the combination of the vertical overflow drain (VOD) and Pinned Photodiode.



In 1975 Yoshiaki Hagiwara at Sony proposed using a PNP transistor as the photodetector which is the combination of the VOD and Pinned Photodiode.

By providing a P + layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated, greatly improving the light sensitivity. This P + layer was also a proposal to reduce the dark current and image lag which became the basis of the pinned photodiode

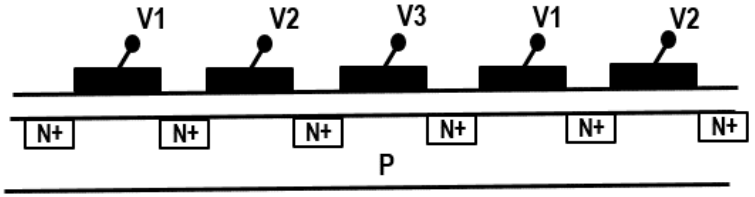
https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

Double Junction Dynamic Photo Transistor (PPD) invented in 1975 by Hagiwara at Sony.

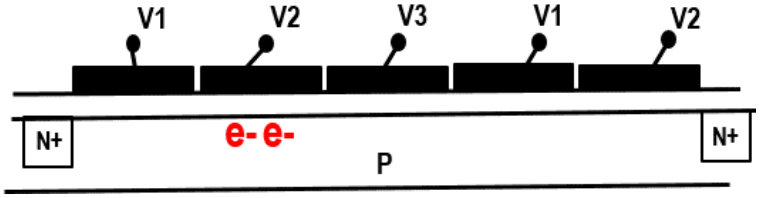
Triple Junction Dynamic Photo Thyristor (HAD) invented in 1975 by Hagiwara at Sony.

See Japanese Patent Application JPA 1975-127646, 1975-127647 and 1975-134985

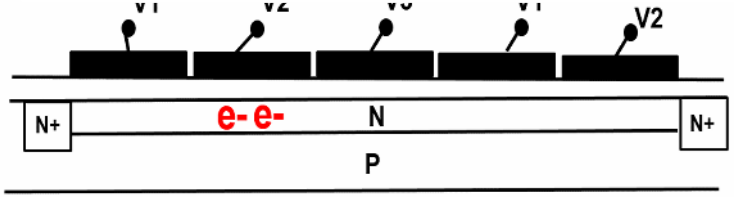
(1) Bucket Brigate Device (BBD)



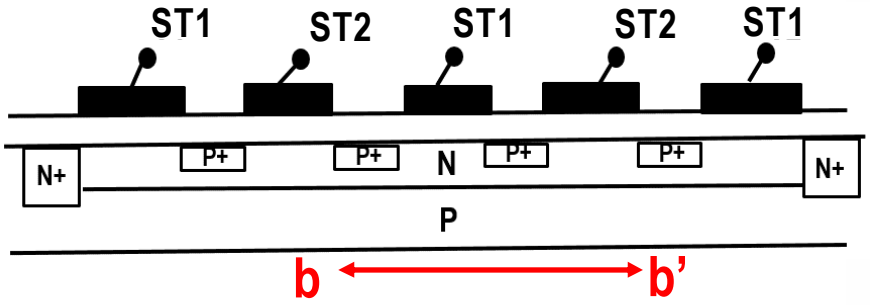
(2) Surface Channel CCD



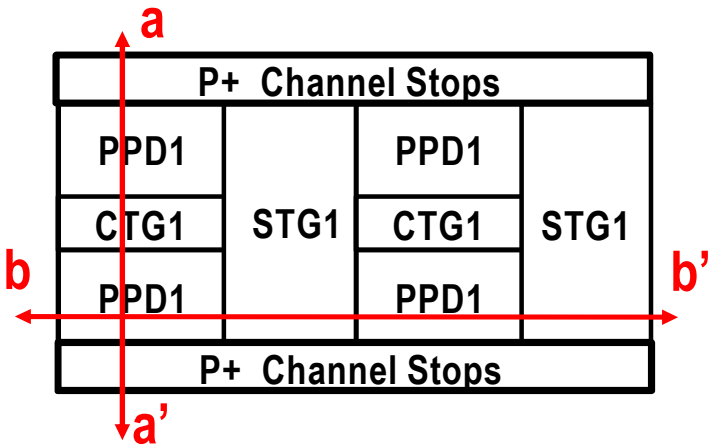
(3) Buried Channel CCD



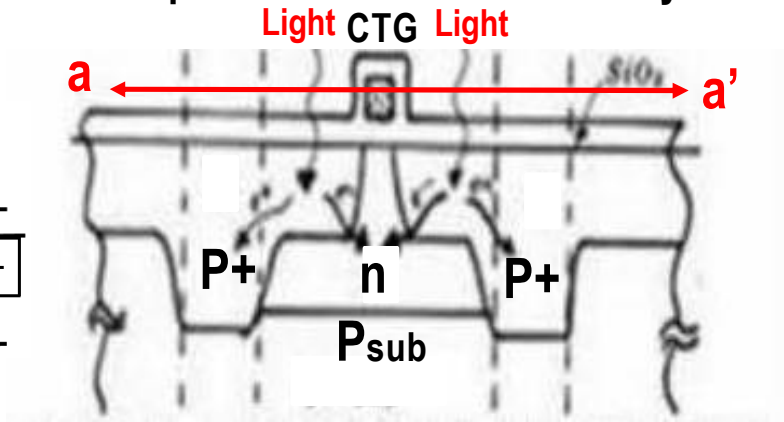
(3) Pinned Photodiode reported at SSDM 1978



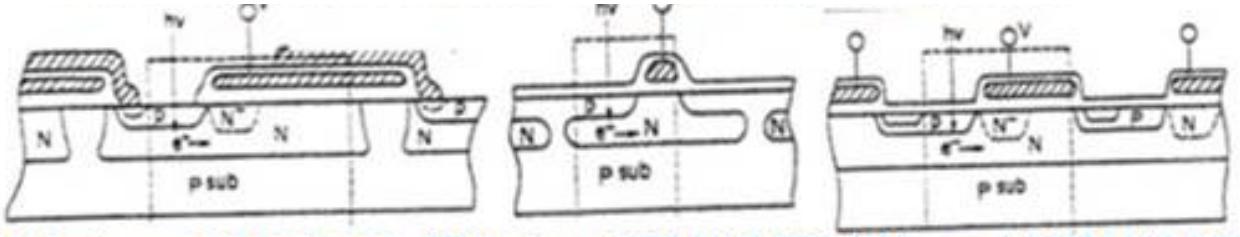
Narrow Charge Transfer Gate (CTG) and Pinned Photodiode (PPD) with the adjacent P+ channel stops



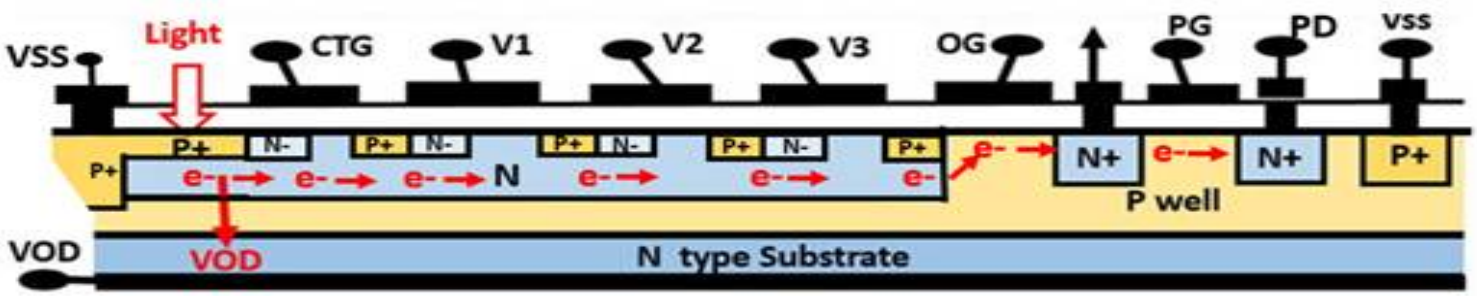
The first Pinned Photodiode(PPD) developed in 1978 by Hagiwara and reported at SSDM1978 in Tokyo.



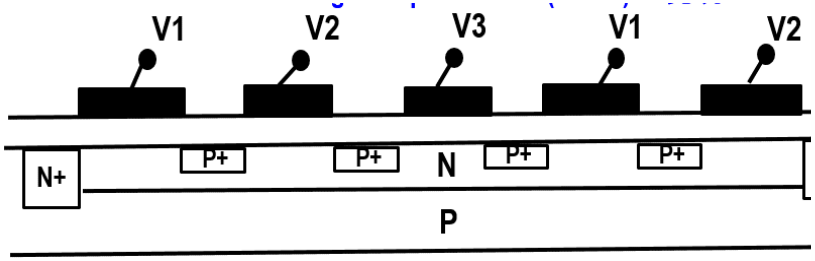
The most important idea of the P+NP Double Junction Buried Pinned Photodiode proposed by Hagiwara in the 1975-134985 Japanese Patent Application is the virtual complete charge transfer operation with no image lag which does not need the conventional double polysilicon overlapping CCD process with very poor productivity.

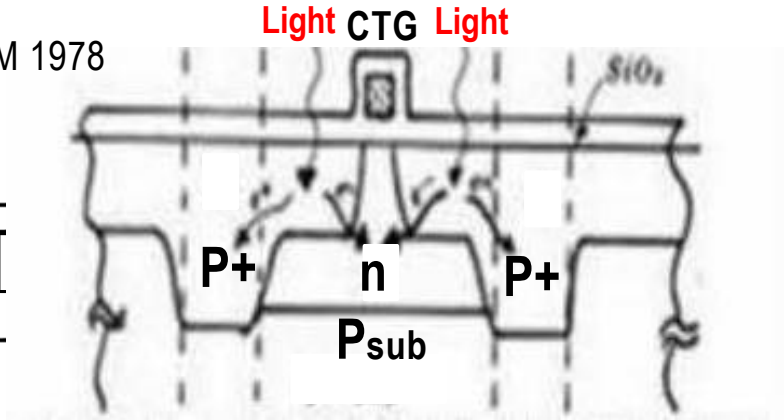


(1) Hagiwara 1975 P+NP PPD (2) Hagiwara 1978 P+NP PPD (3) Henecek 1979 P+NP PPD



Pinned Photodiode reported at SSDM 1978



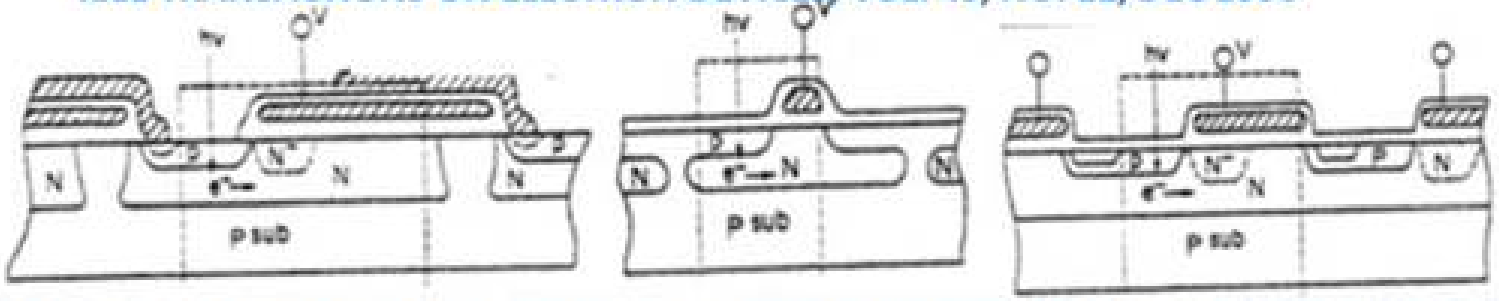


See the Japanese Patent 1975-134985 for the original invention of the Pinned Photodiode

High-Density and High-Quality Frame Transfer CCD Imager with Vey Low Smear, Low Dark Current, and Very High Blue Sensitivity

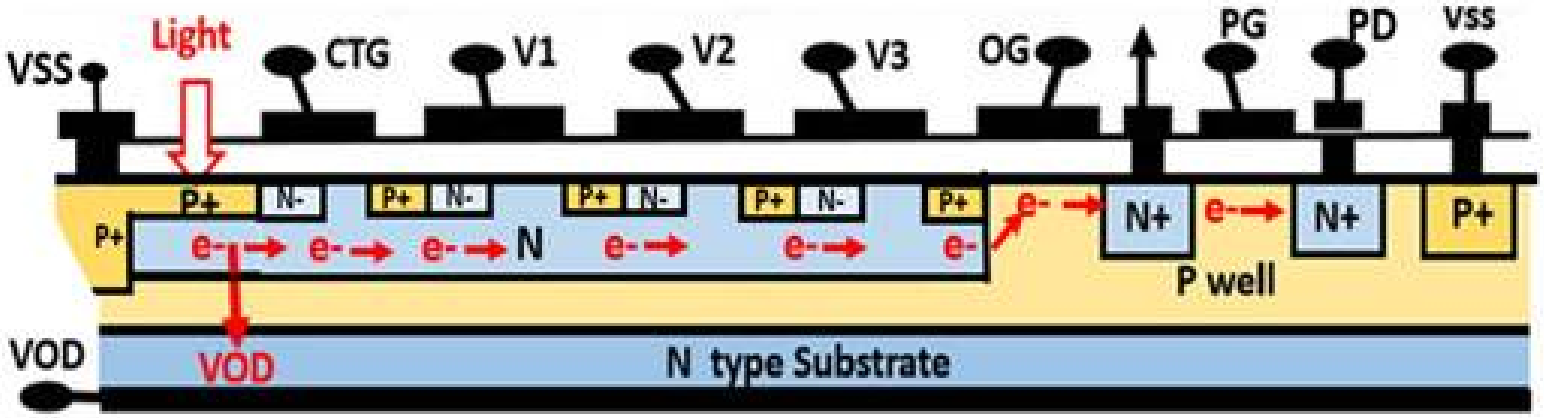
Yoshiaki Hagiwara

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 43, NO. 12, DEC 1996



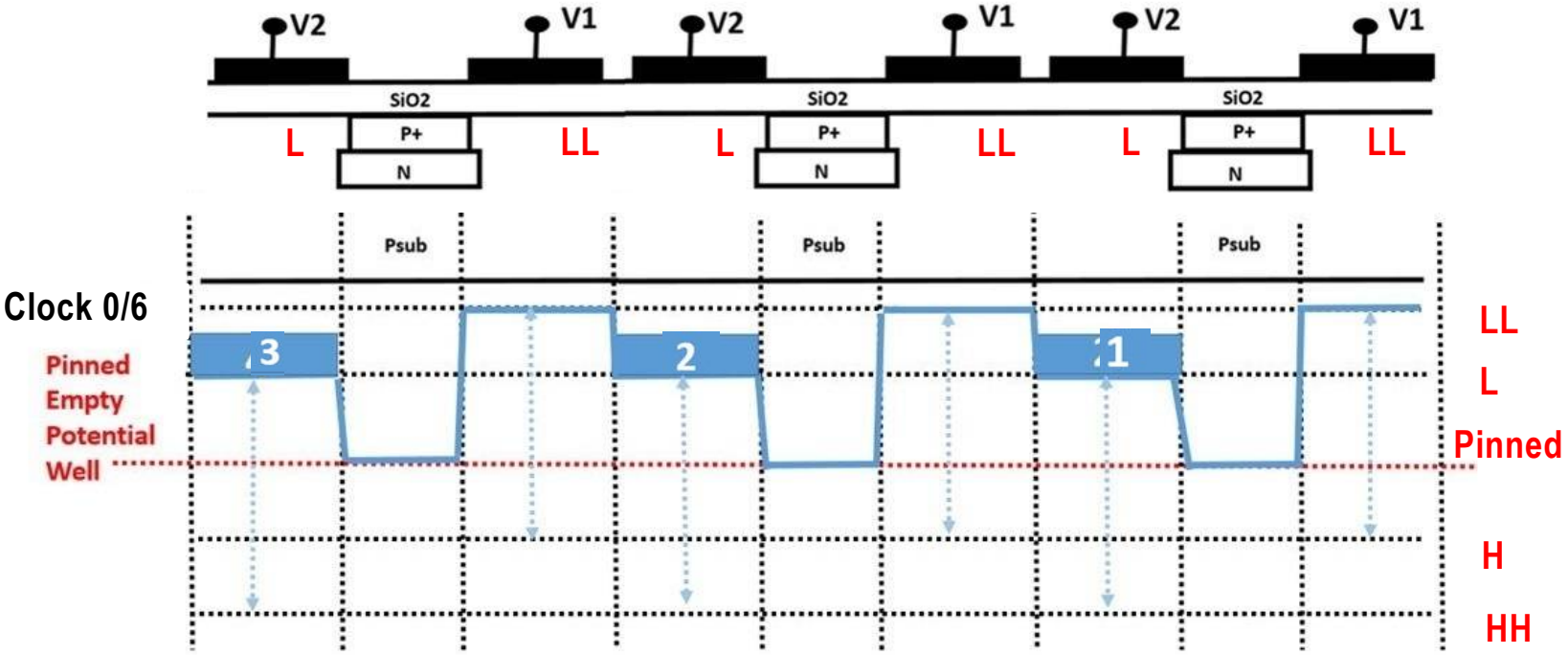
(1) Hagiwara 1975 P+NP PPD (2) Hagiwara 1978 P+NP PPD (3) Henecek 1979 P+NP PPD

The most important idea of the P+NP Double Junction Buried Pinned Photodiode proposed by Hagiwara in the 1975-134985 Japanese Patent Application is the virtual complete charge transfer operation with no image lag which does not need the conventional double polysilicon overlapping CCD process with very poor productivity.



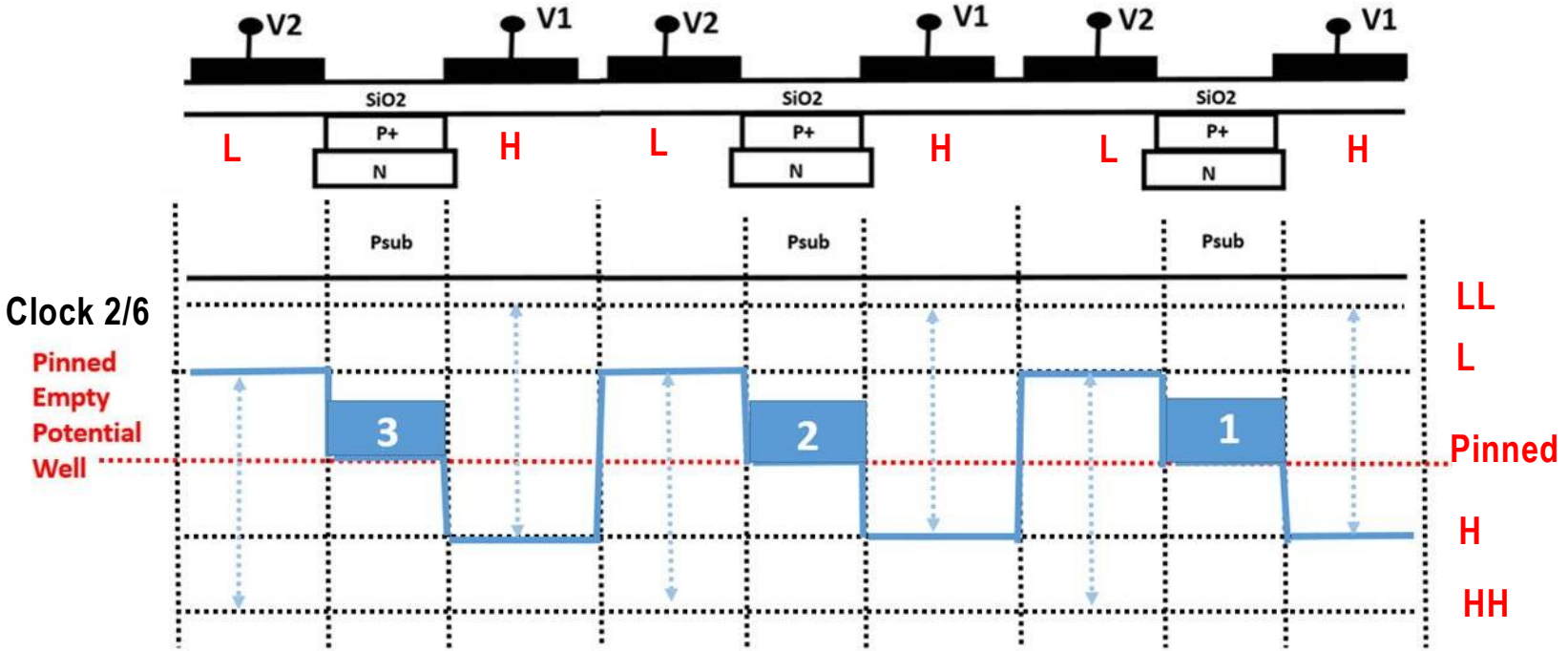
Hagiwara_invented_PPD_and_Virtual_Charge_Transfer_in_1975

Hagiwara in 1975 proposed the PPD Charge Transfer which is later called as Virtual Phase Charge Transfer.
Hagiwara in 1975 proposed also the NEC Buried Photodiode, the KODAK PPD and the Sony HAD.
Study Japanese Patent 1975-127646, 1975-127647 and 1975-134985 for the details.



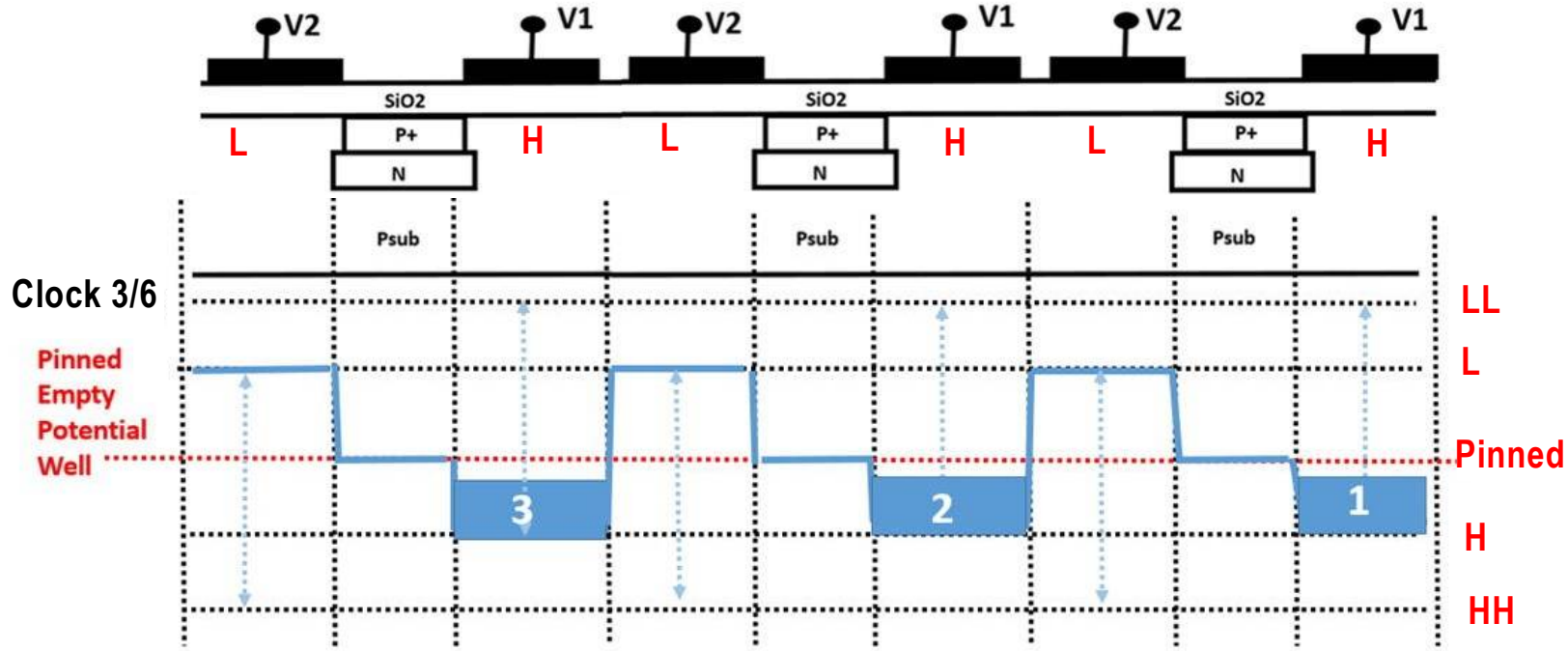
Hagiwara_invented_PPD_and_Virtual_Charge_Transfer_in_1975

Hagiwara in 1975 proposed the PPD Charge Transfer which is later called as Virtual Phase Charge Transfer.
Hagiwara in 1975 proposed also the NEC Buried Photodiode, the KODAK PPD and the Sony HAD.
Study Japanese Patent 1975-127646, 1975-127647 and 1975-134985 for the details.



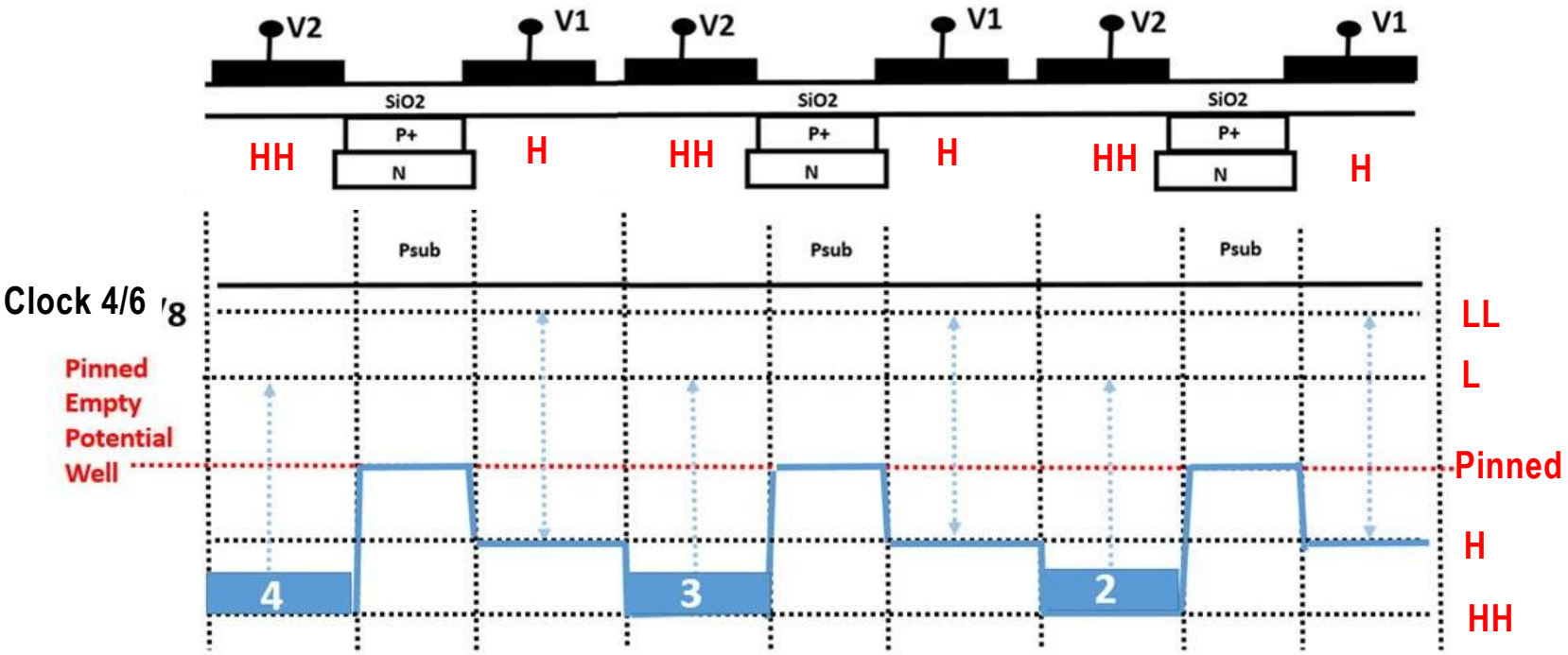
Hagiwara_invented_PPD_and_Virtual_Charge_Transfer_in_1975

Hagiwara in 1975 proposed the PPD Charge Transfer which is later called as Virtual Phase Charge Transfer.
Hagiwara in 1975 proposed also the NEC Buried Photodiode, the KODAK PPD and the Sony HAD.
Study Japanese Patent 1975-127646, 1975-127647 and 1975-134985 for the details.



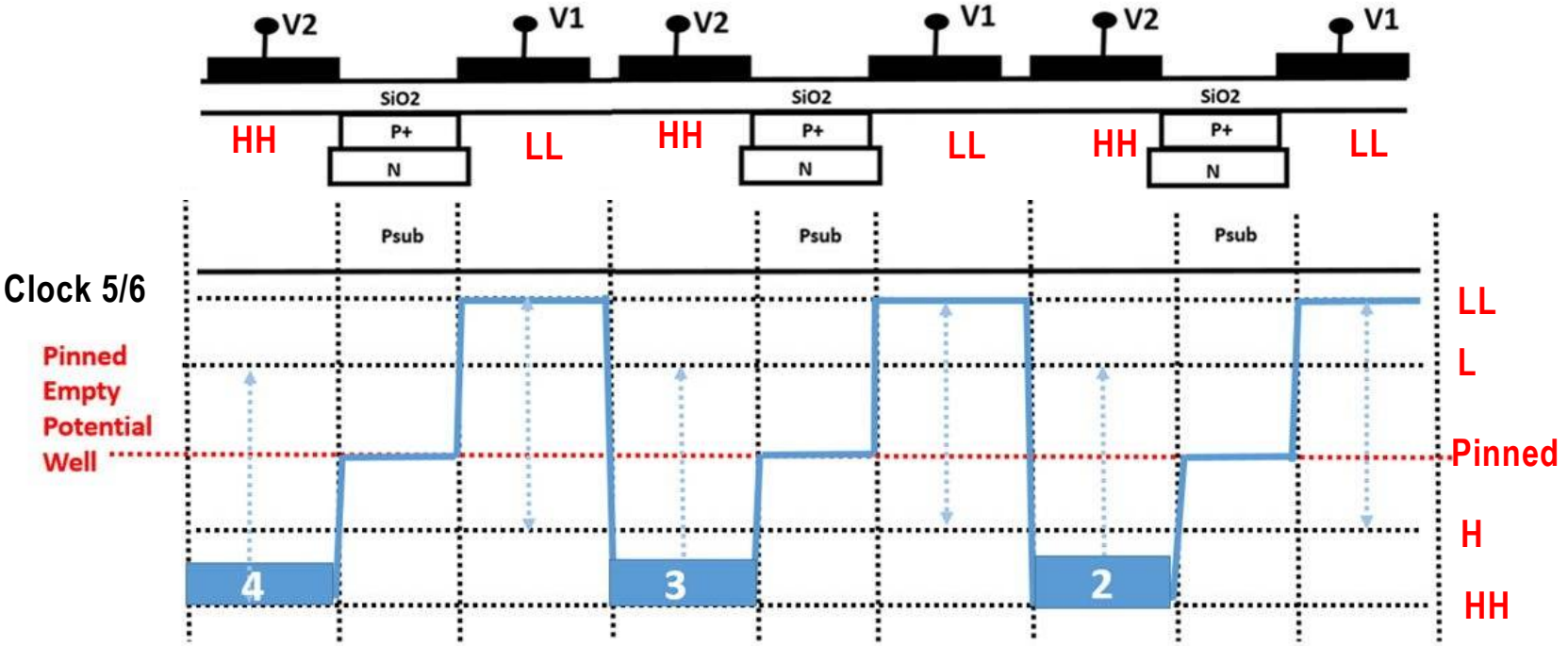
Hagiwara_invented_PPD_and_Virtual_Charge_Transfer_in_1975

Hagiwara in 1975 proposed the PPD Charge Transfer which is later called as Virtual Phase Charge Transfer.
Hagiwara in 1975 proposed also the NEC Buried Photodiode, the KODAK PPD and the Sony HAD.
Study Japanese Patent 1975-127646, 1975-127647 and 1975-134985 for the details.



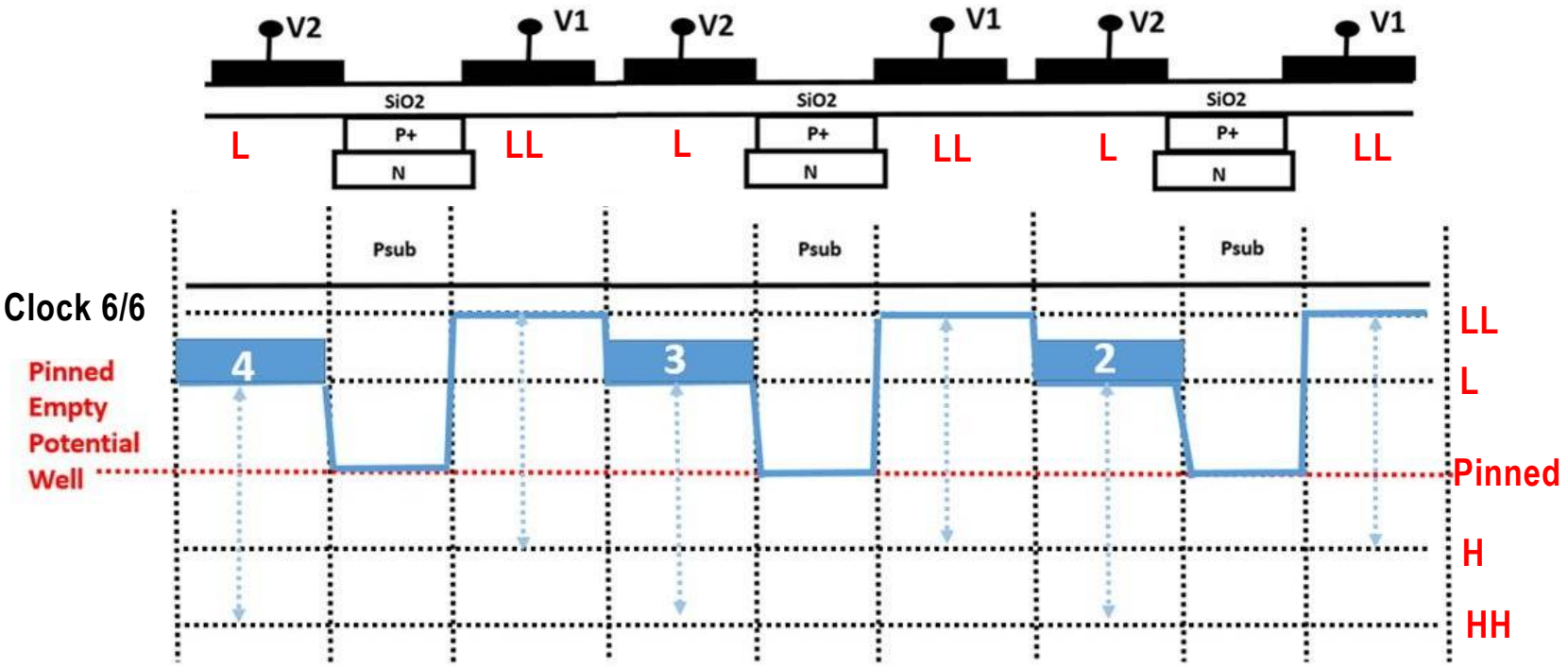
Hagiwara_invented_PPD_and_Virtual_Charge_Transfer_in_1975

Hagiwara in 1975 proposed the PPD Charge Transfer which is later called as Virtual Phase Charge Transfer.
Hagiwara in 1975 proposed also the NEC Buried Photodiode, the KODAK PPD and the Sony HAD.
Study Japanese Patent 1975-127646, 1975-127647 and 1975-134985 for the details.

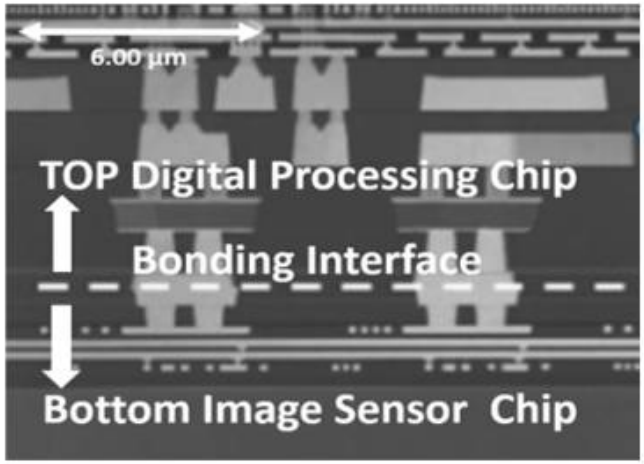


Hagiwara_invented_PPD_and_Virtual_Charge_Transfer_in_1975

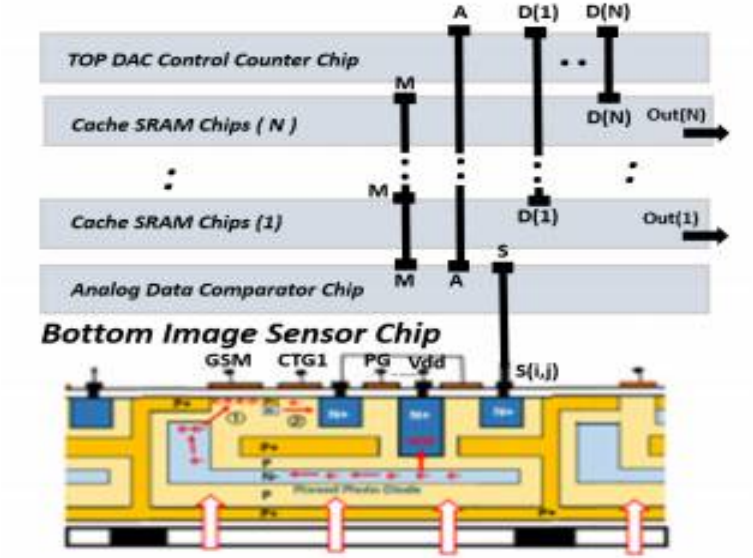
Hagiwara in 1975 proposed the PPD Charge Transfer which is later called as Virtual Phase Charge Transfer.
Hagiwara in 1975 proposed also the NEC Buried Photodiode, the KODAK PPD and the Sony HAD.
Study Japanese Patent 1975-127646, 1975-127647 and 1975-134985 for the details.



Back Light Illumination
Sony CMOS Image Sensor (2020)

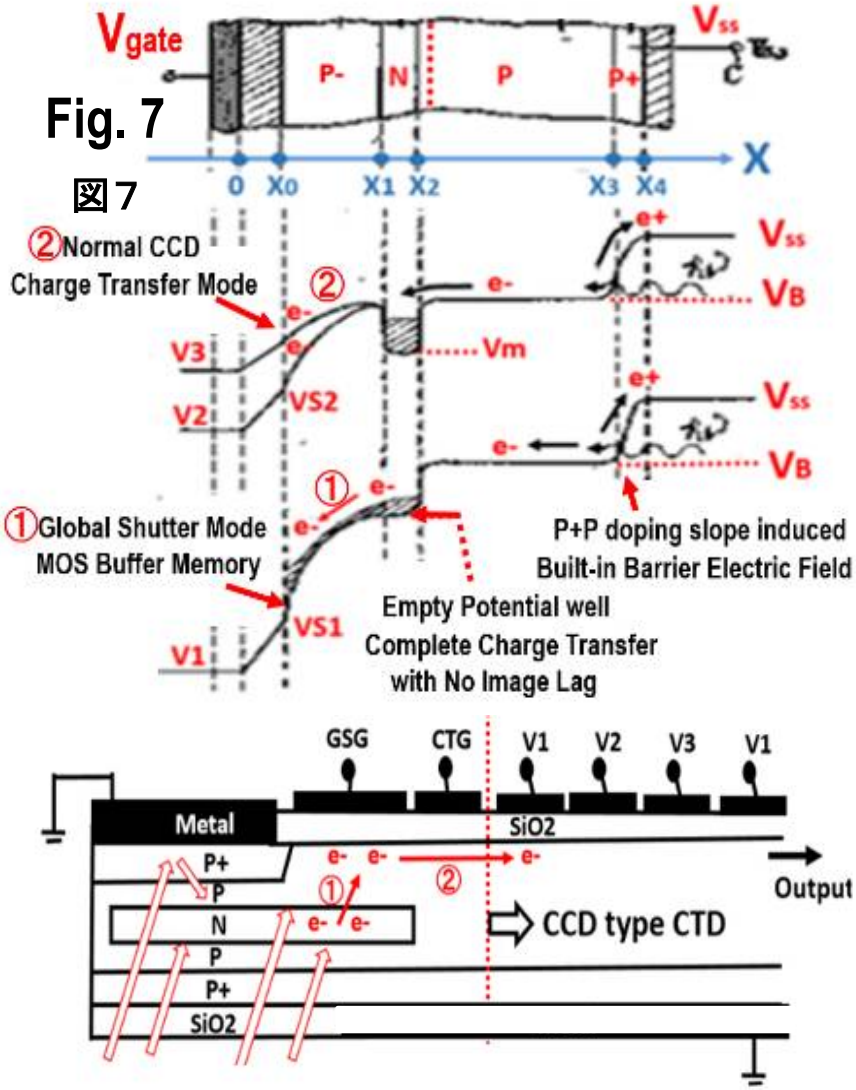


Multi-chips three dimensional LSI chip

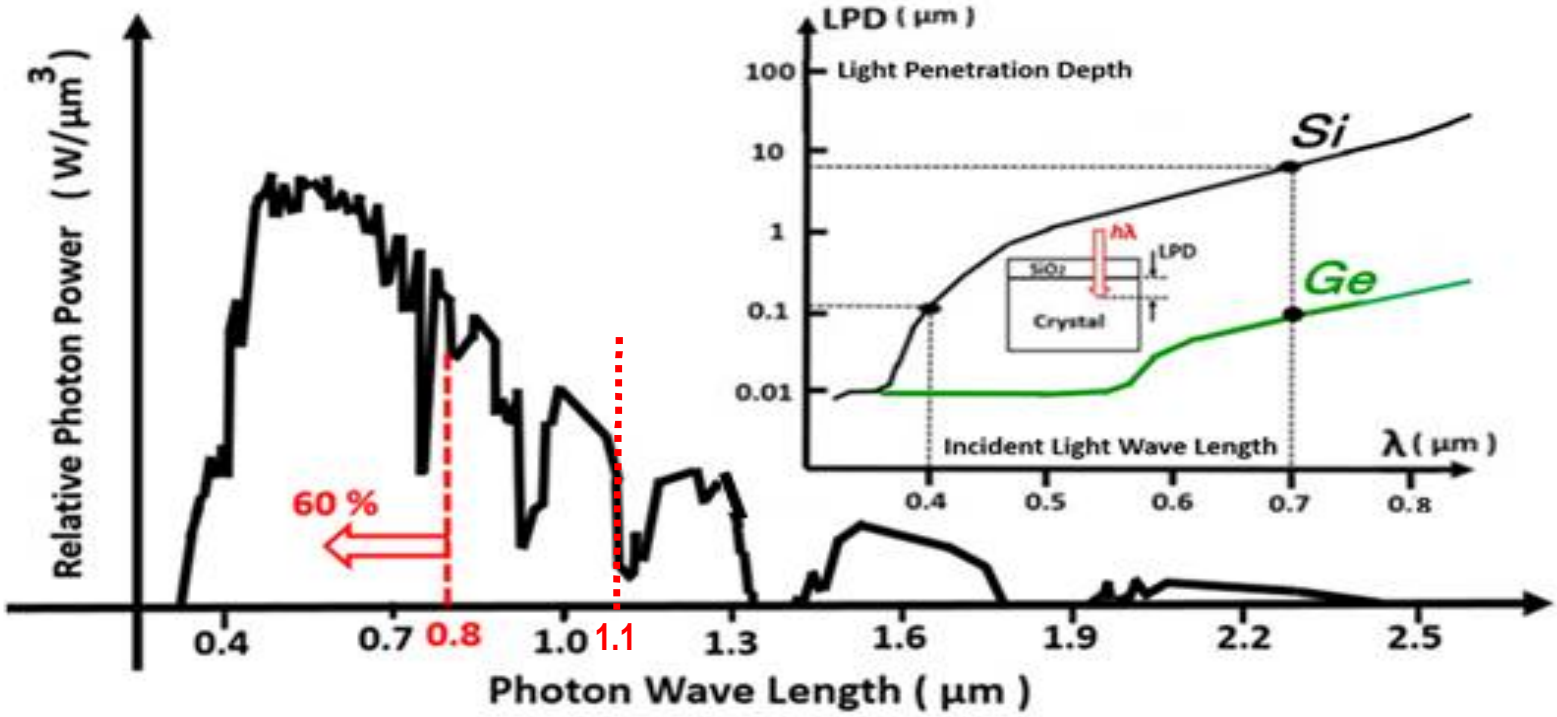


P+PNPP+ Junction Buried Pinned Photodiode
for Back Light (JAP 1975-127647)

Fig. 7
図7



Sun Light Spectrum

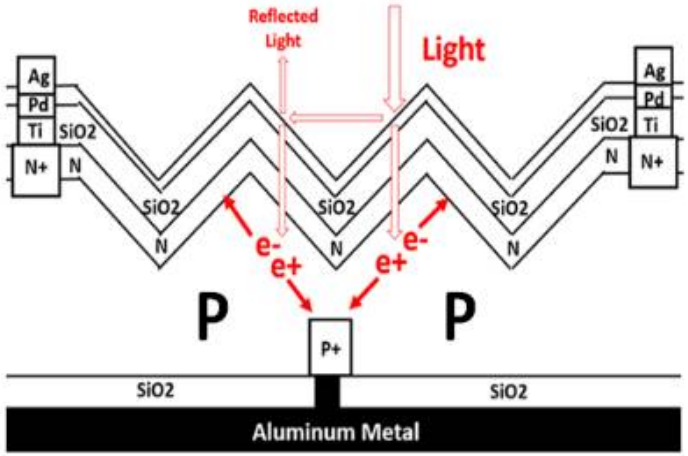


$$E = \hbar\omega = h f = h c / \lambda$$
$$E\,(eV) = 1.24 / \lambda\,(\mu m)$$

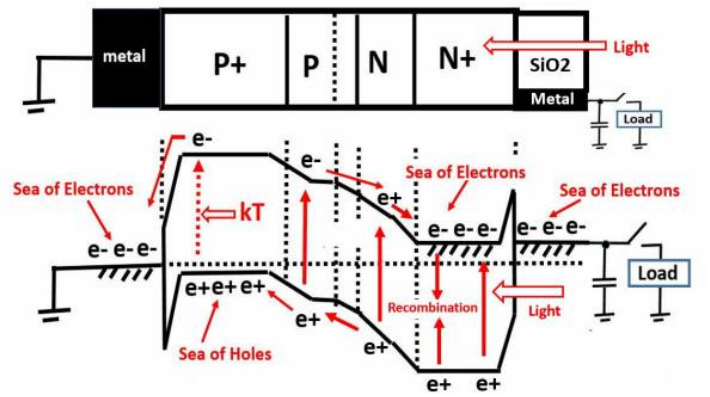
For Silicon, E_G = 1.10 eV and λ = 1.12 μm

The light energy of the wave length more than λ = 1.12 μm can not be converted to electrical energy in the silicon crystal.

Conventional N+P Single junction Type Solar Cell

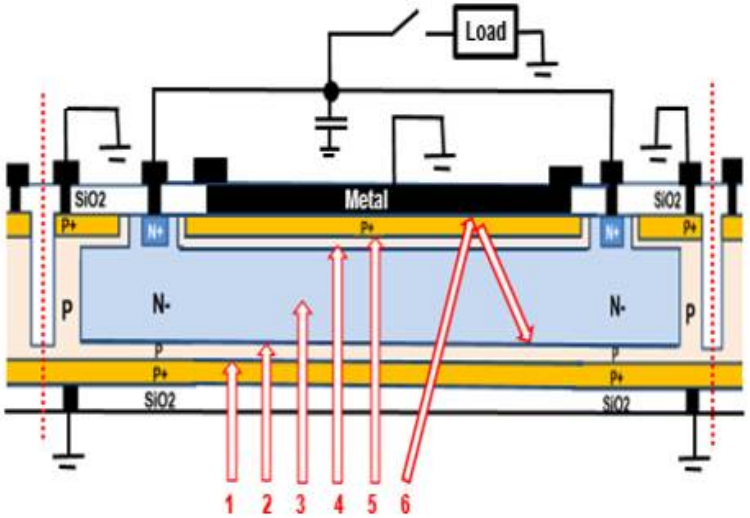


Poor Blue Light Sensitivity Problem

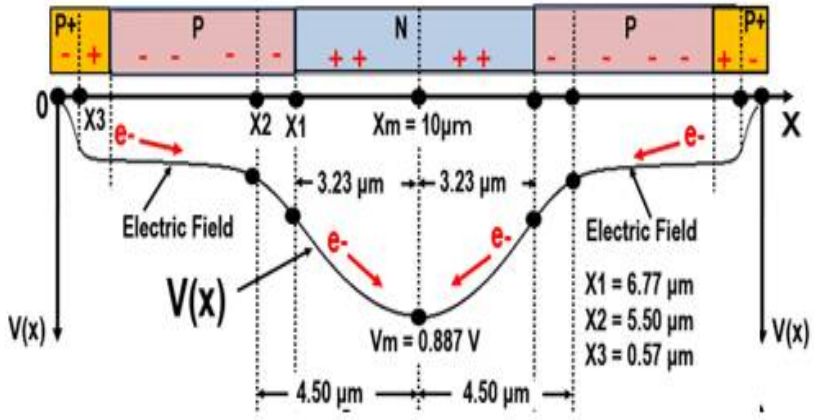


Single Junction N+P type Solar Cell also has a very poor short wave blue light sensitivity.

PNP Double Junction Type Solar Cell proposed by Hagiwara in 2020

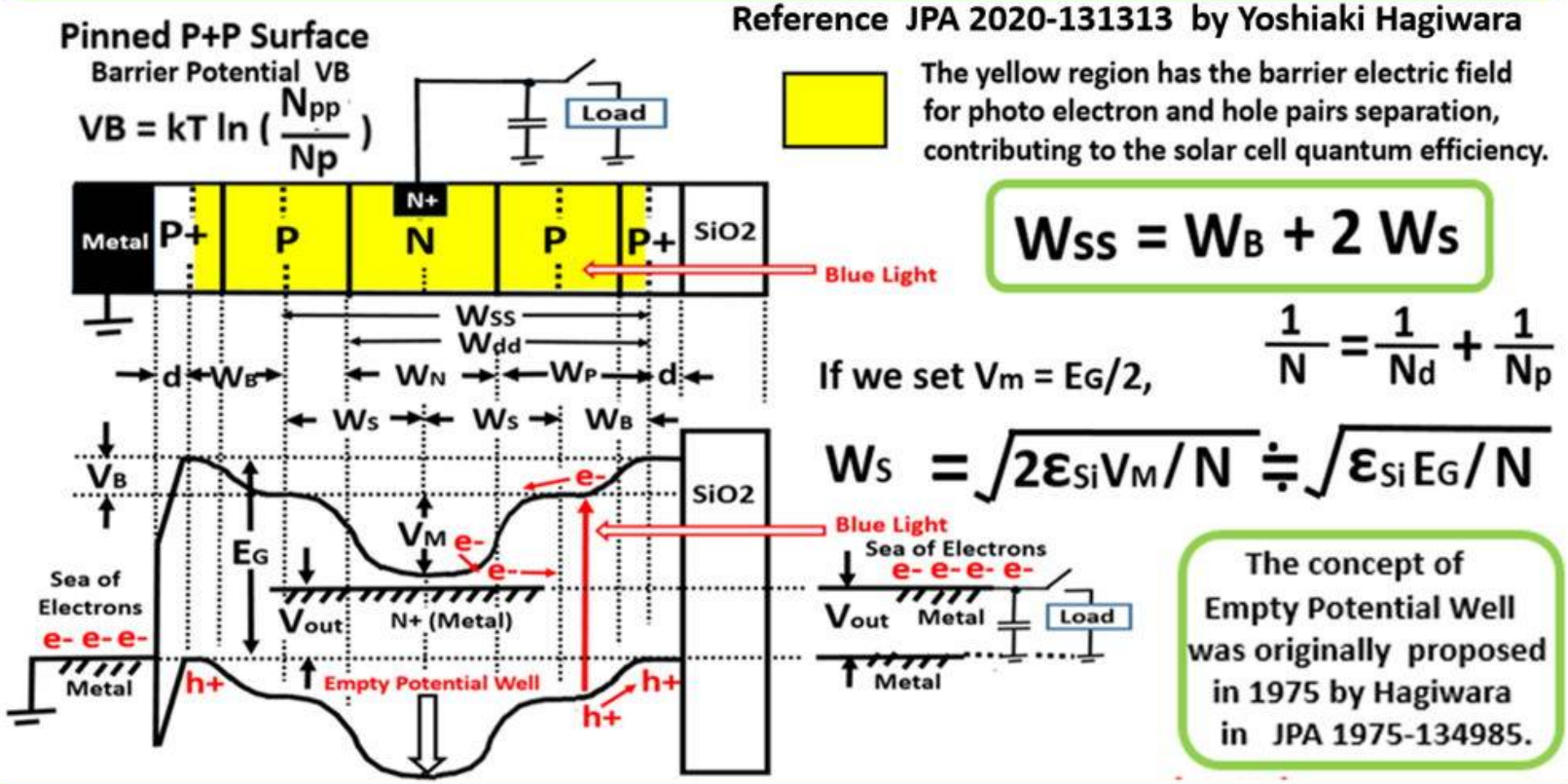


Completely depleted Buried N region In the PNP Double Junction Type Solar Cell proposed by Hagiwara in 2020



The P+PNPP+ Junction Type Pinned Photodiode Solar Cell with Very High Blue Light Sensitivity

Reference JPA 2020-131313 by Yoshiaki Hagiwara



The yellow region has the barrier electric field for photo electron and hole pairs separation, contributing to the solar cell quantum efficiency.

$$W_{SS} = W_B + 2\,W_S$$

If we set $V_m = E_G/2$,

$$\frac{1}{N} = \frac{1}{N_d} + \frac{1}{N_p}$$

$$W_S = \sqrt{2\varepsilon_{Si} V_M / N} \doteqdot \sqrt{\varepsilon_{Si} E_G / N}$$

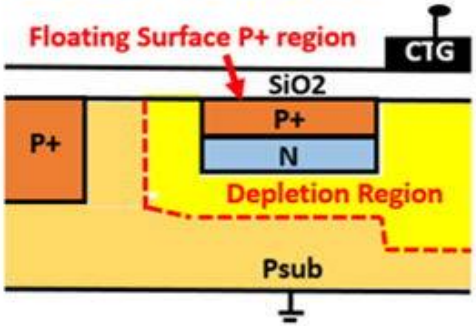
The concept of Empty Potential Well was originally proposed in 1975 by Hagiwara in JPA 1975-134985.

The surface P+P Pinned Surface Solar Cell with the surface P+P Gaussian doping slope is very important to create the surface barrier electric field for separating the photo electron and hole pairs generated by the short wave length blue light which cannot penetrate into the silicon crystal more than 0.2 μm in depth.

Difference of Buried Photodiode and Pinned Photodiode

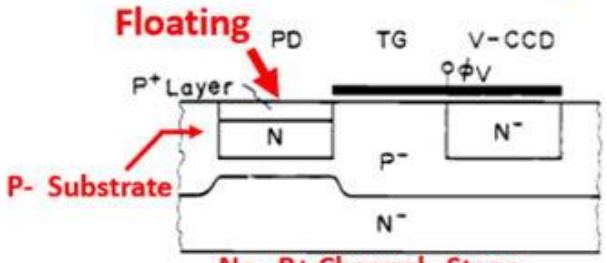
Figure 5 does not have the P+ channel stop nearby.

Buried Photodiode



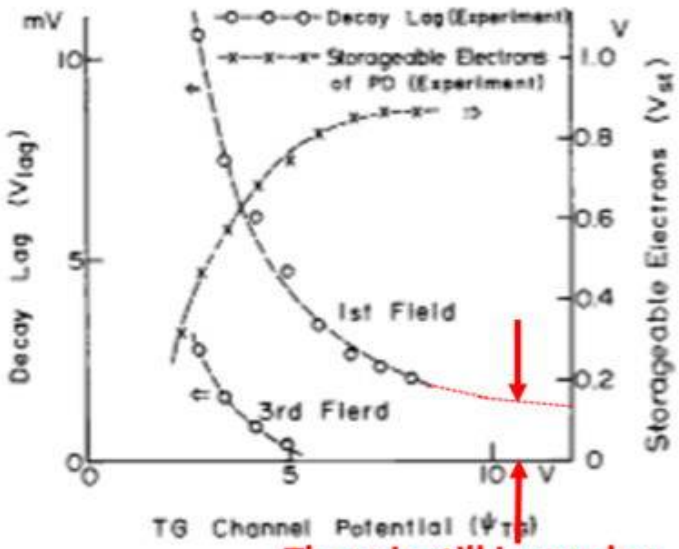
Serious Image Lag Problem

NEC IEDM1982 Paper



No P+ Channel Stops

Fig.5. P⁺NP⁻ structure photodiode
(a) Unit cell cross sectional view



There is still image lag
at the CTD gate voltage more than 10 volt.

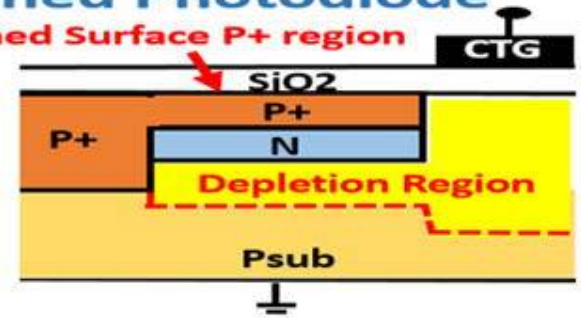
Fig.6. Storageable electrons vs. transfer gate channel potential, and decay lag vs. transfer gate channel potential in the P⁺NP⁻ structure photodiode

NEC IEDM1982 Paper reported Image Lag

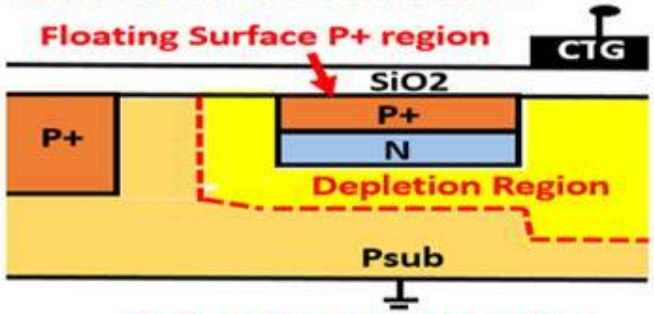
Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 volt.

Difference of Buried Photodiode and Pinned Photodiode

Pinned Photodiode



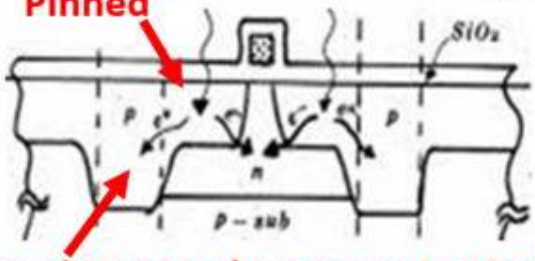
Buried Photodiode



Serious Image Lag Problem

SONY SSDM1978 Paper

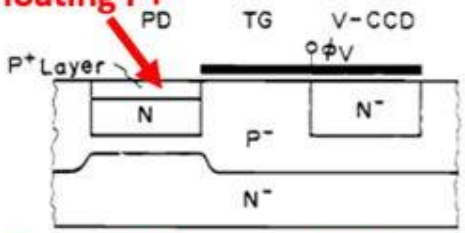
Pinned



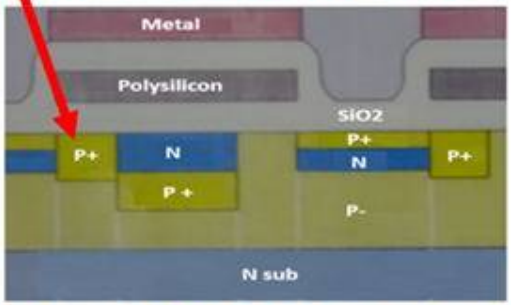
P+ Channel Stops and no Image Lag Problem

NEC IEDM1982 Paper

Floating P+

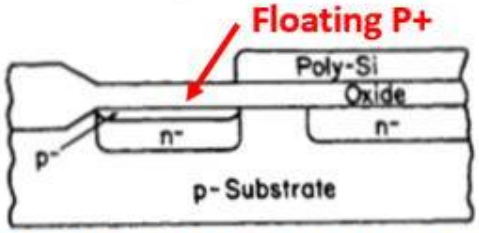


No P+ Channel Stops and Serious Image Lag



SONY 1987 HAD Sensor

Floating P+



KODAK IEDM1984 Paper

Difference of Pinned Photodiode and Buried Photodiode

Pinned Photodiode must have the P+ heavy doped channel stops nearby.

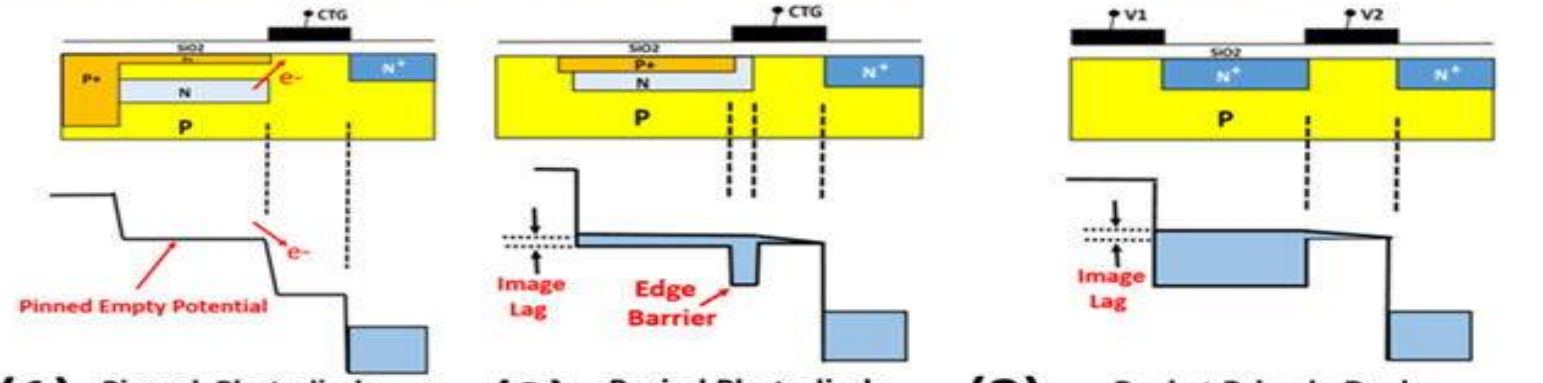
Pinned Photodiode must be a buried photodiode.

Pinned Photodiode must not have the edge barrier to the Charge Transfer Gate

Pinned Buried Photodiode does not have the edge barrier

Buried Photodiode with the edge barrier

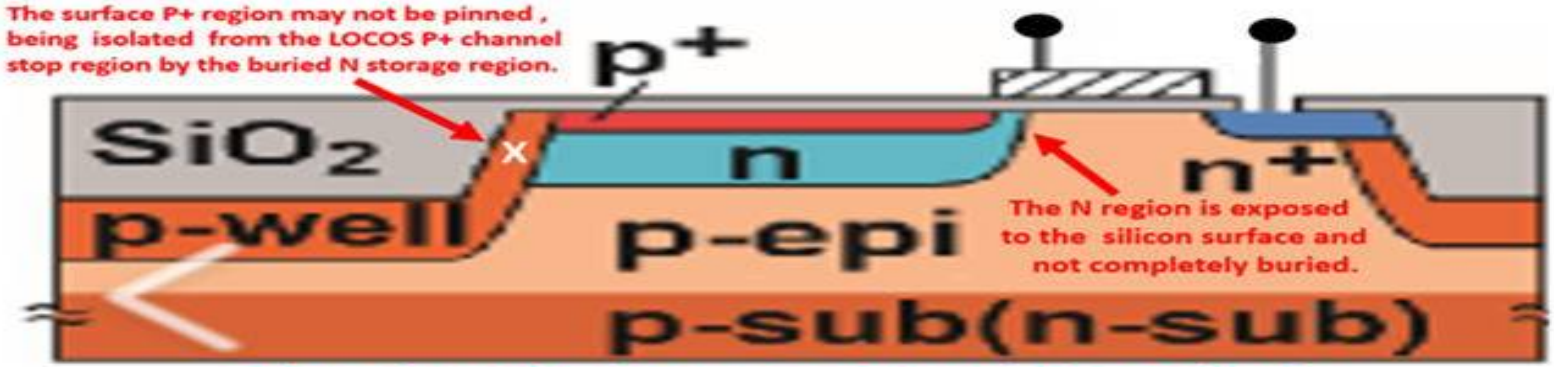
Bucket Bridgade Device (BBD) with Serious Image Lag



(1) Pinned Photodiode with No Image Lag

(2) Buried Photodiode with BBD Barrier

(3) Bucket Brigade Device (BBD)



This photodiode is not Pinned Photodiode since the N storage region is not completely buried.

Albert J.P. Theuwissen, Jan T.J. Bosiers, Edwin Roks, " The Hole Role ", an invited paper at IEDM2005, Washington DC, Techn. Dig. , 2005.

But in the case that parts of the depleted n-type CCD channels are not covered by gate material, their surface potential is undefined ! Such a structure will suffer from charge transport issues during operation, because charge can be trapped in local potential pockets. The effect can be solved by defining the potential in the open areas through an extension of the p^+ channel stopper. A simple self-aligned implant of $2x10^{13}$ /cm^2 boron ions is sufficient to extend the channel stop areas to the gate edge and consequently fix the potential in the open areas [2]. The result after this self-aligned implant is shown in Figure 3. The presence of enough holes plays a crucial role in fixing the potential for the regions "beyond control" of the gates. (Is this structure the mother of the pinned-photodiode or buried diode or hole-accumulation device ?)

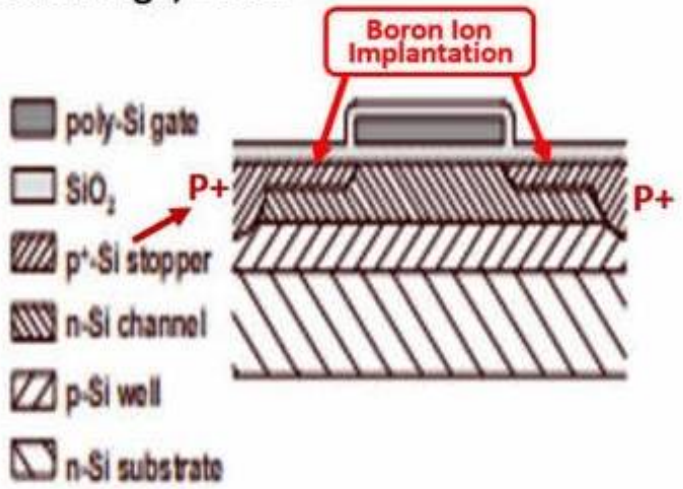


Figure 3. Cross section of a buried-channel CCD on n-Si substrate including light windows and pinned interface potential in the non-covered CCD channels (the cross section is made perpendicular to the CCD channel).

[2] Y. Daimon-Hagiwara et.al., Proc. 10th Conf. on Solid-State Devices, Tokyo, 1978, pp.335-340.

Fossum insulted in his 2014 paper Sony and Hagiwara 1975 PPD invention.

Indeed, Hagiwara invented PPD with VOD and the virtual charge transfer in 1975 !!

IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY, VOL. 2, NO. 3, MAY 2014 33

Sony HAD (PPD+VOD) does not use LOCOS !!!

A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, *Fellow, IEEE*, and Donald B. Hondongwa, *Student Member, IEEE*

Many people now said this is a fake paper !

False

C. Other Contributions to the PPD Invention

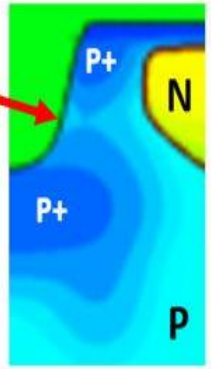
The PPD structure, while invented for low lag ILT CCD application, shares a strong resemblance to the Hynecek virtual-phase CCD structure, with the exception of the VOD. The two inventions were solving different problems with essentially the same device structure and operating principles.

In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a *pnp* vertical structure was disclosed, among several structures [24]. The top *p* layer was connected by metal to a bias used to control full-well capacity and the *n*-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1996, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called "Hole Accumulation Diode," or HAD structure [25]. However, the 1975 application did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the NEC paper was published. However, the "narrow-gate" CCD with an open *p*-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

The PPD, as it is most commonly used today, bears the strongest resemblance to the Teranishi et al. ILT CCD device. Thus, these days Teranishi is considered as the primary inventor of the modern PPD [29].

False

The surface P+ layer is NOT connected to the LOCOS P+ layer. The surface P+ layer may be floating and this photodiode may have serious image lag.



Serious Image Lag ?

NOT connected

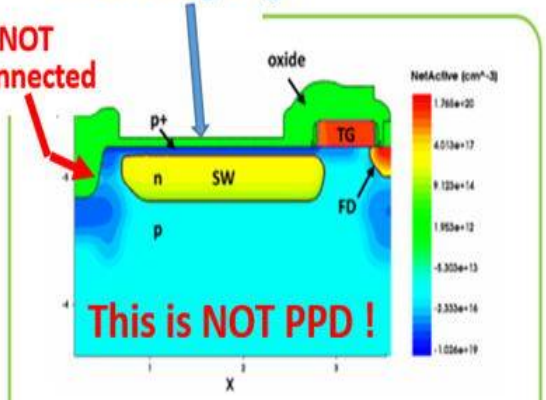


Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

Hagiwara in 1975 invented PPD with VOD and the virtual charge transfer.

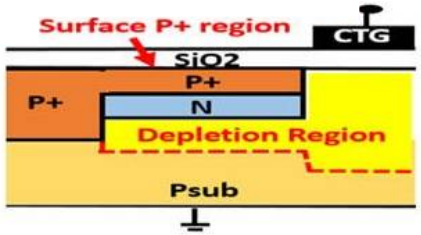
Study the Japanese Patents 1975-127646, 1975-127647 and 1975-134985.

ELECTRICALENGINEERING

Difference between Buried Photodiode and Pinned Photodiode

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode



In 1975 the first PPD was invented by Hagiwara at Sony and used in ILT CCD PDs by Hamazaki at Sony in 1987.

PPD must have the P+ channel stops nearby to pin the surface P+ layer.

This is a commonly misunderstood misused set of terminologies.

First off these are not PIN Photodiodes - which stands for P - Intrinsic- N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though.

Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space.

You can get surface state pinning from the dangling Si/SiO2 bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The Si/SiO2 surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface.

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

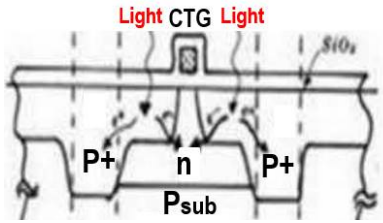
Semiconductor History Museum of Japan

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

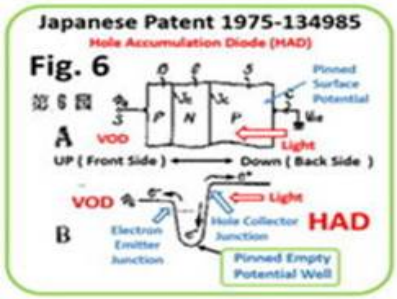
In 1975, Sony proposed using a PNP transistor as the photodetector [3]. By providing a P + layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated, greatly improving the light sensitivity. This P + layer was also a proposal to reduce the dark current and image lag which became the basis of the pinned photodiode.

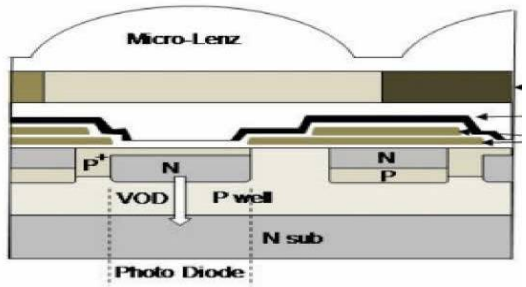
In 1978, Sony presented a 93,000-pixel FT (Frame Transfer) -CCD image sensor compliant with the Analog TV Broadcasting Standard (SDTV) for the first time in the world [5], using the photodiode with the same structure as above. Sony succeeded in 1981 in trial production of a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor by further improvement of this technology [6].

The Pinned Photodiode is a photodiode in which the entire N layer is covered with a P layer. The part of the P layer on the light incident surface is heavily doped P+ (Fig-1). Kodak named this structure Pinned Photodiode in 1984 because the P + surface of the light incident surface was pinned to the substrate potential. This device has features such as high light sensitivity, wide dynamic range, image lag free, much smaller dark current due to reduced influence of GR center on the light receiving surface, and no white scars.



Pinned Photodiode reported at SSDM 1978





References:

【1】M. Hamasaki, T. Suzuki, Y. Kagawa, K. Ishikawa, K. Miyata and H. Kambe, "An IT-CCD imager with electronically variable shutter speed" , Technical Report of The Institute of Image Information and Television Engineers. vol. 12, no. 12, pp. 31-36, (1988)

【3】Y. Hagiwara, Japanese Patent JP1975—134985

【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

【6】I. Kajino, M. Shimada, Y. Nakada, Y. Hirata and Y. Hagiwara, "Single Chip Color Camera Using Narrow channel CCD Imager with Over Flow Drain"、Technical Report of The Institute of Image Information and Television Engineers、vol. 5, no. 29, pp.

SONY Products & Services About Sony Support / Contact Us Global

Japanese | English

Sony's Representative Inventions Supporting Stacked Multi-Functional CMOS Image Sensors

Sony Corporation
Sony Semiconductor Solutions Corporation

https://www.sony.net/SonyInfo/News/notice/20200626/

Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

References:

【1】M. Hamasaki, T. Suzuki, Y. Kagawa, K. Ishikawa, K. Miyata and H. Kambe, "An IT-CCD imager with electronically variable shutter speed" , Technical Report of The Institute of Image Information and Television Engineers. vol. 12, no. 12, pp. 31-36, (1988)

【3】Y. Hagiwara, Japanese Patent JP1975—134985

【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

【6】I. Kajino, M. Shimada, Y. Nakada, Y. Hirata and Y. Hagiwara, "Single Chip Color Camera Using Narrow channel CCD Imager with Over Flow Drain"、Technical Report of The Institute of Image Information and Television Engineers、vol. 5, no. 29, pp.

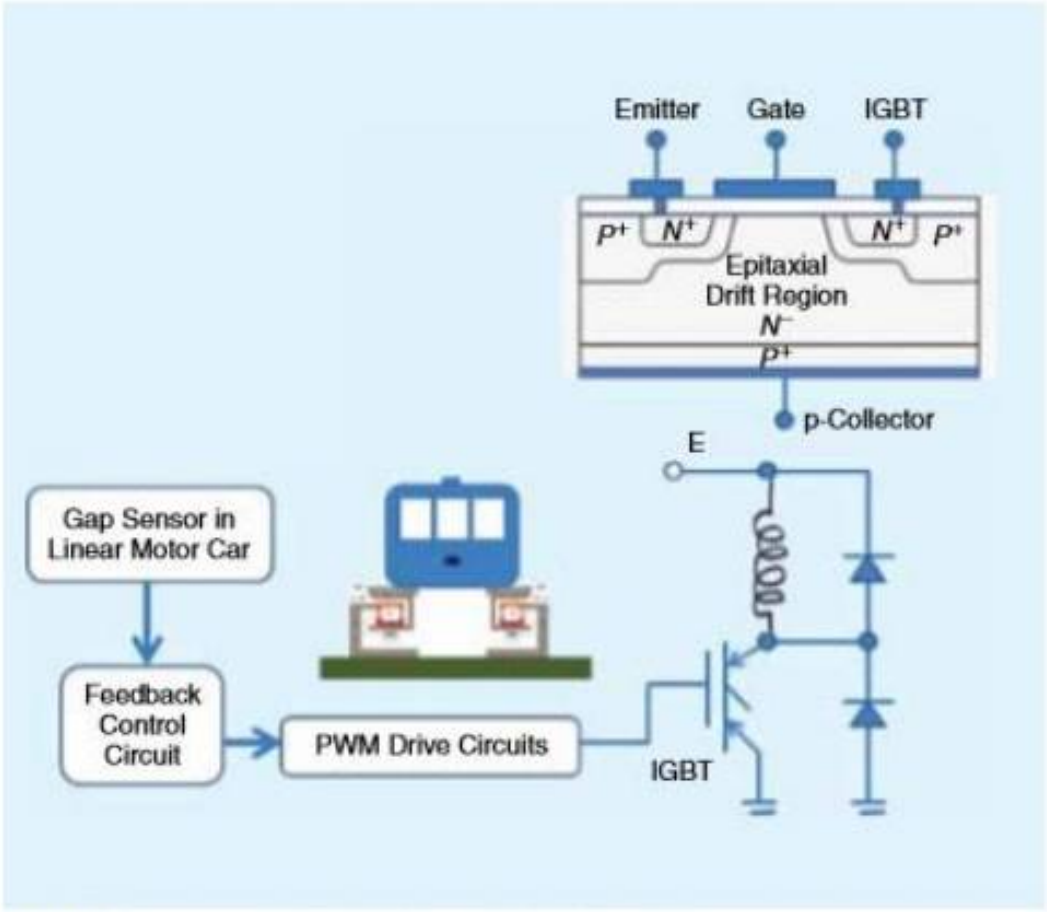
http://isscc.org/

Image Sensor Story

Yoshiaki Higihara: The p-n-p-n Diode in Future Linear Motor Cars and in Modern Imagers

John Louis Moll (1921–2011) was studying a p-n-p-n diode switch in his Ph.D. dissertation work when the first ISSCC was held in 1954. In a normal operation mode, this device works as a thyristor, which can drive a large current and is the key device structure of an IGBT applied for a linear motor car of the future (see Figure 9). In a dynamic operation mode, this device may work as a simple p-n-p-n dynamic capacitance that can detect and store one single electron, which is a key device structure of the modern image sensor (see Figure 10).

I recall, when I was taking his physics course at Caltech, that Feynman once said that an electron is always free, moving around rapidly in free space, even in solid, and it never stops. It is very hard to catch an electron because we do not know exactly where it is. Our civilization today is based on a technology that controls electrons, down to a single one.



URE 9: The p-n-p-n switch diode for a modern linear motor car.

Imagine a photon incident to a bipolar transistor base region. The photon energy creates an electron-hole pair. And the photo-electron can be stored in the base region as one single majority carrier. That is, a bipolar transistor can also function as a photon detector and/or a storage container. I thought that a room in a hotel must be empty and clean before the first hotel guest arrives. So must be this transistor base region empty and clean with no guest electrons at the beginning. This transistor in a dynamic p-n-p capacitor mode is useful since it can capture, confine, and control one single electron. But as a student, I did not know yet how to student, I did not know yet how to move that single photoelectron sitting in the base region to the outside world so that we can make use of it as a signal. I had no way yet to know whether the hotel guest has arrived and is resting in the hotel room or not. We had no way yet to ask the hotel guest to come up to the hotel lobby to meet me. I had to wait a few more years (until 1970

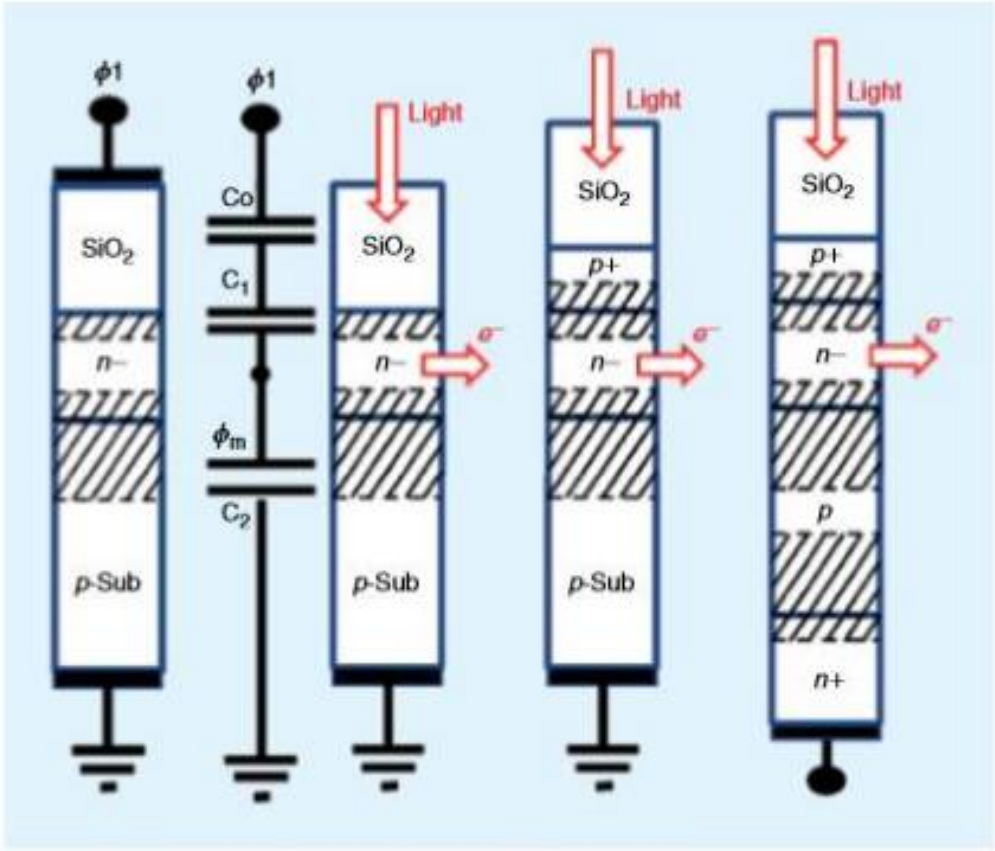
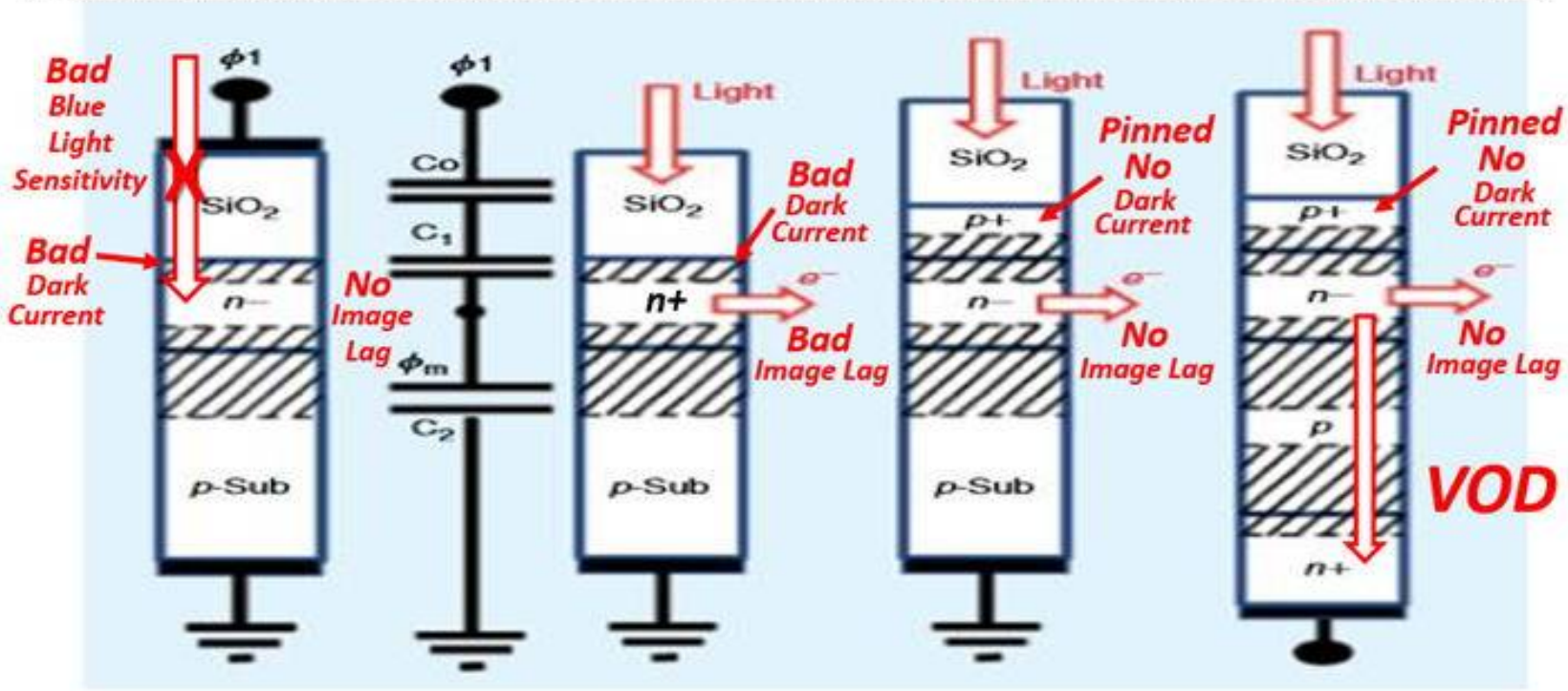


FIGURE 10: From CCD to the dynamic p-n-p-n diode capacitors.

in my senior year in college) to find the answer. We all know now it is the CCD structure that can store and transfer one single electron. With a precharge reset set gate and a source-follower circuit, a scheme invented by Walter Kosonocky. We could finally meet our hotel guest at the hotel lobby.

History of dynamic Solid State image sensing structure from BCCD type MOS capacitor to the P+NPN junction Pinned Photodiode capacitor



(1) CCD type invented by Bell Lab in 1968

(2) N+P type The classical photodiode with serious image lag

(3) P+NP type (4) P+NPN type (3) and (4) are the P+NP junction type Pinned Photodiode invented by Yoshiaki Hagiwara, 1975

In Japanese patent 1975-134985, Hagiwara at Sony invented the Pinned photodiode with very low dark current, which is also the completely depleted Buried Photodiode with image lag free picture quality, and also with the built-in vertical overflow drain (VOD) function.

Reference: IEEE Solid-STATE CIRCUITS MAGAZINE, SUMMER 2013 issue pp. 6～

Difference of the static and dynamic photo transistors are illustrated in these figures.

Sony Hole Accumulation Diode (HAD) is the P+NPNsub junction dynamic photo transistor with the surface P+ hole collecting and accumulation region is pinned and grounded, which is now widely called as Pinned Photodiode with the vertical overflow drain (VOD) function. Only Pinned Photodiode with the VOD function can realize the electrical shutter function.

SONY HAD Sensor 1975 was hinted by SONY PNP Bipolar Transistor Process Technology

Difference of the static and dynamic photo transistors are illustrated in these figures.

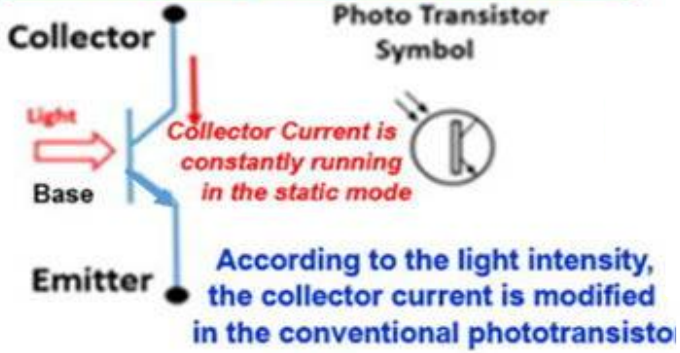
Sony Hole Accumulation Diode (HAD) is the P+NPNsub junction dynamic photo transistor with the surface P+ hole collecting and accumulation region is pinned and grounded, which is now widely called as Pinned Photodiode with the vertical overflow drain (VOD) function. Only Pinned Photodiode with the VOD function can realize the electrical shutter function.

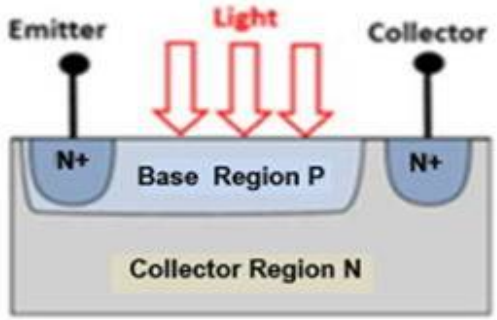
SONY HAD Sensor 1975 was hinted by SONY PNP Bipolar Transistor Process Technology

Conventional Static Phototransistor

(by John Northrup Shive , 1950)

No memory function is involved.





Difference of the static and dynamic photo transistors are illustrated in these figures.

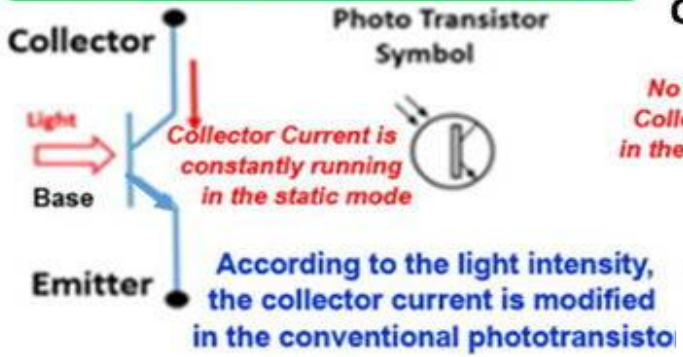
Sony Hole Accumulation Diode (HAD) is the P+NPNsub junction dynamic photo transistor with the surface P+ hole collecting and accumulation region is pinned and grounded, which is now widely called as Pinned Photodiode with the vertical overflow drain (VOD) function. Only Pinned Photodiode with the VOD function can realize the electrical shutter function.

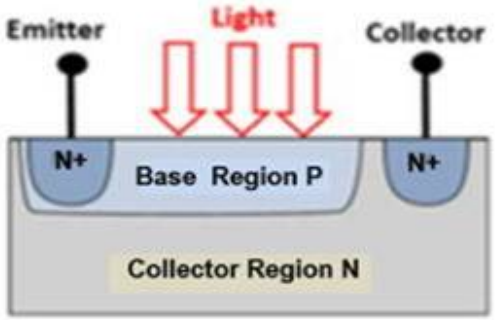
SONY HAD Sensor 1975 was hinted by SONY PNP Bipolar Transistor Process Technology

Conventional Static Phototransistor

(by John Northrup Shive , 1950)

No memory function is involved.

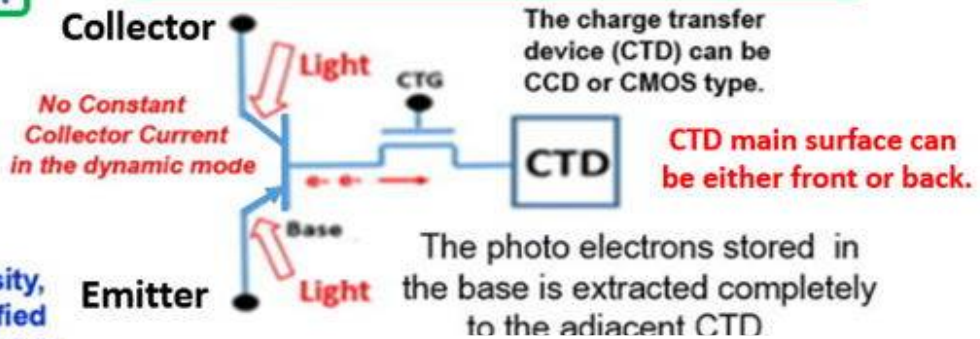




Dynamic Phototransistor Operation

by Yoshiaki Hagiwara at Sony in 1975

Dynamic Memory function is involved.



Difference of the static and dynamic photo transistors are illustrated in these figures.

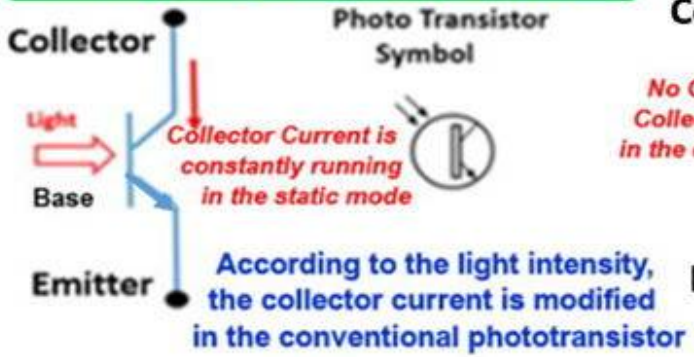
Sony Hole Accumulation Diode (HAD) is the P+NPNsub junction dynamic photo transistor with the surface P+ hole collecting and accumulation region is pinned and grounded, which is now widely called as Pinned Photodiode with the vertical overflow drain (VOD) function. Only Pinned Photodiode with the VOD function can realize the electrical shutter function.

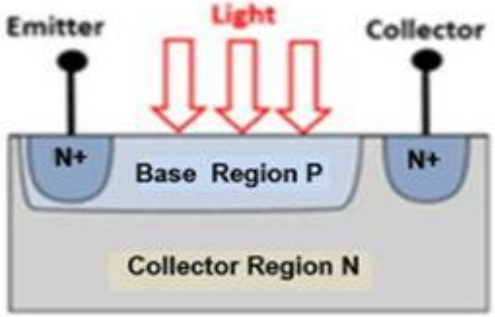
SONY HAD Sensor 1975 was hinted by SONY PNP Bipolar Transistor Process Technology

Conventional Static Phototransistor

(by John Northrup Shive , 1950)

No memory function is involved.

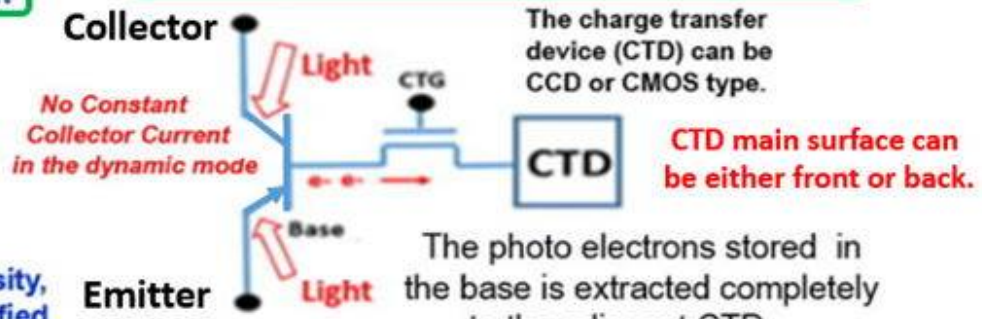


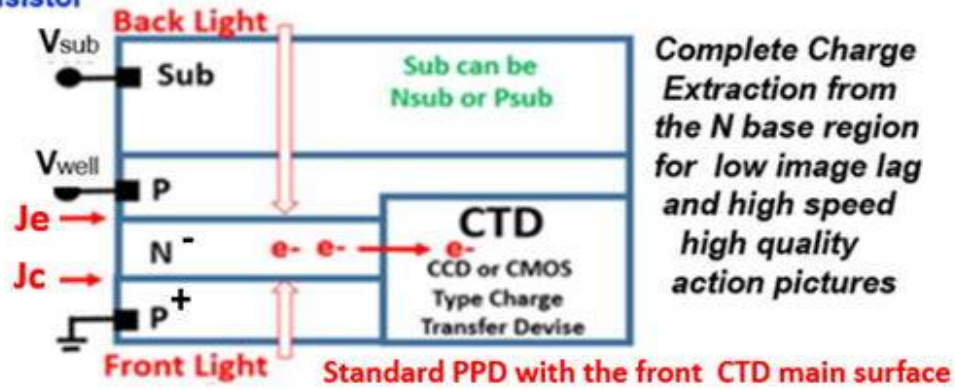


Dynamic Phototransistor Operation

by Yoshiaki Hagiwara at Sony in 1975

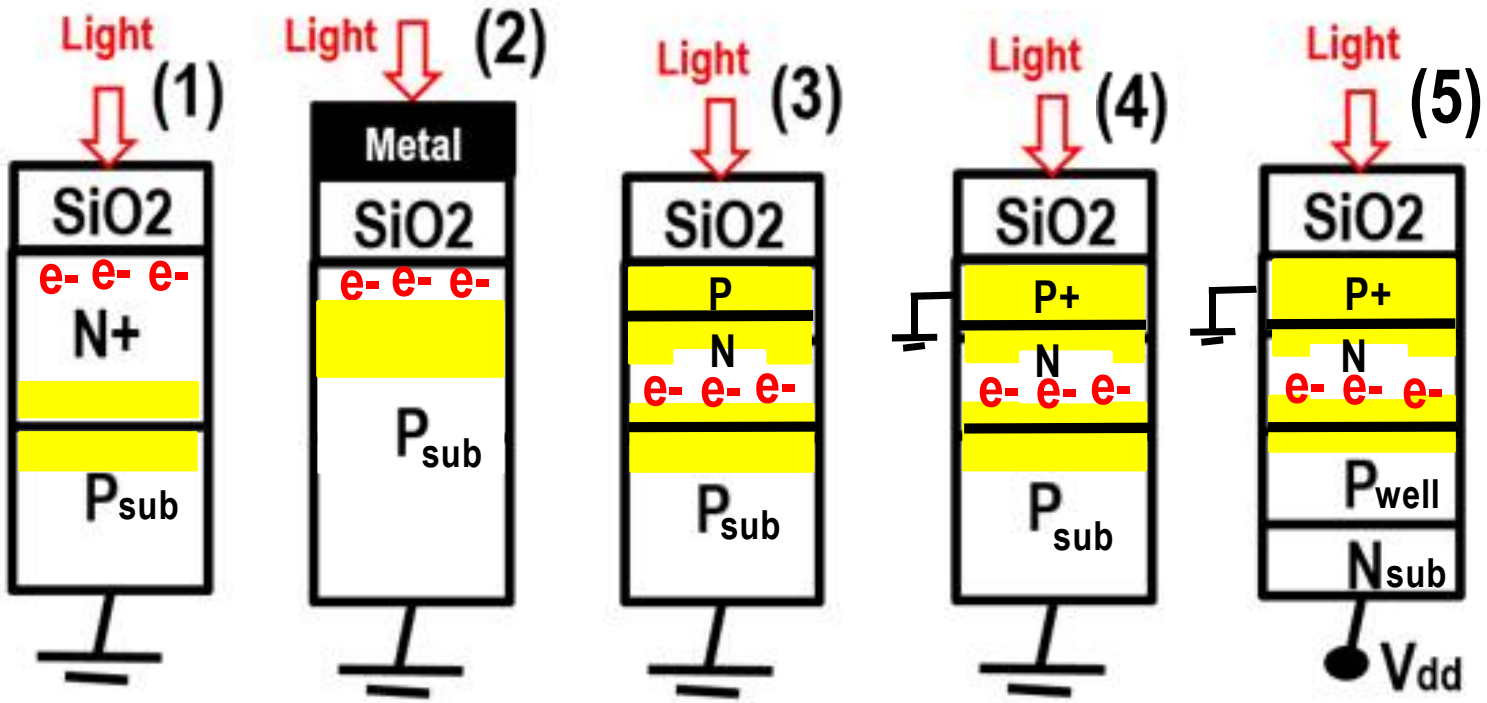
Dynamic Memory function is involved.





Complete Charge Extraction from the N base region for low image lag and high speed high quality action pictures

Standard PPD with the front CTD main surface



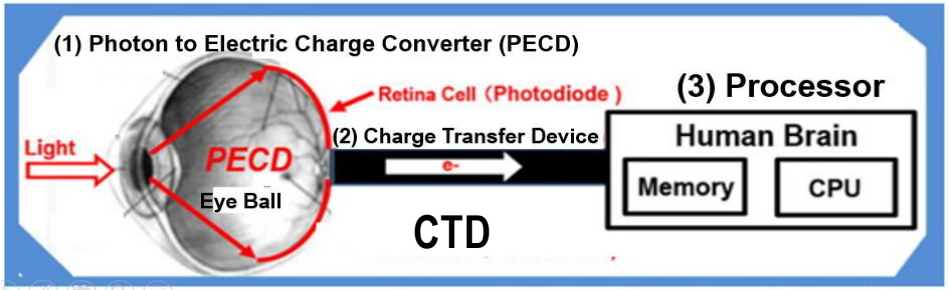
N+P Floating Photodiode (FPD) before 1970

CCD/MOS Photo Capacitor (CCD) invented in 1970

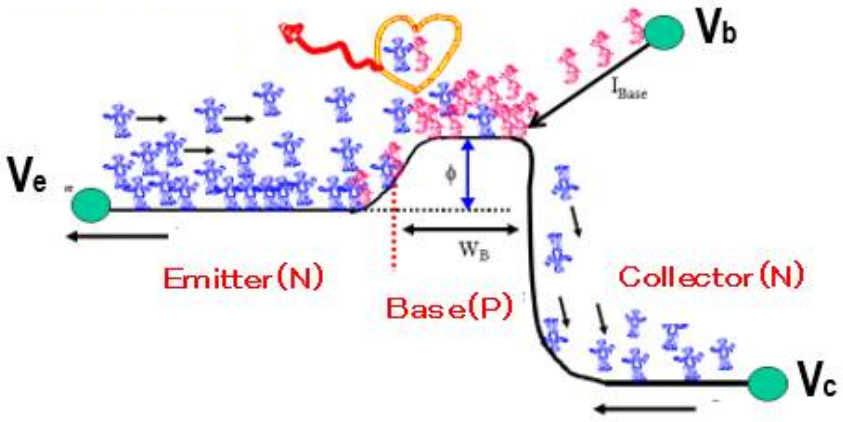
Buried Photodiode (BPD) invented in 1975

Pinned Photodiode (PPD) invented in 1975

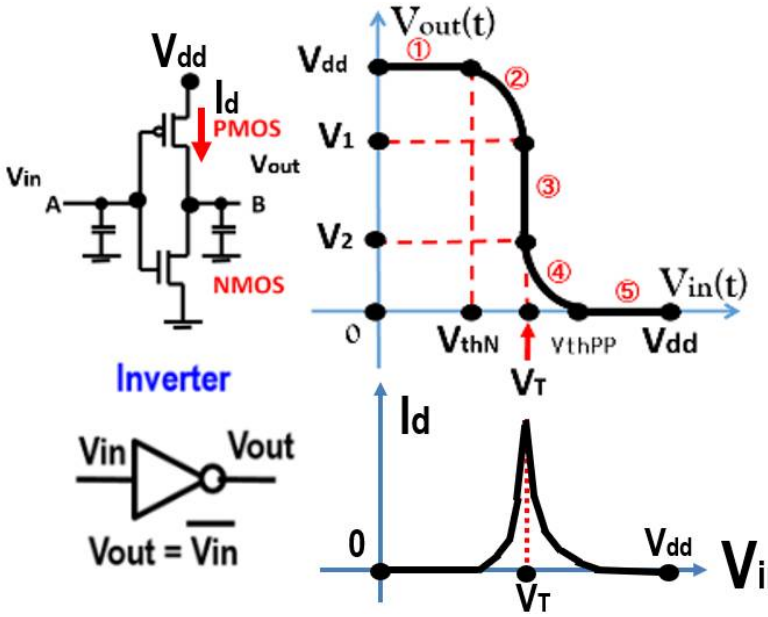
Hole Accumulation Diode (HAD) invented in 1975



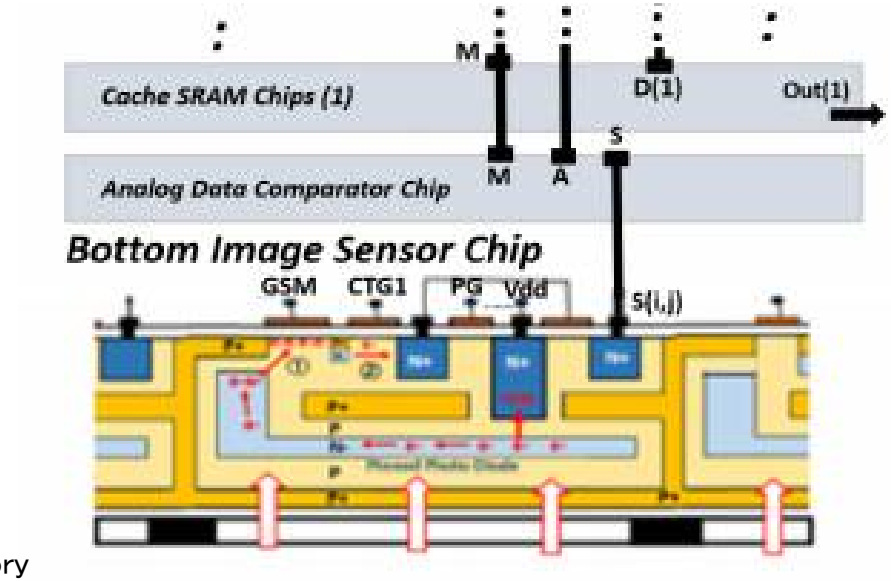
● NPN transistor Current Amplification



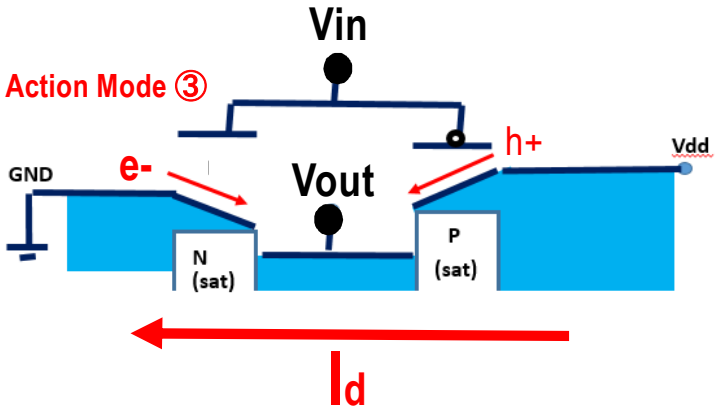
● Low Power CMOS inverter



3-D Multi-chips Intelligent CMOS Image Sensor System

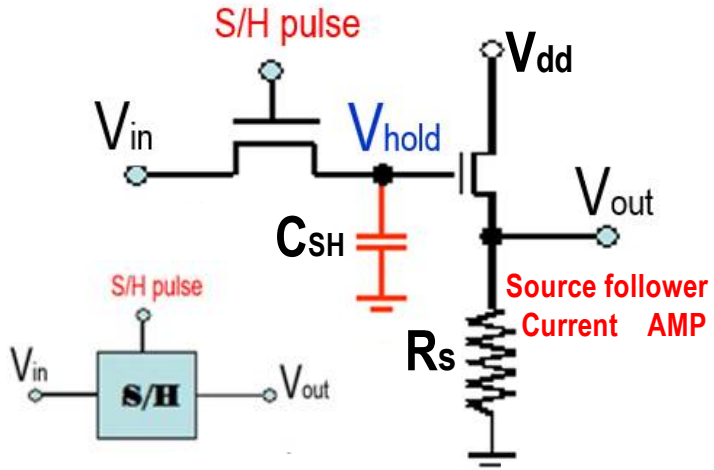


● Water Gate Model for CMOS Inverter

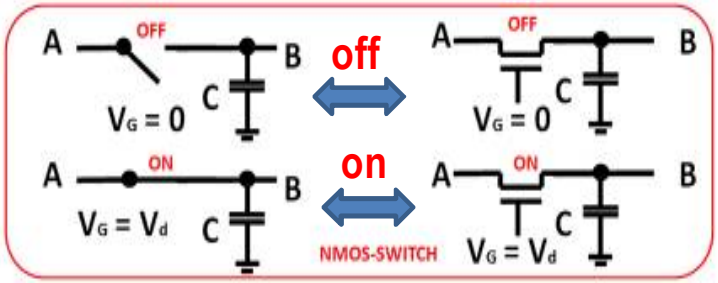


Correlated Double Sampling Hold by Prof. M. White, 1972

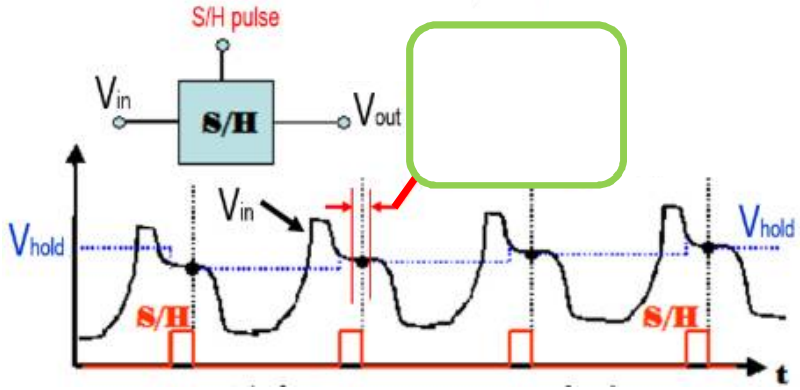
Conventional Single Sampling Hold



MOS Transistor Switch ON/OFF Action



Correlated Double Sampling Hold (CDS)



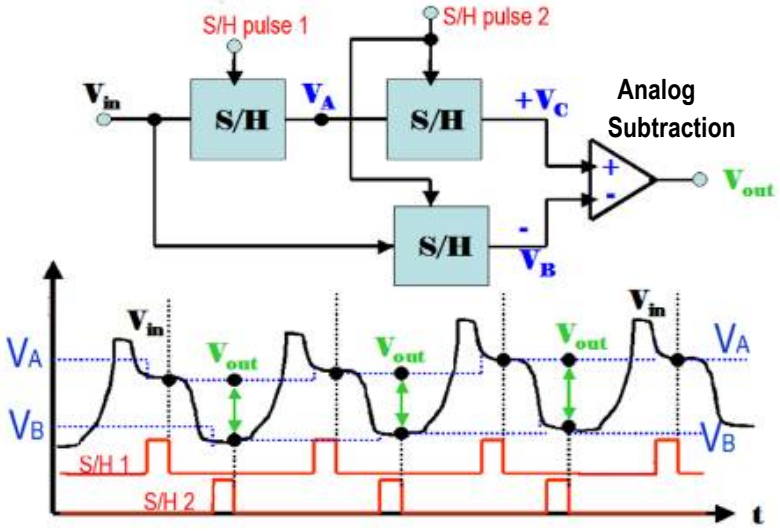


Image Sensor Signals are buried in the clock noises.

Multichip CMOS Image Sensor Structure for Flash Image Acquisition

Yoshiaki Hagiwara
AIPS
Artificial Intelligent Partner Laboratory
Atsugi-city, Japan
hagiwara-yoshiaki@aiplab.com

Abstract— A new 3D Pinned Photodiode (HAD) CMOS image sensor structure applied in the 3-Dimensional multichip high speed digital flash image data acquisition system is explained and the important features are discussed.

Keywords— Cache SRAM, ADC, Pinned Photodiode, Depletion Photodiode, Buried Photodiode, Back Light Illumination, Global Shutter Buffer Memory, In-pixel Three Transistor Current Source Amplifier.

I. Introduction

Basically there are five types of photodiode. They are (1) Classic N+Psub junction with serious image lag problem (2) PNPsub junction Buried Photodiode (3) PN-Psub junction Depletion Photodiode with no image lag feature (4) P+N-P junction Pinned Photodiode with the heavily doped P+ surface hole accumulation with no surface dark current feature and (5) P+N-PNsub junction type hole accumulation diode (HAD) with the vertical overflow drain (VOD) function which is by necessity Buried, Depletion and Pinned Photodiode. Fig. 1 shows the 3D multichip CMOS image sensor structure with the 3D Pinned Photodiode (HAD) image sensors with the MOS capacitor Global Shutter Buffer Memory (GSBM) which was originally invented[1] in 1975.

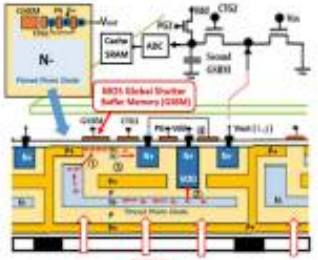


Fig 1. Cross Section of Buried Depletion Pinned Photodiode stacked with two Global Shutter Buffer Memory (GSBM) and CTG stages in two chip configuration for synchronizing data transfer to the receiving ADC and Cache SRAM chips.

II. Hole Role in Pinned Photodiode

The importance of holes in the hole accumulation layer HAD structure of Pinned Photodiode was first reported in Hagiwara 1978 paper[2] , and then explained in details by Theuwissen[3] in relationship with IDEM1982[4] paper and IEDM1984[5] paper. Today's success of super light sensitive digital imaging is based on the SiO2 exposed pinned window invented by Hagiwara in 1975[1] with the surface P+ hole accumulation HAD layer. Pinned Photodiode was originally invented[6] in the form of the back illumination scheme as illustrated in Fig. 2.

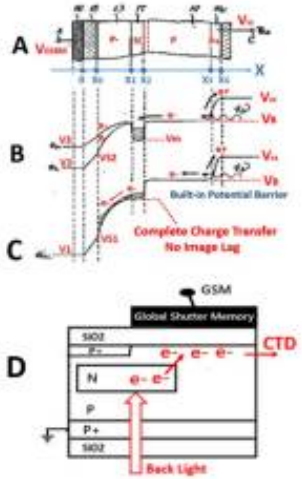


Fig. 2: The P+PNP junction type Buried Depletion Pinned Photodiode with no image lag feature with MOS Capacitor type Global Shutter Buffer Memory (GSBM) invented and defined in Japanese 1975 patent[1] by Hagiwara.

978-1-7281-4870-0/19/$31.00@2019 IEEE

3D IC2019.4817 2019 International 3D Systems Integration Conference (3D IC)

Fig. 3: Exact numerical calculations of Gaussian P+P doping profile D(x), the hole carrier density P(x) and the built-in barrier potential V(x).

III. Role of Built-in Potential Barrier in HAD

Exact numerical calculation of the built-in potential barrier is shown in Fig.3, explaining the hole electron generation and separation in the built-in electric field created by the heavily doped P+ surface hole accumulation HAD.

Note that the local unbalance of the hole concentration P(x) and the impurity boron atom density D(x) gives the local space charge polarization, resulting the built-in potential V_{bi}. The built-in electric field separates photo electron hole pairs, and resulting in the excellent quantum efficiency of the short wave blue light sensitivity.

Although CCD was just a charge transfer device (CTD), later taken over by CMOS type CTD, both CCD and CMOS image sensors have the super sensitive light detecting feature with very good color reproduction at low light level because of the Pinned Photodiode which was invented and described in Japanese 1975 patent[6] by Hagiwara.

In solar cells and image sensors, the photo electron and hole pair generation is considered to occur normally in the PN junction depletion region. However, the photo electron and hole pair generation in Pinned Photodiode is performed by an entire different physical principle. In 1975, Hagiwara proposed[1] that the photo electron and hole pair separation can also be achieved in the strong electric field created by the built-in barrier potential as shown in Fig. 2 that was the result of space charge polarization effect explained in Fig. 3.

Photo electrons are separated from holes in the presence of the surface built-in potential barrier near the border of the surface P+ hole accumulation HAD layer. And then, photo generated electrons can drift towards Buried Photodiode, which is the charge collecting storage, by using the holes, that is, positively charged Si ion atoms, as stepping stones, from one Si atom to another, like an energetic space rocket until it loses energy. If the photo electron, generated at the surface built-in potential barrier electric field, is recombined with a hole drifting deep in the bulk silicon, the hole becomes a neutral silicon atom that cannot move. Then, by the silicon bulk thermal neutrality condition, the excess negative space charge is present in the form of the trapped electron by the negatively charged boron or in the external orbit electron in the neutral Silicon atom at high energy state.

The electron has high energy state and can jump out into the free space. In this way, the excess negative charged electron cannot stay in the neutral silicon atom permanently and can be transferred to the positively charged silicon atom (hole) nearby, acting as stepping stones for the excess electron charge, eventually to drift towards the receiving Buried N type charge collecting region. Eventually the excess electron negative charge is collected in the buried N type diffusion storage region. If the electric field of the PN junction depletion region edge of the buried photodiode is near the surface P+ hole accumulation edge, the drifting photo electrons can be quickly and instantly collected in the buried N type charge collecting storage area.

IV. Vertical Overflow Drain (VOD) Function

Fig. 4 shows Pinned Photodiode with the vertical overflow drain (VOD), which is also Depletion Photodiode with no image lag feature. The following is the direct English translation of the Patent Claim of the Japanese 1975 patent[6] on Pinned Photodiode (HAD) invented by Hagiwara.

1. In the substrate, the first region P1 of the first impurity type is formed, on which, the second region N2 of the second impurity type is formed.
2. The charge e- from the light collecting part is transferred to the adjacent charge transfer device (CTD). Both are placed along the main surface of the semiconductor substrate.
3. In the solid state image sensor so defined, a rectifying junction Jc is formed on the second light collecting region N2 forming the P3 and N2 junction as the emitter junction Je .
4. The result is a photo transistor P3N2P1structure on the substrate with the N2 and P1 junction as the collector junction Jc . The charge, stored in the base N2 region according to the illuminated light intensity, is transferred to the adjacent charge transfer device.

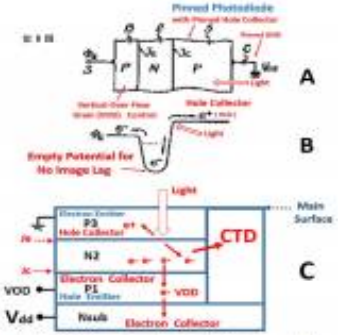


Fig. 4: The P+NPNsub junction type Hole Accumulation Diode (HAD)[6] invented by Hagiwara in 1975.

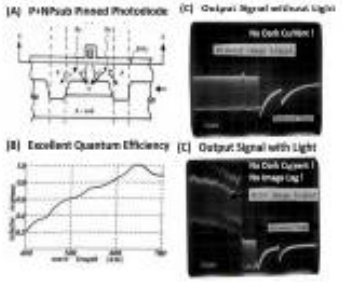


Fig. 5. Reproduction of figures reported in Hagiwara 1978 paper[2]. (A) P+NPsub junction type Pinned Photodiode structure, (B) the Excellent Blue Light Sensitivity (C) no dark current feature and (D) no image lag feature.

It is now well understood that the blue light of short wave length is needed for the satisfactory color reproduction of high image quality. However, the blue light cannot penetrate more than 0.3 micro meter in depth thru the silicon crystal[7]. The built-in surface potential barrier, created by the surface abrupt doping level difference, can in return create the strong electric field at the vicinity of the electron hole pair generation at the silicon surface of 0.3 micro meter in depth, which can effectively separate photo electron and hole pairs, resulting in the excellent quantum efficiency for the blue light needed for the satisfactory color reproduction.

P+NP junction type Pinned Photodiode(A) has the following three very important features, (B) Excellent short wave blue light quantum efficiency, which is the most important feature of Hagiwara 1975 patent[6], (C) no surface dark current problem and (D) no image lag problem, with also the feature of no surface interface trap (Nss) noise (E). But nothing is new about the feature (D) and (E) since CCD had these two features already by 1975.

In 1966, the in-pixel active source follower amplifier circuit for MOS image sensors was invented by Peter Noble. See Fig. 6.

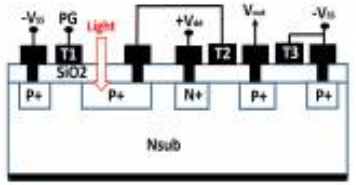


Fig. 6. In-pixel amplifier circuit by Peter Noble, 1966

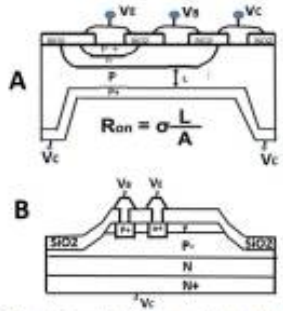


Fig. 7. Bipolar Transistor Process invented and developed by Yoshiyuki Kawana (A) and Toshio Kato (B) in 1950s.

But MOS scaling technology was not so advanced and the CCD type charge transfer device (CTD)[9] was preferred simply because MOS transistors were too large. However, CCD imager process shown in Fig. 4 was not as simple as MOS process for digital circuits. Complex bipolar transistor process experience was required. See Fig. 7. But now, owing to the advancement of CMOS process scaling, the active circuit of Fig. 6 became the most important element needed to build the modern CMOS image sensors[6].

V. NPN Junction Charge Transfer Gating (CTG)

Fig. 8 is a reproduction of the picture drawn in the 1975 patent[10] by Hagiwara. This charge transfer action is very similar to the well-known punch thru operation mode of the PNPN junction thyristor. Note that this is very similar to the P+NPNsub junction type Pinned Photodiode shown in Fig. 4. Both are the same PNPN junction type Pinned Photodiode.

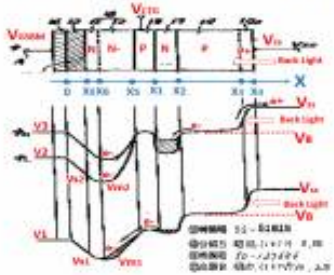


Fig. 8. The P+PNPN junction type Pinned Photodiode[10] with Global Shutter MOS Buffer Memory (GSBM) and the NPN junction type vertical charge transfer gating (CTG).

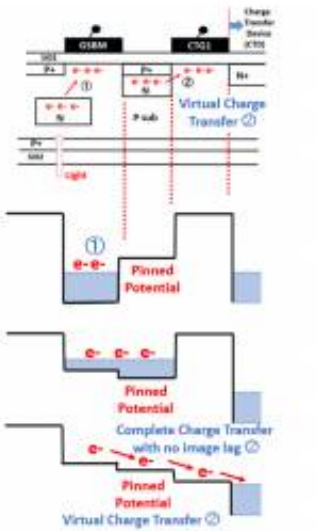


Fig.9 The important concept of Virtual Phase Charge Transfer of the Pinned Photodiode with the complete charge transfer operation mode for no image lag feature, described and invented by Hagiwara 1975 patents[2, 5, 10, 11].

VI. Pinned Surface Virtual Charge Transfer

The charge transfer operation with the pinned surface potential for the virtual gating concept is very similar to the CCD charge transfer operation. Fig. 9 shows the virtual charge transfer concept explained by Hagiwara[2, 5, 11] in 1975. Heinecek[12] invented an additional potential barrier stage to achieve the directionality of the virtual phase signal charge transfer operation, which was hinted by Hagiwara 1975 invention[6] and the virtual phase charge transfer operation of the image lag free Pinned Photodiode [1] as shown in Fig. 1.

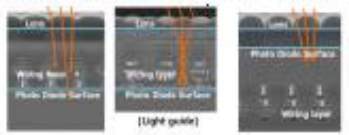


Fig. 10. Cross sectional photos of CMOS image sensors

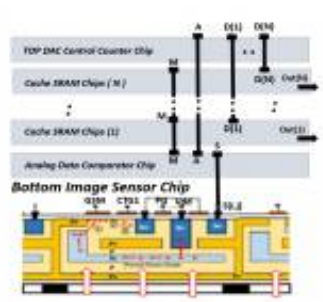


Fig. 11 : Metal Cu pillar signal pass wires thru multichip for the future 3D multichip flash image acquisition system.

VII. 3D Multichip Image Sensor System

Cross sectional photos of back light illuminated CMOS image sensors are shown in Fig. 10 while Fig. 11 shows the 3D multichip CMOS image sensor system. If time sharing scheme is used, we only need one data comparator circuit. However, for fast ADC operations, we must have the in-pixel data comparator circuits that have to be squeezed in each pixel element area. The comparator circuit is a conventional one that can also be used for a simple IR sensor detector as shown in Fig. 12.

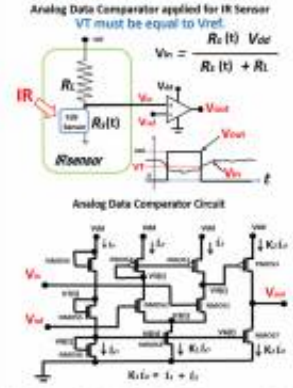


Fig. 12. Conventional Analog Data Comparator Circuit

VIII. Circuit Simulation of Analog Data Comparator

Fig.13 summarized the circuit simulation of the analog data comparator for the various reference voltage Vref values which correspond to the voltage A in Fig. 11. The input voltage Vin which corresponds to the output signal S in Fig.11 is scanned to obtain the value of the threshold voltage VT, which corresponds to the match signal M in Fig.11. With this match signal M, the cache SRAM latches the values of the control counter data D(1) to D(N) in each SRAM level chip. This simulation analysis shows the good circuit performance for the input reference voltage Vref at least in the range of 0 V to 1.5 V.

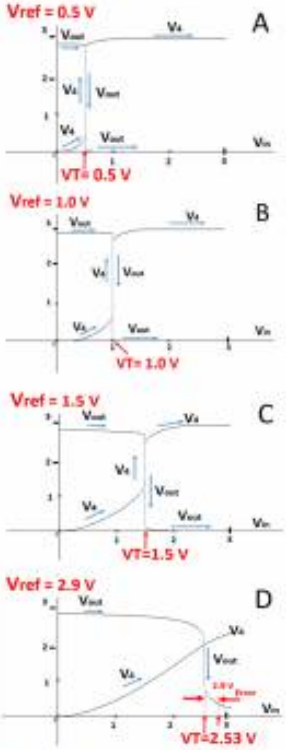


Fig.13: the circuit simulation results of the analog data comparator for the various reference voltage Vref values

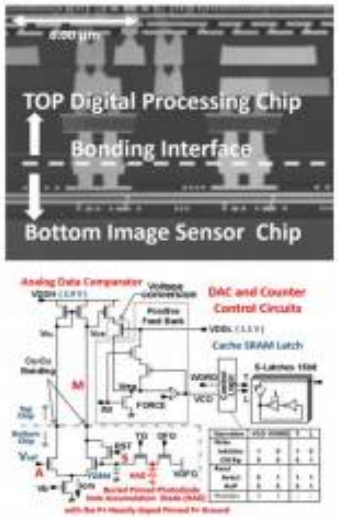


Fig. 14: Cross Sectional View of two chip stacked back-illuminated CMOS Image Sensor[11] with the in-pixel analog comparator control circuits to generate the match signal M from the reference voltage A and the image sensor signal S.

IX. All Solid State Digital Camera

The 25 nanosecond access time fast Cache 4 Mega Bit SRAM[11] was first developed in 1989, with the dynamic bit line load circuits invented by Miyaji, and was used as the very fast Digital Buffer Memory for the early all solid state digital CCD camera to correct and enhance the picture quality such as Jitter correction, color reproduction, pattern correction and image recognition processing system units for industrial and professional applications of high definition television broadcasting level.

Fig. 14 shows the cross sectional view of two chip stacked back-illuminated CMOS image sensor[10,16] with the in-pixel analog comparator control circuits to generate the match signal M from the reference voltage A and the image sensor signal S, as originally illustrated in Fig. 11 for the future multichip system.

Photo electron and hole generation and separation at the surface electric field is performed at the back side silicon surface of the P+ heavily doped pinned hole accumulation (HAD) layer acting as the Pinned Hole Collector Grounded Terminal. Salient physical parameters are defined in Fig. 15 . The all solid state CMOS image sensor technology is now being extended to the 3D multichip flash image acquisition system illustrated in Fig. 1 and Fig. 11.

3D IC2019.4017 2019 International 3D Systems Integration Conference (3D IC)

VIII. Circuit Simulation of Analog Data Comparator

Fig.13 summarized the circuit simulation of the analog data comparator for the various reference voltage Vref values which correspond to the voltage A in Fig. 11. The input voltage Vin which corresponds to the output signal S in Fig.11 is scanned to obtain the value of the threshold voltage VT, which corresponds to the match signal M in Fig.11. With this match signal M, the cache SRAM latches the values of the control counter data D(1) to D(N) in each SRAM level chip. This simulation analysis shows the good circuit performance for the input reference voltage Vref at least in the range of 0 V to 1.5 V.

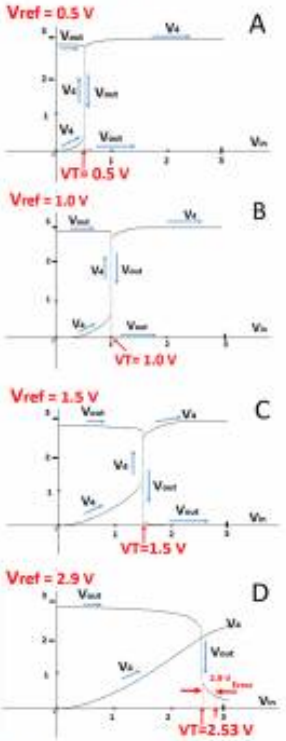


Fig.13: the circuit simulation results of the analog data comparator for the various reference voltage Vref values

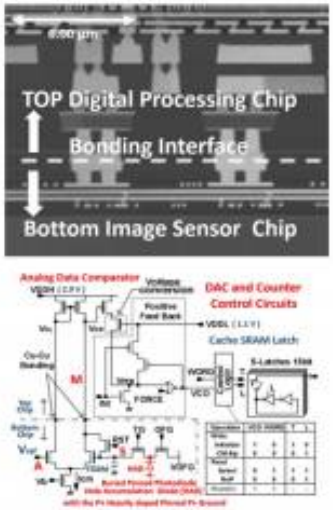


Fig. 14: Cross Sectional View of two chip stacked back-illuminated CMOS Image Sensor[11] with the in-pixel analog comparator control circuits to generate the match signal M from the reference voltage A and the image sensor signal S.

IX. All Solid State Digital Camera

The 25 nanosecond access time fast Cache 4 Mega Bit SRAM[11] was first developed in 1989, with the dynamic bit line load circuits invented by Miyaji, and was used as the very fast Digital Buffer Memory for the early all solid state digital CCD camera to correct and enhance the picture quality such as Jitter correction, color reproduction, pattern correction and image recognition processing system units for industrial and professional applications of high definition television broadcasting level.

Fig. 14 shows the cross sectional view of two chip stacked back-illuminated CMOS image sensor[10,16] with the in-pixel analog comparator control circuits to generate the match signal M from the reference voltage A and the image sensor signal S, as originally illustrated in Fig. 11 for the future multichip system.

Photo electron and hole generation and separation at the surface electric field is performed at the back side silicon surface of the P+ heavily doped pinned hole accumulation (HAD) layer acting as the Pinned Hole Collector Grounded Terminal. Salient physical parameters are defined in Fig. 15 . The all solid state CMOS image sensor technology is now being extended to the 3D multichip flash image acquisition system illustrated in Fig. 1 and Fig. 11.

VIII. Circuit Simulation of Analog Data Comparator

Fig.13 summarized the circuit simulation of the analog data comparator for the various reference voltage Vref values which correspond to the voltage A in Fig. 11. The input voltage Vin which corresponds to the output signal S in Fig.11 is scanned to obtain the value of the threshold voltage VT, which corresponds to the match signal M in Fig.11. With this match signal M, the cache SRAM latches the values of the control counter data D(1) to D(N) in each SRAM level chip. This simulation analysis shows the good circuit performance for the input reference voltage Vref at least in the range of 0 V to 1.5 V.

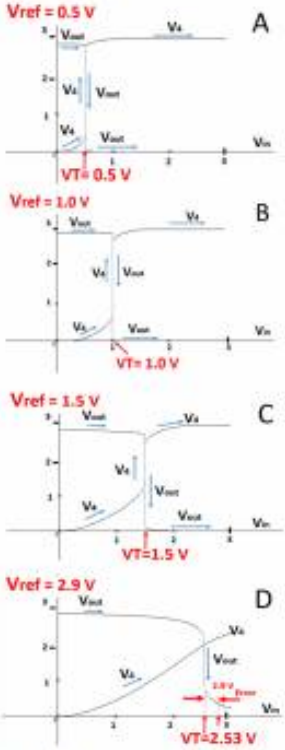


Fig.13: the circuit simulation results of the analog data comparator for the various reference voltage Vref values

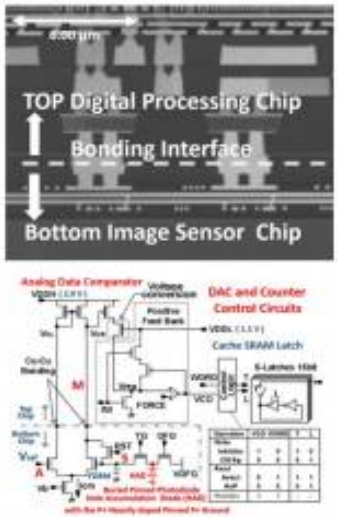


Fig. 14: Cross Sectional View of two chip stacked back-illuminated CMOS Image Sensor[11] with the in-pixel analog comparator control circuits to generate the match signal M from the reference voltage A and the image sensor signal S.

IX. All Solid State Digital Camera

The 25 nanosecond access time fast Cache 4 Mega Bit SRAM[11] was first developed in 1989, with the dynamic bit line load circuits invented by Miyaji, and was used as the very fast Digital Buffer Memory for the early all solid state digital CCD camera to correct and enhance the picture quality such as Jitter correction, color reproduction, pattern correction and image recognition processing system units for industrial and professional applications of high definition television broadcasting level.

Fig. 14 shows the cross sectional view of two chip stacked back-illuminated CMOS image sensor[15,16] with the in-pixel analog comparator control circuits to generate the match signal M from the reference voltage A and the image sensor signal S, as originally illustrated in Fig. 11 for the future multichip system.

Photo electron and hole generation and separation at the surface electric field is performed at the back side silicon surface of the P+ heavily doped pinned hole accumulation (HAD) layer acting as the Pinned Hole Collector Grounded Terminal. Salient physical parameters are defined in Fig. 15 . The all solid state CMOS image sensor technology is now being extended to the 3D multichip flash image acquisition system illustrated in Fig. 1 and Fig. 11.

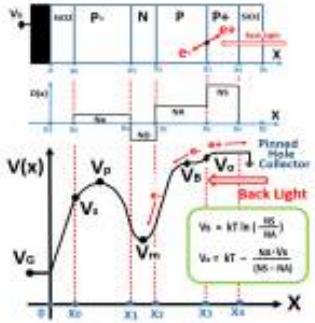


Fig. 15: Electrostatic Analysis of the surface Built-in Barrier Potential Vs and Vo by Depletion Approximation.

X. Conclusion

Hole Accumulation Diode[6] (HAD), with the P+ heavily doped surface hole accumulation layer, invented in 1975, is very important, because first of all it has the excellent short wave length blue light sensitivity feature producing the high picture quality of color reproduction in low level light illumination, which is realized by the photo electron and hole pair generation and separation in the built-in potential barrier[7] and the electric field at the surface heavily doped P+ hole accumulation HAD. No dark current is the second important feature. And no image lag is the third one since CCD was known to have the no image lag feature already. But CCD itself does NOT have the excellent blue light sensitivity and does NOT have the low dark current feature which the Pinned Photodiode[1,2,6,10] invented by Hagiwara has.

HAD is defined as the PNPN junction Photodiode with the VOD function. HAD is also by necessity the P+N-P junction Pinned Photodiode with no dark current feature. HAD is also by necessity the PN-P junction Depletion Photodiode defined as Buried Photodiode with no image lag feature. When Hagiwara invented HAD[1,2,6,10] in 1975, Hagiwara also invented (1) Pinned Photodiode[6], (2) Depletion Photodiode[1], (3) Buried Photodiode[10], (4) the in-pixel vertical overflow drain[6] (VOD) function and (5) the in-pixel Global Shutter function[1, 10]. The surface pinned potential[1, 6, 10] also serves as the hole collector terminal separating the holes from photo electrons which drift more than the distance estimated by Debye length until being collected into the Buried[10], Depletion[1] and Pinned[6] Photodiode (HAD), with the back light illumination scheme[1] which is the most important feature needed to build the super sensitive 3D CMOS image sensor with the high blue-light quantum efficiency and the excellent color reproduction at low light level for fast action pictures with no image lag.

Future AI traffic control system will need at least the high definition 8K image format of 7680H x 4320V, with 33 million pixels, to obtain the details of flash action images, with the in-pixel flash AD converters, and fast Cache SRAM chips in the 3D multichip CMOS image sensor with the more complex future digital circuit system implementations of the human friendly artificial intelligent partner system[17] (AIPS) to realize the smart AI image sensors for the smart AI robot vision system and home AI security and house cares.

Acknowledgment

The author expresses sincere gratitude to Tetsuhi Shimizu, Yasuhiro Ueda, Tadakuni Narabu, Junya Suzuki, Kato Toshio and Yoshiyuki Kawana, my dear friends and respectful mentors throughout private and public life at Sony.

References

[1] Japanese 1975-127647 Patent, filed on Oct 23, 1975 on Buried Depletion and Pinned Photodiode with complete charge transfer and no image lag feature with MOS Capacitor type Global Shutter Buffer Memory (GSBM) function invented by Yoshiaki Hagiwara in 1975.

[2] Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488V CCD imager with narrow channel transfer gates, "Proc. of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese J. Appl. Phys., vol. 18, supplement 18-1, pp. 335-340.

[3] Albert Theuwissen, "The Hole Role ", IEDM2005, IEDM Technical Digest, Dec 2005

[4] N. Tanauchi et.al., IEDM1982 Tech. Digest, pp. 324-32 on Buried Photodiode with no image lag. See also Japanese 1988-123259 patent filed in 1988 , filed later than Japanese 1975-124985 patent in 1975

[5] B.C. Burkey et.al., IEDM Technical Digest, 1984, pp. 28-31 on Pinned Photodiode with the surface P+ hole accumulation layer, a duplicate device defined in the original Japanese 1975-124985 patent.

[6] Japanese 1975-134985 Patent filed on Nov 10, 1975 on the P+/N/P/n/n+ Buried Depletion and Pinned Photodiode with the surface P+ hole accumulation layer and the vertical overflow drain (VOD).

[7] See Fig. 3, p.750, S. M. Sze,"Physics of Semiconductor Devices", 2nd Edition, Wiley.

[8] K Ishikawa and T Kuka, "One inch 2M pixel CCD with Hyper HAD sensor and Camera System for HDTV", SPIE proc. Vol. 1656, pp.39-46, February 1992.

[9] K. Yonemoto and H. Sumi , "A CMOS Image Sensor with a Simple FPN Reduction Technology and a Hole Accumulation Diode", ISSCC2000, Digest of Technical Papers, pp.102-103, February 2000.

[10] Japanese 1975-127646 Patent, filed on Oct 23, 1975 on the P+/N/P/n/n+ junction type Buried Depletion and Pinned Photodiode with the in-pixel MOS capacitor type buffer memory and the vertical N/P/N junction type charge transfer gating (CTG) for Global Shutter operation scheme.

[11] Y. Hagiwara, "High-density and high-quality frame transfer CCD imager with very low smear, low dark current and very high blue sensitivity," IEEE Trans. Electron Devices, vol. 43, no. 12, pp. 2122-2130, Dec. 1996.

[12] J. Hynecek, "Virtual phase CCD technology," in Proc. IEDM1979, pp. 611-614,Dec. 1979.

[13] Fumio Miyaji, Yasushi Matsuyama, Yoshikazu Kanaishi, Katsunori Sonoh, Takashi Emori and Yoshiaki Hagiwara, "A 25 nanosec 4 Mega bit CMOSRAM with Dynamic Bit-Line Loads", ISSCC1989 and J. Solid State Circuits,Vol24, No.5, October 1989.

[14] M. Sakakibara, et al, " A Back-Illuminated Global-Shutter CMOS Image Sensor with Pixel-Parallel 14b Subthreshold ADC", ISSCC2018, Feb. 2018

[15] Y. Kamagai, et al, "Back-illuminated 2.74 um-Pixel-Pitch Global Shutter CMOS Image Sensor with Charge-Domain Memory Achieving 18k e- Saturation Signal " IEDM2018, Dec 2018

[16] Y. Kagawa and H. Ivamoto, "3D Integration Technologies for Stacked CMOS Image Sensors", an invited paper at the IEEE 3DIC2019 conference , Oct 8, 2019, Sendai, Japan

[17] Yoshiaki Hagiwara, "The World of Digital Cinema for Artificial Intelligent Partner System (AIPS)", published by Seimandra.co.jp, in 2016, ISBN978-4-88359-338-2, 450 pages, Hard Cover 9000yen+tax.

Simulation and Device Characterization of the P+PN+P Junction Type Pinned Photodiode and Schottky Barrier Photodiode

Yoshiaki Hagiwara
AIPS
Artificial Intelligent Partner Laboratory
Atsugi-city, Japan
hagiwara-yoshiaki@aiplab.com; +81-80-2062-5657

***Abstract*— Process parameter tolerance of semiconductor device is very important for manufacturability and yield. Pinned Photodiode has by definition the pinned surface potential of the low surface dark current feature and the pinned empty potential well of the no image lag feature with the excellent blue light sensitivity of the ideal quantum efficiency. This paper reports simulation and device characterization of the unique P+PN+P junction type Buried, Depletion and Pinned Photodiode with excellent manufacturability, originally invented in 1975. Related various historical photodiode structures are reviewed, including the metal semiconductor Schottky Barrier photo sensor of Au/ β - Ga_2O_3 type in search for the low leakage and dark current photodiode which led the 1975 invention of the low leakage P+NPNsub junction Pinned Photodiode by Hagiwara.**

Keywords—Buried Depletion Pinned Photodiode, built-in barrier potential, Hole Accumulation Diode (HAD), electron hole pair separation, built-in barrier potential

I. Introduction

Many failures in device applications are related to loss of the device current blocking capability. The very low reverse leakage current feature of the commercially available Trench-based Schottky barrier rectifier switch is a key parameter for device performance, including the high performance required for the super light sensitive, the low surface dark current and the low 1/f noise image sensors[1]at very low light level with the low image lag feature.

Fig. 1 shows the light penetration depth[2] in the silicon crystal with respect to the incident light wave length. The maximum light penetration depth into the silicon crystal is about 0.2 micro meter for the blue light of 0.4 micro meter wave length and 37.6 eV photon energy while the light penetration depth is about 8 micro meter for the red light of 0.7 micro meter wave length and 12.3 eV photon energy. To achieve the best color reproduction picture quality for the CMOS image sensors we need a photodiode which can convert the incident blue light energy into the electric energy very efficiently. Various types of photo sensors are compared in Fig. 2. The N+P+ junction (type A) Esaki Diode has the two states, high and low current modes, in the forward bias. However, it has a relative large leakage current in the reverse bias because both sides of the N+ and P+ regions are very much heavily doped.

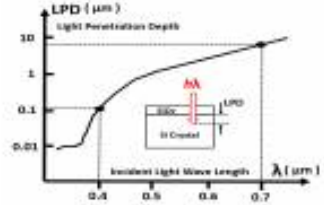


Fig 1: Light Penetration Depth (LPD) in Silicon Crystal.

XXX-X-XXXX-XXXX-X/XX/$XX.00 ©2020 IEEE

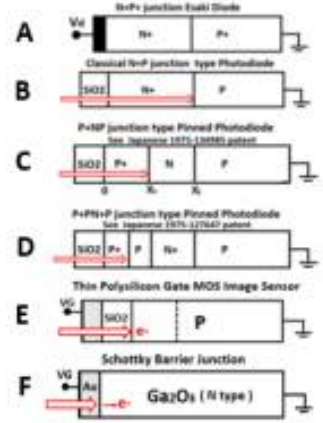


Fig 2: various types of photo sensor structures.

Classical N+P junction type B photodiode is known to have the serious image lag problem. The type C Pinned Photodiode[3], invented in 1975 by Hagiwara, has the pinned surface potential of the no leakage current feature and the pinned empty potential of the no image lag feature. See Fig.3. As originally reported by Hagiwara 1978 paper[4], the P+ surface HAD layer had the Gaussian doping profile with $Qs = 2 \times 10^{13}$ cm^{-2} and $Ns = 1 \times 10^{18}$ cm^{-3} while the buried N region had $Nd = 3 \times 10^{16}$ $cm^{-3}$and $Qd = 1.7 \times 10^{12}$ cm^{-2}. The type D Pinned Photodiode has the unique built-in barrier electric field, enhancing the photo electron pair separation at the surface of the silicon crystal for the short wave length blue light.

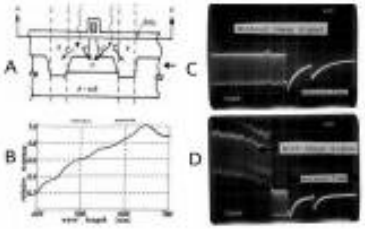


Fig 3: Features of P+PN junction type Pinned Photodiode

2020 Electron Devices Technology and Manufacturing Conference (EDTM)

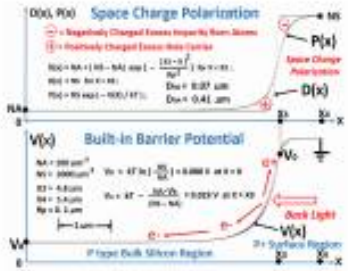


Fig. 4: Exact numerical calculations of Gaussian P+P doping profile D(x), the hole carrier density P(x) and the built-in barrier potential V(x).

The excellent blue light sensitivity is achieved near the silicon surface depth of less than 0. 2 micro meter. The substrate doping level was $Na = 5 \times 10^{16}$ cm^{-3}. This idea of the unique P+NP junction type Pinned Photodiode was introduced for the first time in 1975 by Hagiwara in his three Japanese patents[3] in series, and Hagiwara reported in his 1978 paper[4] the 380H x 499V FT CCD image sensor using this P+NP junction (type C) Pinned Photodiode.

However, the actual formation of the doping profile of Pinned Photodiode is very likely to the type D because the normal ion implantation gives the Gaussian doping profile with smooth tailing slope, effectively resulting in the P+PN+P junction type D profile. See Fig. 4.

The heavily doped surface P+ hole accumulation layer and the relatively heavily doped N+ charge collecting region, connected in between by the lightly doped P region of $Na = 5 \times 10^{14}$ cm^{-3}.

Simulation and electric analysis of the P+PNP junction type D Pinned Photodiode was performed. See Fig. 3 which shows the P+P doping profile with the space charge polarization inducing the built-in barrier electric field enhancing the photo electron hole pair separation inside the built-in barrier potential of **kT ln(NS/NA) – 4 kT ev – 0.1 volt**.

Normally the photo electron and hole pair generation and separation is performed in the electric field inside the depletion region of the PN junction. But the photo electron and hole pair generation and separation of the P+PNP junction (type D) Pinned Photodiode is different and quite unique.

The surface P+P impurity doping slope induces the built-in barrier potential and the resulting built-in barrier electric field enhances the photo electron pair separation at the very near surface region of the silicon crystal to give the excellent blue light sensitivity. This photo electron hole separation mechanism is unique, quite different from the usual photo electron hole pair separation.

The reason why the P+PN+P junction type D Pinned Photodiode can have the excellent blue light sensitivity near the silicon surface depth of 0. 2 micro meter is now explained in details. Simulation and the electrostatic analysis is based on the fact that the maximum depth for the blue light penetration into the silicon crystal is 0. 2 micro meter which is very close to the surface.

Fig. 5: P+PN+P junction type Buried Pinned Photodiode defined in Hagiwara Japanese 1975-127647 patent.

The life time of the photo generated minority carrier can be measured using the photoconduction effect and the diffusion length Ld can be determined, which is needed for electrons to survive in the majority carrier hole-rich P substrate area. See Fig. 5. Photo electrons are expected to reach the buried N charge collecting region. The situation is similar to the minority carrier electrons injected from the emitter terminal into the majority carrier hole-rich base area of a NPN bipolar transistor. If the base region width is narrow, enough, one or two electrons may recombine with the holes in the base, but the most of the electrons can reach the collector terminal of the strongly reverse-biased depletion region. The N buried region of Pinned Photodiode acts as if the collector region of the NPN bipolar transistor does. This photo electron generation separation physical mechanism is unique and quite different from the ordinary electron hole pair separation in the PN junction depletion region.

II. No Image Lag Feature

Classical N+P junction type B photodiode shown in Fig. 2 is known to have the serious image lag problem. The charge transfer gate has a very large channel resistance and the residual signal charge cannot be transferred completely in the short clock reset time. The remaining small signal charge causes the serious image lag and the fast moving objects cannot be captured and the pictures are blurred. The first attempt was the thin-polysilicon electrode MOS Capacitor type E image sensor structure shown in Fig. 2. However the MOS capacitor type E sensor has inherently the strong surface electric field that induces the serious surface dark current which is caused by the oxide silicon surface positive fixed charge Qss and the electron trapping states Nss. The oxide silicon interface has the problem of the incomplete atomic crystal disorders inherently which cannot be avoided. Hagiwara proposed in 1975 to use the Schottky Barrier photo sensing type F structure for the interline transfer CCD imager. The idea was hinted by his Caltech undergraduate unpublished research work in 1971 of the Au/Ga_2O_3 Schottky Barrier junction experiment which was expected to have the very low reverse bias leakage current. Based on the conventional photo sensor structures type E and F, Hagiwara proposed in 1975 the P+NPNsub junction type photo sensor structure type C which is the P+NP junction type photodiode combined with the NPNsub junction type built-in overflow drain (VOD) structure. And in the SSDM1978 paper Hagiwara reported the 380H x488V FT CCD image sensor using the P+NPsub junction type Pinned Photodiode, with the excellent blue sensitivity, the low surface dark current and the low image lag features. See also Fig. 6 for comparison.

2020 Electron Devices Technology and Manufacturing Conference (EDTM)

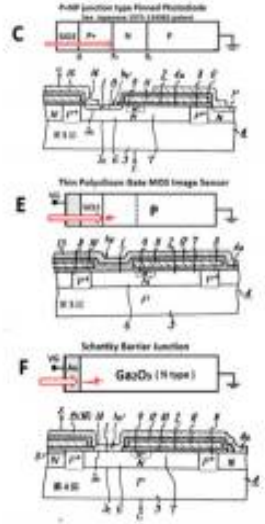


Fig. 6: Cross sectional views of Type C P+NP junction Pinned Photodiode sensor, Type E MOS capacitor photo sensor and Type F Schottky barrier photo sensor.

III. Schottky Barriers on Gallium Oxide

The surface barrier height of gold chemically prepared for the N type β-Ga_2O_3 semiconductor was investigated in details at room temperature by (1) photo response, (2)forward current versus voltage and (3) capacitance-voltage methods. Fig.7 showed the band diagram. The barrier energy was found to be 1.68 eV, with the excellent agreement, within kT of 0.026 eV, obtained by three methods. The diode non-ideality factor was found to be 1.14 ± 0.03 by current-voltage method.

This value is agreement with the value 1.08 ± 0.04 expected as a result of image force lowering using the free electron concentration 4.1 ± 0.09 x 10^{17} cm^{-3} of the un-doped gallium oxide crystal determined by capacitance-voltage measurement. The effective mass m^* of electrons was taken as 0.20 M and the relative permitivities of gallium oxide at the optical and low-frequencies were taken as 4 and 10.2 respectively.

The Barrier energies of gold on the chemically prepared β-Ga_2O_3 was obtained here following the same techniques developed by Neville and Mead[5] for the zinc oxide crystal.

Mead[6] established a semi-empirical approach for predicting the type of contact to be expected at an arbitrary metal-semiconductor interface. Fig. 5 shows the energy band diagram for "no bias" condition for the Au/Ga_2O_3 Barrier.

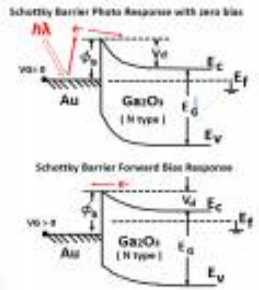


Fig. 7: Au/Ga_2O_3 Schottky Barrier Band Diagram

This approach is now applied for β-Ga_2O_3 . Although five forms of Ga_2O_3 have been reported by 1971, only the monolithic form, having the same structure as β alumina, is stable at room temperature.

The results of this analysis show that the barrier height Φ_B is 1.68 eV and the effective carrier concentration of 4.1 ± 0.09 x 10^{17} cm^{-3} gives the Fermi level below conduction band edge of 0.1 eV at room temperature. When monolithic light from a monochrometer impinges on the semiconductor surface, it induces a short circuit photocurrent in the metal-semiconductor junction.

The square root of the photocurrent normalized to the incident photon flux when plotted as a function of the photon energy results in a straight line for photon energies above (Φ_B + 3 kT). The intercept for zero response of the extrapolated straight line yields a barrier height of 1.68 eV. Typical photo response data is presented in Fig. 8.

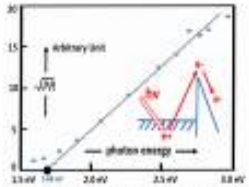


Fig. 8: Photo Response of Ga_2O_3-Au Schottky Barrier

A typical plot of $1/C^2$ as a function of the reverse voltage is shown in Fig. 8. The concentration was found to be 4.1 ± 0.09 x 10^{17} cm^{-3} from the slope using the relation:

$$N_d = \left(-2 / \epsilon_s \epsilon_0 \right) \left(\frac{\delta V}{\delta \left(\frac{S}{C} \right)^2} \right) \qquad (1)$$

where S is the barrier area and δ is the low frequency

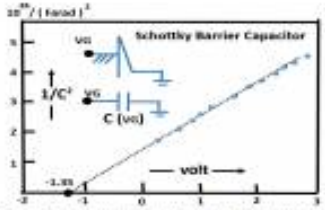


Fig. 9: CV measurement of Ga_2O_3-Au Schottky Barrier

permitivity taken as 10.2 after Neville[5]. See Fig. 9. The extrapolated intercept **Vo** is related to the surface barrier energy by the equation

$$V_0 = \frac{\delta}{\epsilon} - \frac{kT}{q} \left(1 + \ln \left(\frac{N_c}{N_D} \right) \right) \qquad (2)$$

where Nc is the conduction band effective density of states. The intercept **Vo** was found to be 1.36 ± 0.09 eV which gives the barrier height Φ_B = 1.70 ± 0.15 eV. Hence, is taken 1.14 ± 0.03 from the forward voltage-current measurements which is in agreement with the value Φ_B = 1.08 ± 0.04 expected for the forward voltages between 0.7 and 1.2 V from the relation

$$n = 1 + \frac{1}{8} \left(\frac{\lambda_D}{\epsilon_s} \right)^2 \left(\frac{8\pi^2 \epsilon_{sp}^2 \epsilon_{ox}}{} \right)^{1/3} \left[\frac{q}{} - \frac{kT}{q} \left(1 + \ln \left(\frac{N_c}{N_D} \right) \right) \right]^{-1/3} \qquad (3)$$

as a result of image force lowering. In Fig. 10, forward current characteristics are displayed at room temperature. The slope gives **q/nkT**, where **n** is the diode non-ideality factor, seen to be 1.14 ± 0.03, which is consistent with 1.08 ± 0.04 obtained by the capacitance-voltage method. The extrapolated current density at zero applied bias voltage is given by

$$J_0 = A^* T^2 \exp \left(- \frac{q V_d}{nkT} \right) \qquad (4)$$

where A * is the Richardson constant corresponding to the effective mass of the material taken as 0.2 m_o. Using this equation the barrier height was found to be 1.69 ± 0.04 eV. The deviation of the characteristics from the exponential dependence on the applied voltage with the slope of **q/nkT** is due to the series resistance which is fairly independent of the current for the range considered[7].

IV. Conclusion

The photo electron hole separation mechanism of the P+PNP junction type Pinned Photodiode was explained, which is unique and quite different from the conventional photo electron hole pair separation performed by the electric field inside the PN junction depletion region. Related various historical photodiode structures are reviewed, including the 1971 work on the β - Ga_2O_3 Schottky barrier photo sensor in search for the low leakage dark current device which led to the 1975 invention of the Pinned Photodiode with the surface P+ heavily doped hole accumulation (HAD) with the vertical overflow drain (VOD).

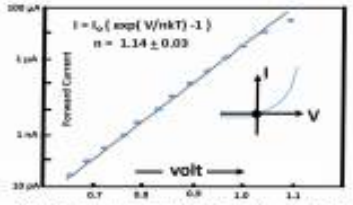


Fig. 10: IV measurement of Ga_2O_3-Au Schottky Barrier

The barrier energy of gold on chemically prepared gallium oxide was shown to be 1.68 eV. The un-doped gallium oxide crystal at room temperature was found to contain 10^{17} free electron per cm^3. The three experimental techniques showed remarkable agreement forming a constant picture of the Ga_2O_3 – Au interface of the minimal atomic disorders, expecting the very low leakage dark current feature, which is desired for super light sensitive video camera applications at very low light level but with the excellent color reproduction. The N type Ga_2O_3-Au Schottky barrier rectifier was investigated. The very low reverse leakage current feature is a key parameter for the super light sensitive, the low surface dark current and the low image lag high performance image sensors with excellent color reproduction at very low light level.

Future AI traffic control system will need at least the high definition 8K image format of 7680H x 4320V, with 33 million pixels, to obtain the details of flash action images, with the in-pixel flash AD converters, and fast Cache SRAM chips in the 3D multichip CMOS image sensor with the more complex future digital circuit system implementations of the human friendly artificial intelligent partner system[8] (AIPS) to realize the smart AI image sensors for the smart AI robot vision system and home AI security and house cares.

Acknowledgment

The author expresses sincere gratitude to Prof. C.A. Mead and Prof. T.C. McGill, for advising my original 1971 work at Caltech on the Ga_2O_3 – Au Schottky Barrier interface study and characterization, and Yoshiyuki Kawana and Toshio Kato for supporting my original 1978 work at Sony on the P+NP junction Pinned Photodiode. They are my dear friends and respectful mentors throughout my private and public life.

References

[1] Y. Hagiwara, " Multichip CMOS Image Sensor Structure for Flash Image Acquisition ", IEEE IDMC2019 conference in Sendai, Japan

[2] S. M. Sze, "Physics of Semiconductor Devices", Fig. 5, p.750.

[3] Japanese 1975-127646, 1975-127647 and 1349885 Patents

[4] Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 3000x4000V CCD imager with narrow channel transfer gates, "Proc. of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese J. Appl. Phys., vol. 18, supplement 18–1, pp. 335–340.

[5] R.C. Neville and C.A. Mead, J. Appl. Phys. 41, 9 (1970).

[6] C.A. Mead, Solid State Electronics–Pergamon Press. 1966, Vol 9, pp.1023-1033.

[7] D. Kahng, Solid State Electronics-Pergamon Press 1963, Vol. 6, pp.281-295.

[8] Yoshiaki Hagiwara, "The World of Digital Circuits for Artificial Intelligent Partner System (AIPS)", published by Seiunsha.co.jp, in 2016, ISBN978-4-88359-339-2, 458 pages, Hard Cover 9000yen+tax.

Symmetrical P+PNPP+ Junction Pinned Photodiode Solar Cell With High Quantum Efficiency

Yoshiaki Hagiwara

APS
Artificial Intelligent Partner Laboratory
hagiwara-yoshiaki@aiplab.com ; Atsugi-city, Japan 243-0201

Abstract

Solar panels on the market today consist of cells made from a single semiconducting material, usually silicon. Since a typical solar cell has the asymmetrical N+PP+ junction type diode structure which absorbs only a narrow band of the solar spectrum, much of sunlight's energy is lost as heat: these panels typically convert less than 20 percent of that energy into electricity. This paper reports the symmetrical P+PNPP+ junction type Pinned Photodiode (PPD) which at least doubles the absorption band of the solar spectrum and more by utilizing the electron hole separation mechanism of the barrier electric field induced by the gradually doped surface P+P doping profiles on both sides of the silicon wafer. The proposed solar cell structure may achieve more than 60 % quantum efficiency.

Conventional N+NPP+ junction type Solar Cell

Blue light cannot penetrate the silicon crystal more than 0.2 micron in depth while red light can penetrate more than 10 micron. If we can collect all the photons within 10 micron depth of the silicon crystal, more than 60% quantum efficiency is possible. A typical solar cell shown in Fig. 1 is very similar to the N+P junction photodiode used in classical MOS image sensors with poor quantum efficiency. Since the surface floating N+N region with no electric field has flat potential with stored photo electron charges, electron hole pairs at the surface cannot be separated and do not contribute to the quantum efficiency. See Fig. 2.

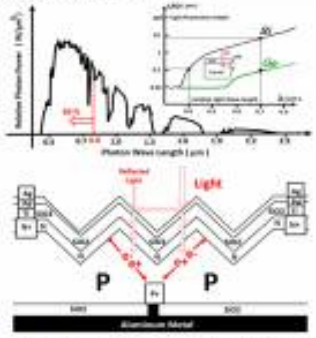


Fig.1 Sun Light Spectrum and Conventional Solar Cell

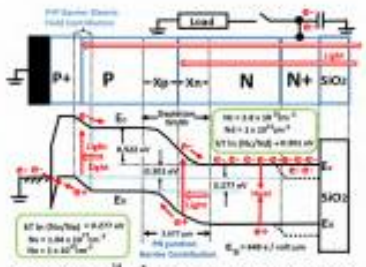


Fig. 2 Conventional Single N+NPP+ junction Solar Cell

Simple P+PNN+ junction type Photodiode

The depletion width of the PN junction is less than 3.1 micron. However, the P+P barrier electric field[1] can also separate the photon generated electron hole pair effectively.

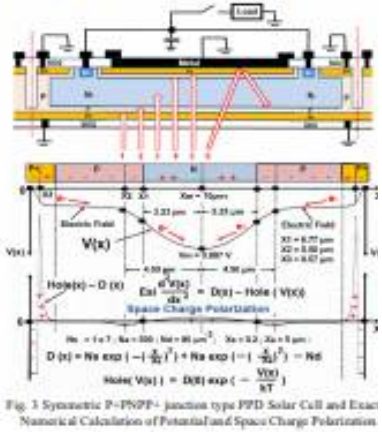


Fig. 3 Symmetric P+PNPP+ junction type PPD Solar Cell and Exact Numerical Calculation of Potential and Space Charge Polarization

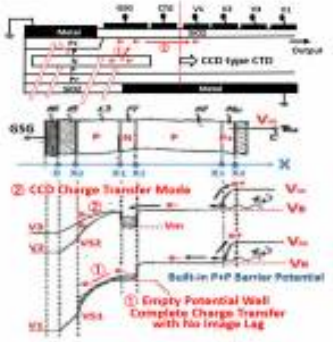


Fig. 4 the P+PNP junction type PPD with the surface P+P barrier electric field used for electron hole pair separation at the surface.

P+PNPP+ junction type Pinned Photodiode Solar Cell

However, the symmetric P+PNPP+ junction type Pinned Photodiode (PPD), as shown in Fig.3, has two PN junction depletion region side by side, and also with the P+P barrier electric fields in both sides. All of them contribute to quantum efficiency. And a solar cell with more than 60% quantum efficiency may not be a dream. The photoelectrons must be collected into the center lightly doped N region, but must be transferred quickly to the adjacent floating N+ heavily doped outlet, keeping the charge collecting N region always empty of electrons with a fixed or pinned empty potential, V_{ss}.

This symmetric P+PNPP+ junction type Buried Depletion and Pinned Photodiode, originally invented for image sensors with back light illumination[2,3] scheme as shown in Fig. 4, is very useful and now applied, not only in the solar cell application as described above, but also modern CMOS image sensor applications as shown in Fig.5.

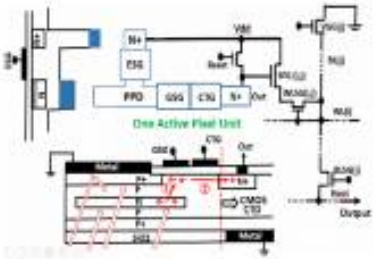


Fig. 5 the P+PNPP+ PPD used in active pixel CMOS image sensor

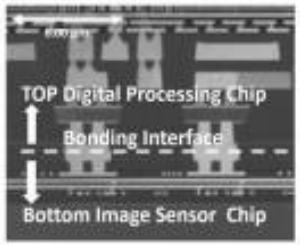


Fig. 6 CMOS image sensor Process applicable to Solar Cell

The symmetric P+PNPP+ junction type Pinned Photodiode (PPD) has three important features[4] of (1) the excellent blue light sensitivity, (2) no surface dark (leakage) current problem and (3) no serious image lag problem with completely depleted empty potential well with CCD like complete signal charge transfer operation mode. These important features are also applied for the proposed symmetric P+PNPP+ junction type PPD solar cell, keeping everywhere with barrier electric field to separate electron hole pairs in the silicon bulk. See Fig.3.

Thanks to the recent advancements of scaling technology of CMOS fabrication process, the modern CMOS image sensors now have, in each pixel, the electrical shutter gate (ESG), the GSG MOS Buffer Memory, and the active in-pixel source follower current amplifier circuits [4, 5]. Now, with the modern 3D stacked multichip integration technology and the very high quantum efficiency solar cell technology, a self-energy intelligent LSI system may not be a dream in near future.

Acknowledgment

The author expresses sincere gratitude to Tetsuhi Shimura, Yasuhiro Ueda, Tadakuni Narabu, Kato Toshio, Yoshiyuki Kawana, and Tsugio Makimoto, my dear friends and respectful mentors throughout private and public life at Sony.

References

[1] Y. Hagiwara, "Simulation and Device Characterization of the P+/N+/P Junction Type Pinned Photodiode and Schottky Barrier Photodiode", IEEE EDTM2020 conference in Penang, Malaysia in March 2020.

[2] Japanese 1973-33647 patent on the backlight illuminated N+NP+/N junction type PPD with the surface N+/N barrier electric field.

[3] Japanese 1975-12695 patent on the P+NPN-sub junction type PPD with the vertical overflow drain (VOD) function and no image lag feature.

[4] Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 1908x1088V CCD imager with narrow channel transfer gates, "Proceeding of the 10th Conference on Solid State Devices, Tokyo, 1978; also in the Japanese Journal of Applied Physics vol. 18, supplement 18-1, pp. 335-340.

[5] Y. Hagiwara, "Multichip CMOS Image Sensor Structure for Flash Image Acquisition", IEEE 3DIC2019 conference in Sendai, Japan

[6] Y. Kamogai, et al, "Back-illuminated 2.74 um-Pixel-Pitch Global Shutter CMOS Image Sensor with Charge-Domain Memory Achieving 10k e- Saturation Signal," IEDM2018, Dec 2018

Simulation and Device Characterization of P+PNPP+ Double Junction Photodiode for Solar Cell Application

Yoshiaki Daimon Hagiwara[1]

[1] Artificial Intelligent Partner System Laboratory
Atsugi-city, 243-0201 Japan

Abstract

A conventional single NP junction type photodiode silicon solar cell is known to have a poor quantum efficiency of about 20% because it can utilize only a single narrow depletion width. This paper reports a P+PNPP+ double junction type photodiode which at least doubles the PN junction depletion width and further more by utilizing the electron hole separation mechanism of the barrier electric field created by the sloped surface P+P doping profile, expecting up to 60 % efficiency.

1. Introduction

The short wave length blue light cannot penetrate silicon crystal more than 0.2 μ m in depth. Most of the sun light energy is concentrated in the short wave blue light spectrum reaching only the floating N+ silicon surface vicinity of 0.2 micro meter in depth. Moreover, in conventional the N+P single junction type solar cells, the N+P junction depletion region width Wd, as shown in Fig. 1, is very narrow because the large portion of the surface portion of the floating N+ region is used as the photo electron storage region which forms the sea of the photo electrons, with a flat photo electron sea level with no barrier electric field where most of the electron hole pairs are recombined and do not contribute to the solar cell quantum efficiency. This is the main reason why the conventional single junction solar cell[1] has a limitation of a poor quantum efficiency of about 20 %.

2. P+P barrier electric field for photo pair separation

Barrier electric field is needed to separate the photo electron and hole pairs in solar cells. There are two methods to create barrier electric field. One approach is to use the PN junction depletion region shown in Fig.1. The second approach utilizes the principle applied in a drift field bipolar transistor[2] base region with the P+P barrier electric field as shown in Fig.2.

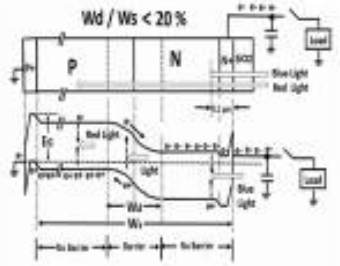


Fig. 1 Conventional Single NP Junction Solar Cell

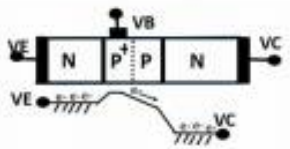


Fig. 2 Drift Field Bipolar Transistor with P+P Barrier Electric Field

The second approach has been applied also in the form of the surface Pinned P+P Hole Accumulation Photodiode[3] (HAD) for highly light sensitive imager sensors. See Fig.3, which shows a cross sectional view of a typical back light illuminated CMOS image sensor in the global shutter scheme with an MOS gate buffer memory (GSG) [3,4]. The barrier electric filed created by the surface P+P impurity doping variation can separate photo electrons pairs created at the near silicon surface P+P region efficiently to achieve the excellent short wave length blue light sensitivity.

Pinned Surface P+PNPP+ double junction type photodiode for solar cell is proposed now in this paper and shown in Fig.4, which doubles the PN junction depletion region width, creating a very wide PN junction type barrier electric field region needed for the photo electron and hole pair separation.

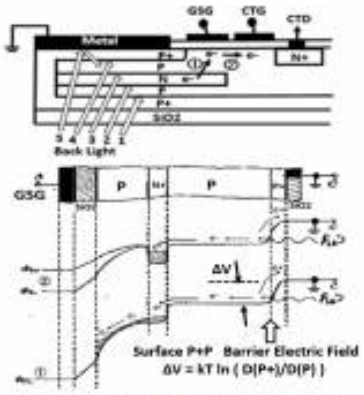


Fig. 3 P+PN+PP+ type Back Light Illumination CMOS Imager

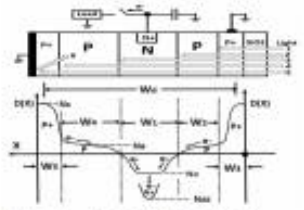


Fig. 4 Doping profile D(x) of P+PNPP+ Solar Cell

3. Numerical Analysis of the P+P barrier electric field

The surface P+P Hole Accumulation Photodiode (HAD) has a smoothly varying shape of Gaussian function given as $G(X) = \exp(-x^2)$. For a double surface ion implantation process we have $D_a(x) = (N_s - N_a)\, G(x/R_s) + N_a\, G(x/R_a)$. The total doping is then $D(x) = D_a(x) + D_d(X_d - x) - N_d$ where Nd is the N-type original substrate doping level. Poisson equations[6] $\partial^2 V(x)/\partial X^2 = \rho(x) / E_s$ was solved numerically for the space charge polarization $\rho(x)$ and the electron potential V(x) with $\rho(X) = D(x) - P(V)$. The positive hole carrier density P(V) is given as $P(V(x)) = N_s \exp(-V(x)/kT)$ while the electron charge concentration N(V(x)) is zero since the N region is completely depleted and no photo electrons present.

If Ns and Na were of uniformly doped average values of the surface P+P regions, the surface barrier potential drop can be obtained as $kT \ln(N_a/N_s) = 0.0776$ eV with $kT = 0.0259$ eV.

Salient physical parameters were set as Nd =100, Na = 10^7, Ns = 5 x 10^3 all in the unit of $e/\mu m^3$ while Ra = 0.57, Rs = 2.5, X_{ox} = 20 in μ m. And the silicon dielectric constant was taken as E_{si} = 648 eV / μ m. Boundary conditions both at x = 0 and x = X_{ox} were set as $V(x) = -E_G = -1.1$ eV, which is at the highest electron energy potential value as shown in Fig.5.

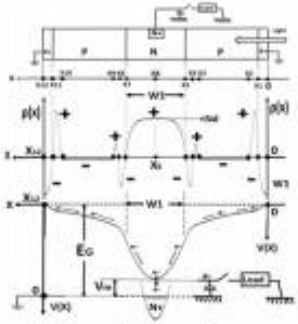


Fig.5 Numerical Calculations of Space Charge Polarization $\rho(x)$ and Electron Potential V(x).

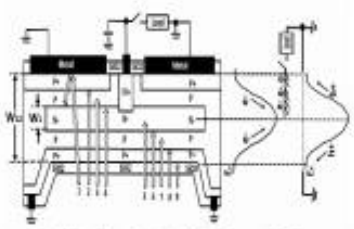


Fig.6 Various Contributions (1~9) to Quantum Efficiency

Note that the empty potential well of the N region is pinned and is given as Vm = – 0.203 eV. All the photo electrons are to be drained down into the center N+ storage region. Other parameters obtained were X_o= 0.828, X_a= 1.726, X_s= 6.315, X_d= 6.705 and X_{ox}=7.292 all in μ m. The buried N region width is given as $W_1 = X_1 - X_o$ = 5.416 μ m. The charge capacity was computed as Qd = 459.5 e / μm^2. The average doping level was then given as <Nd> = Qd/ W_1 = 84.84 e / μm^3 which is close to the initial N type substrate doping level Nd. As shown in Fig.5, note that for this double ion implantation process, the space charge polarization (+ and -) occurs not only at PN junction depletion edges but also at locations of strong P+P barrier electric field for photo pair separation.

Fig. 6 shows various contributions (1~9) to the quantum efficiency of the solar cell including the backside reflection metal.

4. Conclusion

While the conventional single N+P junction type has the low quantum efficiency of 20 %, the P+PNPP+ double junction type Photodiode (PPD) solar cell is expected at least to double the quantum efficiency, and more by the Pinned Surface P+P Hole Accumulation Diode (HAD) image sensor structure.

The surface P+P barrier electric field contributes more to the quantum efficiency, boosting up to 60 % or more for the short wave blue light energy spectrum, and more drastically at the same time, by preventing the hole electron recombination completely in the empty pinned potential well in the N region.

Acknowledgements

The author expresses sincere gratitude to Prof. T.C. McGill, Prof. C.A. Mead, Dr. Tsugio Makimoto, Kiichiro Mukai, Tarushi Shimizu, Yasuhiro Ueda, Tadakuni Narabu, Kato Toshio and Yoshiyuki Kawana, my dear friends and respectful mentors in private and public life.

References

[1] Rühle, Sven. "Tabulated Values of the Shockley–Queisser Limit for Single Junction Solar Cells". Solar Energy. 130: 139–147. Feb 8, 2016.

[2] Herbert Kroemer, "Herb's Bipolar Transistors" IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 48, NO. 11, NOVEMBER 2001

[3] Japanese Patent 1975-117646, 1975-137647, and 1975-124985.

[4] Y Hagiwara, "Simulation and Device Characterization of the P+PN+P Junction Type Pinned Photodiode and Schottky Barrier Photodiode", IEEE EDTM2020 conference in Penang, Malaysia, March 2020.

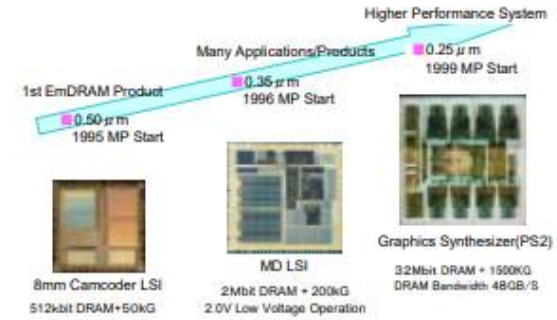
[5] Y. Hagiwara, "Multichip CMOS Image Sensor Structure for Flash Image Acquisition ", IEEE 3DIC2019 conference in Sendai, Japan, Oct 2019.

Microelectronics for Home Entertainment

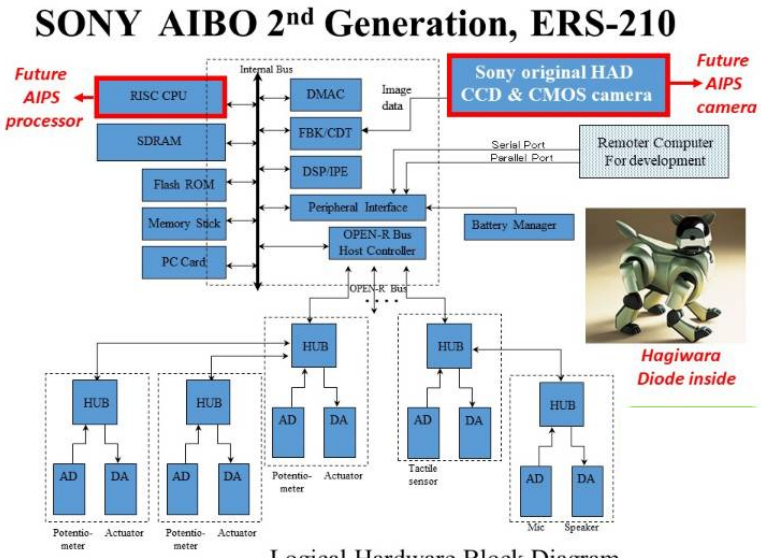
Yoshiaki Hagiwara

Sony Corpoartion, Tokyo Japan
yoshiaki.hagiwara@jp.sony.com

First commercial product for use in consumer products is 0.5 um LSI chips for 8 mm camcorders in 1995. Then we had 0.35 um LSI chips for MD products with low voltage operation of 2.0 volt. Now 0.25 um PlayStation 2 Graphics Synthesizer has eDRAM with 48 GB/sec bandwidth. Fig.19 shows the EmDRAM History.



Embedded DRAM History



Logical Hardware Block Diagram

https://20201128200256965733O.onamaeweb.jp/AIPS_Library/P2001_ESSCIRC2001.pdf

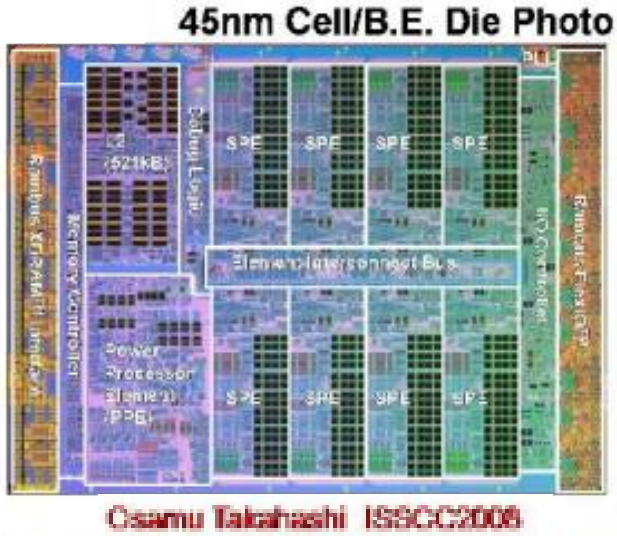
SOI Design in Cell Processor and Beyond

Yoshiaki Daimon Hagihara

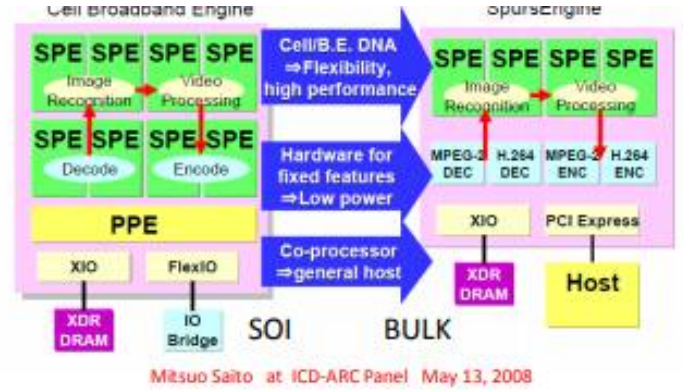
Chairman and CEO , AIPS/AINS Consortium

(Ex-Sony Fellow, Semiconductor Strategic Planning)

Hagihara-Yoshiaki@aiplab.com



By 1994, the games were just starting to move to 0.5-micron processes, while the leading process was 0.35 micron. Eventually over time, the game chips migrated to smaller processes to increase integration and reduce costs.



Cell/B.E. and Toshiba SpursEngine

To address the latency issue, the emotion engine was developed in 1998. This groundbreaking graphics chip needed the latest technologies to achieve its performance and level of integration. By reducing the number of pipeline stages and increasing integration – with 10.5 million transistor and a 128-bit dual vector processor – the Playstation pushed all of the existing limits of the 250-nanometer process.

https://202011282002569657330.onamaeweb.jp/AIPS_Library/P2008_ESSCIRC2008Hagiwara.pdf

Reference

Buried Pinned Hole Accumulation Photodiode

Invention 1975

Japanese Patent Applications 1975-127646, 1975-127647,

and 1975-134985 invented by Y.Hagiwara

Development 1978

Y. Hagiwara, M. Abe, and C. Okada,

"A 380H x 488V CCD imager with narrow channel transfer gates",

Proc. The 10th Conference on Solid State Devices, Tokyo, (1978):
Japanese Journal of Applied Physics, vol. 18, Supplements 18-1,
pp. 335-340, (1979)

Reference

Electric Shutter Clocking Scheme

Invention 1975

Japanese Patent Application 1977-126885

invented by Y. Hagiwara, S. Ochi and T. Hashimoto.

Development 1987

Masaharu Hamazaki, Tomoyuki Suzuki, Noriaki Kagawa,
Kikue Ishikawa, Katsurou Miyata, Hideo Kanbe,
"ILT CCD Image Sensor with Electrical Shutter Fuction Control",
Journal of Japanese TV Society, vol.12, no.12, pp.31-36, (1988)

Invention 1975 — Electric Shutter Clocking Scheme

Japanese Patent Application 1977-126885

invented by Y. Hagiwara, S. Ochi and T. Hashimoto.

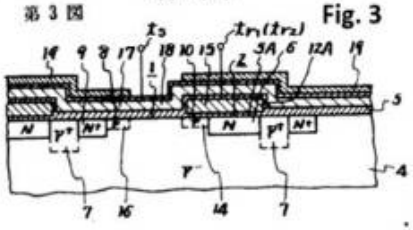
Japanese Patent JPA 1977-126885 on Electrical Shutter Clocking Scheme invented by Y. Hagiwara, S. Ochi and T. Hashimoto in 1977.

⑩公開特許公報 (A) 昭54—51318

⑳特　　願　昭52—126885
㉒出　　願　昭52(1977) 9 月29日
㊸公開　昭和54年(1979) 4 月23日
㉗発 明 者　荻原良昭
㉗発 明 者　越智成之
　同　　橋本武夫

Type(A)

第 3 図 Fig. 3



Type(B)

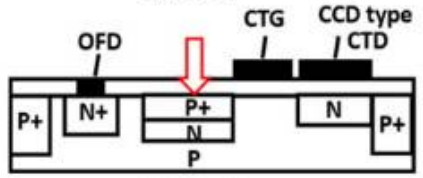
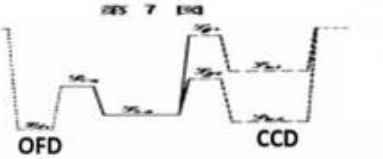
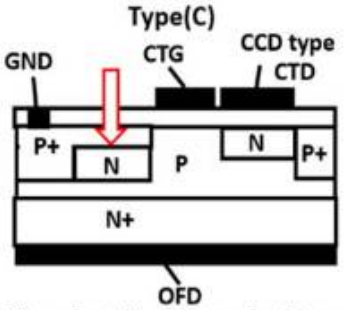


Fig. 7



Type(C)



Type(D)

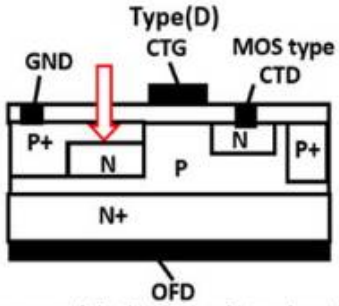


Fig. 8

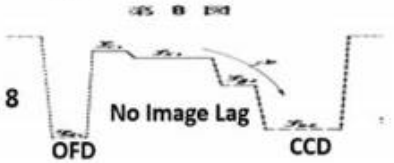
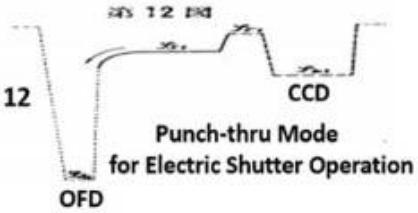


Fig. 12



The electric shutter clocking scheme with the complete signal charge draining of no image lag can be achieved by the OFD punch-thru voltage control for any photodiodes, including not only the type (A) of the conventional CCD/MOS photo capacitor but also (B), (C) and (D) type Pinned Photodiodes.

Reference

****
Active in-Pixel MOS Image Sensor
****

Invention 1968

++

Peter J. W. Noble,

IEEE Transaction of Electron Devices, 15-4, pp.202-209, (1968)

++

Development 1990

++

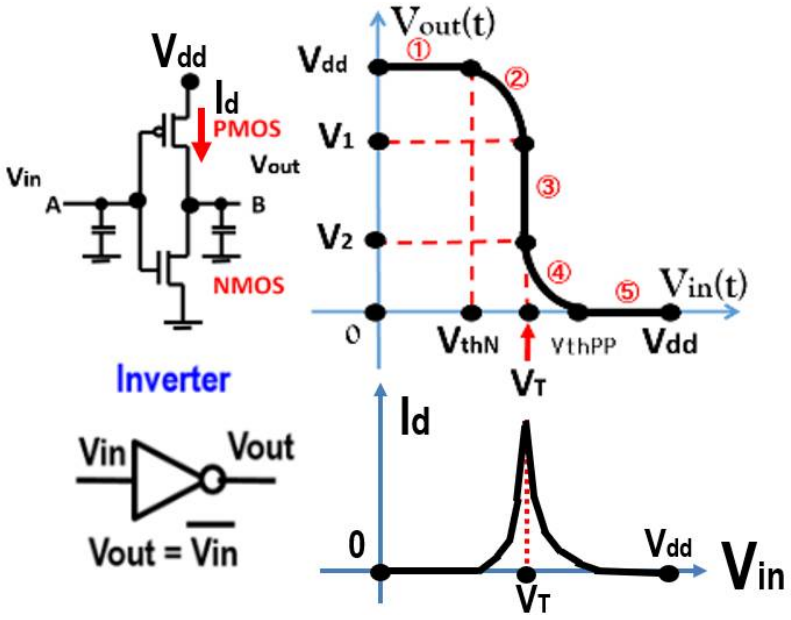
Fumihiko Andoh, Kazuhisa Taketoshi, Junichi Yamazaki,
Masayuki Sugawara, Yoshi hiro Fujita, Kohji Mitani,
Yukio Matuzawa, Kenji Miyata, Shuichi Araki,

"A 25 0,000-Pixel Image Sensor with FET Amplification
at Each Pixel for High-Speed Television Cameras",

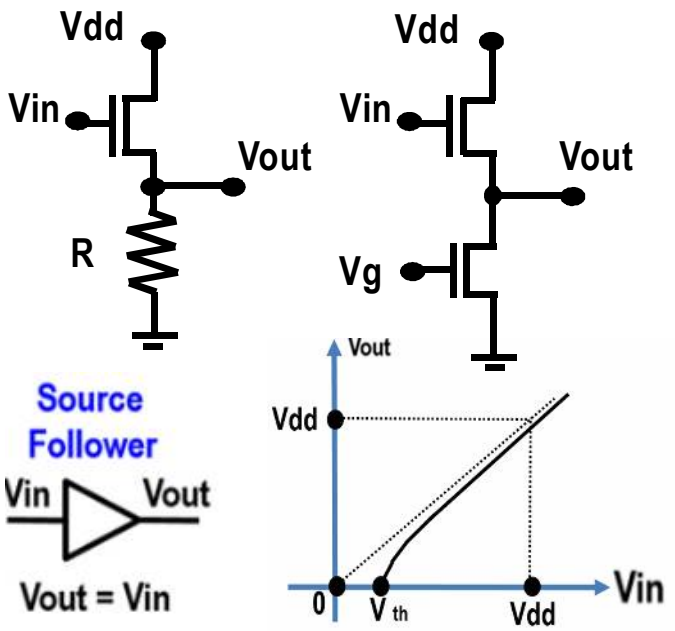
ISSCC Digest of Technical Papers, pp. 212-213,298, February 1990.

++

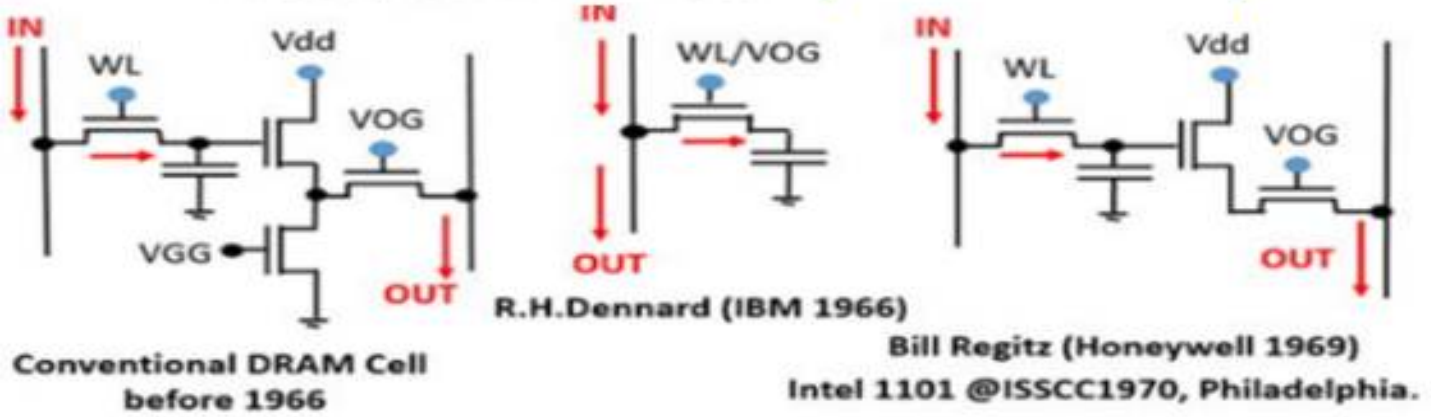
● Low Power CMOS inverter



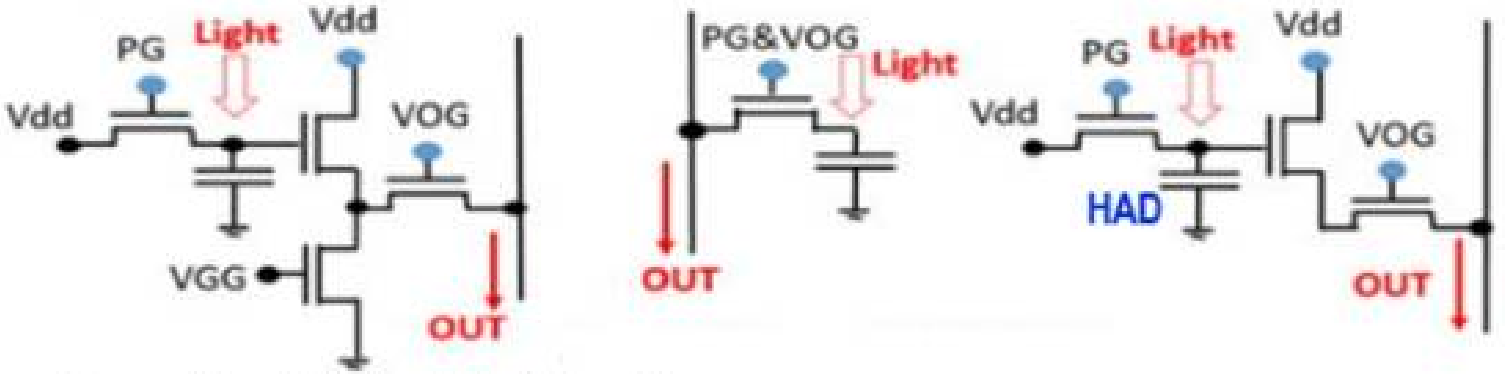
● Source Follower Current Amplifier



History of DRAM Cell (Source Follower)



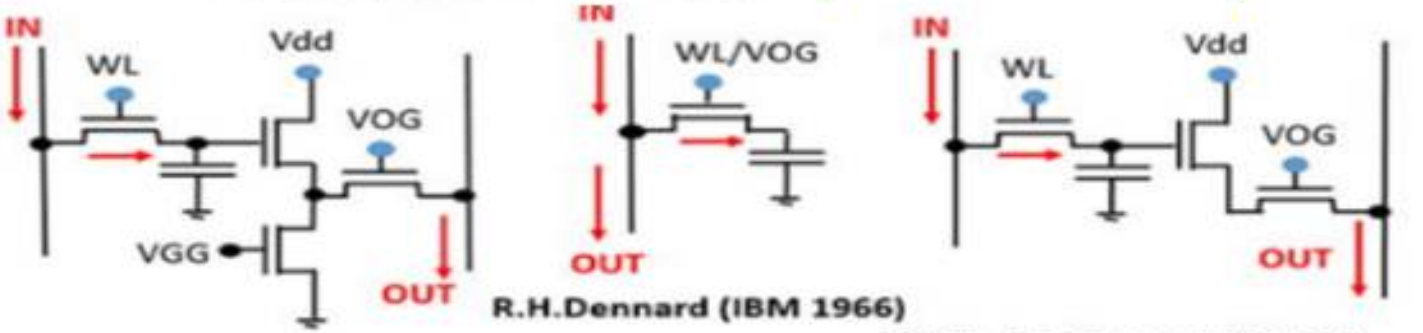
History of Photo Diode Cell (Source Follower)



Conventional Active Pixel Circuit
Photo Diode in 1966

after Peter Nobel,1966~1968

History of DRAM Cell (Source Follower)

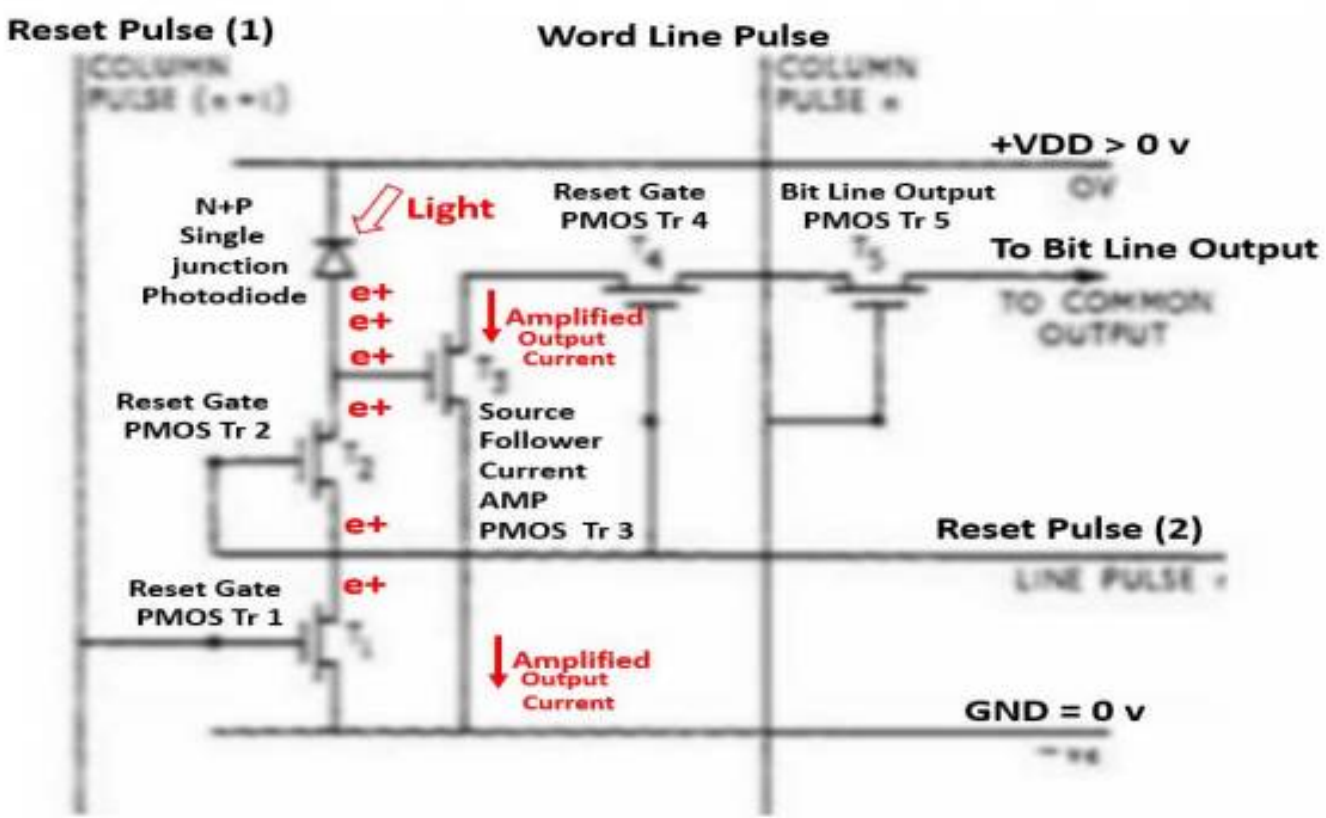


Conventional DRAM Cell
before 1966

R.H.Dennard (IBM 1966)

Bill Regitz (Honeywell 1969)
Intel 1101 @ISSCC1970, Philadelphia.

Peter Noble invented the in-Pixel Amp MOS Image Sensor in 1968.
See IEEE Transaction Electron devices 15-4 (1968) pp.202-209.



Active Pixel Sensor (APS) with a photodiode and buffer amplifier as proposed by Peter Noble in 1968

＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊

●CCD Image Sensor

＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊

Invention and Development 1970

++

W.S.Boyle and G.E. Smith,

Bell System Technical Journal, 49, pp.587-593(1970)

++

＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊

Correlated Double Sampling (CDS) Hold Circuit

＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊＊

Invention and Development 1974

++

M.H.White, D.R.Lanpe, F.C.Blaha and I.A.MAck,

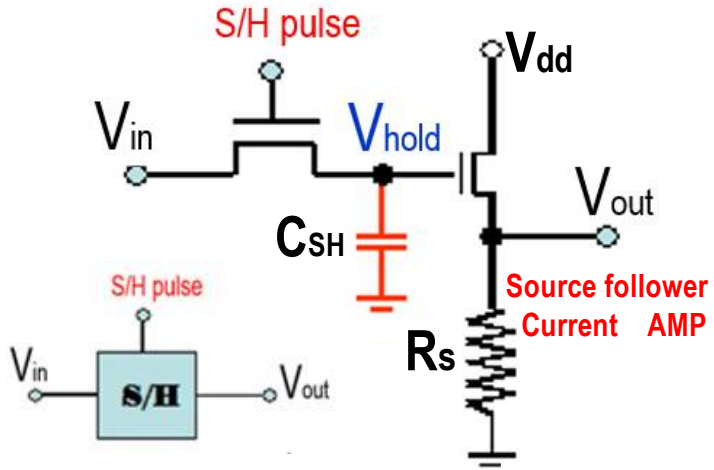
"Characterization of Surface Channel CCD Image Arrays at Low Light Level.

IEEE Journal of Solid State Circuits, SC-9, pp.1-13 (1974)

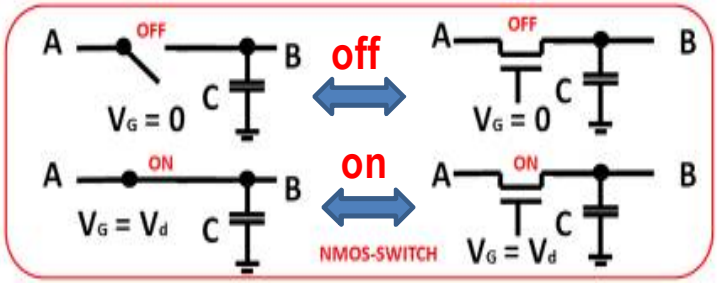
++

Correlated Double Sampling Hold by Prof. M. White, 1972

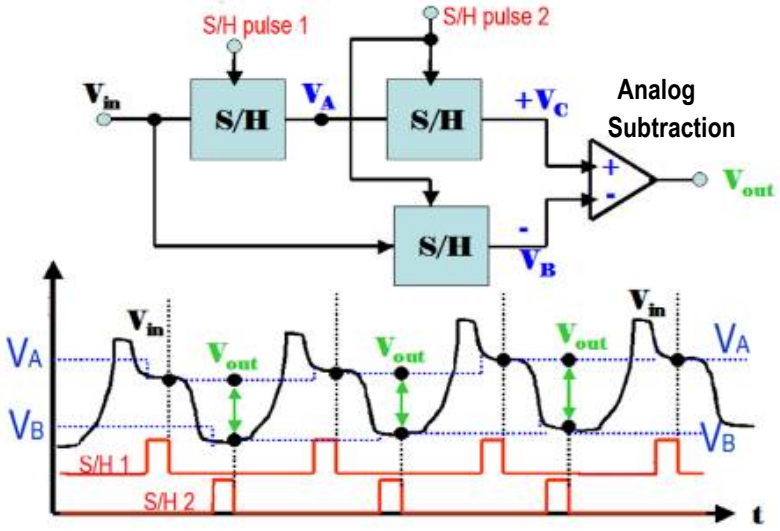
Conventional Single Sampling Hold



MOS Transistor Switch ON/OFF Action



Correlated Double Sampling Hold (CDS)



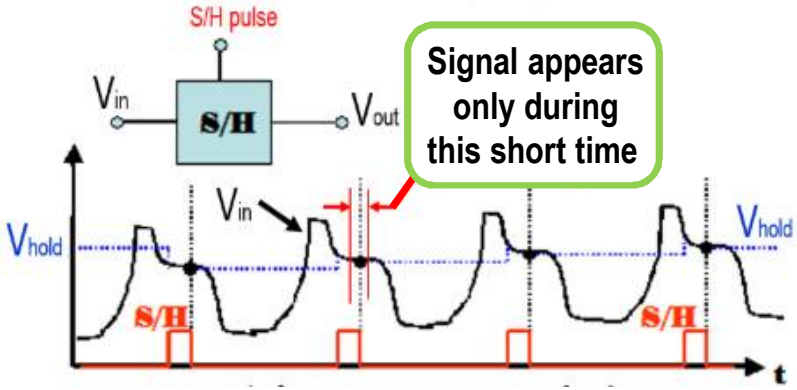


Image Sensor Signals are buried in the clock noises.

27.5 High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor

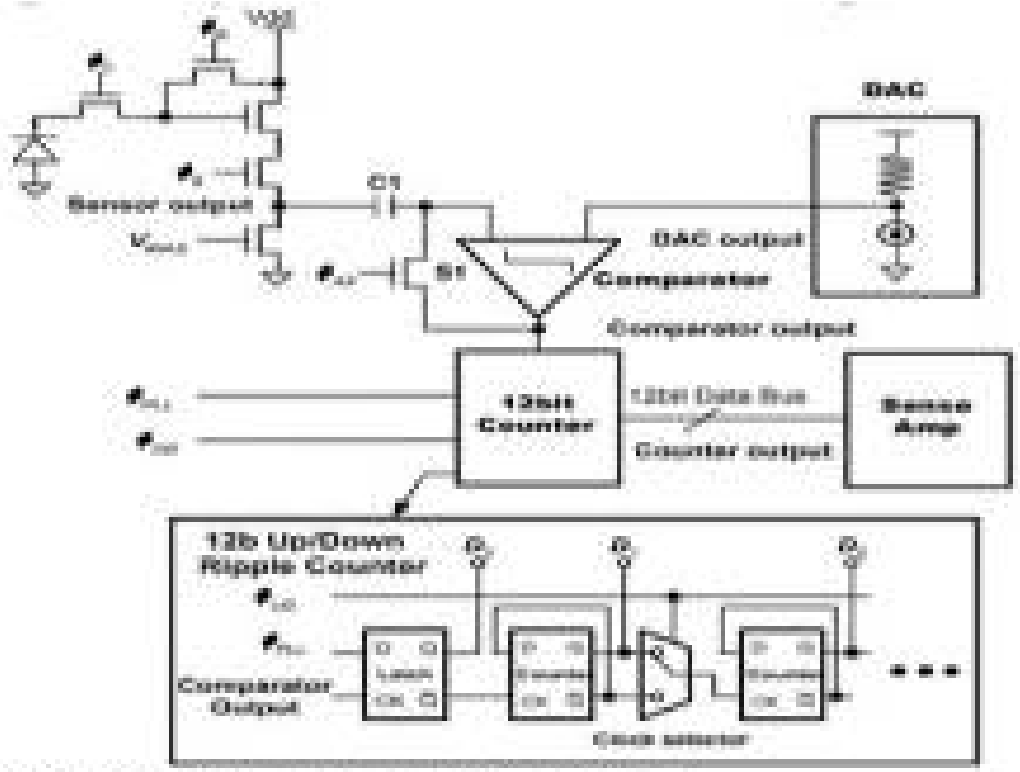


Figure 27.5.2: Column-inline dual CDS architecture.

ISSCC 2006 / SESSION 27 / IMAGE SENSORS / 27.5

ISSCC 2006 / SESSION 27 / IMAGE SENSORS / 27.5

Modern CMOS Image Sensors have (1) HAD (2) APS and (3) CDS.

(1) HAD (PPD) was invented by Y. Hagiwara in 1975.
(2) APS was invented by Peter Noble in 1968.
(3) CDS was invented by M. White in 1972.
(4) Sony engineers perfected these technologies in 2006.

27.5 High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor

Yoshikazu Nitta, Yoshinori Muramatsu, Kiyotaka Amano, Takayuki Toyama, JunYamamoto, Koji Mishina, Atsushi Suzuki, Tadayuki Taura, Akihiko Kato, Masaru Kikuchi, Yukihiro Yasui, Hideo Nomura, Noriyuki Fukushima

Sony, Atsugi, Japan

Traditionally, the advantages of compact image sensors (CISs) over CCDs have been low power consumption and the capability for system integration. Additionally, the image quality of CISs has recently begun to rival and even surpass that of CCDs in the area of high-speed imaging [1]. Compared to high-speed CCDs, CISs utilize the advantage of a column-parallel pixel readout.

The pixels are conventional 4T active pixel sensor (APS) pixels that use hole accumulation diodes (HADs). HADs enable image sensors such as CCDs and CISs to realize ideal properties of low dark current, no kTC noise, and no image lag [2]

Digital double-sampling architecture is proposed to remove device variation and circuit offset that cause vertical FPN [3]. Our column-inline dual-CDS architecture (Fig. 27.5.2) implements digital double-sampling (digital CDS) and analog CDS in parallel columns. A high-speed 297MHz clock is utilized to reduce the double digital sampling period. Additionally, an analog CDS is used to reduce the ADC period for the reset signal V_{RST} by eliminating the analog offset of the pixel and the comparator output.

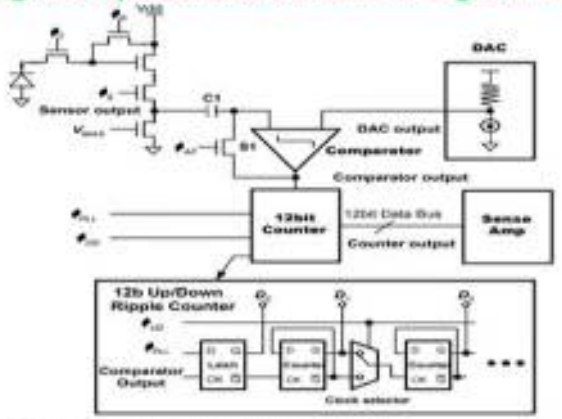


Figure 27.5.2: Column-inline dual CDS architecture.

References:

[1] A. I. Krymski, N. E. Bock, N. Tu, D. Van Blerkom, E. R. Fossum, "A High Speed, 240frames/s, 4.1-Megapixel CMOS Sensor," *IEEE Trans. Electron Devices*, vol. 50, no. 1, pp. 130-135, Jan., 2003.

[2] K. Mabuchi, N. Nakamura, E. Funatsu, T. Abe, T. Umeda, T. Hoshino, R. Suzuki, H. Sumi, "CMOS Image Sensor Using a Floating Diffusion Driving Buried Photodiode," *ISSCC Dig. Tech. Papers*, pp. 102-103, Feb., 2004.

Hagiwara 1975 invention (JPA 1975-134985)

[3] W. Yang, O. Kwon, J. Lee, G. Hwang, S. Lee, "Integrated 800×600 CMOS Imaging System," *ISSCC Dig. Tech. Papers*, pp.304-305, Feb., 1999.

Why is SONY so strong in Semiconductor Business from the beginning to now ?

(0) Sony could purchase the Bipolar Transistor Patent Right with a very low price of $ 500 (?) from Bell Lab USA in 1954.

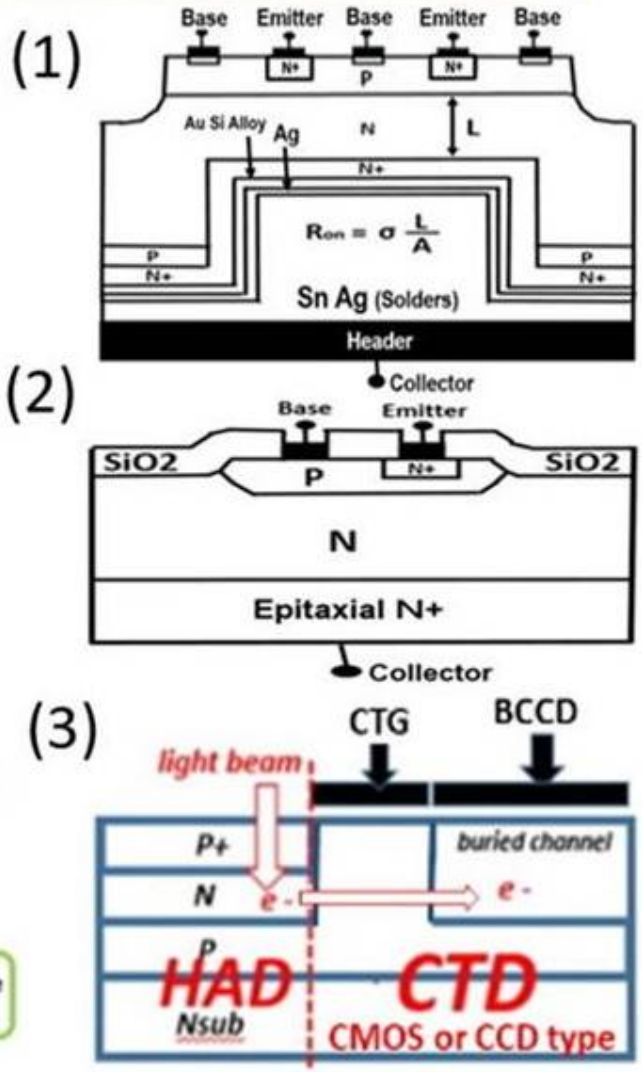
(1) Kawana, Yoshiyuki at Sony invented the low collector On-Resistance N+PN junction type Bipolar transistor by thinning the back side of silicon wafer, a technique now used for the backside illumination CMOS image sensors widely to improve sensitivity.

(2) Kato, Toshio at Sony invented the silicon surface light etching and new SiO2 Passivation technique for the N+PN junction type Bipolar transistor with the MESA like isolation, which is now known as the shallow trench isolation with the excellent side wall SiO2 formation to reduce the leakage current.

(3) Hagiwara, Yoshiaki at Sony invented the P+NPNsub junction (thyristor) type Pinned Photodiode, which is identical to SONY Hole Accumulation Diode (HAD), with the built-in vertical overflow drain (VOD) function, the image lag free electric shutter function and good light sensitivity to realize fast action video cameras.

See Japanese Patent 1975-134985

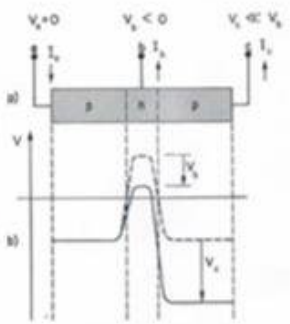
Hagiwara invented SONY HAD which is identical to the Pinned Photodiode which is also the Depletion Photodiode and the Buried Photodiode.



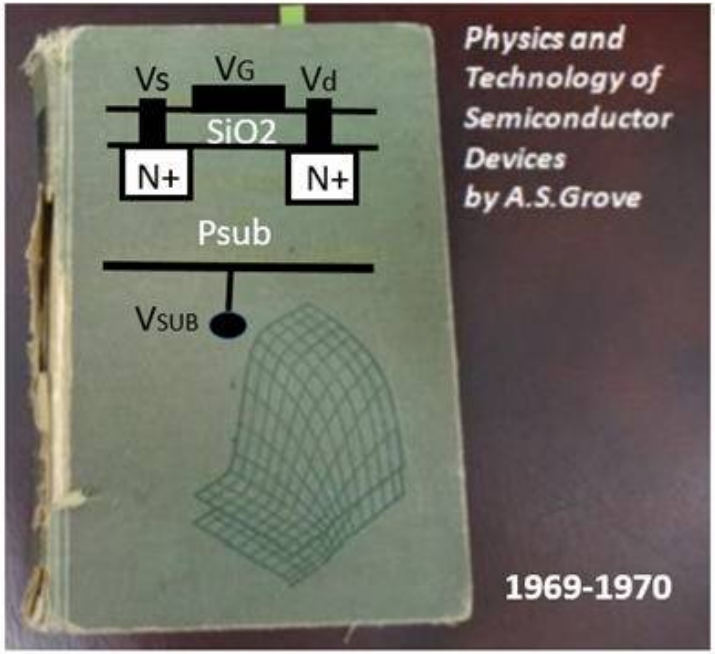
with Prof. James McCaldin @Newport Beach

with Prof. Tom McGill @Caltech Campus

Feynman Physics 1967-1969



Bipolar Transistor



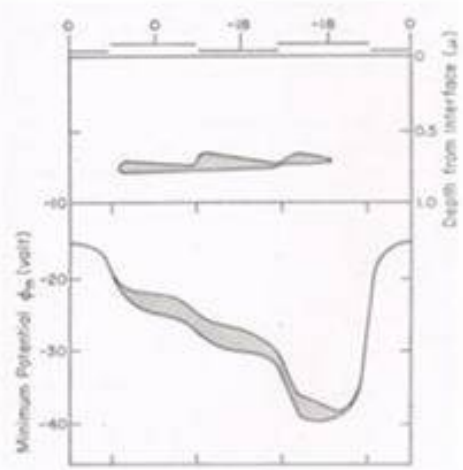
Hagiwara had five important ideas in 1975 for the pinned photodiode sensor structures.

Charge-Coupled Devices and Applications

Chairman

Lewis M. Terman

My PhD thesis paper
on buried channel CCD
at ISSCC1974 in Philadelphia, USA



Prof. T. C. McGill

Prof. C. A. Mead

My first publication was a PhD thesis paper published at the ISSCC1974 in Philadelphia in Feb 1974. CalTech/JPL NASA (IBM) computers were used to perform three dimensional (x, y and t) BCCD device simulations for polysilicon and aluminum overlapping gate buried channel CCD structure with the two dimensional Poisson 's equation and time domain continuity equation.

See Japanese Patent 1975-134985 (filed on November 10, 1975)

which defines a P+NP/Sub junction type Pinned Photodiode with Vertical Overflow Drain (VOD)

Sony Original HAD Sensor

HAD = Hole Accumulation Diode

And see also Japanese Patent 1975-127647 (filed on October 23, 1975)

which defines an NPN/Sub junction type Pinned Photodiode with a built-in Global Shutter Function and Back Light Illumination Scheme

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976

128-Bit Multicomparator

CARVER A. MEAD, RICHARD D. PASHLEY, MEMBER, IEEE, LEE D. BRITTON, YOSHIAKI T. DAIMON, AND STEWART F. SANDO, JR., MEMBER, IEEE

Abstract—A 128-bit multicomparator was designed to perform the search-sort function on arbitrary length data strings. Devices can be cascaded for longer block lengths or paralleled for bit-parallel, word-serial applications. The circuit utilizes a 3-phase static-dynamic shift register cell for data handling and a unique gated EXCLUSIVE-NOR circuit to accomplish the compare function. The compare operation is performed bit parallel between a "data" register and a "key" register with a third "mask" register containing don't care bits that disable the comparator. The multicomparator was fabricated using p-channel silicon-gate metal-oxide-semiconductor (MOS) technology on a 167 × 159 mil chip containing 3350 devices. With transistor-transistor logic (TTL) input, data rates in excess of 2 MHz have been attained. The average power dissipation was 250 mW in the dynamic mode and 300 mW in the static mode.

Introduction

OVER the past several years, there have been significant amounts of energy devoted to the fabrication of larger and faster semiconductor memories and conventional central processing units (CPU's) in chip form. In the process, many other applications of large-scale integration (LSI) to computer architecture have been neglected [1]. LSI has removed the technological distinction between logic and memory. It is now economically feasible to decentralize the CPU of a computer by replacing much of its maintenance software with functional hardware to improve system efficiency. Presently, an inordinate amount of processing time is spent on organizing and accessing files in peripherals. Peripherals are usually controlled directly by the CPU and have little or no associated logic of their own. A great improvement in this situation can be made by developing peripheral logic units. This would allow each peripheral to accomplish its own internal processing and thus reduce CPU housekeeping duties. This paper describes a 128-bit multicomparator that is designed to perform the search-sort function.

The block diagram of the multicomparator is shown in Fig. 1. The circuit consists of three independently clocked static-dynamic shift registers with associated EXCLUSIVE-NOR gating. In operation, the device indicates a match between the data word and the unmasked bits of the key word. The multicomparator is loaded with a key word by serially shifting the word into the key register and locking the register in static mode. While the key word is being loaded, the comparator is enabled by entering zeros[1] in the appropriate locations of the mask register. Masking allows the multicomparator to search for bit strings of varying length and composition. For example, assume it is necessary to search for all words containing a specific 113-bit code. By entering the 113-bit code in the key register and masking out the rest of the comparator, the multicomparator is conformed to search for this code wherever it occurs in the data file. Once the multicomparator is loaded with "key" and "mask" words, the file being searched is serially shifted through the data register. The data words are compared in bit parallel with the unmasked bits of the key word as they pass through the data register. When a match is found, the compare output goes high.

Large multicomparators can be constructed of the 128-bit circuits. Cascaded [Fig. 2(a)], the comparator can be used to search for words longer than 128 bits. By implementing multicomparators in parallel [Fig. 2(b)], a word-serial, bit-parallel

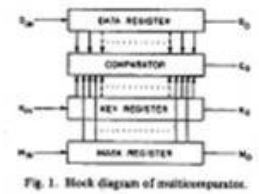


Fig. 1. Block diagram of multicomparator.

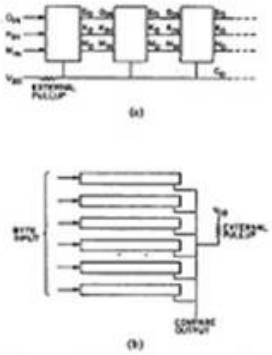


Fig. 2. Possible connections of multicomparator. (a) Cascaded. (b) Bit-parallel, word-serial.

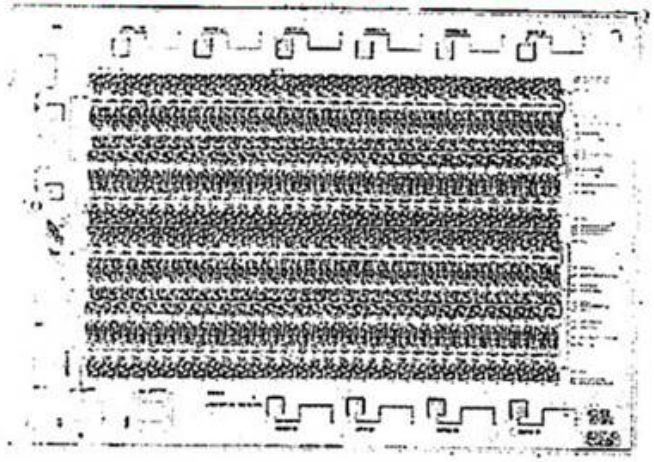
Manuscript received March 15, 1976; revised July 18, 1976.

C. A. Mead is with the California Institute of Technology, Pasadena, CA 91125.
R. D. Pashley and S. F. Sando, Jr., are with the Intel Corporation, Santa Clara, CA.
L. D. Britton is with the Hewlett-Packard Laboratories, Cupertino, CA.
Y. T. Daimon is with the Sony Corporation, Tokyo, Japan.

[1]Voltage convention: high="1"=V_{DD}, low="0"=V_{CC}. Note that since V_{DD} is negative for p-channel MOS and positive for n-MOS transistor-transistor logic (TTL) levels may or may not have reverse polarity depending on the processing used.

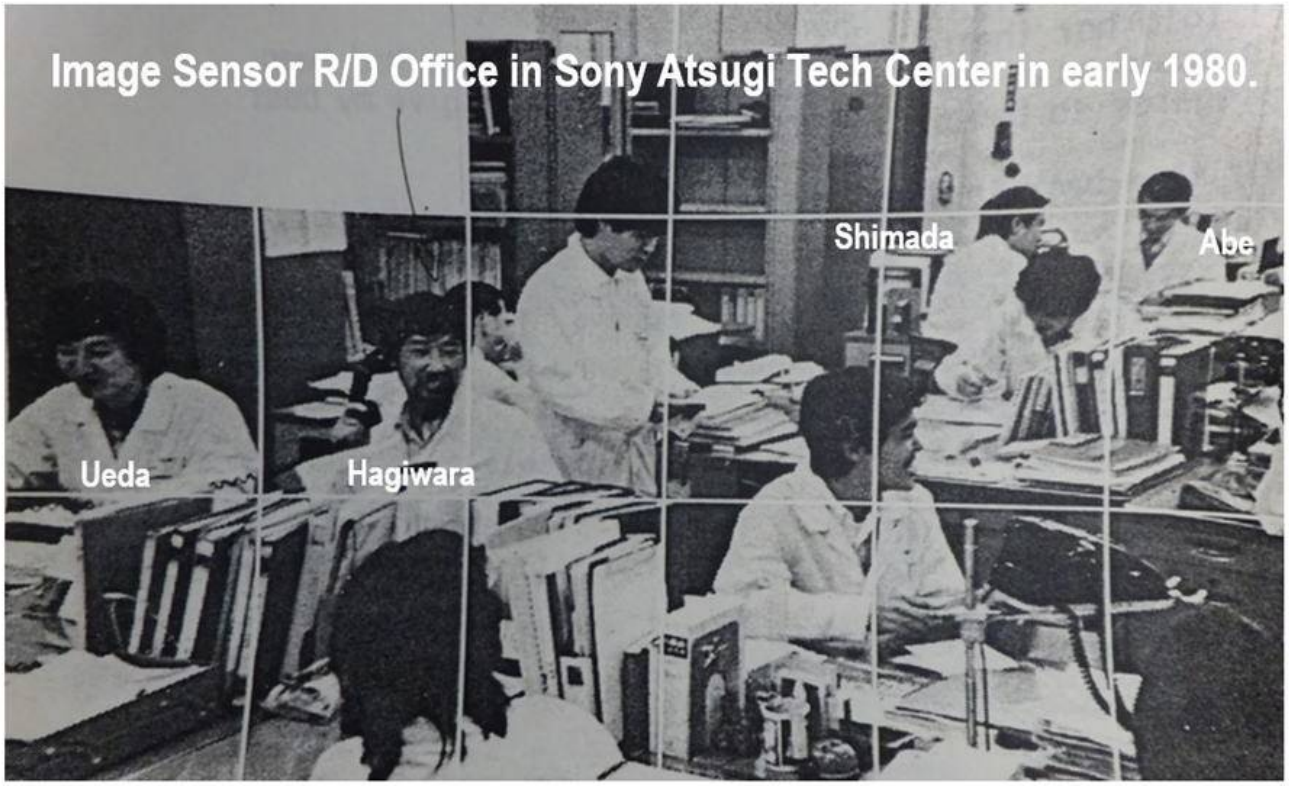
Prof. C. A. Mead and Yoshiaki Daimon Hagiwara working on the silicon chip design at Caltech in 1972

128-bit Multicomparator chip, designed by Hagiwara in 1972-1973 and fabricated by Intel PMOS process.



Acknowledgements

The author expresses sincere gratitude to Prof. T. C. McGill, Prof. C. A. Mead, Prof. James McCaldin, Dr. Tsugio Makimoto, Kiichiro Mukai, Terushi Shimizu, Yasuhiro Ueda, Dr. Tadakuni Narabu, Kato Toshio, Seiichi Watanabe and Yoshiyuki Kawana, my dear friends and respectful mentors in private and public life.



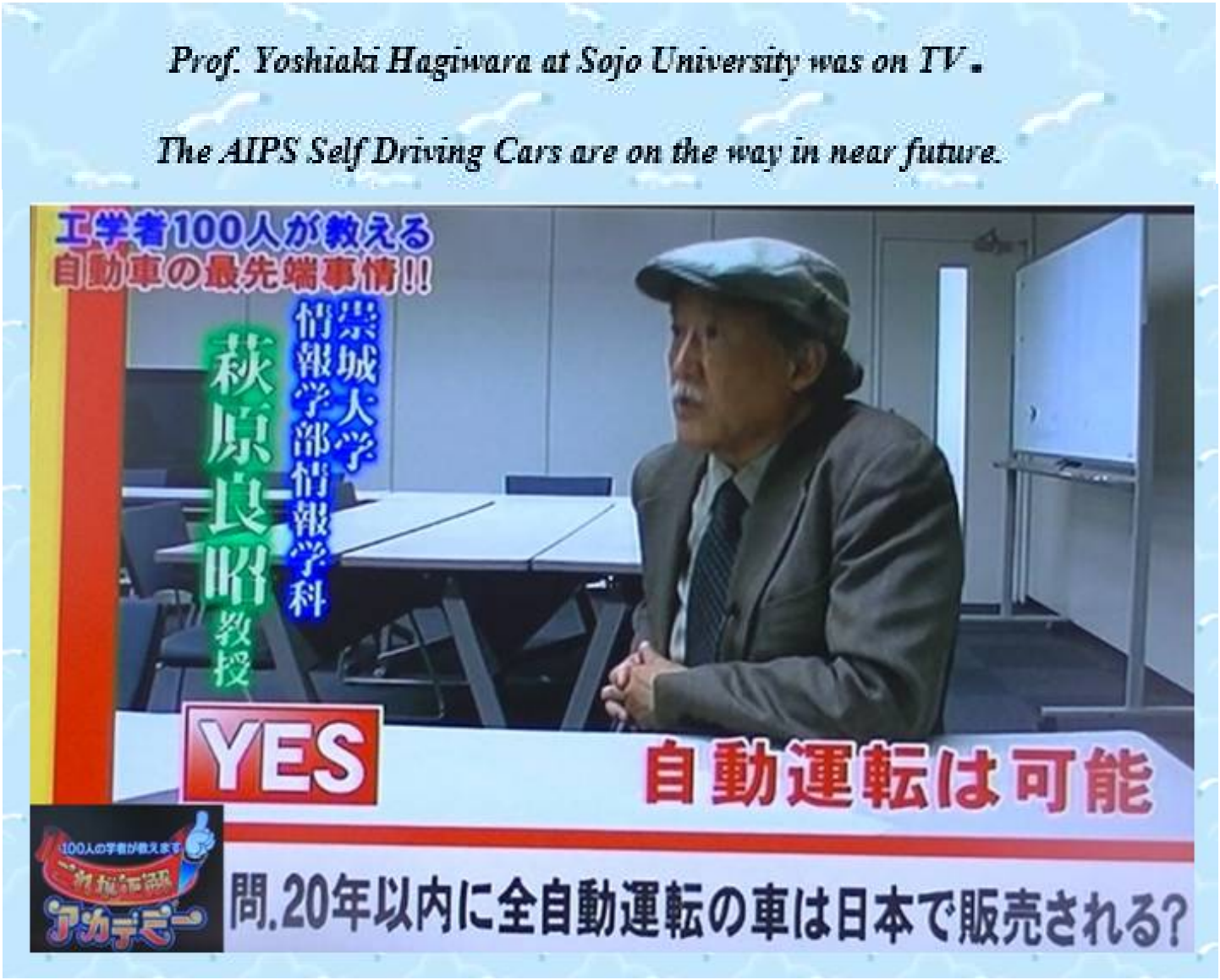
Yoshiaki Daimon Hagiwara BIO in 1976

Yoshiaki Hagiwara was born in Kyoto, Japan, on July 4, 1948. He received the B.S., M.S., and Ph.D. degrees from the California Institute of Technology, Pasadena, in 1971, 1972, and 1975, respectively.

Since 1967, he has served several research groups in the Institute. He worked as a Data Processor in hydraulics from 1967 to 1969, engaging in the analysis of the pressure distribution of solitary waves, the influence of the geological features of a harbor upon the induced standing-wave amplitude in the harbor, and the diffusion mechanism of polluted objects in moving fluids. From 1969 to 1971, he worked as an Experimentalist in the Material Science Department and studied the switching and other electronic properties of newly developed amorphous alloys from the low temperature of 4 K to room temperature. From 1971 to 1975 he was a Research and Teaching Assistant both in the Electrical Engineering and Physics Departments at the California Institute of Technology. In the summer of 1971 and 1973, he visited Sony Corporation, Tokyo, Japan, as a Product-Appraisal Engineer at the Atsui plant and engaged in developments and applications of bipolar technologies in video and power integrated circuits. He is presently with the Sony Corporation, Tokyo, Japan. His interests lie in the areas of digital and linear integrated circuit designs, the physics of microelectronics, and artificial intelligence.

Prof. Yoshiaki Hagiwara at Sojo University was on TV .

The AIPS Self Driving Cars are on the way in near future.



Artificial Intelligent Partner System(AIPS) Home Page Top

hagiwara-yoshiaki@aiplab.com