A 25-ns 4-Mbit CMOS SRAM with Dynamic Bit-Line Loads

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has been developed. The RAM was fabricated using a 0.5-μm ... and double-aluminum CMOS technology and was assembled ... 400-mil DIP. A small cell size of 3.6×5.875 μm² and a chip ...46×17.41 mm² were obtained. A fast address access time of 25 ... a single 3.3-V supply voltage has been achieved using our newly ... dynamic bit-line load (DBL) circuit scheme incorporated with an ... transition detector (ATD), divided word-line structure (DWL), ... sense amplifier, and low-noise output circuit approach. A low ... current of 46 mA at 40 MHz and low standby currents of 70 μA ... 5 μA (CMOS) were also attained.

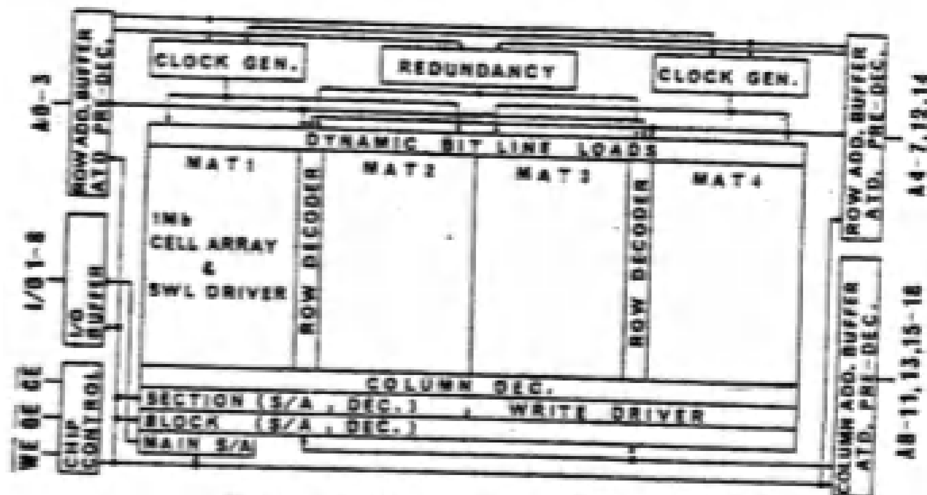


Fig. 1. Block diagram of the RAM.

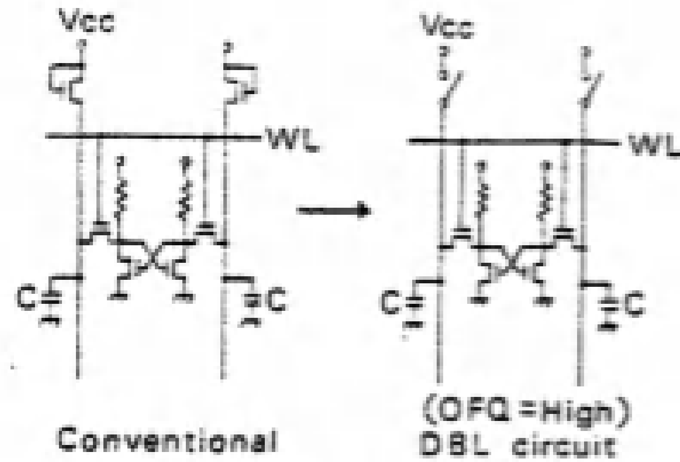


Fig. 6. Concept of DBL.

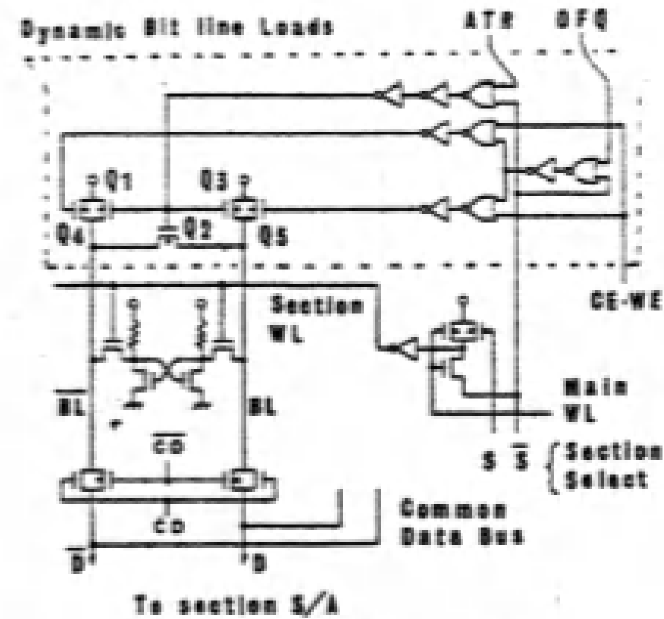
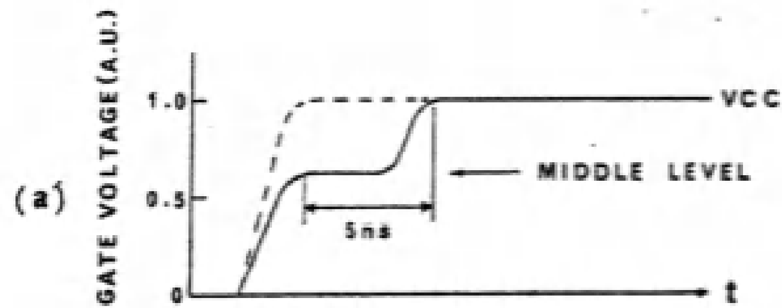
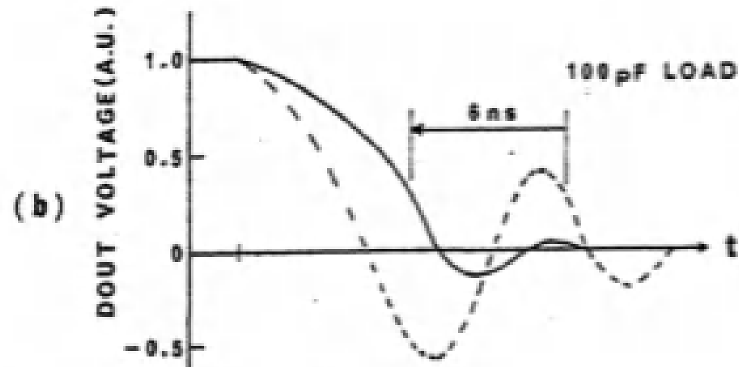


Fig. 4. DBL circuit.





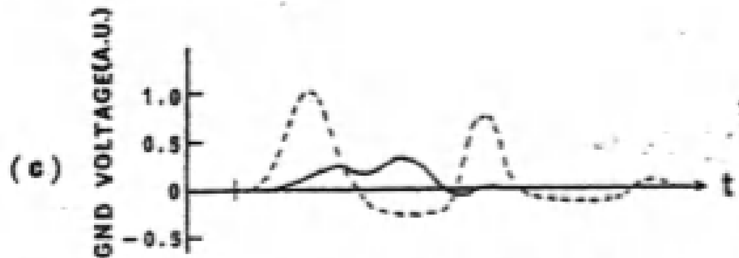


Fig. 9. Waveforms of proposed (solid line) and conventional (dotted line) output circuits: (a) gate bias, (b) data output, and (c) GND bounce.

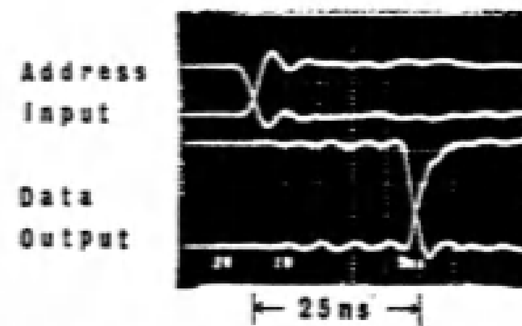


Fig. 10. Waveforms of the address access time.

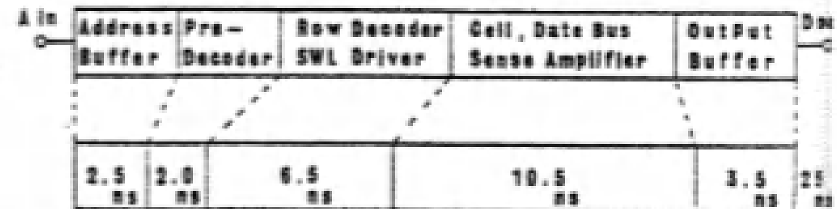


Fig. 11. Components of the access time in the 4-Mbit SRAM.

against collection of charge carriers from the substrate the retrograde P-well with a 1.2-μm junction depth used. This technology utilizes a double-level polysili and a double-level aluminum layer. The gate oxide thi ness is 11 nm. The first polysilicon layer, tungsten po cide, is used for gate electrodes, and the second polysili layer is used for high-resistance memory cell loads. T first aluminum is used for GND lines in the memory and the main word lines to reduce the delay time. T second aluminum is used for the bit lines to reduce stray capacitance. The minimum contact and via hole si

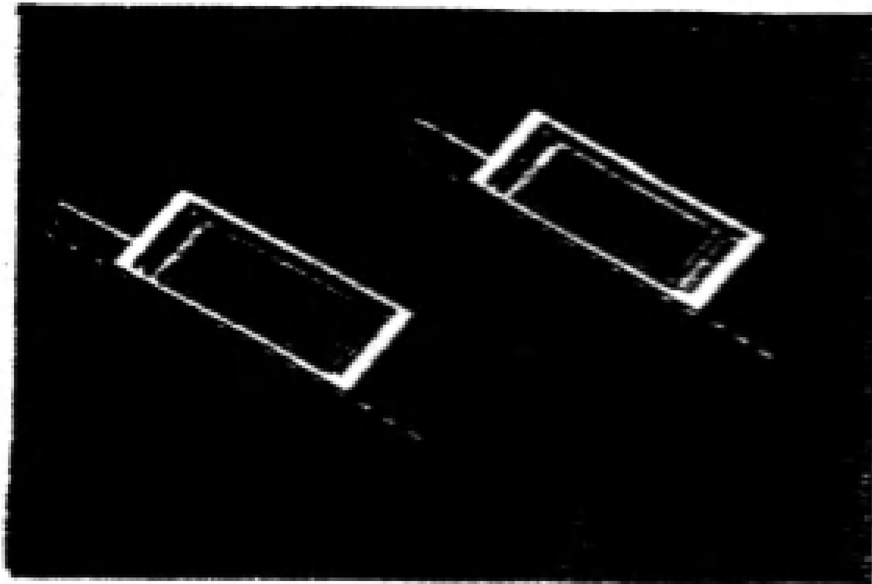


Fig. 12. 4-Mbit SRAM assembled into a 400-mil DIP.

TABLE I
TYPICAL CHARACTERISTICS

Organization	512KW x 8bit
Chip size	7.46 x 17.41 mm²
Cell size	3.6 x 5.875 um²
Power supply	3.3V
Address access time	25ns
Active current	33mA at 10MHz
	46mA at 40MHz
Standby current	70uA at V_{IH}=2.2V
Package	32Pin. 400mil DIP
Redundancy	8 rows

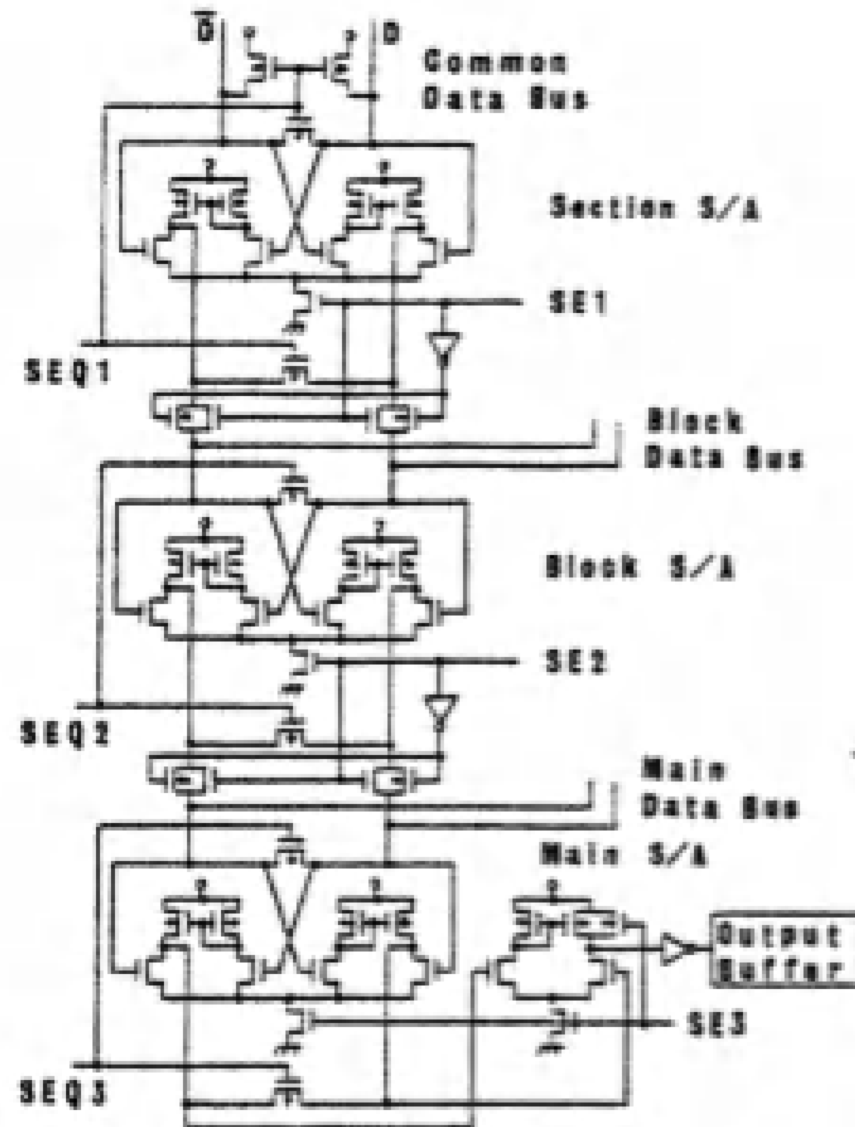


Fig. 7. Three-stage sense amplifier circuit.