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A 380H × 488V CCD Imager with Narrow Channel Transfer Gates

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The original P+NP junction type Pinned Photodiode Paper reporting the excellent Blue light sensitivity and the very low dark current level of the Pinned Photodiode image sensor.

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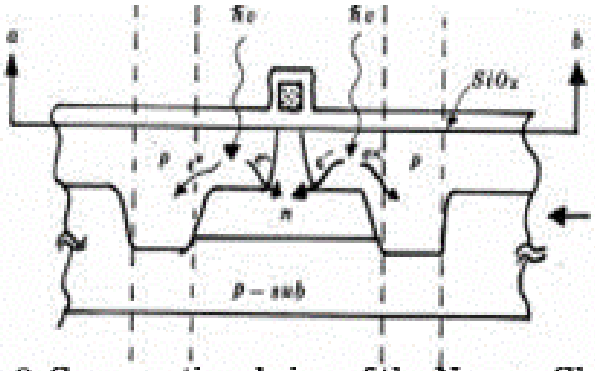

Fig.3 Cross sectional view of the Narrow Channel Transfer Electrode with the SiO2 exposed Pinned Window and the Pinned Photodiode P+ surface.

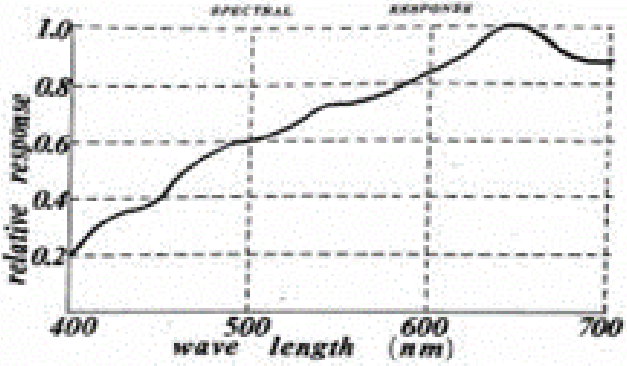

Fig.13 Spectral Response of the Pinned Photodiode with Pinned SiO2 Window and Pinned Surface.

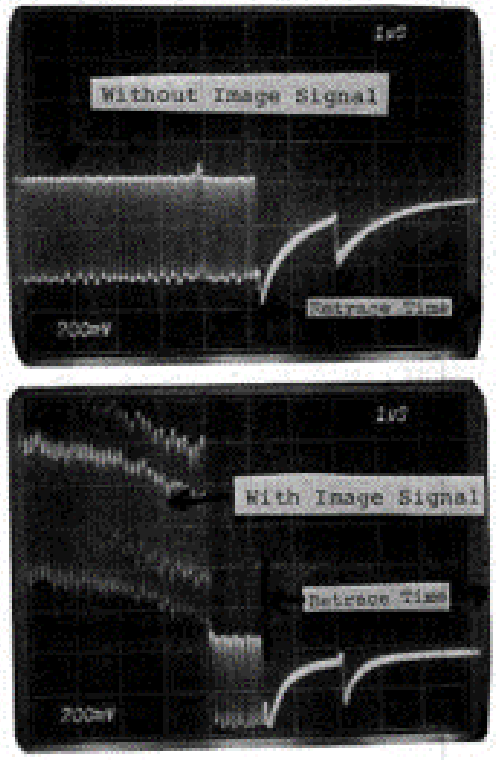

Fig.12 Comparison of the Pinned Photodiode image sensor with and without image signal gives the very low dark current level at retrace time.

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When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of threshold voltage is observed. This narrow-channel effect has been applied successfully in creating an asymmetric potential well under an electrode for two phase CCD operations. The feasibility of this new structure has been confirmed in a 242 element analog delay line and the application is now extended to a 380H × 488V CCD Imager. In the constructed B/W CCD camera,

§1. Introduction

When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of threshold voltage is observed. 1, 2) This narrow channel effect has been applied successfully in creating an asymmetrical potential well under an electrode for two phase CCD operations. The feasibility of this new structure has been confirmed in a 242 element analog delay line 3) and the application is now extended to a 380H × 488V CCD Imager. Figure 1 shows the block diagram of the CCD Imager. The device has been organized for a frame transfer CCD. It consists of 380 × 244 bit imaging area, 380 × 244 bit storage area, and 380 bit horizontal shift register. The chip size of the device is 10.1 mm × 14.6 mm in which the imaging area is 8.8 mm × 6.6 mm determined by 2/3-inch picture format of the optical system. The transfer efficiency of the vertical and horizontal shift registers are more than 99.995% per transfer. And high image resolution of 280 TV lines/p.h. (Horizontal) and 350 TV lines/p.h. (Vertical) have been obtained.

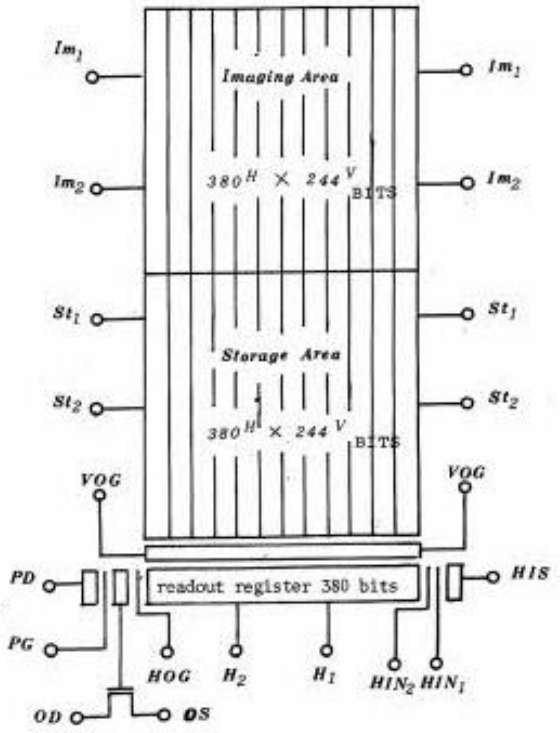

Fig. 1. The block diagram of a 380 H × 488 V CCD imager in frame transfer organization.

The typical dark current level is less than 3% of the maximum signal level at the room temperature of 20°C. The spectral response of the imager shows that this inherently SiO_2 exposed structure has high enough quantum efficiency at 450 nm wavelength and functions as a color imager with high sensitivity.

§2. Device Structure

Figure 2 shows cross sectional views of the electrode for two phase CCD structure. For the structure fabricated, each electrode of the horizontal readout register has one large storage region of 70 μm width and seven narrow-channel transfer regions of 3 μm width. The channel lengths of the storage and transfer parts of the electrode are 7 μm and 5 μm respectively. Each electrode of the vertical shift register has one large storage region of 18 μm width and one narrow-channel transfer region of 3 μm width. The channel lengths of the storage and transfer parts of the electrode are 8 μm and 6 μm respectively. The width of the channel stop between vertical registers is

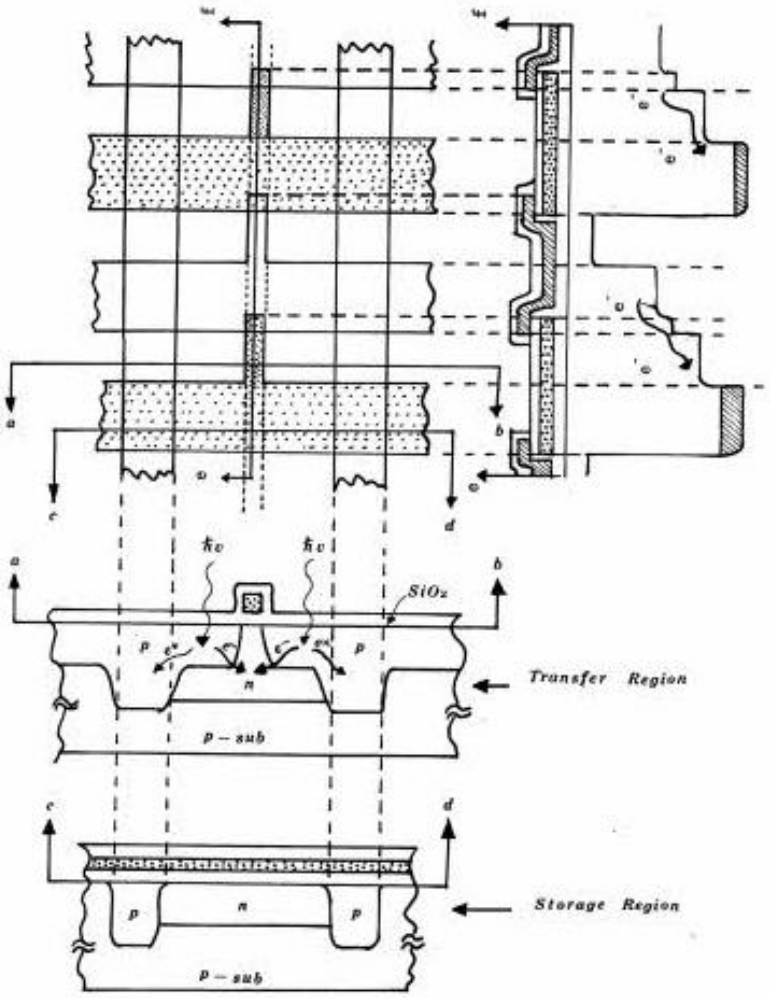

Fig. 2. Top and cross sectional views of the electrode for two phase CCD structure.

6 μm.

The unit cell of vertical registers is 24 μm × 14 μm. In the imaging area, an SiO_2 exposed window of 21 μm × 6 μm is used as the photosensor window with high sensitivity at 450 nm wavelength. Figure 3–5 show the photograph of the device, the unit cell of the imaging area, and the horizontal readout shift register.

§3. Device Fabrication

The device is fabricated in buried-channel version on a p-type (100) oriented, 10–20 ohm-cm silicon substrate with standard double-layer overlapping polysilicon gate definitions. A first level of phosphorus-doped polysilicon is deposited onto an oxidized silicon wafer and defined to form the first set (H1, St1, and Im1) of electrodes. The exposed oxide is then removed and a new gate oxide is thermally grown. Subsequently, the second set (H2, St2, and Im2) of electrodes are formed by the second level of polysilicon deposition. Then, using the polysilicon patterning as an ion im-

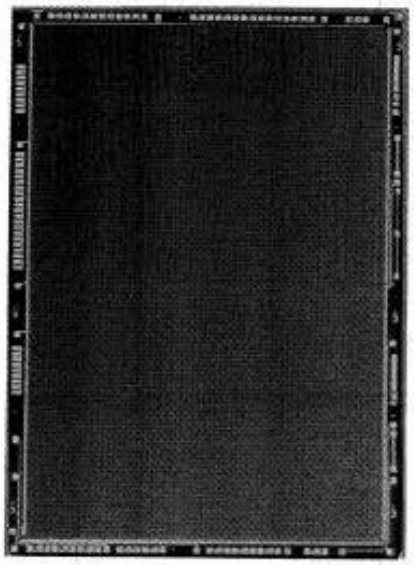

Fig. 3. Photomicrograph of the 380 H × 488 V CCD imager. The chip size is 14.6 mm by 10.1 mm.

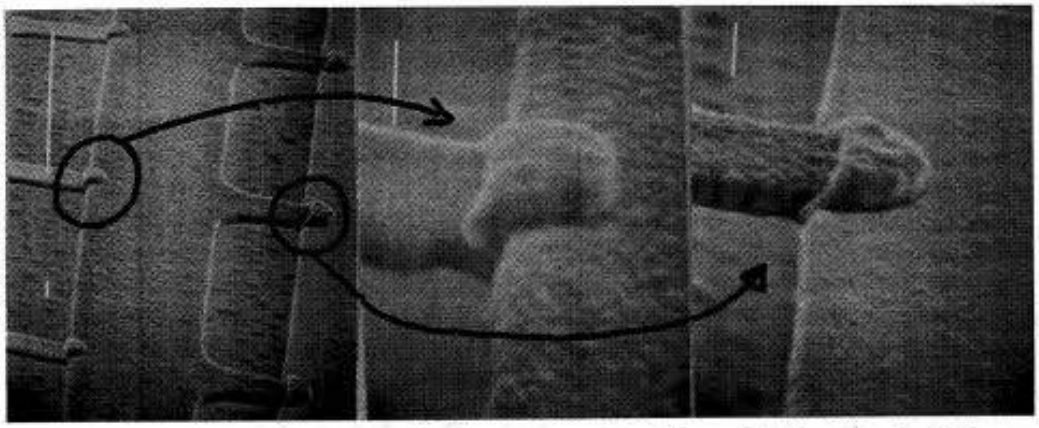

Fig. 4. SiO_2 exposed photo-sensor window of 21 μm × 6 μm located in the unit cell of 24 μm × 14 μm. The width of the narrow channel is 3 μm throughout the device. The electrode overlap is 2 μm.

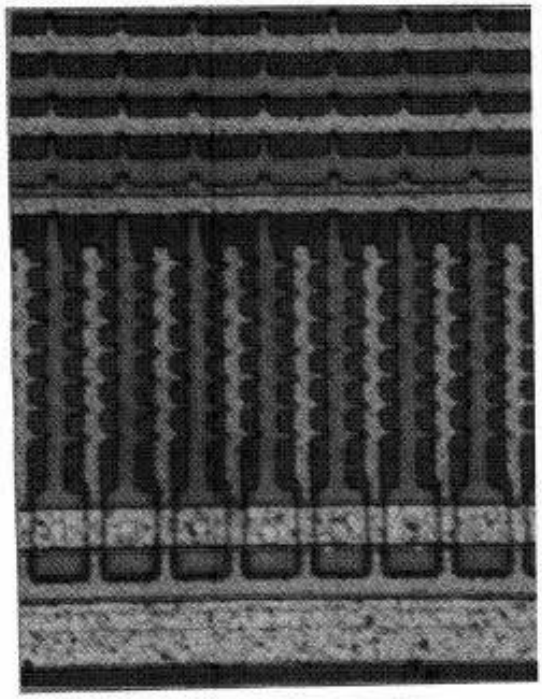

Fig. 5. The horizontal readout register with 14 μm-pitch-per bit electrode structure.

plantation mask, boron ions with the dose level of 2×10^{13} cm^{-2} are implanted into the silicon substrate throughout the exposed portions of the thermally grown oxide. This step provides self-aligned channel stops which surround the narrow-channel transfer part of each electrode. The gate oxide thickness is 130 nm throughout the device. Phosphorus doped polysilicon with the sheet resistivity of 50–70 ohm/M and the thickness of 500 nm is used for the gate electrode structure. To eliminate oxidation-induced stacking faults and other generation-recombination centers, high density (more than 1×10^{20}/cm^3) phosphorus gettering at 1100°C and HCl oxidation were employed. The typical dark current level is less than 5 nA/cm^2. For the particular device reported in this paper, the ion implantation dose of the buried channel is taken to be 1.7×10^{12} cm^{-2}.

§4. Imager Characteristics

The transfer efficiency of the vertical and horizontal shift registers are more than 99.995% per transfer. And high image resolution of 280 TV lines/p.h. (Horizontal) and 350 TV lines/p.h. (Vertical) have been obtained. See Fig. 6–8. Operating conditions of the CCD imager are listed in Table I. As seen in Fig. 9 of the actual measured channel potentials plotted against the gate voltage for the buried channel version, no clock overlap is necessary both for the vertical and horizontal shift registers. This simplifies drastically the construction of a

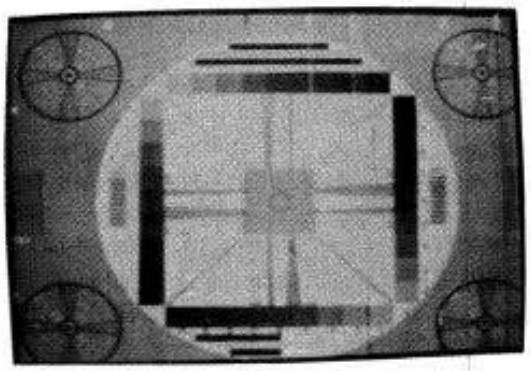

Fig. 6. A TV picture of a resolution chart. The maximum resolution seen in the picture are 280 TV lines/p.h. (Horizontal) and 350 TV lines/p.h. (Vertical).

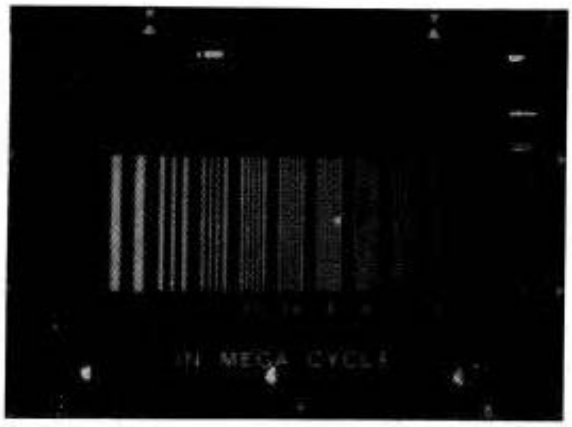

Fig. 7. A TV picture of a multi burst chart. The maximum resolution is near 4 MHz burst lines.

Fig. 8. A TV picture of an image.

Table I. Operating conditions of the CCD imager.

Integration time	16 msec
Vertical clock voltage	from −2 volt to −12 volt
Frame shift frequency	14.31818 MHz/32 =447.4 KHz
Line shift frequency	15.7 KHz
Horizontal clock voltage	from 3 volt to −12 volt
Readout frequency	14.31818 MHz/2 =7.15909 MHz
Interlace	2:1

timing system for the imager. See Fig. 10. The electrode voltages of the vertical registers in the imaging area are set off at −12 volt except the time of frame-shift. At this voltage, the surface of the narrow channel transfer regions is at accumulation, and also the channel conductance of the narrow channel is very low. This mechanism seems working for antiblooming. This effect has been verified as seen in the picture taken against the light coming through the laboratory window. See Fig. 11.

The dark current level is less than 3% of the maximum signal level at the room temperature of 20°C. The waveforms of the signal output from the horizontal readout register are shown in Fig. 12. The 380 bit horizontal register shifts

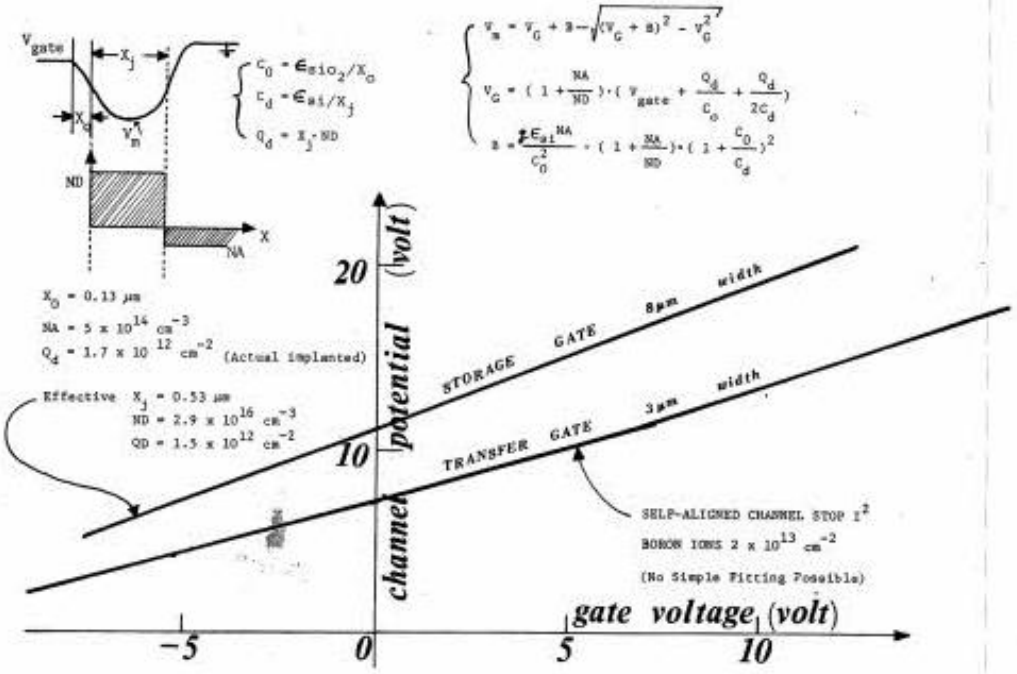

Fig. 9. The actual measured channel potentials plotted against the gate voltage for the buried channel version. The curve fitting with the simple relations by depletion approximation gives the effective values of X_j, ND and QD as seen in the figure.

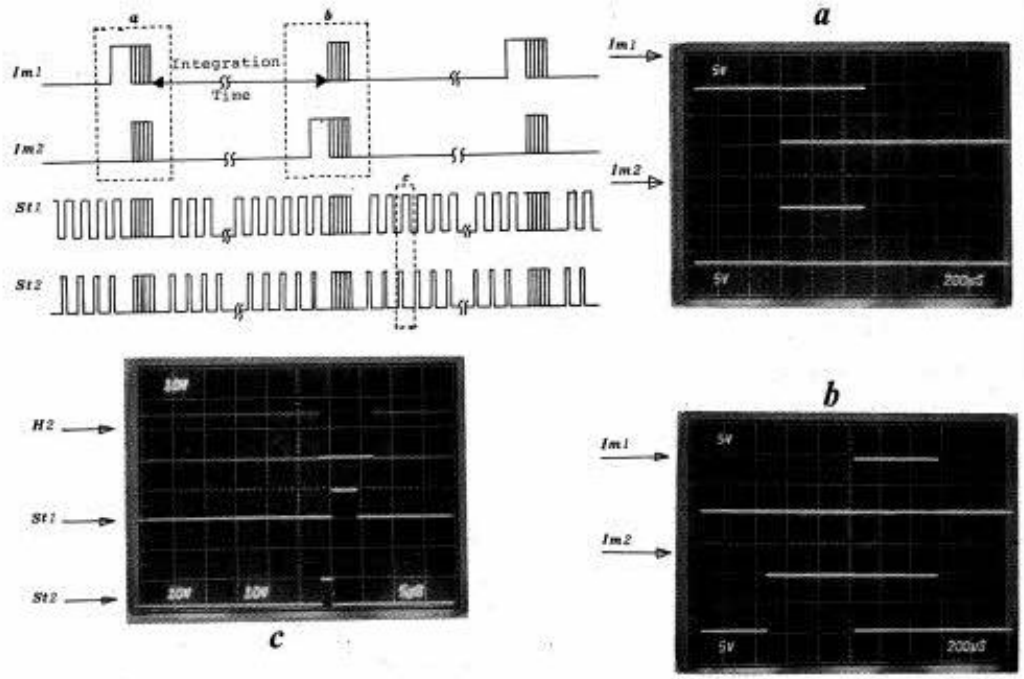

Fig. 10. The timing diagram of the imager.

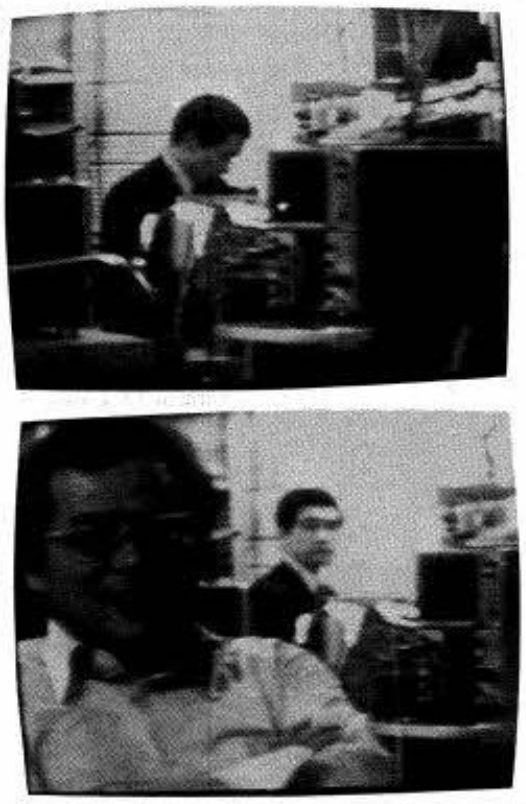

Fig. 11. TV pictures of scenes against light. Anti-blooming effects seem working. The maximum light intensity through the lab-window corresponds to about ten times of the maximum handling charge of the imager.

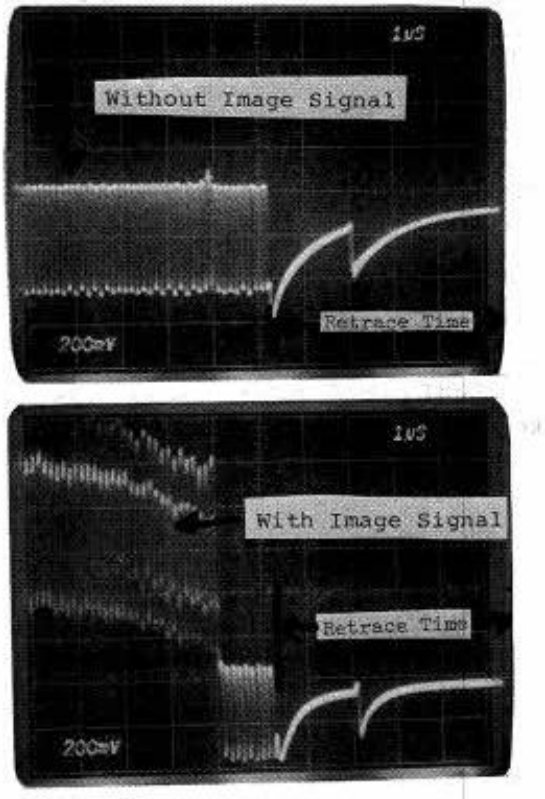

Fig. 12. The output wave forms of the horizontal readout register at the tailing end of a TV picture line, that is, right before the horizontal retrace time. The comparison of the output levels with and without image signal gives the dark current level of the imager.

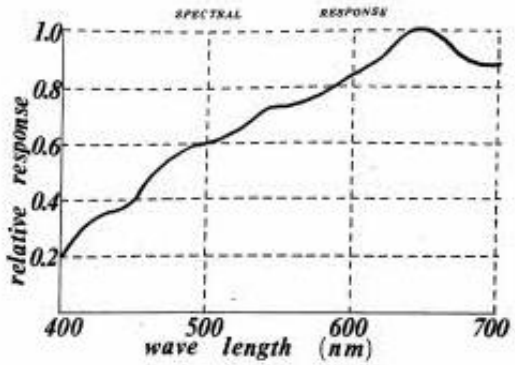

Fig. 13. Spectral Response of the photosensors.

389 bits for each TV picture line. Hence, the last 9 bits of the output do not contain the image information nor dark current of the vertical registers.

The spectral response of the imager is also analyzed and reported in Fig. 13. Effective window size is 24 μm × 14 μm at 700 μm wavelength and 21 μm × 6 μm at 400 nm wavelength. Measurements were performed by reading the signal output of the imager while imaging a monocromatic spot light. It is expected that this inherently SiO_2 exposed structure has high enough quantum efficiency at 450 nm wavelength and functions as a color imager with high sensitivity and resolution when the smearing problem assosiated with the frame-transfer organization itself, is solved by use of a mechanical shutter.

§5. Summary

The feasibility of the narrow transfer channel CCD structure is confirmed by the realization of 380H × 488V CCD Imager with frame transfer organization. The transfer efficiency of the vertical and horizontal shift registers are more than 99.995%. And high image resolution of 280 TV lines/p.h. (Horizontal) and 350 TV lines/p.h. (Vertical) have been obtained. The typical dark current level is less than 3% of the maximum signal level at the room temperature of 20°C. It is expected that this inherently SiO_2 exposed structure has high enough quantum efficiency at 450 nm wavelength and functions as a color imager with high sensitivity and resolution.

Acknowledgement

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