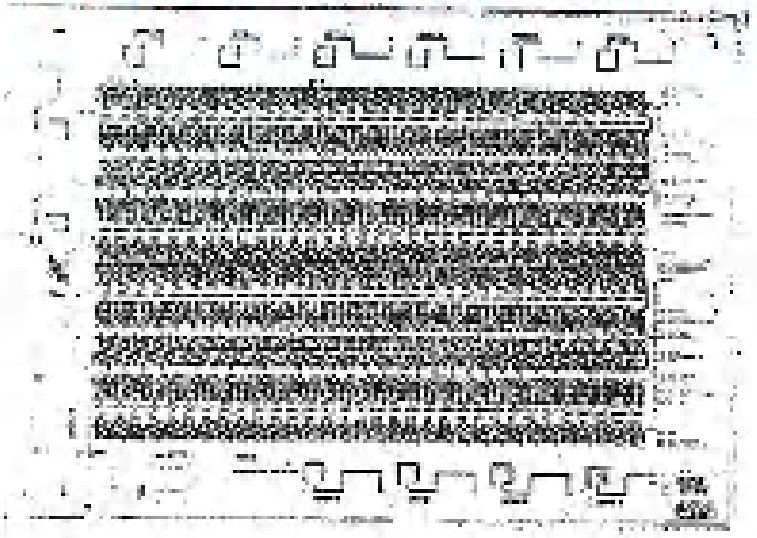
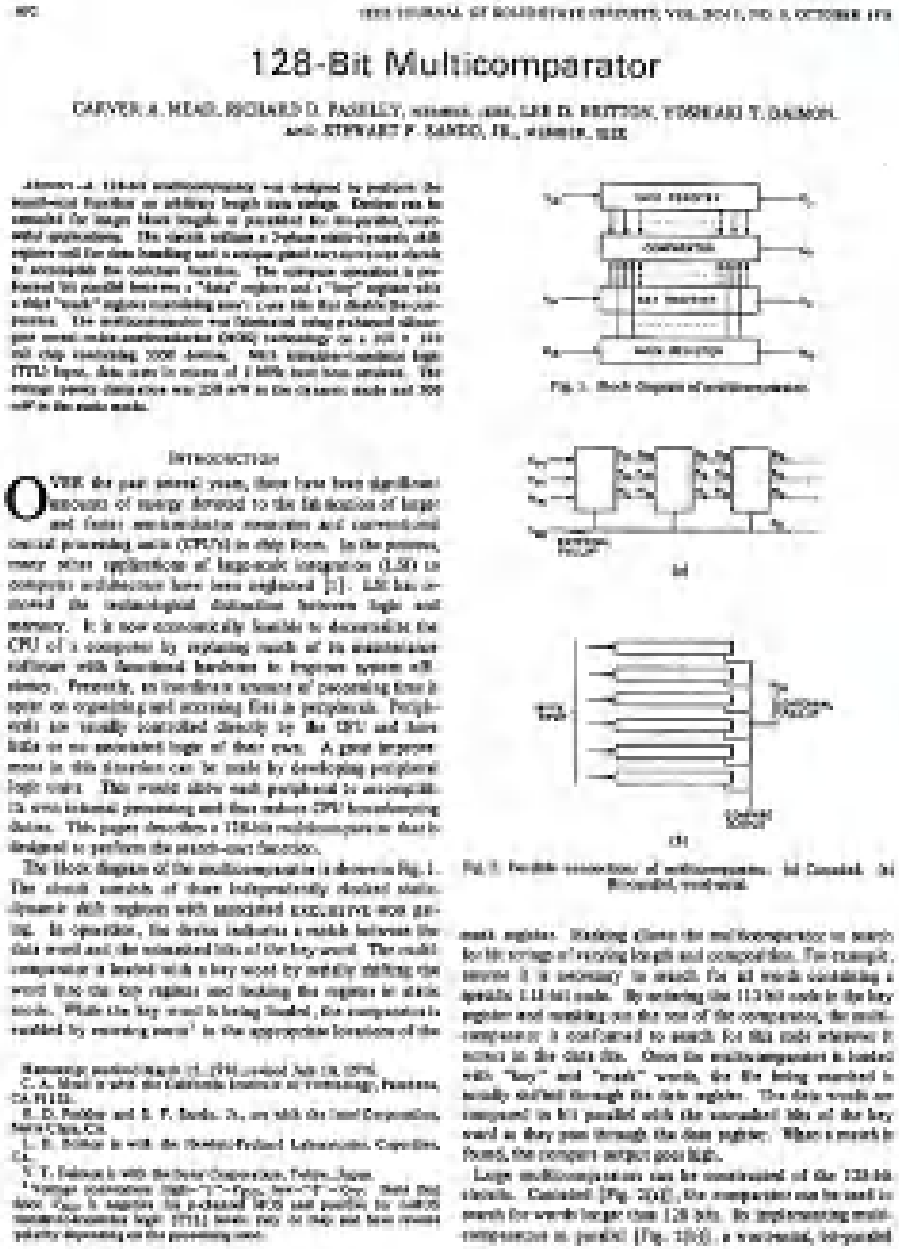
128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976

Prof. C. A. Mead and Yoshiaki Daimon Hagiwara working on the silicon chip design at Caltech in 1972

128-bit Multicomparator chip, designed by Hagiwara in 1972-1973 and fabricated by Intel PMOS process.





128-Bit Multicomparator

CARVER A. MEAD, RICHARD D. PASLEY, [illegible], LEE D. RITTON, YOSHIAKI T. DAIMON, AND STEWART F. SAREO, JR., [illegible]

INTRODUCTION

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

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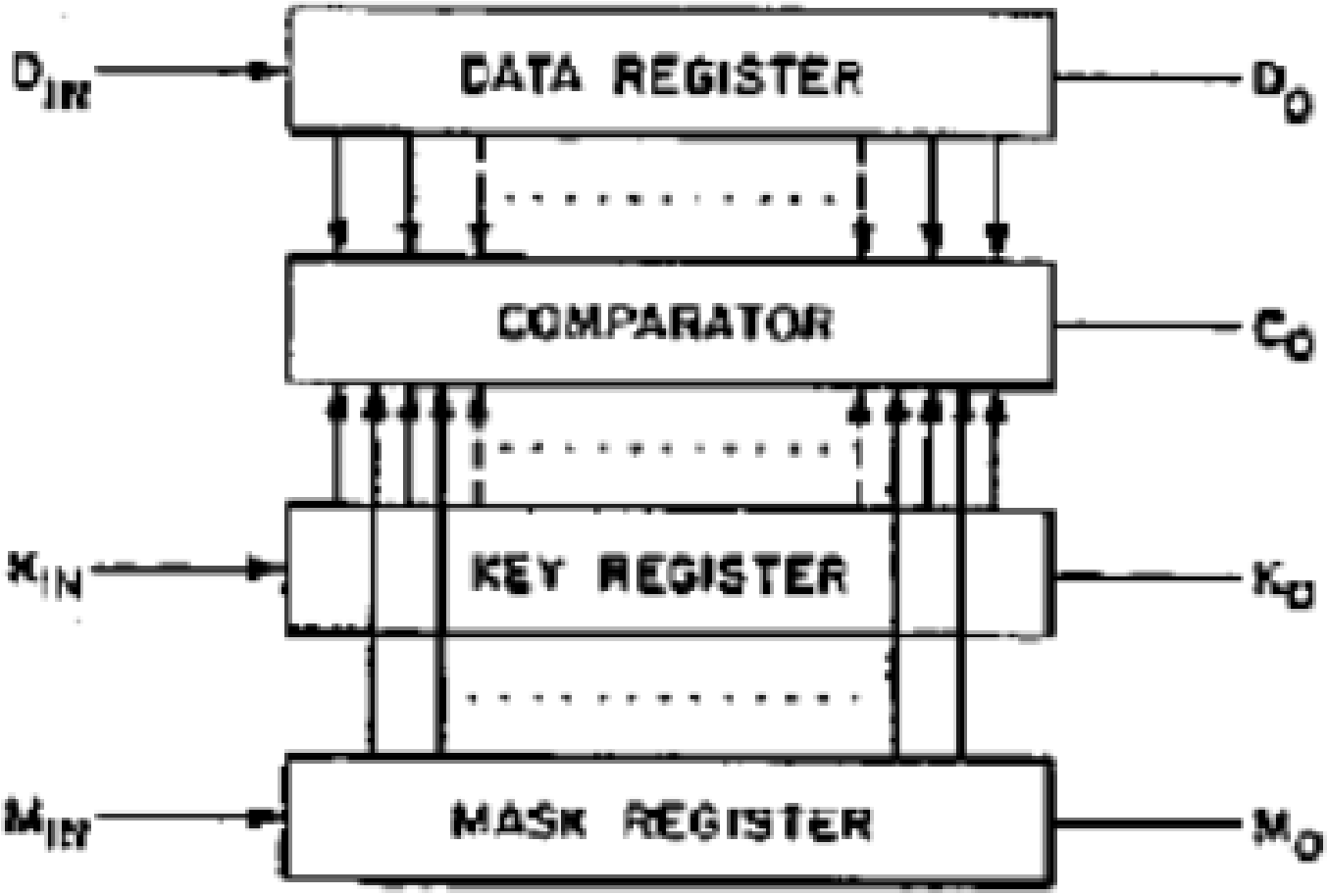

Fig. 1. Block diagram of multicomparator.

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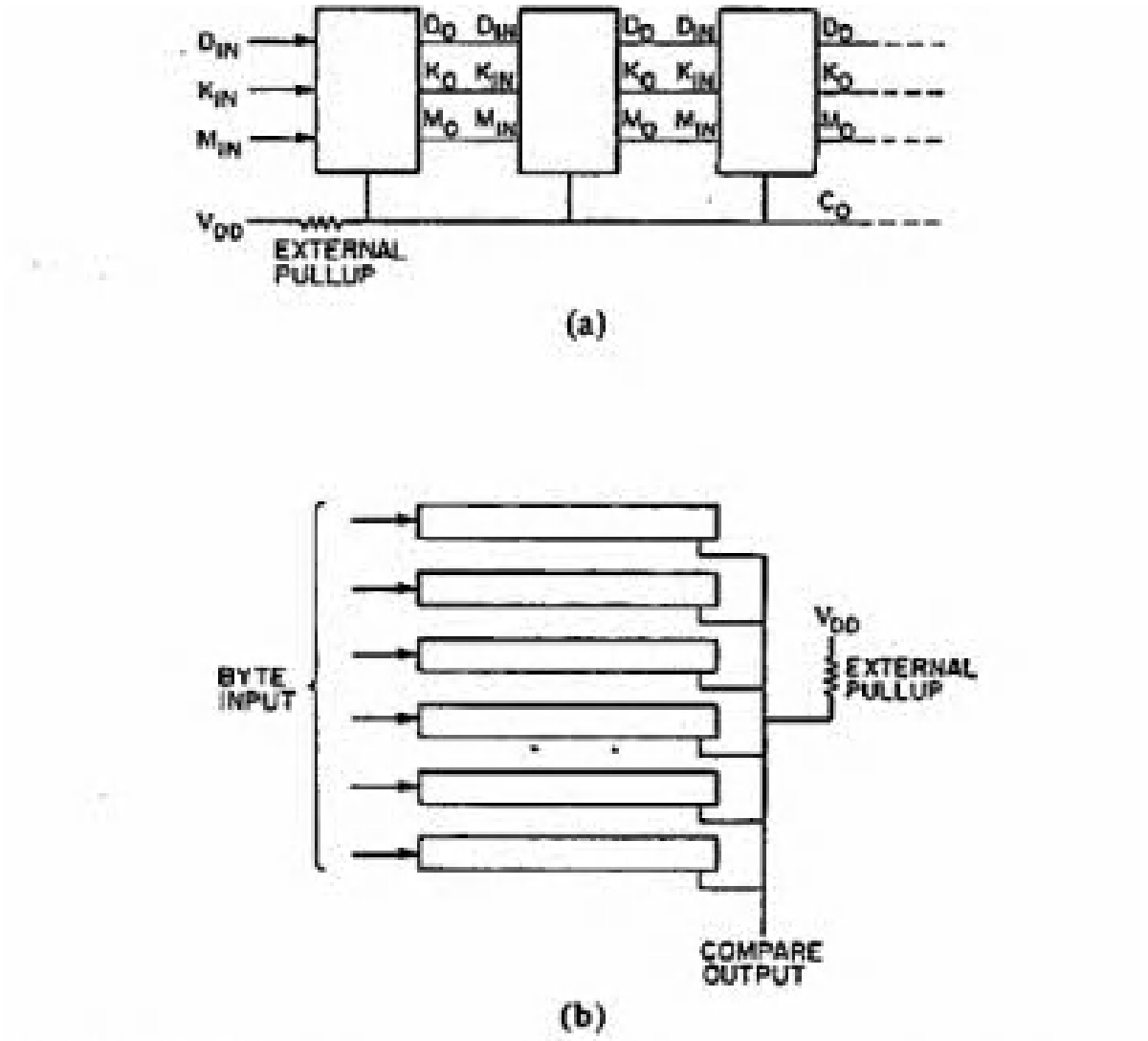

Fig. 2. Possible connections of multicomparator. (a) Cascaded. (b) Bit-parallel, word-serial.

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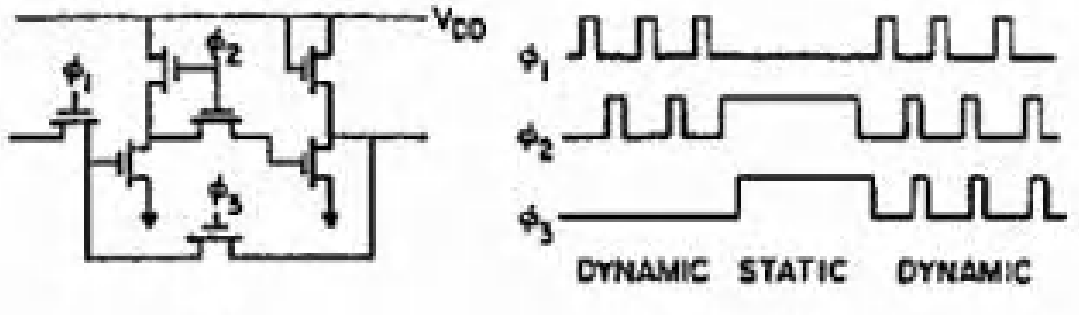

Fig. 3. Basic shift register cell. (a) Schematic. (b) Clock timing.

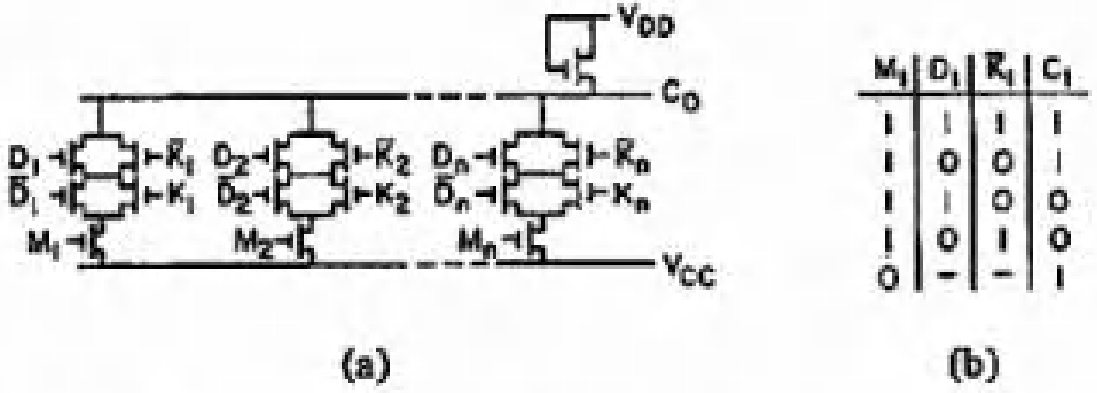

Fig. 4. Gated EXCLUSIVE-NOR gate. (a) Schematic. (b) Truth table.

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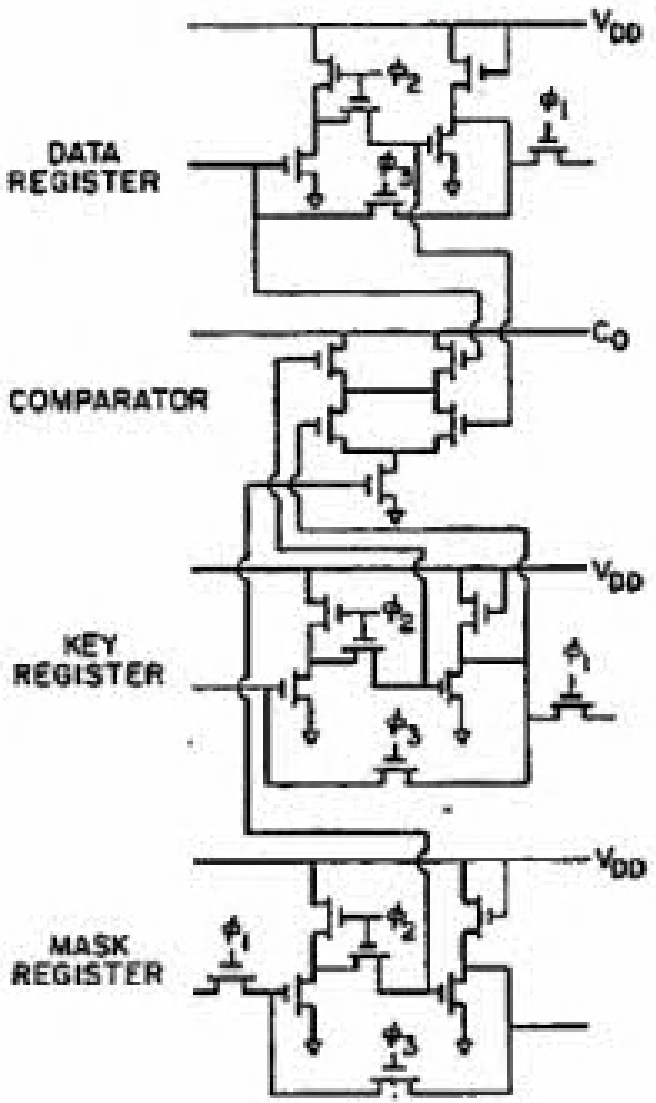

Fig. 5. Full schematic of one bit slice of the multicomparator.

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serial-in/serial-out fast 128 bit parallel data comparator chip fabricated by Intel corporation p-channel E/D MOS fabrication line

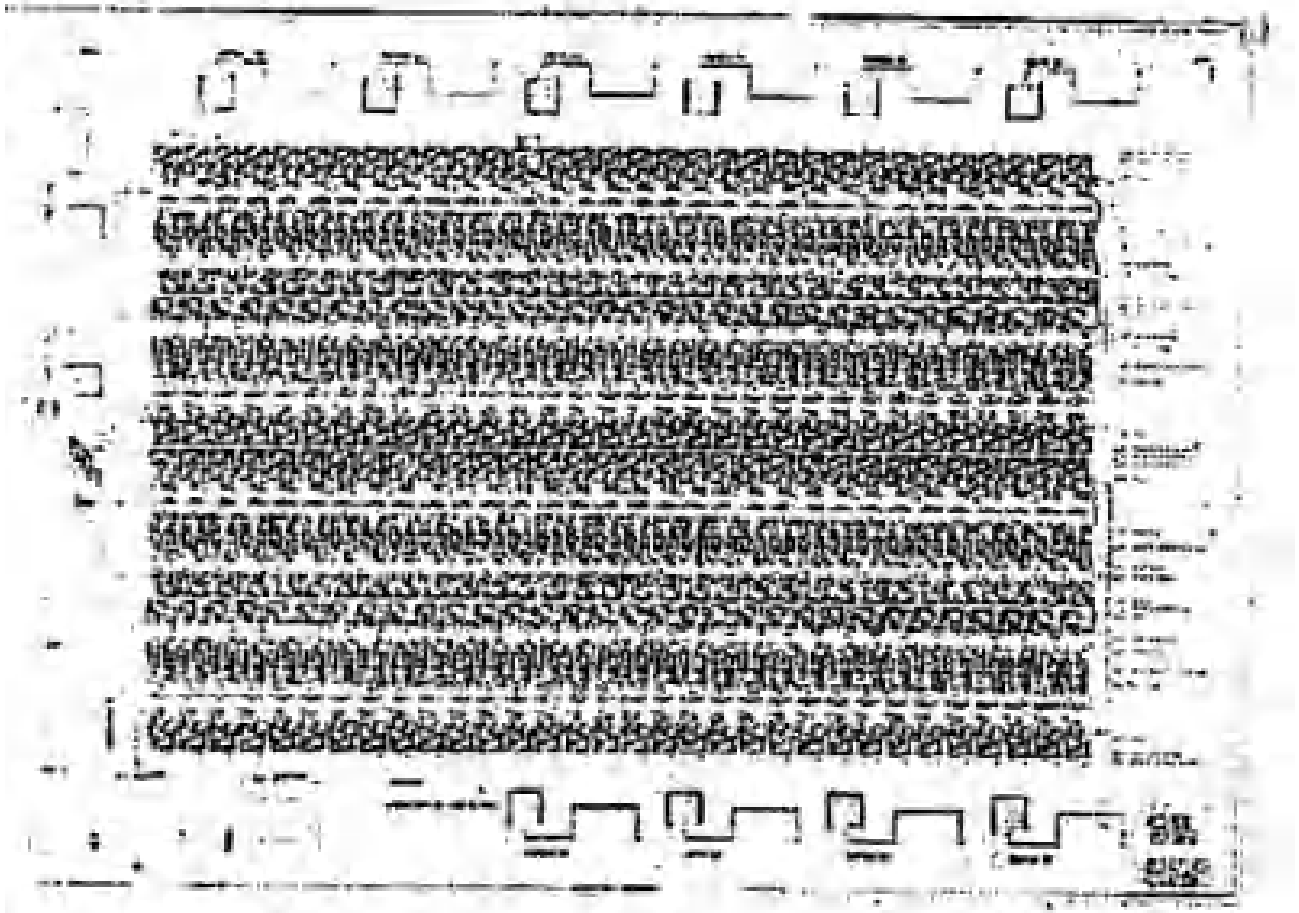

Fig. 6. Photomicrograph of multicomparator chip.

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TABLE I

Parameter	Performance[a]
Clock rate	0.0001–2 MHz
Dynamic supply current	25 mA
Static supply current	30 mA
Clock leakage current (ϕ_1)	120 nA
Clock leakage current (ϕ_2)	300 nA
Clock capacitance (ϕ_1)	40 pF
Clock capacitance (ϕ_2)	60 pF
Clock capacitance (ϕ_3)	40 pF
Interclock capacitance	7 pF
Input capacitance	10 pF
Output capacitance	10 pF

[a] *Test Conditions:*

$$T = 23^{\circ}\text{C}, V_{cc} = 5\text{ V}, V_{DD} = -5\text{ V},$$

$$V_{\phi L} = +5\text{ V}, V_{\phi H} = -5\text{ V}, V_{\text{input}} = 0.5\text{ V}.$$

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ACKNOWLEDGMENT

The authors are pleased to acknowledge Intel Corporation for wafer fabrication.

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[2] F. Faggin and T. Klein, "Silicon gate tec...," Solid-State Electron., vol. 13, pp. 1125-1144, 1970.

Dr. Lee Barton at Hewlett-Packard
Caltech Graduate, 1973

Lee D. Britton received the B.S.E.E. degree from the California Institute of Technology, Pasadena, in 1973.

He then invented and marketed a computer-aided memory for theater lighting control, and now works for Hewlett-Packard Laboratories, Cupertino, CA, designing and testing LSI integrated circuits for mini-computers.

Dr. Yoshiaki Hagiwara at Sony
Caltech Graduate, 1975

Yoshiaki Hagiwara was born in Kyoto, Japan, on July 4, 1948. He received the B.S., M.S., and Ph.D. degrees from the California Institute of Technology, Pasadena, in 1971, 1972, and 1975, respectively.

Since 1967, he has served several research groups in the Institute. He worked as a Data Processor in hydraulics from 1967 to 1969, engaging in the analysis of the pressure distribution of solitary waves, the influence of the geological features of a harbor upon the induced standing-wave amplitude in the harbor, and the diffusion mechanism of polluted objects in moving fluids. From 1969 to 1971, he worked as an Experimentalist in the Material Science Department and studied the switching and other electronic properties of newly developed amorphous alloys from the low temperature of 4 K to room temperature. From 1971 to 1975 he was a Research and Teaching Assistant both in the Electrical Engineering and Physics Departments at the California Institute of Technology. In the summer of 1971 and 1973, he visited Sony Corporation, Tokyo, Japan, as a Product-Appraisal Engineer at the Atsugi plant and engaged in developments and applications of bipolar technologies in video and power integrated circuits. He is presently with the Sony Corporation, Tokyo, Japan. His interests lie in the areas of digital and linear integrated circuit designs, the physics of microelectronics, and artificial intelligence.

Prof. C.A.Mead at Caltech

Carver A. Mead received the B.S., M.S., and Ph.D. degrees from the California Institute of Technology, Pasadena, ... 1957, and 1960, respectively.

He has been a member of the faculty of the California Institute of Technology, Pasadena, CA, since 1957. His research has contributed to the understanding of ... in solids, current flow mechanisms in thin dielectric films, metal-semiconductor barriers, band energies in semiconductors, and ... processes in insulators. He has proposed and demonstrated the operation of a number of new solid-state electronic devices and holds several U.S. patents.

Dr. Mead is a Fellow of the American Physical ... and a member of Sigma Xi.

Dr. Richard Pashley at Intel
Caltech Graduate, 1974

Richard D. Pashley (M'...) was born in Ft. Belvoir, VA, on September ... 1947. He re-...

...opment, and static ... formance MOS techn...
Dr. Pashley is a me... Physikalische Gesell...

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