High-Density and High-Quality Frame Transfer CCD Imager with Very Low Smear, Low Dark Current, and Very High Blue Sensitivity

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Abstract—**When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of the threshold voltage is observed. This narrow channel effect has been applied successfully in creating an asymmetric potential well under an electrode for two-phase CCD operation. The feasibility of this structure has been confirmed in a 242-element analog delay line. The application is now extended to a 800 H × 492 V frame transfer-type buried channel CCD imager with 14.31818 MHz frame shift, which results in a very low smear level of 0.01%, which is good enough for low-cost multimedia video camera applications.**

I. Introduction

Since their introduction in the 1970's, CCD sensors have improved dramatically. CCD's, however, have a number of disadvantages in multimedia applications. Ackland emphasized the potential application of CMOS sensors with built-in current amplification by source-follower MOS circuit [1]. He dealt mainly with the comparison between the interline transfer CCD sensors and the CMOS sensors. In his report, the quoted CCD charge transfer efficiency is 99.95%, which is a very low value, and very unrealistic. Moreover, in CMOS sensors, one has to remember that the built-in amplifier also amplifies the fixed-pattern noise in each picture element. The signal-to-fixed-pattern-noise ratio had been a very critical issue.

Moreover, in the author's early paper [2], the author reported that the charge transfer efficiency was higher than 99.998%, which is much higher than the value quoted by Ackland [1]. The value of the charge transfer efficiency is still improving. The author believes the charge loss per BCCD charge transfer will be less than 0.0001% in the future. Moreover, the clock amplitude in the actual CCD operations is also constantly decreasing for power savings [3]–[6]. Besides, the CCD is also fabricated as one modification of a CMOS process, and the CMOS random logic circuits can be incorporated in the process similar to the DRAM, fast SRAM [7], and logic blocks. The analog CMOS process, such as for the ADC's and DAC's, can also be included.

In this paper, the author felt a strong urge to point out that there is another type of CCD imager, the frame-transfer CCD imager, that should be considered again in multimedia applications, because it has a much simpler structure compared to the interline-type CCD imager, yet holds a large signal charge packet. The on-chip frame memory can also be used as a buffer memory for various multimedia applications.

On these points, some brief discussions regarding a new frame-transfer CCD structure and their results are reported. The new structure is bipolar-type image sensing element with a p-n-p SUB structure. The structure was originally proposed by the author in 1975 [8]. Some related ideas, hidden in the form of difficult legal wording, and other efforts, disclosed in the form of published papers, will be reviewed and discussed in details to explain the background and originality of the author's proposed structure.

II. Bipolar Image Sensing Element

Conceptually, the structure of image sensing elements in this frame transfer-type CCD imager originates from a structure very similar to the one widely used in current interline transfer-type CCD imagers. It is shown in Fig. 1(a). This structure has many features in common with the structure proposed originally by the author in 1975 [8]. It concerns only the structure of the boxed region in Fig. 1(a). But it is the core region of the image sensing element which is now widely used in commercial interline transfer-type CCD imagers. Since it has only been published in Japanese, the exact wording is quoted below for convenience.

"In the bulk silicon substrate, there is a region of the first conduction-type, P1. And then, another region of the second type, N2, is formed on top of it. A rectifying junction, J_e, is then attached to the region of the second type, which is regarded as the emitter junction of a transistor. Then, the junction between the first- and second-type regions is considered to be the collector junction of the transistor, J_c. The region of the second type, N2, acts as the base of the transistor. The electric charges created by the incident light are stored in this base region, N2, and transferred to the adjacent charge coupled device."

So, it is a simple bipolar-type image sensing element of a p-n-p SUB structure. In Fig. 1(b), for comparison, a MOS capacitance-type image sensing element was quoted, which was well known and considered to be conventional in the 1970's.

The idea was simply to use a bipolar transistor instead of the MOS capacitance for the image sensing element. However, as compared to the MOS capacitance case shown in Fig. 1(b),

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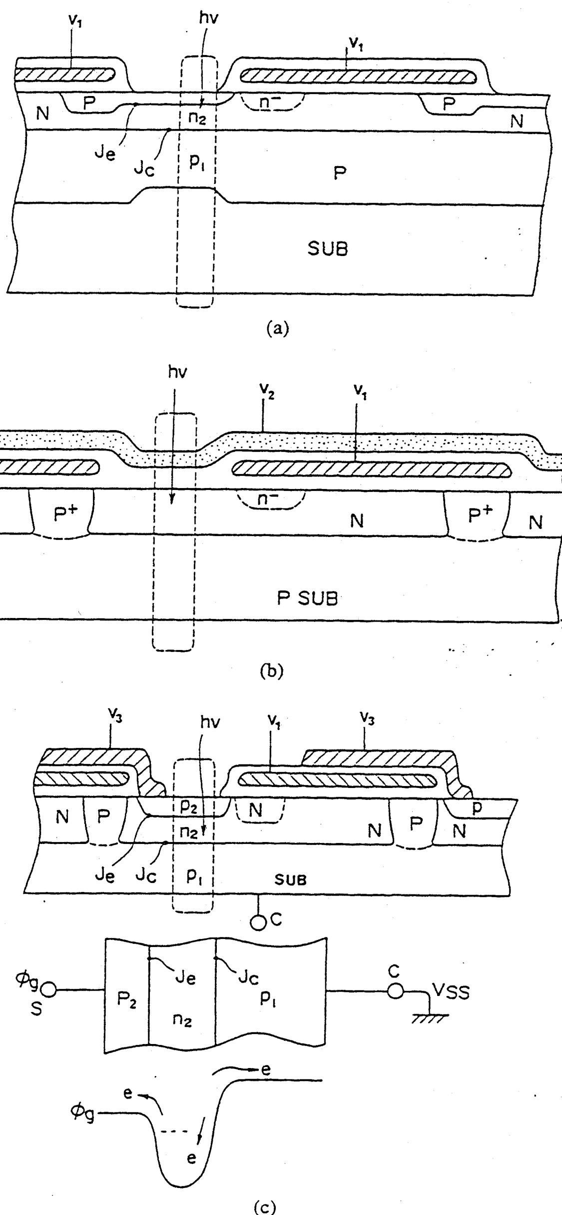


Fig. 1. (a) Basic structure of bipolar junction-type image sensing element now widely adapted in interline transfer CCD imagers. The hatched regions (V_1) covering the top are the polysilicon electrodes for the vertical CCD shift registers. The sensor regions are not covered by the polysilicon electrodes. (b) MOS capacitance-type imaging sensing element quoted in the author's invention of November 10, 1975, and known then as a conventional structure. The top layer (V_2) can be either a thin polysilicon or a transparent sensor electrode. (c) Bipolar junction-type image sensing element with a top wiring lead (V_3). In this case, as a simple example, the first p-region (P_1) is set equal to the silicon substrate.

the bipolar-type shown in Fig. 1(a) would give plenty of freedom in the practical world, and would result in much better performance.

III. Concept of Junctions for Vertical Overflow Protection (OFP)

In the above wording, no restriction was made on the conduction-type of the bulk silicon substrate. But it could also be made the same as the first conduction-type, P1. That is, SUB = P1. In this case, the first conduction part becomes the bulk substrate itself. This is the structure given in Fig. 1(c). However, in this case, the voltage of the collector, P1, is the substrate voltage itself. Since there is a large capacitance between the substrate and the power line, the voltage of the substrate is normally fixed at a fixed reference or DC voltage. Hence, the collector junction, J_c, cannot be controlled easily. Instead, in this case, the emitter junction was chosen to be controlled externally by introducing wiring lead from the top. Fig. 2(a) illustrates the actual operations.

Since it was a new structural concept that was to be specified, the functions of the top and bottom junctions, J_e and J_c, were intentionally not explained in detail. However, it also meant that the bottom junction J_c could also be used for the vertical overflow protection. In this case, the substrate is chosen to be different from p-type, as illustrated in Fig. 2(b). As long as the P2(J_e)–N2 (sensor base)–P1(J_c)–SUB(P/N) is meant to be a transistor, a variety of known transistor actions are meant to be considered, including punchthrough modes of p-n-p and p-n-p-n (when SUB = N) devices. The actual claim given in the legal wording is simple and general, but its structure is very basic and can be applied in a variety of image sensors including a Schottky-barrier imager as claimed in the specification [8].

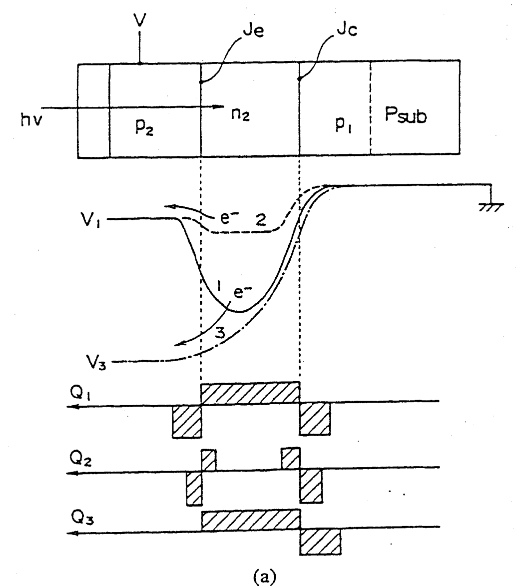
IV. Experimental Verifications by Frame Transfer Type CCD Imagers

Although the CCD imager type was not specified in the claim, and the structure is equally applicable to a frame transfer-type CCD imager, the original Japanese document has an example of an interline transfer-type CCD application as seen in Fig. 1(c). At that time, however, the structure was very difficult to fabricate. So, the author applied the principle in the frame transfer CCD imagers [2], [9].

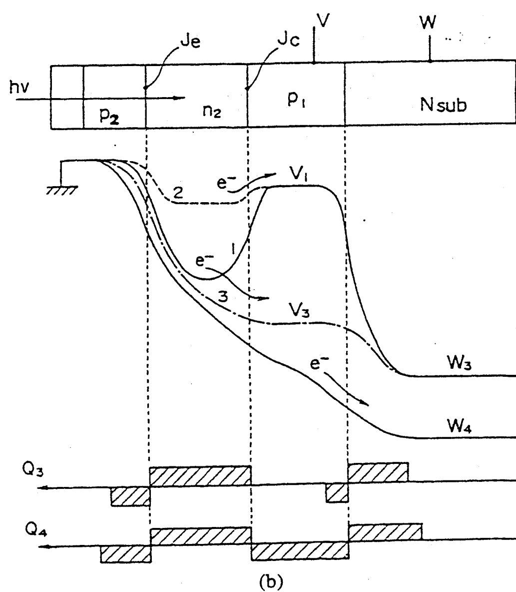
Moreover, the realization of the original concept of the vertical OFP was still very difficult. The author had to cope with the conventional lateral-type. It was not built at the top nor the bottom of the base region. But, the charges are still stored in the base extended storage region and are then transferred to the neighboring buried channel-type CCD shift register as originally conceived.

In the structure, it was proposed that by first transforming the incident light into electrons at the emitter and collector junction depletion regions, electrons stored in the base could then be transferred from the base region to the adjacent buried channel charge coupled device. It was described that the base region had the same concentration as the buried channel CCD because it could be easily adjusted by the ion implantation technique [see Fig. 1(a)–(c)].

By depleting the charge completely from the base region by the buried channel CCD transfer operation, image lag-free picture quality is assured. The high electron charge transfer efficiency of the buried channel CCD guaranteed the high resolution image quality. Moreover, the SiO_2 exposed sensor is expected to give high blue sensitivity since there is no gate structure for the incident light to pass through. By quenching the Si–SiO_2 interface recombination centers, very low dark current level was also expected in this p-n-p SUB structure.



(a)



(b)

Fig. 2. (a) Operations of bipolar junction-type image sensing element when the substrate is chosen to be the same as the P1 region. Q1, Q2, and Q3 are fixed charges in the depletion regions. (b) Operations of a bipolar junction-type image sensing element when the substrate is different from the P1 region. Q3 and Q4 are fixed charges in the depletion regions, where no mobile carriers are present.

Moreover, by controlling the relative voltage of the emitter and the collector, the amount of electrons stored in the base could be controlled independently from the incident light intensity level, and be easily adjusted from zero to the maximum storage capacity. These were the basic concepts that led to the current vertical OFP and the electrical shutter options. Fig. 2(a) and (b) show the points.

V. 800 H × 492 V Narrow-Channel FT CCD Imager

The actual bipolar imaging structure was applied first in the frame transfer-type CCD structure rather than the interline transfer-type CCD by the author [2], [9]. This frame transfer-type CCD structure is reviewed again in this paper. Some improvements are proposed to obtain better performance in order to compete with the MOS sensors quoted by Ackland.

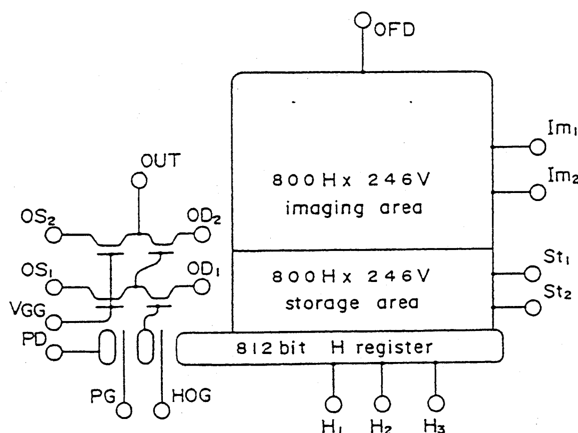


Fig. 3. Block diagram of 800 H × 492 V FT CCD imager. The architecture of the on-chip frame memory of the 800 H × 492 V storage area can be designed to meet special functional demands in various future multimedia applications.

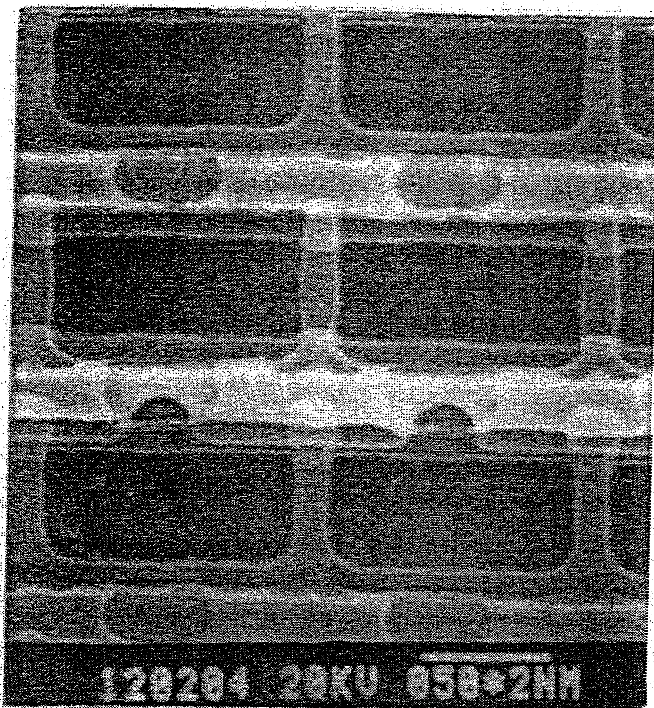
The device is a frame transfer CCD imager with a narrow channel transfer gate structure and a self-aligned overlapping three-polysilicon but two-phase CCD operation. The block diagram of this imager is shown in Fig. 3, in which the imaging area and the temporary storage area have the same CCD structure but different vertical cell pitches as those SEM pictures seen in Fig. 4(a) and (b).

Compared to the conventional overlapping gate-type CCD shift registers, the electrode overlap capacitance is very small in this narrow channel-type CCD shift register due to the very small overlapping portions. Moreover, aluminum wiring can be easily laid out on this electrode to shunt the relatively high resistivity polysilicon gate material by introducing contacts between the polysilicon electrodes and aluminum wirings for a large scale imager application.

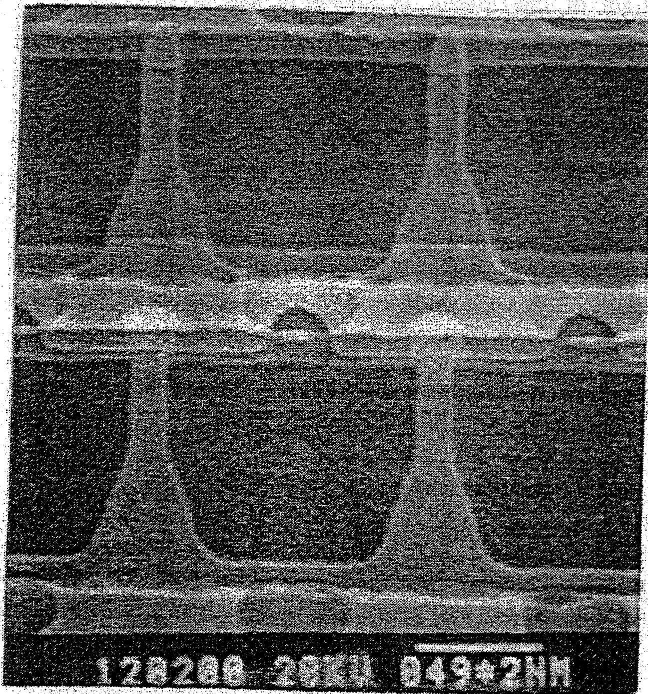
The cell size of the imaging area is $11\,\mu m \times 13\,\mu m$ while the storage area has $11\,\mu m \times 9\,\mu m$ cell size to keep the area occupation in the chip to the minimum. The chip size of the device is 10.0 mm × 12.5 mm. The device is fabricated in a buried-channel version of a p-type (100) oriented 10–15 Ω·cm silicon substrate with standard triple-layer overlapping-electrode-type polysilicon gate definitions.

A first level of phosphorus doped polysilicon is deposited onto an oxidized silicon wafer and defined to form the first set (H1 and storage electrodes of St1 and Im1). After the thermal oxidation of the electrodes, the second set (H2, St2, and Im2) is formed by the second level of polysilicon deposit. Similarly, the third set (H3 and transfer electrodes of St1 and Im1) is formed by the third polysilicon electrodes. Fig. 5 shows the brief process flow.

Then, using the polysilicon patterning as an ion implantation mask, boron ions with a dose level of 7×10^{12} cm^{-2} were implanted into the silicon substrate throughout the exposed portions of the thermally grown oxide. This step provides self-aligned channel stops which surround the narrow-channel



(a)



(b)

Fig. 4. (a) SEM picture of storage area. Cell size is 11 μm H × 9 μmV. (b) SEM picture of imaging area. Cell size is 11 μm H × 13 μmV.

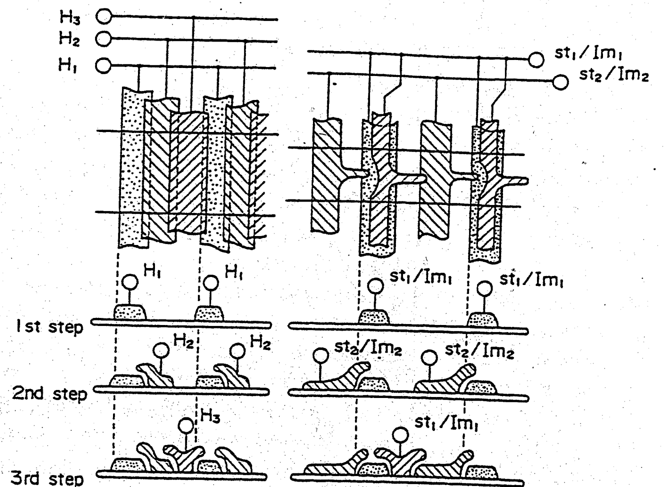


Fig. 5. Brief process flow of the electrode formation in a narrow channel frame transfer CCD imager. Three polysilicon layers were used for the formation of vertical and horizontal CCD registers.

TABLE I
OPERATION CONDITIONS

Integration Time	1/60 sec
Image Clock	10 volt
Storage Clock	10 volt
Frame Shift	14.31818MHz
Horizontal Clock	8 volt
Horizontal Readout	14.31818MHz
Precharge Clock	5 volt
Output	800 mv
Dark @ 25 ^{0}C	4 mv*
Smear	0.01 %

* for clock swings from Gnd to +10 volt

transfer part of each electrode. Since the early 1960's, this technique of ion implantation into the silicon substrate, using the polysilicon patterns as mask [10] and [11], has been known to produce many practical device structures. It is now widely used to form the source and drain of self-aligned polysilicon gate CMOS transistors. It is a very basic and practical technique, and also applied here to form the shallow junction layer at the Si–SiO_2 interface of the image sensing element.

The operating conditions of the CCD imager are shown in Table I. Clocks are operated simply from GND to +10 V or +8 V with the substrate grounded. But there is no protection diode attached to any of the electrodes, and negative clocks are also possible. The precharge gate has a typical amplitude of 5 V, which is directly accessible from the TTL logic level with a conventional DC adjustment using a large capacitance and two series resistances. This approach was used throughout the chip evaluations, and also in the early publications [2], [9].

A high image resolution of 560 TV lines/p.h. (horizontal) and 350 TV lines/p.h. (vertical) was obtained. High frame shift operations were also tested up to 14.31818 MHz, which was the limit of the commercially available regular clock driver [see Fig. 6(a) and (b)] for reproduced images. The smear level was 0.01% at 14.31818-MHz frame shift, and 0.02%

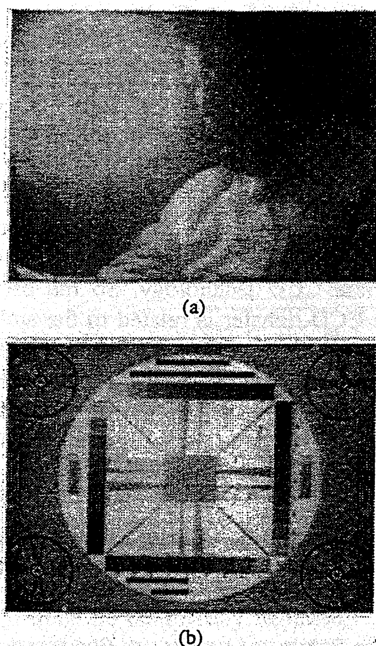


Fig. 6. (a) Reproduced resolution chart. Horizontal resolution 560 TV lines, vertical resolution 350 TV lines. (b) High light image reproduced. The FT imager with a large dynamic range gives a natural image in a dark room even if a strong back light illumination is directed from behind the shoulders.

at 7.15909 MHz, as was expected theoretically. No power increase nor image degradation was observed. The observed dark current of the imager is 4 mV for the clock voltage swing from GND to +10 V.

A low dark current, especially at higher temperature, is desirable. The dark current generated through the surface states [12] at the Si–SiO_2 interface in the sensor elements is kept low by the presence of holes. The diffusion dark current does not contribute significantly below 55 °C. The negative voltage applied on vertical registers also suppress the generation of the dark current from the surface states since the emission time constant of the dark current generated at the surface states is known to be more than 1 ms. The negative voltage below −8.0 V gives the minimum dark current level. The value of the output capacitance of the floating diffusion is 0.03 pF. The voltage gain is 4 μV/e. The observed dark current is equivalent to 10 electrons/pixel, of which 8 electrons are from the vertical registers. The value of the dark current is less than 1/10 of the conventional levels [13], [14] in optimized operations.

The value of the maximum signal voltage is 800 mV, which is equivalent to the 200 000 signal electrons. Consequently, the dynamic range of 83 dB is achieved. The salient device characteristics are summarized in the Table II. The relative spectrum response of this bipolar-type image sensing element is compared in Fig. 7 with those of the conventional polysilicon electrode MOS-type imager. The solid curve 1 shows an overall stable response characteristics with high blue sensitivity for the bipolar-type structure. The dashed curves, 2 and 3, are of the polysilicon electrodes of thicknesses 50 and 150 nm, respectively.

Although the imager in this work has a conventional overflow drain structure as shown in the Fig. 8(a), the vertical

TABLE II
DEVICE CHARACTERISTICS

Characteristic	Value
Optical Format	2/3 inch
Transfer System	Frame Transfer
Total Number of Pixels	800 H x 492 V
Chip Size	10.0 mm H x 12.5 mm V
Cell Size Imaging Area	11 µm H x 13 µm V
Cell Size Storage Area	11 µm H x 9 µm V
Silicon Substrate	p-type (100) 10-15 ohm-cm
Horizontal Resolution	560 TV lines
Vertical Resolution	350 TV lines
Smear	0.01 %
Noise	10 electrons/pixel
Output Gain	4 µV/e
Lag	Undetectable
Dynamic Range	83 dB
Charge Capacity	200,000 electrons/pixcel
Minimum Illumination (F1.4)	1.6 lux

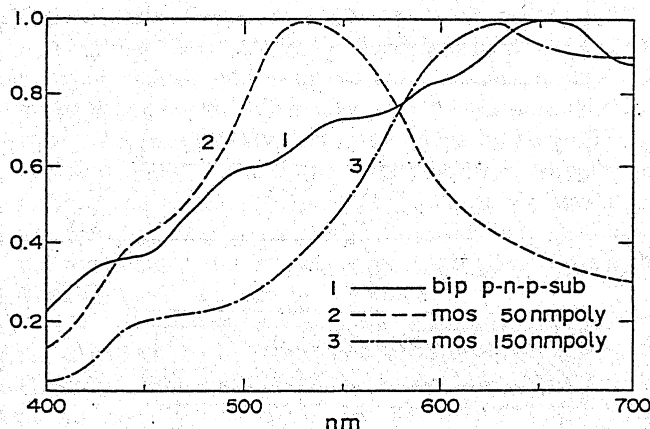


Fig. 7. Relative spectrum response. The relative response of the bipolar-type SiO_2–P2–N1–P1–SUB structure is compared with poly–SiO_2–N2–P(SUB) structures of the polysilicon thickness of 50 and 150 nm.

OFP can also be incorporated in any FT imagers as well [15]. The proposed image sensing element structure with OFP is similar to the structure that have been widely adopted now in the conventional interline transfer CCD imagers [13] but it is much simpler and compact. As seen in Fig. 8(b) and (c), very simple and compact structures in future applications for imaging can be expected. This bipolar-type image sensing element is not only equipped with a potential built-in function of overflow protection, it is also inherently image lag-free.

VI. IMAGE LAG-FREE, "VIRTUAL" CCD MODE COMPLETE CHARGE TRANSFER

The majority carriers in the base region of this bipolar-type structure are the signal electrons themselves, which are being generated by the incident light. The carriers are depleted

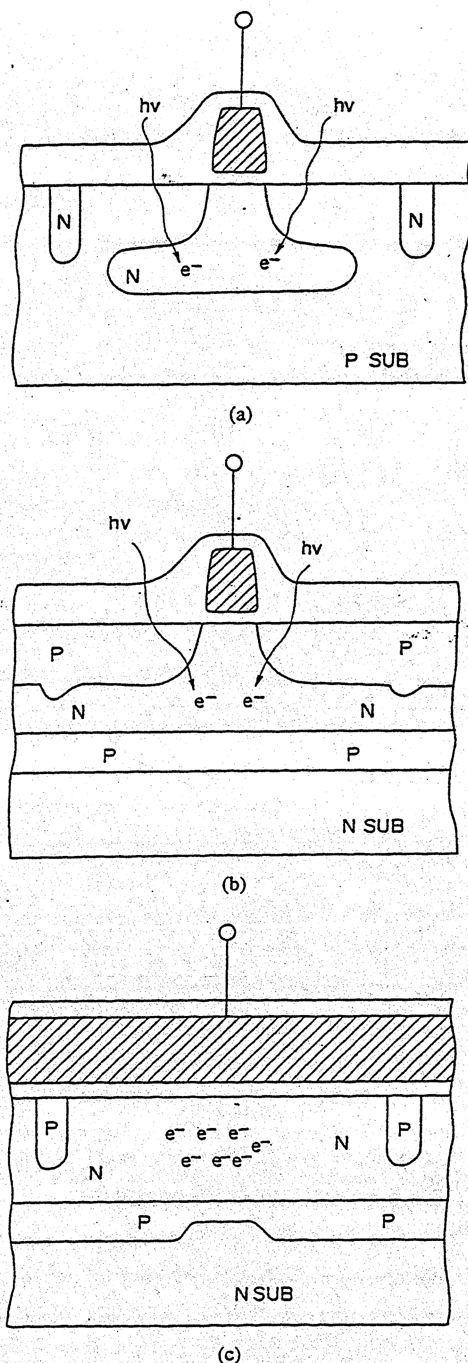


Fig. 8. (a) Cross section of imaging sensing element transfer region (this work). (b) Cross section of imaging sensing element transfer region (proposed). (c) Cross section of imaging sensing element storage region (proposed).

and transferred to the adjacent vertical CCD register. The operation is in the CCD transfer mode. The CCD high transfer efficiency guarantees the complete depletion of the majority carriers from the base region. This makes it possible to realize a complete image lag-free video camera system. The concept was verified in another form by Hynecek [16] in his "virtual" phase CCD transfer mode. See the structure shown in Fig. 9 labeled Hynecek 1979.

When the attention was focused along the direction of the charge transfer to the adjacent vertical CCD shift register, the charge transfer corresponds to 1/2 of the 1-b charge transfer of the well known CCD shift register structure. The sensor portion does not have any electrodes and this is so-called "virtual" phase CCD mode charge transfer as described by Hynecek.

The author's 1975 proposal has the same structural and operational features. It is same as the one described by Hynecek in his virtual phase CCD technology. So the originality of the virtual phase CCD transfer is related to the author's 1975 conception of the bipolar-type image sensing element.

In CSSD, Tokyo, Aug. 1978, the author introduced a 380 H× 488 V CCD imager with narrow channel transfer gates (Hagiwara, 1978). In Fig. 9, the sensor structure was also compared with Hynecek's virtual phase CCD structure (Hynecek, 1979), and to the author's original structure (Hagiwara, 1975). Note that the core portions of both frame transfer imagers [9], [16] are very alike.

VII. Physics of Built-In Overflow Protection (OFP)

In the author's 1975 invention [8], the voltage control of the junction J_e and J_c was strongly emphasized. It is the transistor structure and its junction physics that are important in controlling the OFP mechanism.

The OFP function can be achieved by controlling the voltages of either emitter or collector junction, J_e and J_c. During the integration time of 1/60 s, the amount of the signal electrons can be adjusted any time, and any value from zero up to the maximum capacity by biasing either J_e or J_c properly.

In the case shown in Fig. 2(a), the biasing of the emitter junction is chosen to be controlled for the OFP function. Instead, when the collector junction is chosen to be controlled, the emitter region can be shorted to the surrounding channel stop region. See the Hagiwara, 1978, structure in Fig. 9. There are still enough hole carriers in the emitter region P2(J_e) to quench the surface states which are the source of the undesired dark current. In the case shown in Fig. 2(b), there are two methods to control the J_c bias voltage as explained below.

One method is to let the collector junction bias be controlled by the voltage applied on the collector, provided the majority carrier holes are present in the collector region. Controlling the voltage V is the only possible way to control the collector junction, J_c, because the majority carrier holes in the collector region would block the influence from any external control, such as W in Fig. 2(b). In other words, controlling the "sea" level of the majority carrier holes is the only way to control the collector junction bias since the substrate voltage, $W3$, cannot reach the collector junction J_c. Some external wiring lead is needed to connect this collector region. This is the case of $V = V1$ or $V3$ in Fig. 2(b).

However, when there are no majority carriers present in the collector region, P1, there is nothing to block the electrical influence. So the collector junction bias can be easily controlled by the substrate voltage W. This is similar to the bipolar transistor punchthrough case. In order to have the substrate region, SUB, properly function as the charge sink in this P2

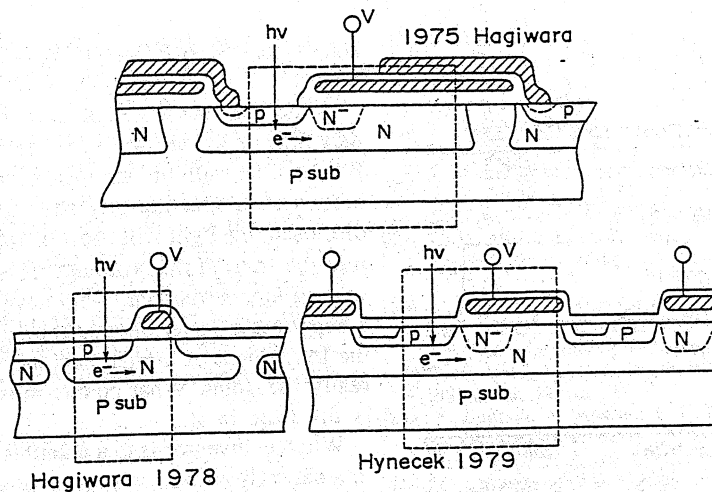


Fig. 9. Three image sensors, Hagiwara 1975/1978, and Hynecek 1979, are compared. The boxed regions in the three sensors operate in the same charge transfer mechanism named by Hynecek, who applied this structure to realize a high performance virtual phase frame transfer CCD imager.

(J_e)–N2(sensor base)–P1(J_c)–SUB(N) structure, the collector region P1(J_c) must be completely depleted.

These essential features mentioned above can be read from the bipolar-type image sensing element structure proposed by the author in 1975 [8]. It had been well known that the charge injection device and the vertical FET structures have similar charge sinks in the bulk. But the presence of the charge sink itself is not a critical issue here. It is the transistor structure and its junction physics that are important in controlling the OFP mechanism.

In the proposed bipolar-type image sensing element, the voltage control of the junctions, J_e and J_c, is to be strongly emphasized. It is well understood that the proper OFP function is essential for realization of a practical video camera system. To this end, it is noted that the structure is now the very basic of the image sensing element of the current commercially widely available interline transfer CCD imagers. And as proposed in Fig. 8(b) and (c), its further applications in the forms of frame transfer CCD imagers with the vertical OFP structure is very promising for future multimedia low-cost video camera applications. See the reference for the FT-imager pioneering works done by Roks [15] and Hyneck [16].

VIII. Background and Origin of the Bipolar-Type Image Sensing Element

In order to explain the originality of the bipolar-type image sensing element an N–SUB–N(sink)–SUB structure by Early [17] is shown in Fig. 10(a) and (b) for comparison. A main feature of the Early's structure deals with a charge sink region N1(Sink) located at a given depth around the substrate.

The imaging structure is a MOS sensor-type which is very similar to the one the author quoted in Fig. 1(b) as a well known structure with the problem of a very poor blue sensitivity.

In the basic unit cell in Fig. 10(b), the Early's structure required the charge sink region N1(sink) to be surrounded by the silicon bulk substrate SUB(P1) and SUB(P2). Since the majority carriers in the substrate SUB(P2) fix the voltage of the substrate, there is no way to get the electrical influence from the charge sink region N1(sink). The electrical field from the charge sink N1(sink) cannot pass through the substrate region SUB(P2) to reach the N2(sensor) region as long as there are some majority carrier holes in the SUB(P2) region.

As in Fig. 10(a) and (b), the depletion region, D1, extended from the charge sink region N1(sink) is quite shallow while the depletion region D2 extended from the N2(sensor) is much wider. According to the description given by Early [17], the depletion region D2 from the surface N2(sensor) region was to be extended much deeper by controlling the sensor gate voltage G as seen in Fig. 10(b). However, it is now known that it is possible only by making the sensor gate voltage higher from G_2 to G_1, as seen in Fig. 10(b).

It is very clear that the presence of the majority carriers in the SUB(P2) region is blocking the electric field from the N1(sink) region. And there is no transistor action possible in this case. This is why, in the case of Fig. 1(c), the OFP function was attached to the emitter junction, simply because the voltage of the region, P1, is hard to be controlled. The same things could be said in the case of Fig. 10(a). The corresponding region SUB(P2) is the substrate itself which has a very large cross coupling capacitance connected to the external power line by the bulk SUB(P1) for stable device operations.

To deplete the SUB(P2) region, Early proposed to raise the gate voltage G, higher to the direction to deepen the potential well. It then increases the electron charge handling capacity of the sensor region N2(sensor) as seen in Fig. 10(b). And more electron charges, generated by the incident light, will be accumulated in the sensor area. This makes the originally intended OFP function much difficult to be achieved. It is actually impossible to achieve the function. Apparently, the physics of the buried channel CCD itself was not properly understood.

The structure claimed by Early is very difficult to function properly as OFP in practice. Moreover, this structure is also specified to have a contact lead to the wafer surface vertically.

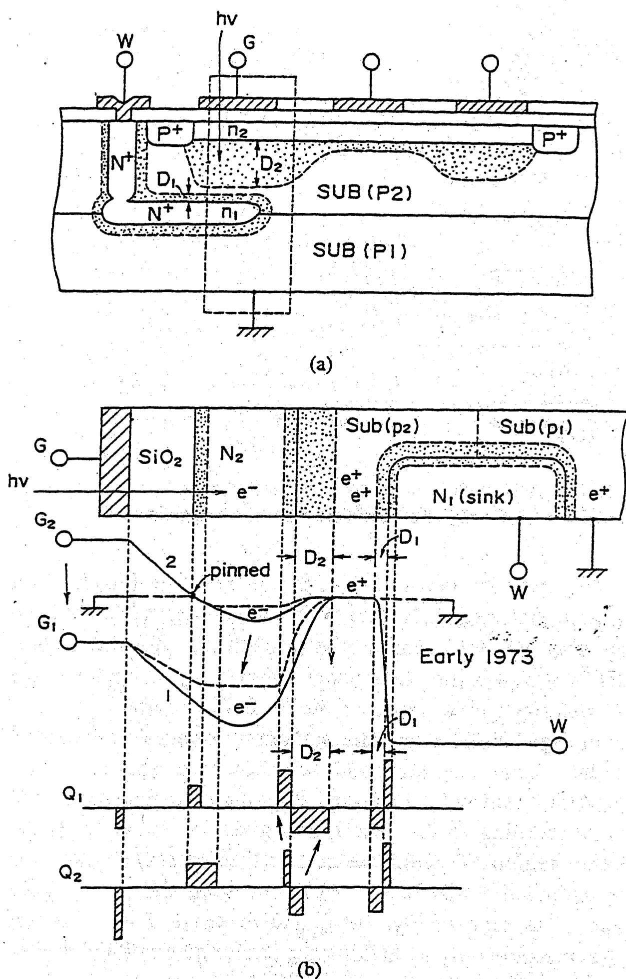


Fig. 10. (a) MOS-type image sensing element with a charge sink a N2–P(sub)–N1(sink)–SUB(p) structure with much deeper depletion region extended from the N2 region. Note that the depletion region surrounding the N1(sink) region extends a fairly short way into the P(sub) region. Note also that the majority hole carriers are present in the P(sub) region. The operation is not in the punchthrough mode. (b) Operations of the MOS-type image sensing element when the charge is present in the p-region. Q1 and Q2 are fixed charges in the depletion regions, where no mobile carriers are present. Note that in order to extend the depletion region, D2, by the gate voltage G, the voltage must become higher, (G_2 to G_1), creating much deeper potential well in the buried channel region N2 that will allow more electron charges to accumulate in N2. No OFP mechanism as claimed by Early is possible in this configuration.

And besides, between the surface lead contact and the image sensing area, a highly doped channel stop region was also required. To prevent ohmic short between the highly doped n^+ region and the highly doped p^+ region, wide spacing is needed, and it still consumes quite a large area of silicon chip area and the structure is not quite attractive.

According to these results and speculations, obtained from the author's cross reference checks, including the Early's 1973 structure [17], the author's original Japanese publication [8] seems to be the origin of this important bipolar-type image sensing element structure, with an inherently built-in overflow protection option. It is a practical and functioning P2(J_e)–N2(sensor base)–P1(J_c)–SUB(P/N) structure, entirely different from the Early's version of the N2(sensor)–SUB(P2)–N1(sink)–SUB(P1) which had never reported to be functioning properly.

Sometimes the words of an inventor are misleading because they may be written while the idea is still in an immature stage. But it is the truth hidden inside the words that is important. A hidden truth does not give any light to us. Only if the truth is disclosed, the light will show us the way to follow. As we look into the truth in the wording, (if it contains a truth), we often find an ardent visionary who never gives up his dream. He is a beautiful dreamer deep in thought, in search of the truth for the betterment of human happiness. The legal wording is not really the point. What counts most for our human happiness is the truth in it.

What an inventor is to a manufacturer is not what a master is to a slave. Inventors and manufacturers are beautiful dreamers both in the same boat in search of "the truth that shall make us all free." The author heard these words when he was a freshman at the California Institute of Technology in September 1967. He gradually began to feel that he understood the meaning of these word. The original idea gradually formed in the author's mind while he was working on his Ph.D. research on CCD's in 1972 under the guidance of Prof. C. A. Mead [18], [19], and Prof. T. C. McGill [20].

When the CCD was invented in early 1970's [21], the seemingly well-understood common physics of CCD imaging sensors of today was not quite properly understood. So, the author felt a strong urge to perform intensive computer device simulations [22] and [23], and dreamed of the possibility of high performance buried channel CCD for the potential low-light imaging applications.

The author was attracted by the inherently high speed and the good transfer efficiency of the buried channel CCD characteristics. And the need for portable video cameras with very high sensitivity in dark scenes had guided the author to the idea of the bipolar-type image sensing element in 1975.

IX. Conclusion

The concept and origin of the bipolar-type image sensing element was explained in detail. Its realization in the form of narrow-channel-type frame transfer CCD imagers was reviewed and the application was now extended to a 800 H × 492 V frame transfer-type buried channel CCD imager with a proposed vertical overflow protection and inherently built-in buffer memory structure for future low cost multimedia applications.

After more than 25 years of worldwide work with experimental trials, and intensive production efforts by dreaming engineers, scientists, and manufacturers, the present high-performance industrial and low-cost consumer CCD imagers finally have come to life. It is not only the author's strong conviction but also his humble wish that the CCD imager's current status will last, as it is, for another 25 years.

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