Historical Development Efforts of Solid State Image Sensors

Four Types of Image Sensor Structure

	Blue Light Sensitivity	Image Lag	Surface Dark Current	Electric Shutter
(1) the N+P Single Junction type Classical Floating Surface Dynamic Photodiode	△	×	○	×
(2) the CCD/MOS Metal Oxide Gate Dynamic Photo Capacitor invented and developed by Boyle/Smith in 1969	×	○	×	×
(3) the P+NPsub Double Junction type Pinned Photodiode invented by Hagiwara in 1975 and developed in 1978 by Hagiwara Team in Sony with Excellent Blue Light Sensitivity No Image Lag and No Surface Dark Current	○	○	○	×
(4) the P+NPNsub Triple Junction type Pinned Photodiode invented by Hagiwara in 1975 and developed in 1987 by Hamazaki Team in Sony with Completely Mechanical-Parts Free No Image Lag Electrica Shutter	○	○	○	○

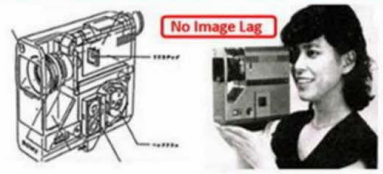
In the Japanese Patent Applications JPA1975-127647 and JPA1975-134985, Hagiwara at Sony described the image lag feature of the Pinned Photodode, using the Empty Potentential Well of the N type Buried Base Storage Region which is the result of the complete charge transfer. In IEDM1982, NEC reported the same PNP double junction type dynamic photodiode, called it as Buried Photodiode and explained more in details analytically about the image lag feature.

In the SSDM1978 paper, Hagiwara Team in Sony in 1978 reported the P+NP double junction type dynamic photodiode with very low surface dark current of less than 3 % with the P+ surface hole accumulation region pinned and grounded by the adjacent P+ channel Stops. In IEDM1984, KODAK also reported the same P+NP double junction type dynamic photodiode, called it as Pinned Photodiode and explained the details of the low surface dark current feature.

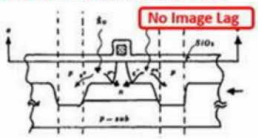
In 1987, Sony developped the P+NPNsub triple junction type dynamic photodiode, called it as Hole Accumulation Diode (HAD) and explained the details of the Electrical Shutter Function.

Buried Photodiode of NEC, Pinned Photodiode of KODAK and Hole Accumulation Diode (HAD) of Sony are all the same multi-junction dynamic photodiodes invented by Hagiwara in 1975.

Sony original 570H x 498 V one-chip FT CCD Image Sensor with Pinned Photodiode, July 1980



P+NP Junction Pinned Photodiode



On July 1980, Iwama Kazuo at Sony Tokyo Press Conference and Morita Akio at New York Press Conference announced the one chip CCD video camera with the 8 mm VTR in one box.

See the Original 1978 Publication of the Pinned Photodiode Sensor

Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488V CCD imager with narrow channel transfer gates," Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Appllied Physics , vol. 18, supplement 18-1, pp. 335-340, 1979

High quality picture of SONY CMOS Imager is also based on SONY HAD (Pinned Photodiode).

These figures shows (1) Excellent Blue Light Sensitivity (2) Low Surface Dark Current and (3) NO Image Lag Features of the P+NP junction type Pinned Photodiode.

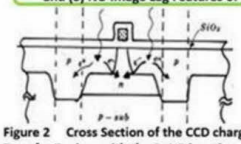
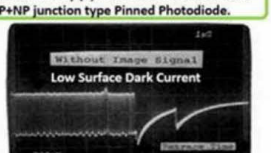


Figure 2 Cross Section of the CCD charge Transfer Region with the P+NP junction type Pinned Photodiode (PPD)



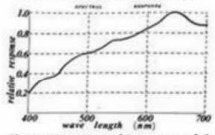


Figure 13 Spectral Response of the P+NP junction Pinned Photodiode (PPD) with the excellent blue light sensitivity

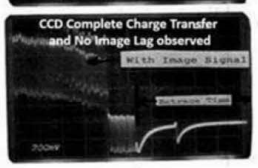


Figure 14 Comparison of CCD image sensor output signals with and without image signal.

Pinned Photodiode and Sony Hole Accumulation Diode (HAD)

PNPN junction Transistor type Pinned Photodiode

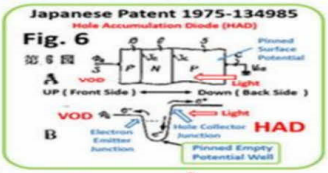
Visit https://www.j-platpat.inpit.go.jp/ and put the patent number 1975-134985

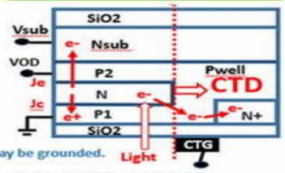
File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

Patent Claim in English Translation

(1) In the semiconductor substrate (Nsub), the first region(P1) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N) is is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N) . And (6) Collector junction (Jc) is formed by the second region (N) and the first region (P1), forming a transistor structure (P2NP1) (7) Photo charge is stored in the Base region (N) according to the illuminated light intensity, and transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.

Japanese Patent 1975-134985





Yoshiaki Hagiwara, Japanese Patent JP 1975-134985

Pinned Photodiode defined in JPA 1975-127647 by Hagiwara in 1975