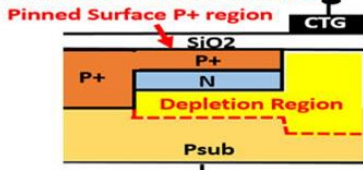
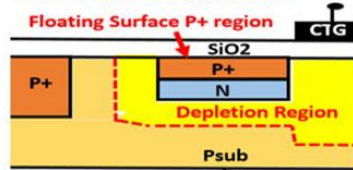


Difference of Buried Photodiode and Pinned Photodiode

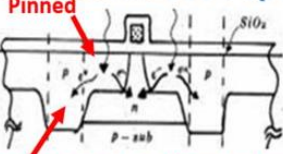
Pinned Photodiode



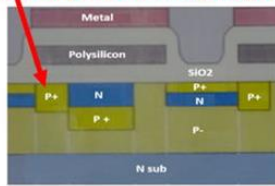
Buried Photodiode



SONY SSDM1978 Paper

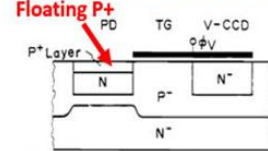


P+ Channel Stops and no Image Lag Problem

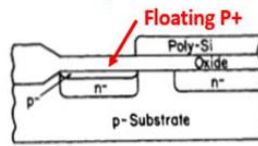


SONY 1987 HAD Sensor

NEC IEDM1982 Paper



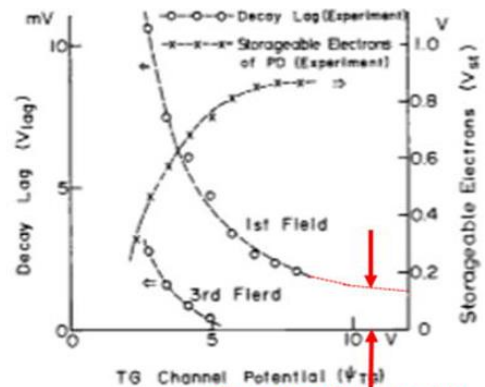
No P+ Channel Stops and Serious Image Lag



KODAK IEDM1984 Paper

NEC IEDM1982 Paper reported Image Lag

Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 volt.



There is still image lag at the CTD gate voltage more than 10 volt.

Fig.6. Storageable electrons vs. transfer gate channel potential, and decay lag vs. transfer gate channel potential in the P⁺N⁺ structure photodiode

KODAK had LOCOS Channel Stops but NEC did not have any P+ Channel Stops. NEC buried N region may be floating?

Difference of Pinned Photodiode and Buried Photodiode

Pinned Photodiode must have the P+ heavy doped channel stops nearby.

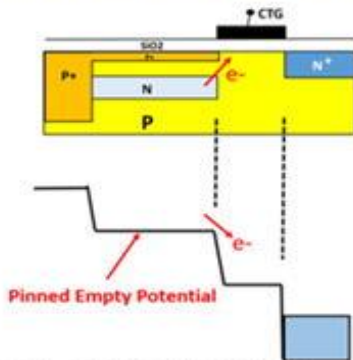
Pinned Photodiode must be a buried photodiode.

Pinned Photodiode must not have the edge barrier to the Charge Transfer Gate

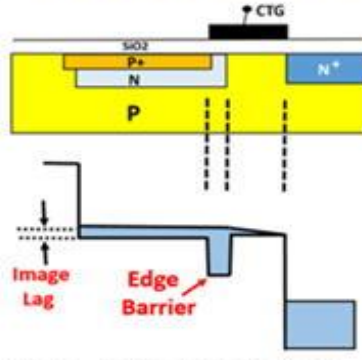
Pinned Buried Photodiode does not have the edge barrier

Buried Photodiode with the edge barrier

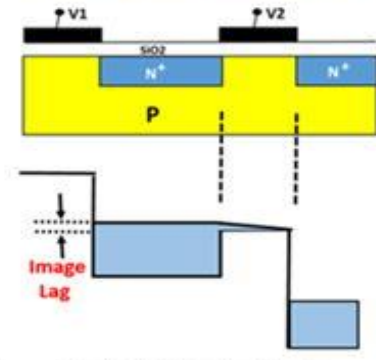
Bucket Brigade Device (BBD) with Serious Image Lag



(1) Pinned Photodiode with No Image Lag

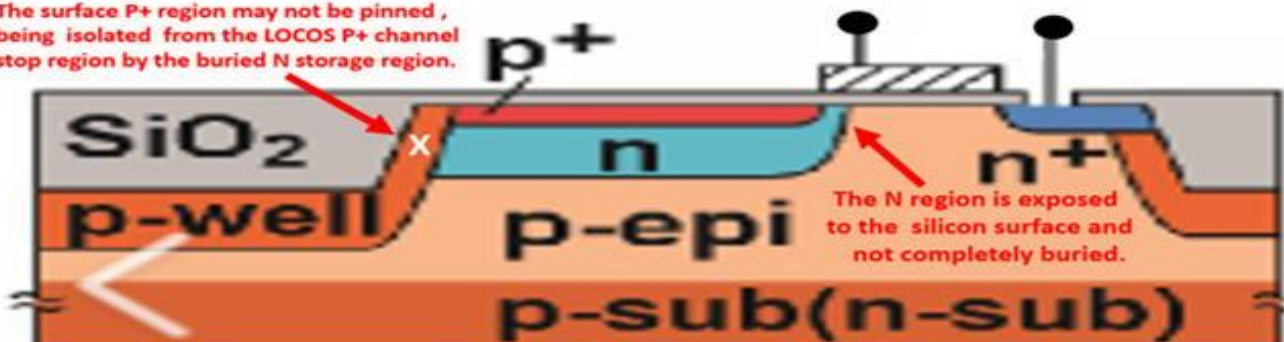


(2) Buried Photodiode with BBD Barrier



(3) Bucket Brigade Device (BBD)

The surface P+ region may not be pinned, being isolated from the LOCOS P+ channel stop region by the buried N storage region.



This photodiode is not Pinned Photodiode since the N storage region is not completely buried.