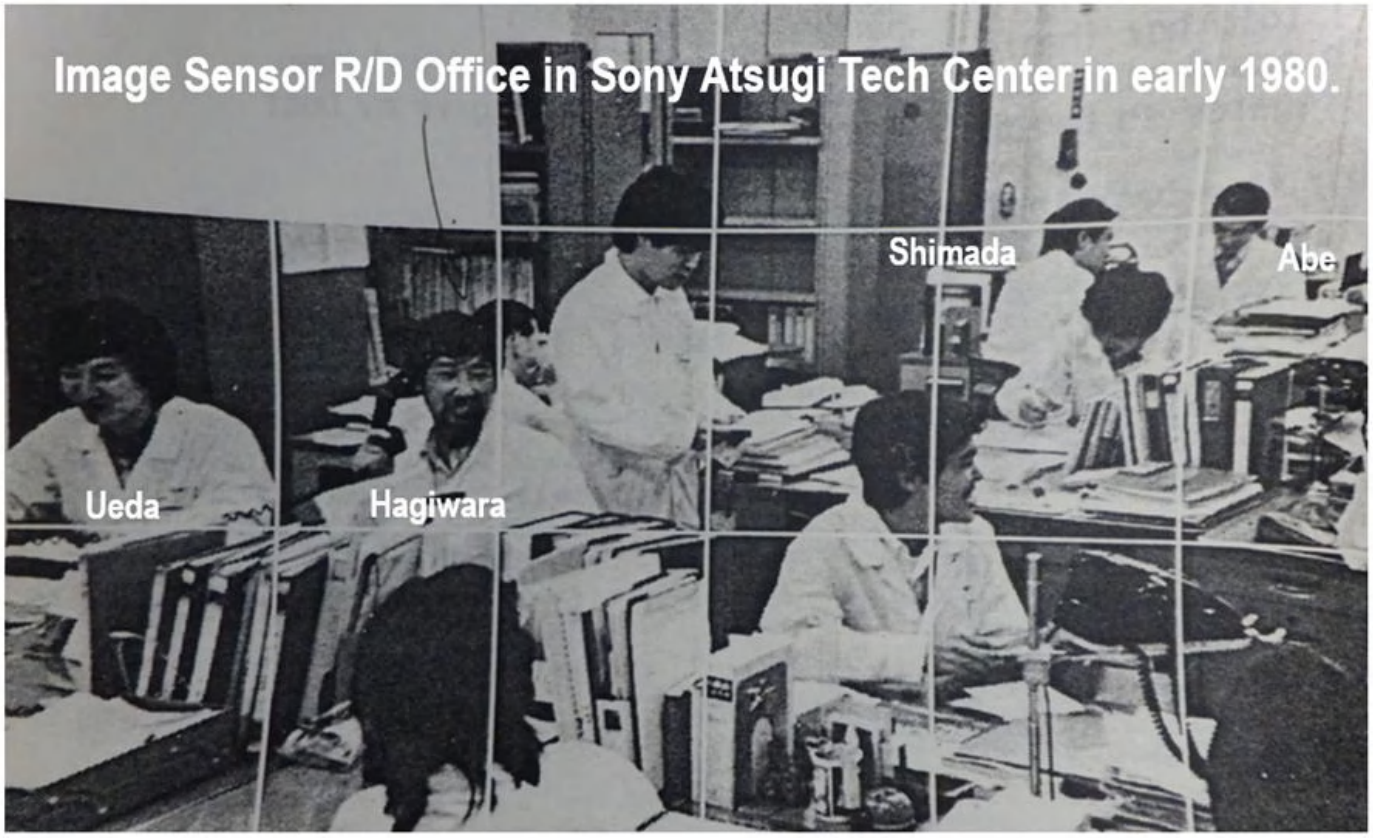
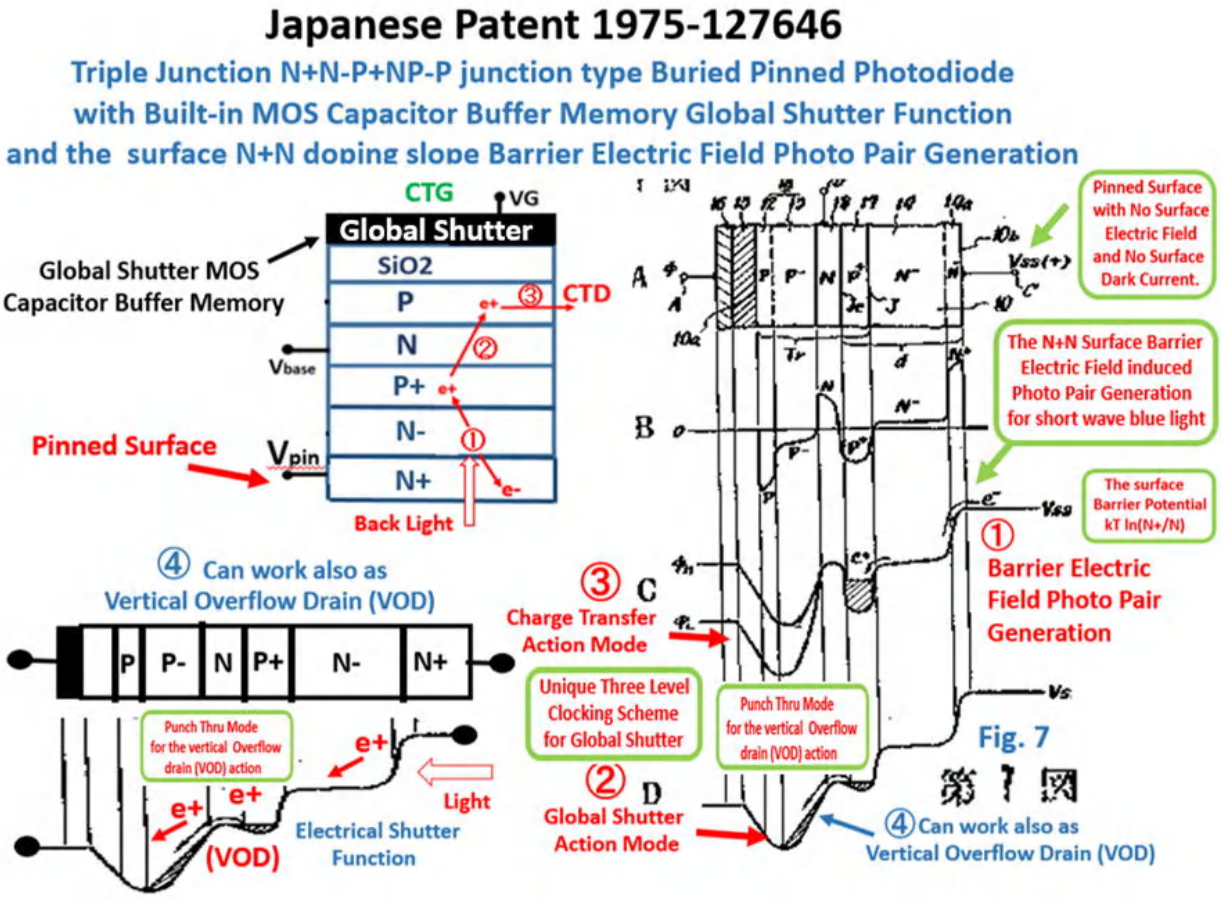



N+N-P+NP Triple Junction Pinned Photodiode invented by Hagiwara in 1975.

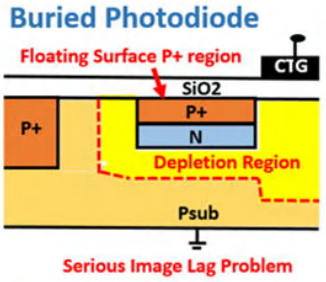



This is the evidence that Hagiwara is the inventor of the Triple junction type Pinned Photodiode with the Pinned Surface.

●There is no adjacent P+ channel Stops in the NEC Teranishi IEDM1982 paper.

## Difference of Buried Photodiode and Pinned Photodiode

**Figure 5 does not have the P+ channel stop nearby.**



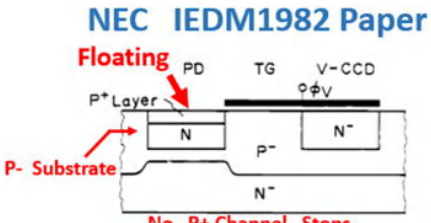
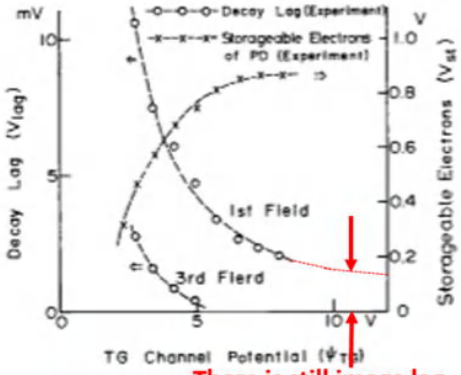




Fig.5. P+NP- structure photodiode
(a) Unit cell cross sectional view



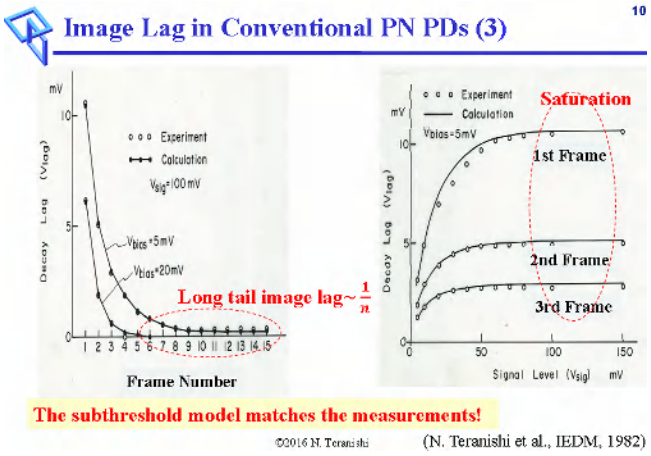

There is still image lag
at the CTD gate voltage more than 10 volt.

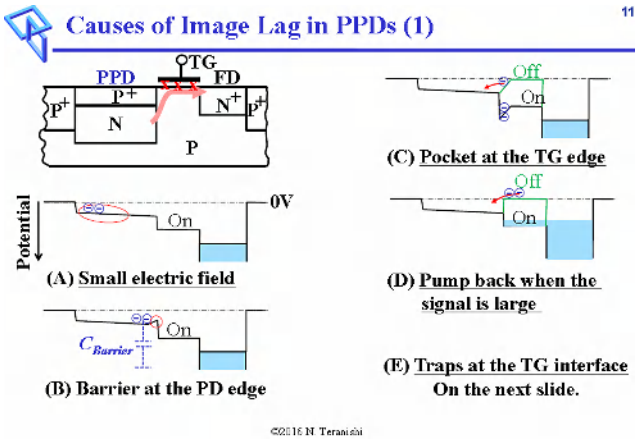
Fig.6. Storageable electrons vs. transfer gate channel potential, and decay lag vs. transfer gate channel potential in the P+NP- structure photodiode

## NEC IEDM1982 Paper reported Image Lag

**Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 volt.**

●However, Teranishi showed the adjacent P+ channel Stops near the PNP buried photodiode in his 2016 presentation slides, which was not his idea in 1982.

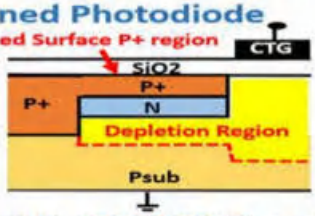


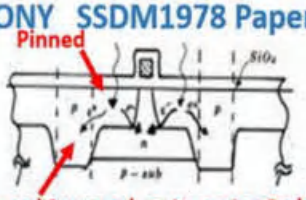

The actual P+NP Buried Phtoodiode may not be the double junction PNP photodiode reported by SONY(Hagiwara) in SSDM1978 and also nor the Pinned Photodiode reported by KODAK in IEDM1984. The NEC Buied Photodiode reported in IEDM1982 did not have the adjacent P+ heavily doped channel stops. And it may the reason why the NEC IEDM1982 paper has the image lag problem. Hagiwara reported no image lag in SSDM1978 P+NP double juntion type photodiode with the adjacent Pinned P+ channel stops.

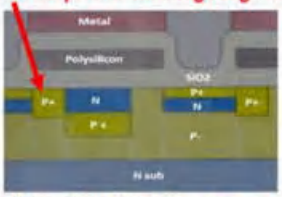
## Difference of Buried Photodiode and Pinned Photodiode

### Pinned Photodiode



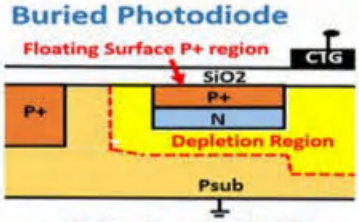

SONY SSDM1978 Paper



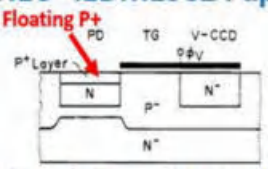

SONY 1987 HAD Sensor

### Buried Photodiode

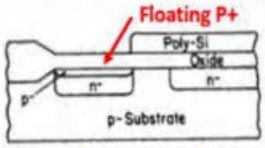



Serious Image Lag Problem

NEC IEDM1982 Paper



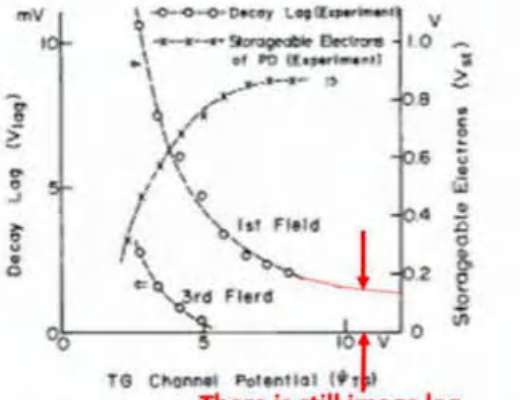

No P+ Channel Stops and Serious Image Lag




KODAK IEDM1984 Paper

### NEC IEDM1982 Paper reported Image Lag

Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 vo




There is still image lag at the CTD gate voltage more than 10 volt

Fig.6. Storageable electrons vs. transfer gate channel potential, and decay lag vs. transfer gate channel potential in the P+NP- structure photodiode

KODAK had LOCOS Channel Stops but NEC did not have any P+ Channel Stops. NEC buried N region may be floating ?

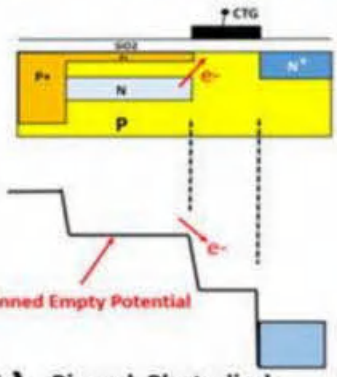
## Difference of Pinned Photodiode and Buried Photodiode

Pinned Photodiode must have the P+ heavy doped channel stops nearby.

Pinned Photodiode must be a buried photodiode.

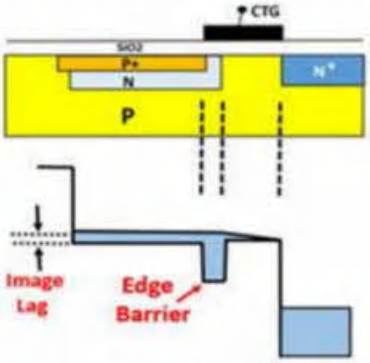
Pinned Photodiode must not have the edge barrier to the Charge Transfer Gate

### Pinned Buried Photodiode does not have the edge barrier



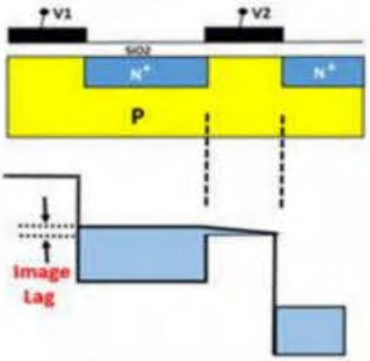

(1) Pinned Photodiode with No Image Lag

### Buried Photodiode with the edge barrier



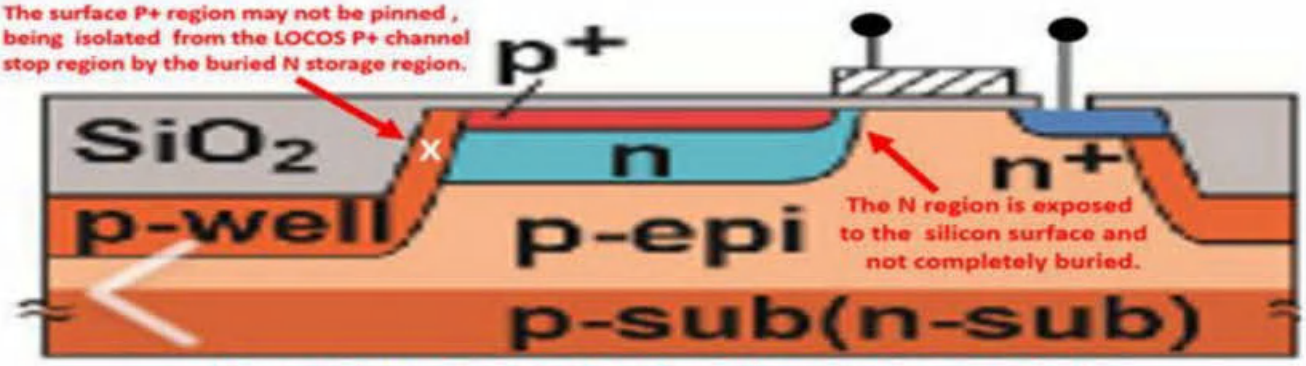

(2) Buried Photodiode with BBD Barrier

### Bucket Bridgade Device (BBD) with Serious Image Lag




(3) Bucket Brigade Device (BBD)

The surface P+ region may not be pinned , being isolated from the LOCOS P+ channel stop region by the buried N storage region.




This photodiode is not Pinned Photodiode since the N storage region is not completely buried.

# A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, *Fellow, IEEE,* and Donald B. Hondongwa, *Student Member, IEEE*

***Abstract*—The pinned photodiode is the primary photodetector structure used in most CCD and CMOS image sensors. This paper reviews the development, physics, and technology of the pinned photodiode.**

The photocurrent depends on the wavelength-dependent photon flux $\phi(\lambda)$ incident on the semiconductor and the wavelength-dependent quantum efficiency $\eta(\lambda)$ which accounts for optical reflection, absorption and carrier collection:

## ACKNOWLEDGMENTS

The authors gratefully acknowledge the helpful comments of N. Teranishi, J. Nakamura, J. Solhusvik, J. Hynecek, A. Theuwissen, D. Murphy, M. Guidash, X. Cao and others in the imaging community. The authors also wish to thank R. Fontaine and Chipworks for supplying state-of-the-art cross-section data and to G. Agranov and Aptina for providing sample device structures as a starting point for academic simulation purposes.

These people did not see any fake in this Fossum Paper ???

**Fossum insulted in his 2014 paper Sony and Hagiwara 1975 PPD invention.**

**Indeed, Hagiwara invented PPD with VOD and the virtual charge transfer in 1975 !!**

IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY, VOL. 2, NO. 3, MAY 2014 33

**Sony HAD (PPD+VOD) does not use LOCOS !!!**

A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, *Fellow, IEEE,* and Donald B. Hondongwa, *Student Member, IEEE*

**False**

**Many people now said this is a fake paper !**

*C. Other Contributions to the PPD Invention*

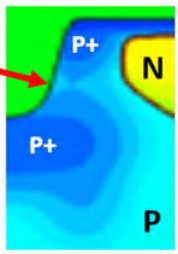
The PPD structure, while invented for low lag ILT CCD application, shares a strong resemblance to the Hynecek virtual-phase CCD structure, with the exception of the VOD. The two inventions were solving different problems with essentially the same device structure and operating principles.

In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a *pnp* vertical structure was disclosed, among several structures [24]. The top *p* layer was connected by metal to a bias used to control full-well capacity and the *n*-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1996, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called "Hole Accumulation Diode," or HAD structure [25]. However, the 1975 application did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the NEC paper was published. However, the "narrow-gate" CCD with an open *p*-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

**False**

The PPD, as it is most commonly used today, bears the strongest resemblance to the Teranishi et al. ILT CCD device. Thus, these days Teranishi is considered as the primary inventor of the modern PPD [29].

The surface P+ layer is NOT connected to the LOCOS P+ layer. The surface P+ layer may be floating and this photodiode may have serious image lag.




**Serious Image Lag ?**

**NOT connected**

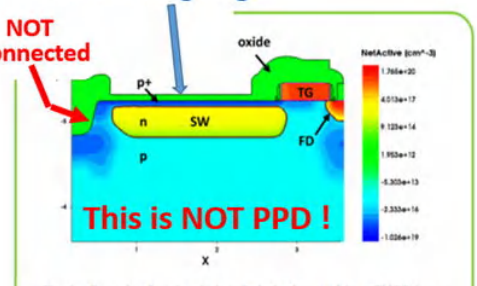



Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

**Hagiwara in 1975 invented PPD with VOD and the virtual charge transfer.**

**Study the Japanese Patents 1975-127646, 1975-127647 and 1975-134985.**

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# Sony's Representative Inventions Supporting Stacked Multi-Functional CMOS Image Sensors

Sony Corporation
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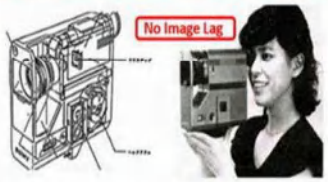
## Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

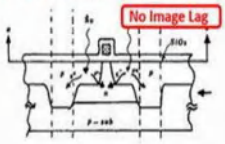
The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

**Sony original 570H x 498 V one-chip FT CCD Image Sensor with Pinned Photodiode, July 1980**




P+NP Junction Pinned Photodiode




On July 1980, Iwama Kazuo at Sony Tokyo Press Conference and Morita Akio at New York Press Conference announced the one chip CCD video camera with the 8 mm VTR in one box.

**See the Original 1978 Publication of the Pinned Photodiode Sensor**

Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488V CCD imager with narrow channel transfer gates," Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Appllied Physics , vol. 18, supplement 18–1, pp. 335–340, 1979

**High quality picture of SONY CMOS Imager is also based on SONY HAD ( Pinned Photodiode).**

**These figures shows (1) Excellent Blue Light Sensitivity (2) Low Surface Dark Current and (3) NO Image Lag Features of the P+NP junction type Pinned Photodiode.**

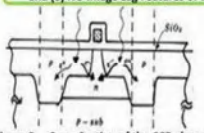
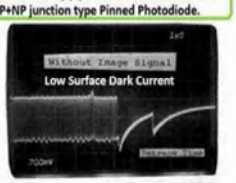


Figure 2 Cross Section of the CCD charge Transfer Region with the P+NP junction tvoe Pinned Photodiode (PPD)



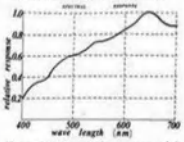



Figure 13 Spectral Response of the P+NP junction Pinned Photodiode (PPD) with the excellent blue light sensitivity


Figure 14 Comparison of CCD image sensor output signals with and without image signal.

# Pinned Photodiode and Sony Hole Accumulation Diode (HAD)

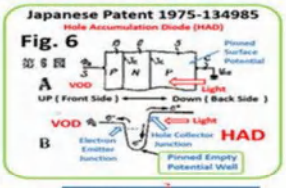
## PNPN junction Transistor type Pinned Photodiode

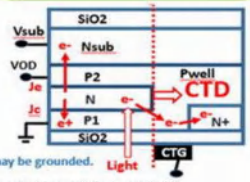
Visit https://www.j-platpat.inpit.go.jp/ and put the patent number 1975-134985

| | | | |
|---|---|---|---|
| File | 1975-134985 | Filed | 1975/11/10 |
| Public | 1975-058414 | Public | 1977/05/13 |
| | | Grant | 1983/10/19 |

**Patent Claim in English Translation**

**(1) In the semiconductor substrate (Nsub), the first region( P1 ) of the first impurity type is formed, (2) on which, the second region ( N ) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N) is is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction ( Je ) is formed on the second region (N) of the light collecting part (N) . And (6) Collector junction ( Jc ) is formed by the second region (N) and the first region (P1), forming a transistor structure ( P2NP1 ) (7) Photo charge is stored in the Base region (N) according to the illuminated light intensity, and transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.**




Yoshiaki Hagiwara, Japanese Patent JP 1975-134985

## Pinned Photodiode defined in JPA 1975-127647 by Hagiwara in 1975

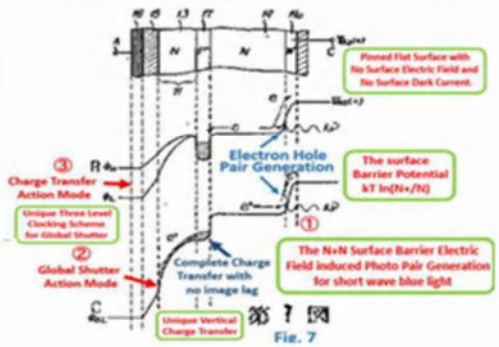



Fig. 7

To search page

# 1975-80
# Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

**~ Discrete Semiconductor/Others ~**

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

Photodiodes are used for photodetectors of image sensors. In 1987, Sony introduced a 2 / 3-inch, 380,000-pixel CCD image sensor (ICX022) using a new type of photodetector, now called a Pinned Photodiode (Sony named it HAD: Hole Accumulation Diode)[1].

The Pinned Photodiode is a photodiode in which the entire N layer is covered with a P layer. The part of the P layer on the light incident surface is heavily doped P+ (Fig-1). Kodak named this structure Pinned Photodiode in 1984 because the P + surface of the light incident surface was pinned to the substrate potential. This device has features such as high light sensitivity, wide dynamic range, image lag free, much smaller dark current due to reduced influence of GR center on the light receiving surface, and no white scars.

In 1975, Sony proposed using a PNP transistor as the photodetector[3]. By providing a P + layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated, greatly improving the light sensitivity. This P + layer was also a proposal to reduce the dark current and image lag which became the basis of the pinned photodiode.

In 1978, Sony presented a 93,000-pixel FT (Frame Transfer) -CCD image sensor compliant with the Analog TV Broadcasting Standard (SDTV) for the first time in the world[5], using the photodiode with the same structure as above. Sony succeeded in 1981 in trial production of a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor by further improvement of this technology[6].

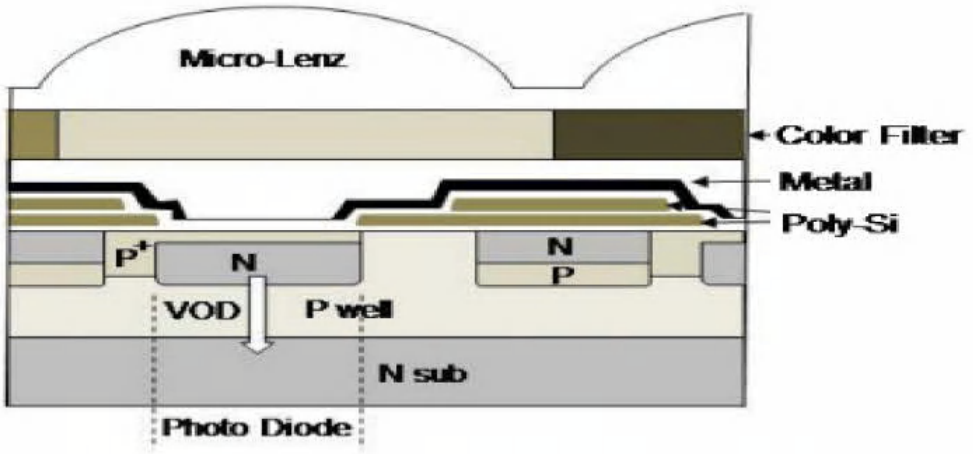



Fig-1 Recent Image Sensor with Pinned Photodiode

References:

【1】M. Hamasaki, T. Suzuki, Y. Kagawa, K. Ishikawa, K. Miyata and H. Kambe, "An IT-CCD imager with electronically variable shutter speed" , Technical Report of The Institute of Image Information and Television Engineers. vol. 12, no. 12, pp. 31-36, (1988)

【3】Y. Hagiwara, Japanese Patent JP1975—134985

【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

【6】I. Kajino, M. Shimada, Y. Nakada, Y. Hirata and Y. Hagiwara, "Single Chip Color Camera Using Narrow channel CCD Imager with Over Flow Drain"、Technical Report of The Institute of Image Information and Television Engineers、vol. 5, no. 29, pp.

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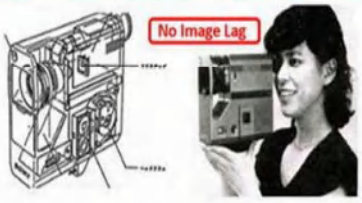
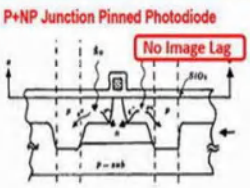
In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

**Sony original 570H x 498 V one-chip FT CCD Image Sensor with Pinned Photodiode, July 1980**




On July 1980, Iwama Kazuo at Sony Tokyo Press Conference and Morita Akio at New York Press Conference announced the one chip CCD video camera with the 8 mm VTR in one box.

**See the Original 1978 Publication of the Pinned Photodiode Sensor**

Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488V CCD imager with narrow channel transfer gates," Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Appllied Physics , vol. 18, supplement 18–1, pp. 335–340, 1979

**High quality picture of SONY CMOS Imager is also based on SONY HAD ( Pinned Photodiode).**

**These figures shows (1) Excellent Blue Light Sensitivity (2) Low Surface Dark Current and (3) NO Image Lag Features of the P+NP junction type Pinned Photodiode.**

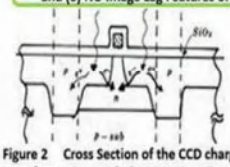
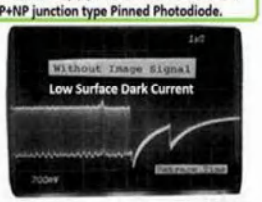


Figure 2 Cross Section of the CCD charge Transfer Region with the P+NP junction type Pinned Photodiode (PPD)



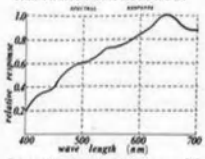




Figure 13 Spectral Response of the P+NP junction Pinned Photodiode (PPD) with the excellent blue light sensitivity

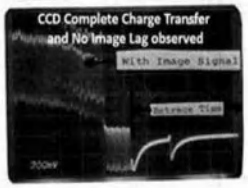



Figure 14 Comparison of CCD image sensor output signals with and without image signal.

# Pinned Photodiode and Sony Hole Accumulation Diode (HAD)

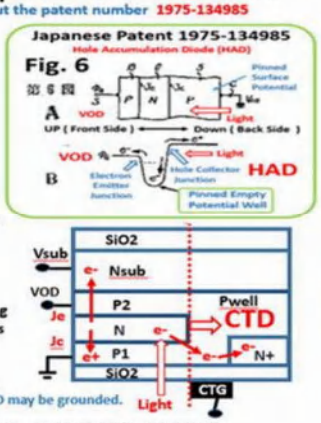
## PNPN junction Transistor type Pinned Photodiode

Visit https://www.j-platpat.inpit.go.jp/ and put the patent number 1975-134985

| | | | |
|---|---|---|---|
| File | 1975-134985 | Filed | 1975/11/10 |
| Public | 1975-058414 | Public | 1977/05/13 |
| | | Grant | 1983/10/19 |

**Patent Claim in English Translation**

**(1) In the semiconductor substrate (Nsub), the first region( P1 ) of the first impurity type is formed, (2) on which, the second region ( N ) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N) is is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction ( Je ) is formed on the second region (N) of the light collecting part (N) . And (6) Collector junction ( Jc ) is formed by the second region (N) and the first region (P1), forming a transistor structure ( P2NP1 ) (7) Photo charge is stored in the Base region (N) according to the illuminated light intensity, and transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.**

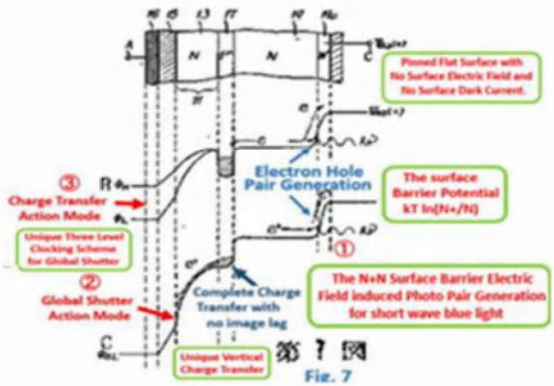




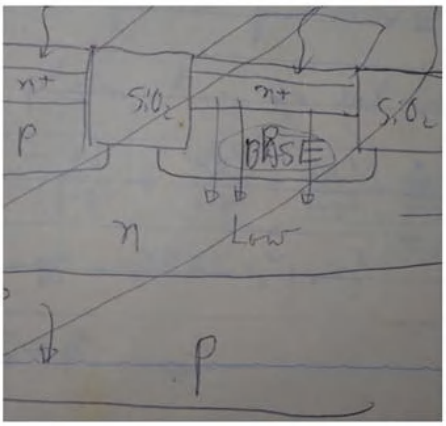


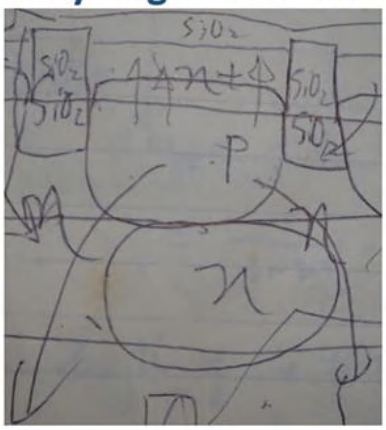
Yoshiaki Hagiwara, Japanese Patent JP 1975-134985

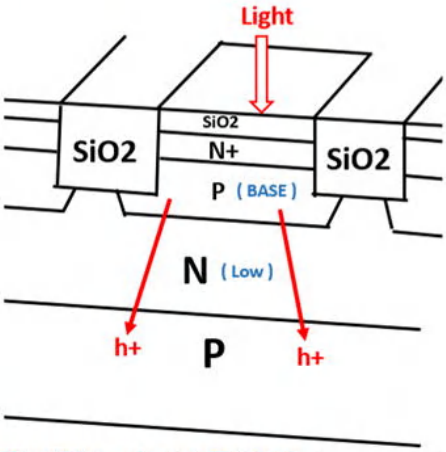
## Pinned Photodiode defined in JPA 1975-127647 by Hagiwara in 1975



# The N+PNP junction type Dynamic Photo Transistor Structure Pinned Photodiode and Sony Hole Accumulation Diode (HAD) with the vertical overflow drain (VOD) function invented by Hagiwara at Sony in 1975




## Hagiwara's Lab Note at Sony in February 1975

In 1975 at Sony, Yoshiaki Hagiwara filed three Japanese patents JPA1975-127646, JPA1975-127647 and JPA1975-134985 on the Pinned Surface Photodiode with the VOD function which is later called as Sony Hole Accumulation Diode (HAD). Hagiwara did not file a patent on the SiO2 device isolation but this lab note shows that Hagiwara had an idea of forming the Shallow Trench Isolation by the Local Oxidation Method, which was hinted by the LOCOS isolation in 1970s.

Please see for details the Japanese Patent Applications JPA 1975-127646, 1975-127647 and 1975-134985.

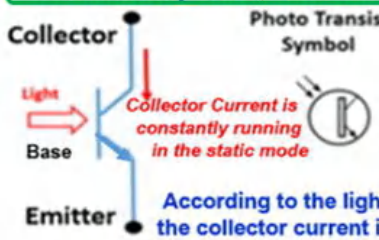
**Difference of the static and dynamic photo transistors are illustrated in these figures.**
**Sony Hole Accumulation Diode (HAD) is the P+NPNsub junction dynamic photo transistor with the surface P+ hole collecting and accumulation region is pinned and grounded, which is now widely called as Pinned Photodiode with the vertical overflow drain (VOD) function. Only Pinned Photodiode with the VOD function can realize the electrical shutter function.**

**SONY HAD Sensor 1975 was hinted by SONY PNP Bipolar Transistor Process Technology**

*Conventional Static Phototransistor*

*( by John Northrup Shive , 1950 )*

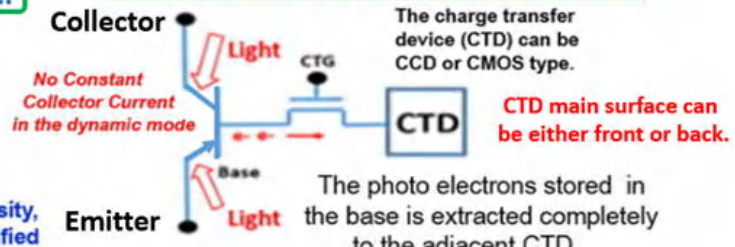
No memory function is involved.

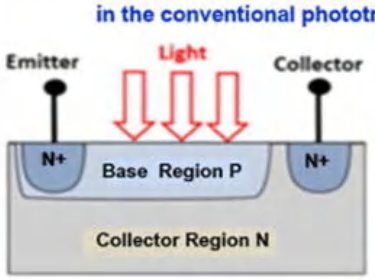


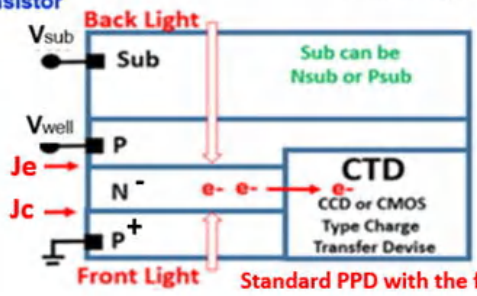

*Dynamic Phototransistor Operation*

**by Yoshiaki Hagiwara at Sony in 1975**

Dynamic Memory function is involved.




*Complete Charge Extraction from the N base region for low image lag and high speed high quality action pictures*

Standard PPD with the front CTD main surface

See JPA 1975-134985 for the details of Pinned Photodiode invented by Yoshiaki Hagiwara at Sony in 1975.