Simulation and Device Characterization of the P+PN+P Junction Type Pinned Photodiode and Schottky Barrier Photodiode

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***Abstract*— Process parameter tolerance of semiconductor device is very important for manufacturability and yield. Pinned Photodiode has by definition the pinned surface potential of the low surface dark current feature and the pinned empty potential well of the no image lag feature with the excellent blue light sensitivity of the ideal quantum efficiency. This paper reports simulation and device characterization of the unique P+PN+P junction type Buried, Depletion and Pinned Photodiode with excellent manufacturability, originally invented in 1975. Related various historical photodiode structures are reviewed, including the metal semiconductor Schottky Barrier photo sensor of Au/ β - Ga_2O_3 type in search for the low leakage and dark current photodiode which led the 1975 invention of the low leakage P+NPNsub junction Pinned Photodiode by Hagiwara.**

Keywords—Buried Depletion Pinned Photodiode, built-in barrier potential, Hole Accumulation Diode (HAD), electron hole pair separation, built-in barrier potential

I. INTRODUCTION

Many failures in device applications are related to loss of the device current blocking capability. The very low reverse leakage current feature of the commercially available Trench-based Schottky barrier rectifier switch is a key parameter for device performance, including the high performance required for the super light sensitive, the low surface dark current and the low 1/f noise image sensors[1]at very low light level with the low image lag feature.

Fig. 1 shows the light penetration depth[2] in the silicon crystal with respect to the incident light wave length. The maximum light penetration depth into the silicon crystal is about 0.2 micro meter for the blue light of 0.4 micro meter wave length and 37.6 eV photon energy while the light penetration depth is about 8 micro meter for the red light of 0.7 micro meter wave length and 12.3 eV photon energy. To achieve the best color reproduction picture quality for the CMOS image sensors we need a photodiode which can convert the incident blue light energy into the electric energy very efficiently. Various types of photo sensors are compared in Fig. 2. The N+P+ junction (type A) Esaki Diode has the two states, high and low current modes, in the forward bias. However, it has a relative large leakage current in the reverse bias because both sides of the N+ and P+ regions are very much heavily doped.

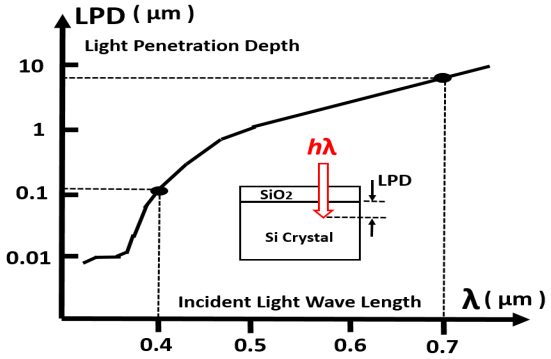

Fig 1: Light Penetration Depth (LPD) in Silicon Crystal.

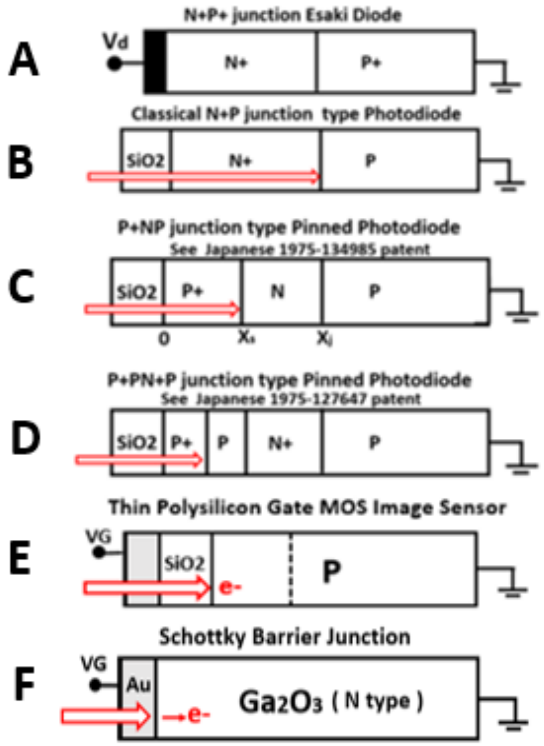

Fig 2: various types of photo sensor structures.

Classical N+P junction type B photodiode is known to have the serious image lag problem. The type C Pinned Photodiode[3], invented in 1975 by Hagiwara, has the pinned surface potential of the no leakage current feature and the pinned empty potential of the no image lag feature. See Fig.3. As originally reported by Hagiwara 1978 paper[4], the P+ surface HAD layer had the Gaussian doping profile with Qs = 2 x 10^{13} cm^{-2} and Ns =1 x 10^{18} cm^{-3} while the buried N region had Nd = 3 x 10^{16} $cm^{-3}$and Qd = 1.7 x 10^{12} cm^{-2}. The type D Pinned Photodiode has the unique built-in barrier electric field, enhancing the photo electron pair separation at the surface of the silicon crystal for the short wave length blue light.

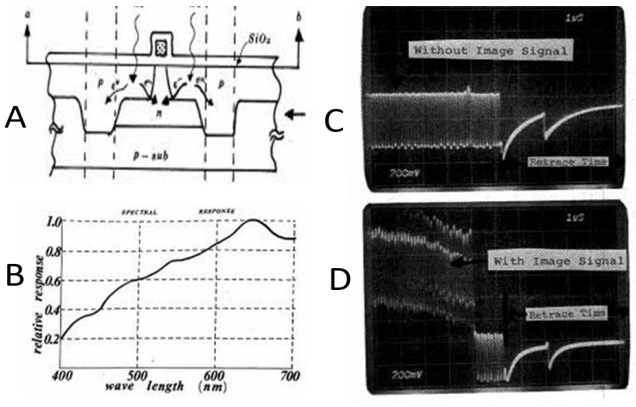

Fig 3: Features of P+PN junction type Pinned Photodiode

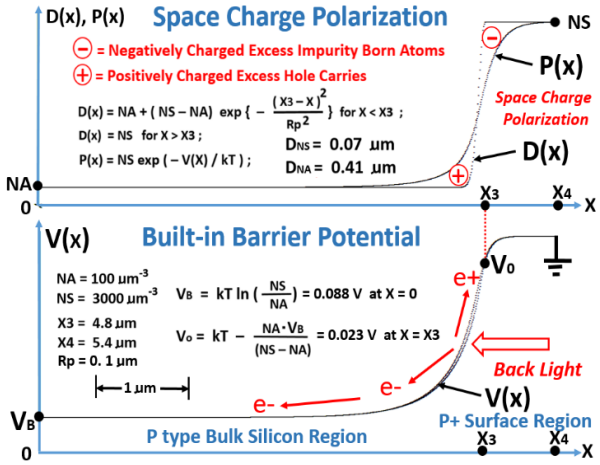

Fig. 4: Exact numerical calculations of Gaussian P+P doping profile D(x), the hole carrier density P(x) and the built-in barrier potential V(x).

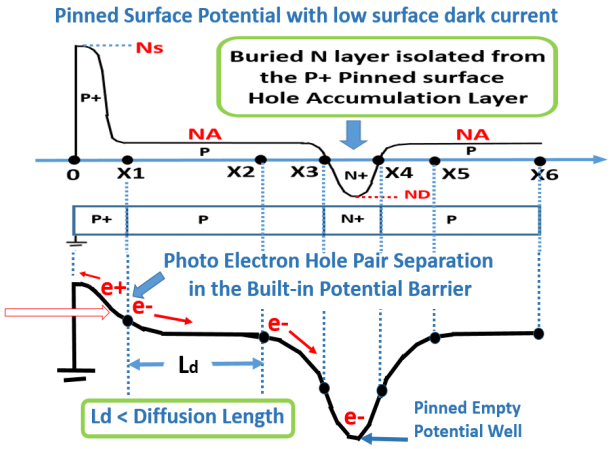

Fig. 5: P+PN+P junction type Buried Pinned Photodiode defined in Hagiwara Japanese 1975-127647 patent.

The excellent blue light sensitivity is achieved near the silicon surface depth of less than 0. 2 micro meter. The substrate doping level was Na = 5 x 10^{14} cm^{-3}. This idea of the unique P+NP junction type Pinned Photodiode was introduced for the first time in 1975 by Hagiwara in his three Japanese patents[3] in series, and Hagiwara reported in his 1978 paper[4] the 380H x 499V FT CCD image sensor using this P+NP junction (type C) Pinned Photodiode.

However, the actual formation of the doping profile of Pinned Photodiode is very likely to the type D because the normal ion implantation gives the Gaussian doping profile with smooth tailing slope, effectively resulting in the P+PN+P junction type D profile. See Fig. 4.

The heavily doped surface P+ hole accumulation layer and the relatively heavily doped N+ charge collecting region, connected in between by the lightly doped P region of Na = 5 x 10^{14} cm^{-3}.

Simulation and electric analysis of the P+PNP junction type D Pinned Photodiode was performed. See Fig. 3 which shows the P+P doping profile with the space charge polarization inducing the built-in barrier electric field enhancing the photo electron hole pair separation inside the built-in barrier potential of **kT ln(NS/NA) ~ 4 kT ev ~ 0.1 volt**.

Normally the photo electron and hole pair generation and separation is performed in the electric field inside the depletion region of the PN junction. But the photo electron and hole pair generation and separation of the P+PNP junction (type D) Pinned Photodiode is different and quite unique.

The surface P+P impurity doping slope induces the built-in barrier potential and the resulting built-in barrier electric field enhances the photo electron pair separation at the very near surface region of the silicon crystal to give the excellent blue light sensitivity. This photo electron hole separation mechanism is unique, quite different from the usual photo electron hole pair separation.

The reason why the P+PN+P junction type D Pinned Photodiode can have the excellent blue light sensitivity near the silicon surface depth of 0. 2 micro meter is now explained in details. Simulation and the electrostatic analysis is based on the fact that the maximum depth for the blue light penetration into the silicon crystal is 0. 2 micro meter which is very close to the surface.

The life time of the photo generated minority carrier can be measured using the photoconduction effect and the diffusion length Ld can be determined, which is needed for electrons to survive in the majority carrier hole-rich P substrate area. See Fig. 5. Photo electrons are expected to reach the buried N charge collecting region. The situation is similar to the minority carrier electrons injected from the emitter terminal into the majority carrier hole-rich base area of a NPN bipolar transistor. If the base region width is narrow, enough, one or two electrons may recombine with the holes in the base, but the most of the electrons can reach the collector terminal of the strongly reverse-biased depletion region. The N buried region of Pinned Photodiode acts as if the collector region of the NPN bipolar transistor does. This photo electron generation separation physical mechanism is unique and quite different from the ordinary electron hole pair separation in the PN junction depletion region.

II. No Image Lag Feature

Classical N+P junction type B photodiode shown in Fig. 2 is known to have the serious image lag problem. The charge transfer gate has a very large channel resistance and the residual signal charge cannot be transferred completely in the short clock reset time. The remaining small signal charge causes the serious image lag and the fast moving objects cannot be captured and the pictures are blurred. The first attempt was the thin-polysilicon electrode MOS Capacitor type E image sensor structure shown in Fig. 2. However the MOS capacitor type E sensor has inherently the strong surface electric field that induces the serious surface dark current which is caused by the oxide silicon surface positive fixed charge Qss and the electron trapping states Nss. The oxide silicon interface has the problem of the incomplete atomic crystal disorders inherently which cannot be avoided. Hagiwara proposed in 1975 to use the Schottky Barrier photo sensing type F structure for the interline transfer CCD imager. The idea was hinted by his Caltech undergraduate unpublished research work in 1971 of the Au/Ga_2O_3 Schottky Barrier junction experiment which was expected to have the very low reverse bias leakage current. Based on the conventional photo sensor structures type E and F, Hagiwara proposed in 1975 the P+NPNsub junction type photo sensor structure type C which is the P+NP junction type photodiode combined with the NPNsub junction type built-in overflow drain (VOD) structure. And in the SSDM1978 paper Hagiwara reported the 380H x488V FT CCD image sensor using the P+NPsub junction type Pinned Photodiode, with the excellent blue sensitivity, the low surface dark current and the low image lag features. See also Fig. 6 for comparison.

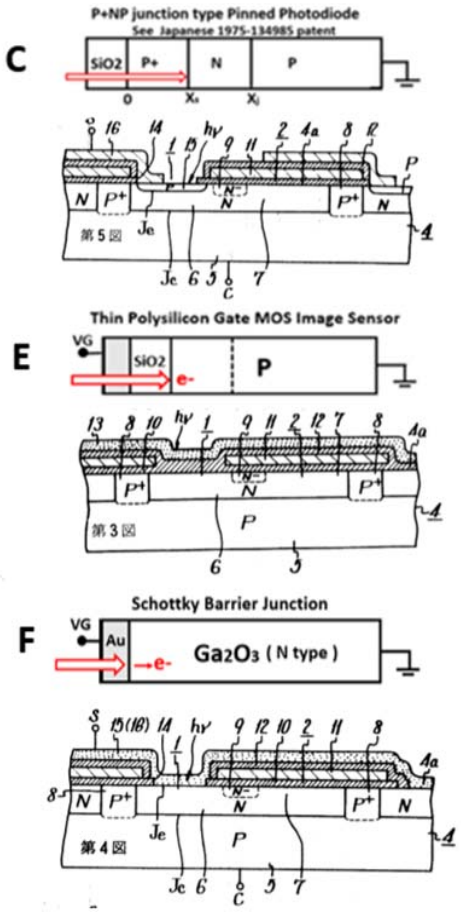

Fig. 6: Cross sectional views of Type C P+NP junction Pinned Photodiode sensor, Type E MOS capacitor photo sensor and Type F Schottky barrier photo sensor.

III. Schottky Barriers on Gallium Oxide

The surface barrier height of gold chemically prepared for the N type β-Ga_2O_3 semiconductor was investigated in details at room temperature by (1) photo response, (2)forward current versus voltage and (3) capacitance-voltage methods. Fig.7 showed the band diagram. The barrier energy was found to be 1.68 eV, with the excellent agreement, within kT of 0.026 eV, obtained by three methods. The diode non-ideality factor was found to be 1.14 ± 0.03 by current-voltage method.

This value is agreement with the value 1.08 ± 0.04 expected as a result of image force lowering using the free electron concentration 4.1 ± 0.09 x 10^7 cm^{-3} of the un-doped gallium oxide crystal determined by capacitance-voltage measurement. The effective mass m* of electrons was taken as 0.20 M and the relative permitivities of gallium oxide at the optical and low-frequencies were taken as 4 and 10.2 respectively.

The Barrier energies of gold on the chemically prepared β-Ga_2O_3 was obtained here following the same techniques developed by Neville and Mead[5] for the zinc oxide crystal.

Mead[6] established a semi-empirical approach for predicting the type of contact to be expected at an arbitrary metal-semiconductor interface. Fig. 5 shows the energy band diagram for "no bias" condition for the Au/Ga_2O_3 Barrier.

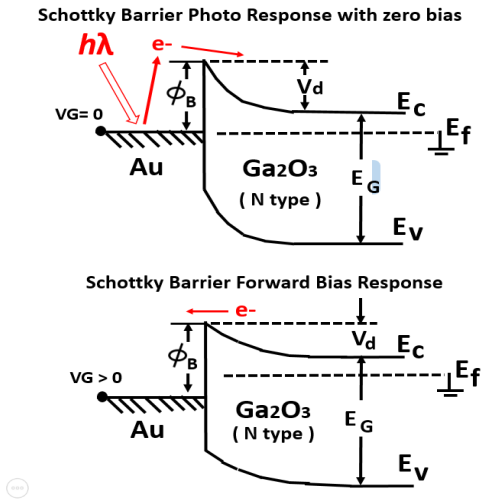

Fig. 7: Au/Ga_2O_3 Schottky Barrier Band Diagram

This approach is now applied for β-Ga_2O_3. Although five forms of Ga_2O_3 have been reported by 1971, only the monolithic form, having the same structure as θ alumina, is stable at room temperature.

The results of this analysis show that the barrier height ϕ_B is 1.68 eV and the effective carrier concentration of 4.1 ± 0.09 x 10^7 cm^{-3} gives the Fermi level below conduction band edge of 0.1 eV at room temperature. When monolithic light from a monochrometer impinges on the semiconductor surface, it induces a short circuit photocurrent in the metal-semiconductor junction.

The square root of the photocurrent normalized to the incident photon flux when plotted as a function of the photon energy results in a straight line for photon energies above (ϕ_B + 3 kT). The intercept for zero response of the extrapolated straight line yields a barrier height of 1.68 eV. Typical photo response data is presented in Fig. 8.

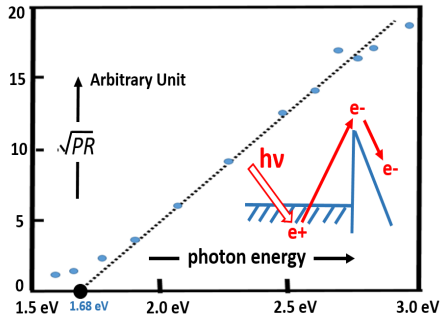

Fig. 8: Photo Response of Ga_2O_3-Au Schottky Barrier

A typical plot of $1/C^2$ as a function of the reverse voltage is shown in Fig. 8. The concentration was found to be 4.1 ± 0.09 x 10^7 cm^{-3} from the slope using the relation:

$$N_d = \left(-2/q\varepsilon_{dc}\varepsilon_o\right)\left(\frac{\delta V}{\delta\left(\frac{S}{C}\right)^2}\right) \qquad (1)$$

where **S** is the barrier area and ε_{dc} is the low frequency

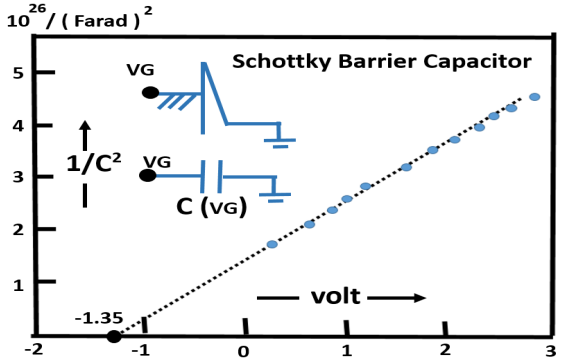

Fig. 9: CV measurement of Ga_2O_3-Au Schottky Barrier

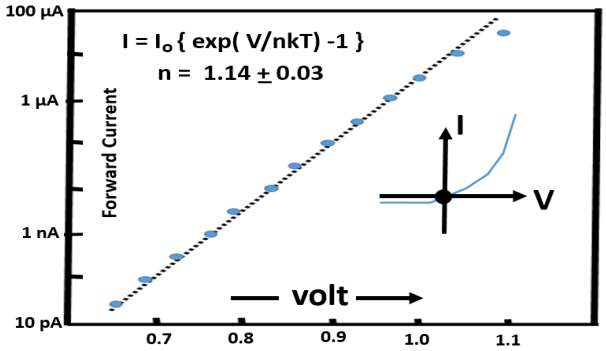

Fig. 10: IV measurement of Ga_2O_3-Au Schottky Barrier

permitivity taken as 10.2 after Neville[5]. See Fig. 9. The extrapolated intercept **Vo** is related to the surface barrier energy by the equation

$$V_o = \frac{\phi}{\eta} - \frac{kT}{q}\left(1 + \ln\left(\frac{N_C}{N_D}\right)\right) \qquad (2)$$

where Nc is the conduction band effective density of states. The intercept **Vo** was found to be 1.36 ± 0.09 eV which gives the barrier height: ϕ_B = 1.70 ± 0.15 eV. Hence, is taken 1.14 ± 0.03 from the forward voltage-current measurements which is in agreement with the value ϕ_B = 1.08 ± 0.04 expected for the forward voltages between 0.7 and 1.2 V from the relation

$$\eta = 1 + \frac{1}{4}\left(q^3 N_D / \varepsilon_o^3\, 8\pi^2 \varepsilon_{op}^2 \varepsilon_{DC}\right)^{1/4} \left[\phi - V - \frac{kT}{q}\left(1 + \ln\left(\frac{N_C}{N_D}\right)\right)\right]^{-3/4} \qquad (3)$$

as a result of image force lowering. In Fig. 10, forward current characteristics are displayed at room temperature. The slope gives **q/nkT,** where **n** is the diode non-ideality factor, seen to be 1.14 ± 0.03, which is consistent with 1.08 ± 0.04 obtained by the capacitance-voltage method. The extrapolated current density at zero applied bias voltage is given by

$$J_o = A^* T^2 \exp\left(-\frac{q V_d}{nkT}\right) \qquad (4)$$

where A * is the Richardson constant corresponding to the effective mass of the material taken as 0.2 $\mathbf{m_e}$. Using this equation the barrier height was found to be 1.69 ± 0.04 eV. The deviation of the characteristics from the exponential dependence on the applied voltage with the slope of **q/nkT** is due to the series resistance which is fairly independent of the current for the range considered[7].

IV. Conclusion

The photo electron hole separation mechanism of the P+PNP junction type Pinned Photodiode was explained, which is unique and quite different from the conventional photo electron hole pair separation performed by the electric field inside the PN junction depletion region. Related various historical photodiode structures are reviewed, including the 1971 work on the β - **Ga_2O_3** Schottky barrier photo sensor in search for the low leakage dark current device which led to the 1975 invention of the Pinned Photodiode with the surface P+ heavily doped hole accumulation (HAD) with the vertical overflow drain (VOD).

The barrier energy of gold on chemically prepared gallium oxide was shown to be 1.68 eV. The un-doped gallium oxide crystal at room temperature was found to contain 10^{17} free electron per cm^3. The three experimental techniques showed remarkable agreement forming a constant picture of the Ga_2O_3 – Au interface of the minimal atomic disorders, expecting the very low leakage dark current feature, which is desired for super light sensitive video camera applications at very low light level but with the excellent color reproduction. The N type Ga_2O_3-Au Schottky barrier rectifier was investigated. The very low reverse leakage current feature is a key parameter for the super light sensitive, the low surface dark current and the low image lag high performance image sensors with excellent color reproduction at very low light level.

Future AI traffic control system will need at least the high definition 8K image format of 7680H x 4320V, with 33 million pixels, to obtain the details of flash action images, with the in-pixel flash AD converters, and fast Cache SRAM chips in the 3D multichip CMOS image sensor with the more complex future digital circuit system implementations of the human friendly artificial intelligent partner system[8] (AIPS) to realize the smart AI image sensors for the smart AI robot vision system and home AI security and house cares..

Acknowledgment

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References

[1] Y. Hagiwara, " Multichip CMOS Image Sensor Structure for Flash Image Acquisition ", IEEE 3DIC2019 conference in Sendai, Japan

[2] S. M. Sze,"Physics of Semiconductor Devices", Fig. 5, p.750.

[3] Japanese 1975-127646, 1975-127647 and 134985 Patents

[4] Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488V CCD imager with narrow channel transfer gates, "Proc. of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese J. Appl. Phys., vol. 18, supplement 18–1, pp. 335–340.

[5] R.C. Neville and C.A. Mead, J. Appl. Phys. 41, 9 (1970).

[6] C.A. Mead, Solid Sate Electronics--Pergamon Press 1966, Vol.9, pp.1023-1033.

[7] D. Kahng, Solid Sate Electronics-Pergamon Press 1963, Vol. 6, pp.281-295.

[8] Yoshiaki Hagiwara, "The World of Digital Circuits for Artificial Intelligent Partner System (AIPS)", published by Seizansha.co.jp, in 2016, ISBN978-4-88359-339-2, 450 pages, Hard Cover.9000yen+tax.