Multichip CMOS Image Sensor Structure for Flash Image Acquisition

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Abstract— A new 3D Pinned Photodiode (HAD) CMOS image sensor structure applied in the 3-Dimensional multichip high speed digital flash image data acquisition system is explained and the important features are discussed.

Keywords— Cache SRAM, ADC, Pinned Photodiode, Depletion Photodiode, Buried Photodiode, Back Light Illumination, Global Shutter Buffer Memory, In-pixel Three Transistor Current Source Amplifier.

I. INTRODUCTION

Basically there are five types of photodiode. They are (1) Classic N+Psub junction with serious image lag problem (2) PNPsub junction Buried Photodiode (3) PN-Psub junction Depletion Photodiode with no image lag feature (4) P+N-P junction Pinned Photodiode with the heavily doped P+ surface hole accumulation with no surface dark current feature and (5) P+N-PNsub junction type hole accumulation diode (HAD) with the vertical overflow drain (VOD) function which is by necessity Buried, Depletion and Pinned Photodiode. Fig. 1 shows the 3D multichip CMOS image sensor structure with the 3D Pinned Photodiode (HAD) image sensors with the MOS capacitor Global Shutter Buffer Memory (GSBM) which was originally invented[1] in 1975.

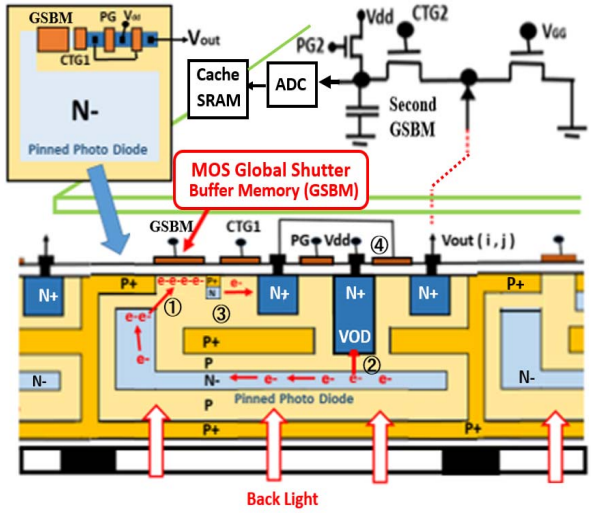

Fig.1: Cross Section of Buried Depletion Pinned Photodiode stacked with two Global Shutter Buffer Memory (GSBM) and CTG stages in two chip configuration for synchronizing data transfer to the receiving ADC and Cache SRAM chips.

II. HOLE ROLE IN PINNED PHOTODIODE

The importance of holes in the hole accumulation layer HAD structure of Pinned Photodiode was first reported in Hagiwara 1978 paper[2] , and then explained in details by Theuwissen[3] in relationship with IDEM1982[4] paper and IEDM1984[5] paper. Today's success of super light sensitive digital imaging is based on the SiO2 exposed pinned window invented by Hagiwara in 1975[1] with the surface P+ hole accumulation HAD layer. Pinned Photodiode was originally invented[1] in the form of the back illumination scheme as illustrated in Fig. 2.

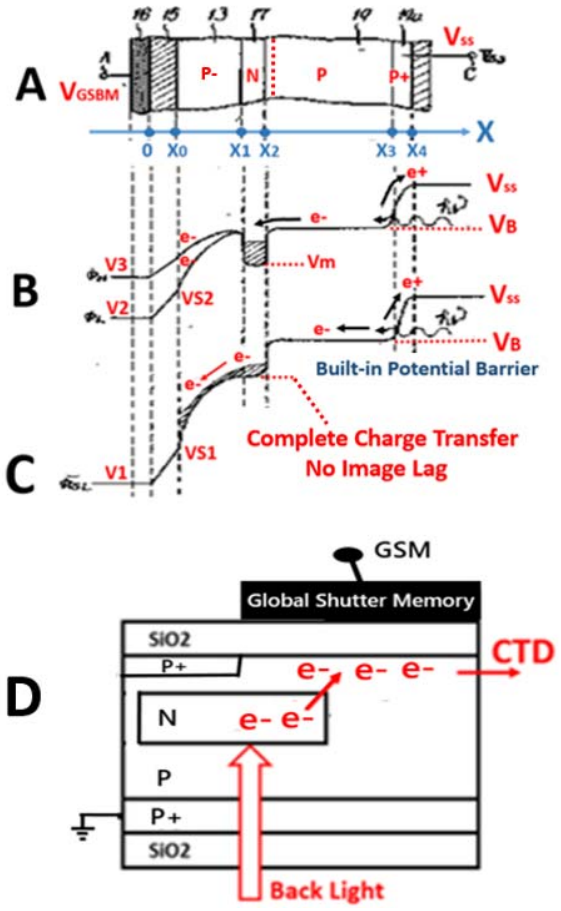

Fig. 2: The P+PNP junction type Buried Depletion Pinned Photodiode with no image lag feature with MOS Capacitor type Global Shutter Buffer Memory (GSBM) invented and defined in Japanese 1975 patent[1] by Hagiwara.

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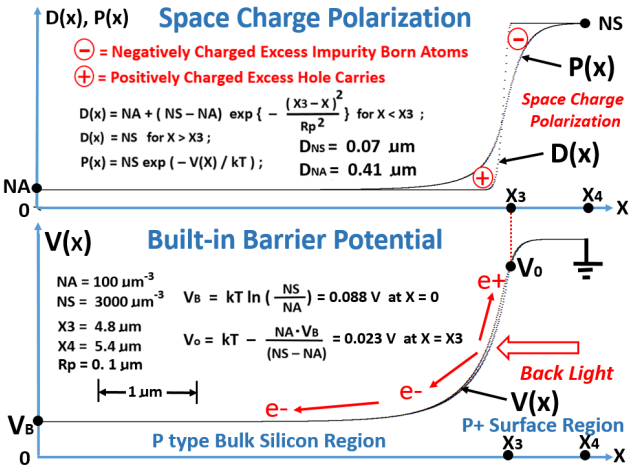

Fig. 3: Exact numerical calculations of Gaussian P+P doping profile D(x), the hole carrier density P(x) and the built-in barrier potential V(x).

III. Role of Built-in Potentail Barrier in HAD

Exact numerical calculation of the built-in potential barrier is shown in Fig.3, explaining the hole electron generation and separation in the built-in electric field created by the heavily doped P+ surface hole accumulation HAD.

Note that the local unbalance of the hole concentration P(x) and the impurity boron atom density D(x) gives the local space charge polarization, resulting the built-in potential V_m. The built-in electric field separates photo electron hole pairs, and resulting in the excellent quantum efficiency of the short wave blue light sensitivity.

Although CCD was just a charge transfer device (CTD), later taken over by CMOS type CTD, both CCD and CMOS image sensors have the super sensitive light detecting feature with very good color reproduction at low light level because of the Pinned Photodiode which was invented and described in Japanese 1975 patent[6] by Hagiwara.

In solar cells and image sensors, the photo electron and hole pair generation is considered to occur normally in the PN junction depletion region. However, the photo electron and hole pair generation in Pinned Photodiode is performed by an entire different physical principle. In 1975, Hagiwara proposed[1] that the photo electron and hole pair separation can also be achieved in the strong electric field created by the built-in barrier potential as shown in Fig. 2 that was the result of space charge polarization effect explained in Fig. 3.

Photo electrons are separated from holes in the presence of the surface built-in potential barrier near the border of the surface P+ hole accumulation HAD layer. And then, photo generated electrons can drift towards Buried Photodiode, which is the charge collecting storage, by using the holes, that is, positively charged Si ion atoms, as stepping stones, from one Si atom to another, like an energetic space rocket until it loses energy. If the photo electron, generated at the surface built-in potential barrier electric field, is recombined with a hole drifting deep in the bulk silicon, the hole becomes a neutral silicon atom that cannot move. Then, by the silicon bulk thermal neutrality condition, the excess negative space charge is present in the form of the trapped electron by the negatively charged boron or in the external orbit electron in the neutral Silicon atom at high energy state.

The electron has high energy state and can jump out into the free space. In this way, the excess negative charged electron cannot stay in the neutral silicon atom permanently and can be transferred to the positively charged silicon atom (hole) nearby, acting as stepping stones for the excess electron charge, eventually to drift towards the receiving Buried N type charge collecting region. Eventually the excess electron negative charge is collected in the buried N type diffusion storage region. If the electric field of the PN junction depletion region edge of the buried photodiode is near the surface P+ hole accumulation edge, the drifting photo electrons can be quickly and instantly collected in the buried N type charge collecting storage area.

IV. Vertical Overflow Drain (VOD) Function

Fig. 4 shows Pinned Photodiode with the vertical overflow drain (VOD), which is also Depletion Photodiode with no image lag feature. The following is the direct English translation of the Patent Claim of the Japanese 1975 patent[6] on Pinned Photodiode (HAD) invented by Hagiwara.

1. In the substrate, the first region P1 of the first impurity type is formed, on which, the second region N2 of the second impurity type is formed.
2. The charge e- from the light collecting part is transferred to the adjacent charge transfer device (CTD). Both are placed along the main surface of the semiconductor substrate.
3. In the solid stare image sensor so defined, a rectifying junction Je is formed on the second light collecting region N2 forming the P3 and N2 junction as the emitter junction Je .
4. The result is a photo transistor P3N2P1structure on the substrate with the N2 and P1 junction as the collector junction Jc . The charge, stored in the base N2 region according to the illuminated light intensity, is transferred to the adjacent charge transfer device.

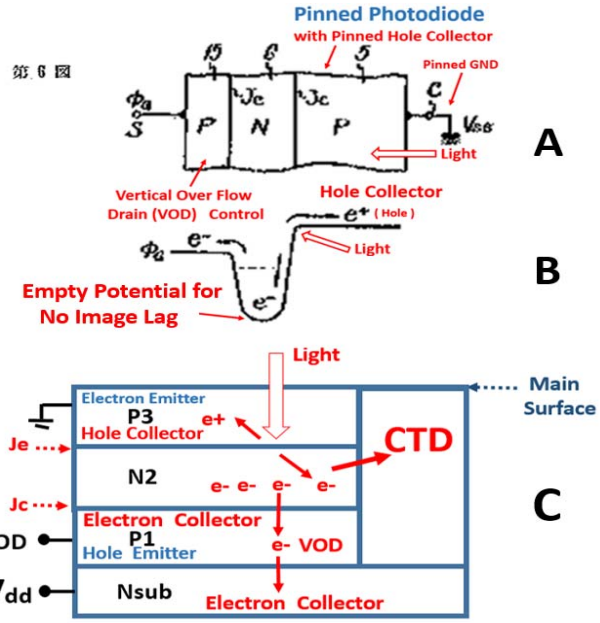

Fig. 4: The P+NPNsub junction type Hole Accumulation Diode (HAD)[6] invented by Hagiwara in 1975.

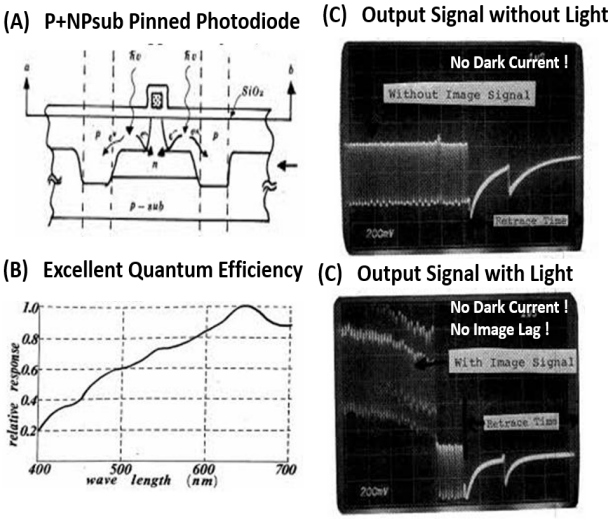

Fig. 5: Reproduction of figures reported in Hagiwara 1978 paper[2], (A) P+NPsub junction type Pinned Photodiode structure, (B) the Excellent Blue Light Sensitivity (C) no dark current feature and (D) no image lag feature.

It is now well understood that the blue light of short wave length is needed for the satisfactory color reproduction of high image quality. However, the blue light cannot penetrate more than 0.3 micro meter in depth thru the silicon crystal[7]. The built-in surface potential barrier, created by the surface abrupt doping level difference, can in return create the strong electric field at the vicinity of the electron hole pair generation at the silicon surface of 0.3 micro meter in depth, which can effectively separate photo electron and hole pairs, resulting in the excellent quantum efficiency for the blue light needed for the satisfactory color reproduction.

P+NP junction type Pinned Photodiode(A) has the following three very important features, (B) Excellent short wave blue light quantum efficiency, which is the most important feature of Hagiwara 1975 patent[6], (C) no surface dark current problem and (D) no image lag problem, with also the feature of no surface interface trap (Nss) noise (E). But nothing is new about the feature (D) and (E) since CCD had these two features already by 1975.

In 1966, the in-pixel active source follower amplifier circuit for MOS image sensors was invented by Perter Noble. See Fig. 6.

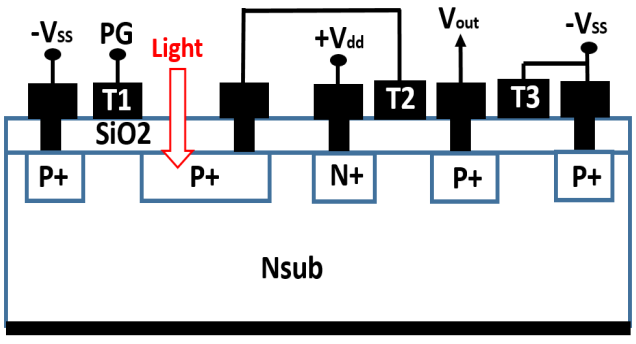

Fig. 6: In-pixel amplifier circuit by Peter Noble, 1966

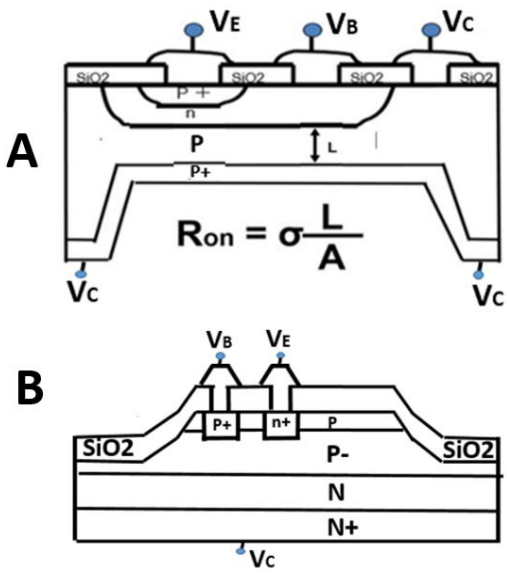

Fig. 7: Bipolar Transistor Process invented and developed by Yoshiyuki Kawana (A) and Toshio Kato (B) in 1950s.

But MOS scaling technology was not so advanced and the CCD type charge transfer device (CTD)[8] was preferred simply because MOS transistors were too large. However, CCD imager process shown in Fig. 4 was not as simple as MOS process for digital circuits. Complex bipolar transistor process experience was required. See Fig. 7. But now, owing to the advancement of CMOS process scaling, the active circuit of Fig. 6 became the most important element needed to build the modern CMOS image sensors[9].

V. NPN Junction Charge Transfer Gating (CTG)

Fig. 8 is a reproduction of the picture drawn in the 1975 patent[10] by Hagiwara. This charge transfer action is very similar to the well-known punch thru operation mode of the PNPN junction thyristor. Note that this is very similar to the P+NPN$_{sub}$ junction type Pinned Photodiode shown in Fig. 4. Both are the same PNPN junction type Pinned Photodiode.

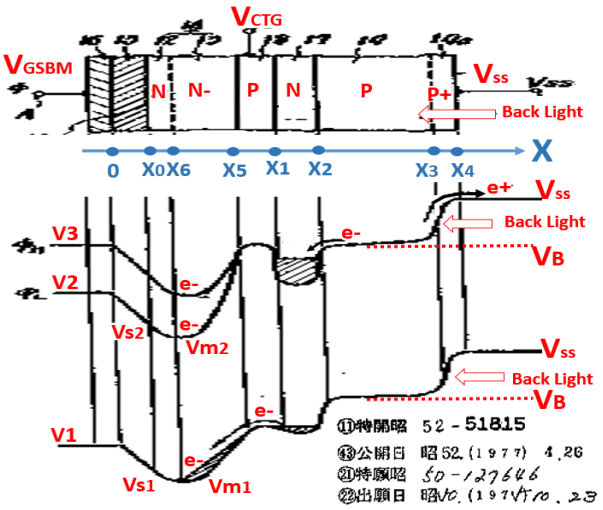

Fig. 8: The P+PNPN junction type Pinned Photodiode[10] with Global Shutter MOS Buffer Memory (GSBM) and the NPN junction type vertical charge transfer gating (CTG).

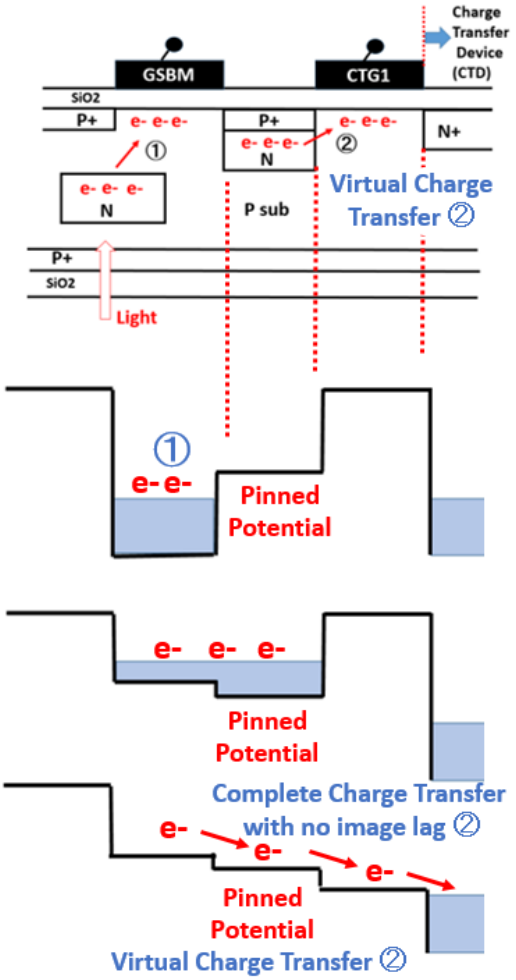

Fig.9: The important concept of Virtual Phase Charge Transfer of the Pinned Photodiode with the complete charge transfer operation mode for no image lag feature, described and invented by Hagiwara 1975 patents[1, 6, 10, 11].

VI. Pinned Surface Virtual Charge Transfer

The charge transfer operation with the pinned surface potential for the virtual gating concept is very similar to the CCD charge transfer operation. Fig. 9 shows the virtual charge transfer concept explained by Hagiwara[1,6,11] in 1975. Henecek[12] invented an additional potential barrier stage to achieve the directionality of the virtual phase signal charge transfer operation, which was hinted by Hagiwara 1975 invention[6] and the virtual phase charge transfer operation of the image lag free Pinned Photodiode [1] as shown in Fig. 1.

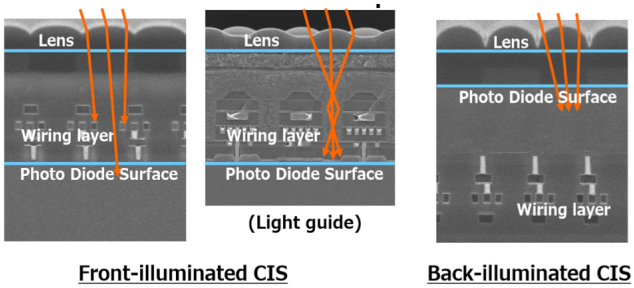

Fig. 10: Cross sectional photos of CMOS image sensors

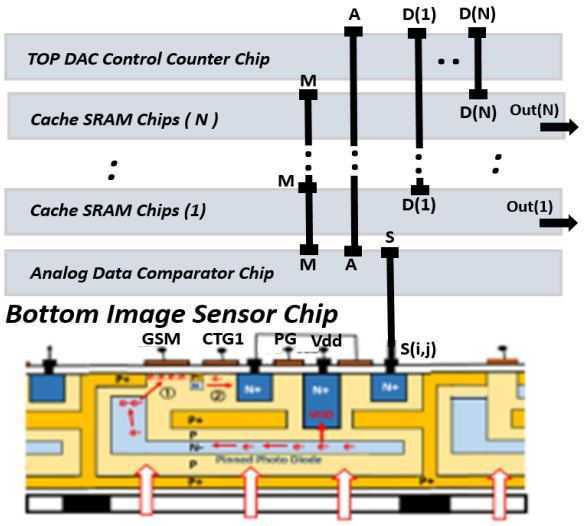

Fig. 11 : Metal Cu pillar signal pass wires thru multichip for the future 3D multichip flash image acquisition system.

VII. 3D Multichip Image Sensor System

Cross sectional photos of back light illuminated CMOS image sensors are shown in Fig. 10 while Fig. 11 shows the 3D multichip CMOS image sensor system. If time sharing scheme is used, we only need one data comparator circuit. However, for fast ADC operations, we must have the in-pixel data comparator circuits that have to be squeezed in each pixel element area. The comparator circuit is a conventional one that can also be used for a simple IR sensor detector as shown in Fig. 12.

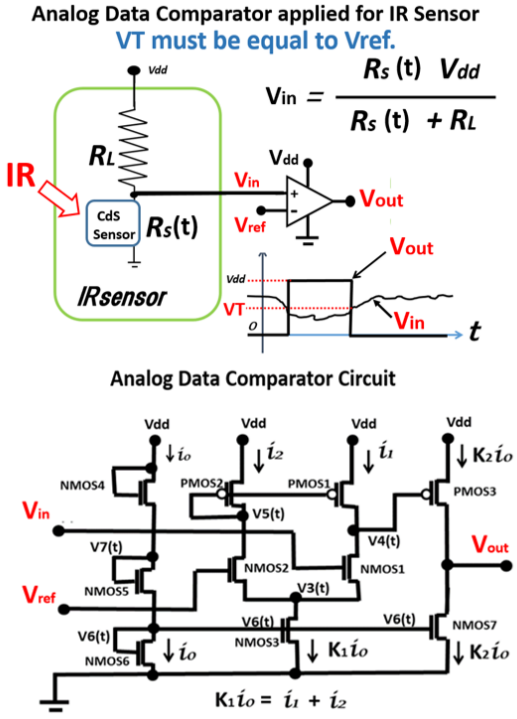

Fig. 12: Conventional Analog Data Comparator Circuit

VIII. Circuit Simulation of Analog Data Compator

Fig.13 summarized the circuit simulation of the analog data comparator for the various reference voltage Vref values which correspond to the voltage A in Fig. 11. The input voltage Vin which corresponds to the output signal S in Fig.11 is scanned to obtain the value of the threshold voltage VT, which corresponds to the match signal M in Fig.11. With this match signal M, the cache SRAM latches the values of the control counter data D(1) to D(N) in each SRAM level chip. This simulation analysis shows the good circuit performance for the input reference voltage Vref at least in the range of 0 V to 1.5 V.

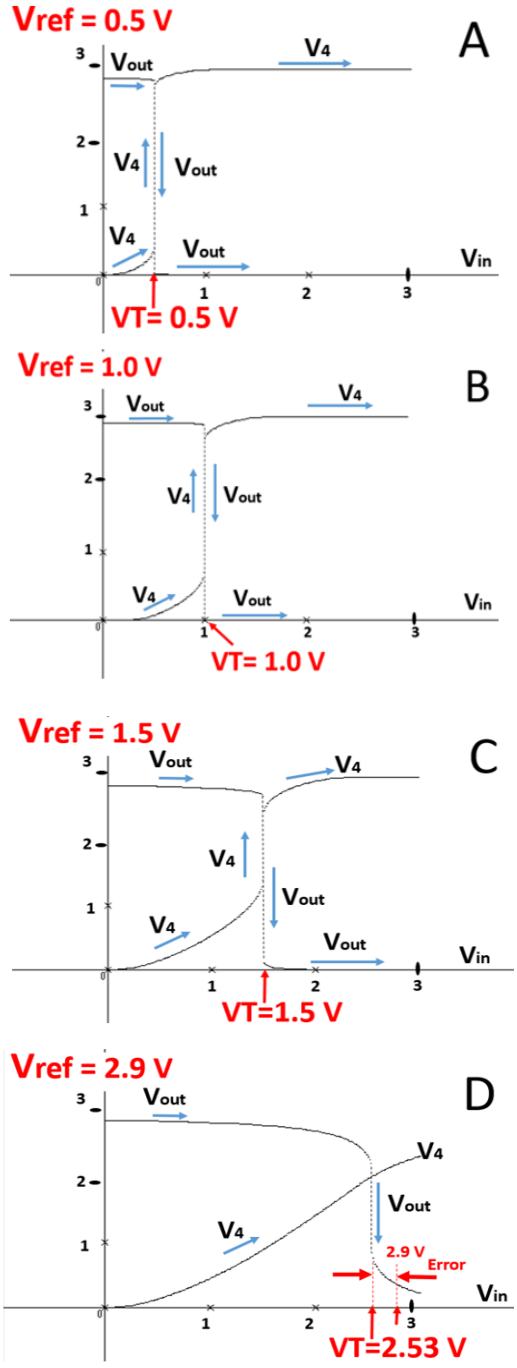

Fig.13: the circuit simulation results of the analog data comparator for the various reference voltage Vref values

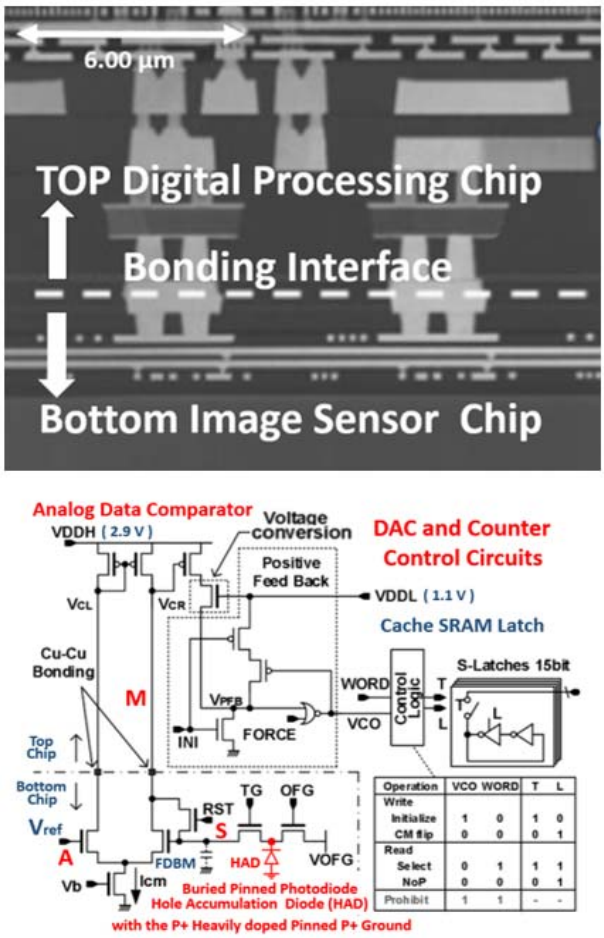

Fig. 14: Cross Sectional View of two chip stacked back-illuminated CMOS Image Sensor[14] with the in-pixel analog comparator control circuits to generate the match signal M from the reference voltage A and the image sensor signal S.

IX. All Solid State Digital Camera

The 25 nanosecond access time fast Cache 4 Mega Bit SRAM[13] was first developed in 1989, with the dynamic bit line load circuits invented by Miyaji, and was used as the very fast Digital Buffer Memory for the early all solid state digital CCD camera to correct and enhance the picture quality such as Jitter correction, color reproduction, pattern correction and image recognition processing system units for industrial and professional applications of high definition television broadcasting level.

Fig. 14 shows the cross sectional view of two chip stacked back-illuminated CMOS image sensor[14-16] with the in-pixel analog comparator control circuits to generate the match signal M from the reference voltage A and the image sensor signal S, as originally illustrated in Fig. 11 for the future multichip system.

Photo electron and hole generation and separation at the surface electric field is performed at the back side silicon surface of the P+ heavily doped pinned hole accumulation (HAD) layer acting as the Pinned Hole Collector Grounded Terminal. Salient physical parameters are defined in Fig. 15 . The all solid state CMOS image sensor technology is now being extended to the 3D multichip flash image acquisition system illustrated in Fig. 1 and Fig. 11.

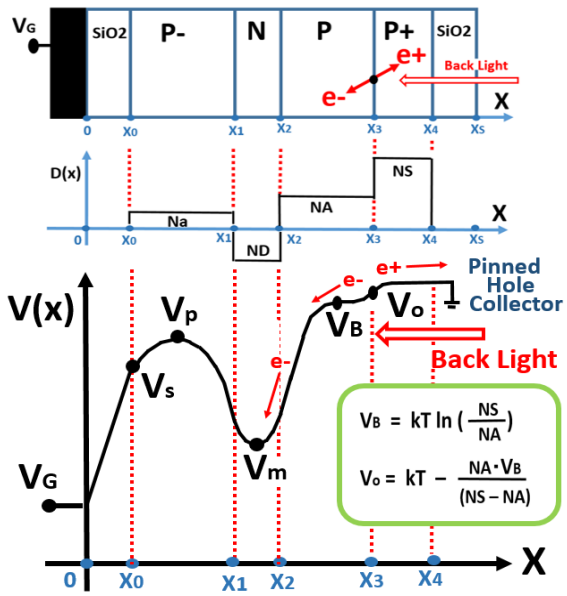

Fig. 15: Electrostatic Analysis of the surface Built-in Barrier Potential V_B and V_o by Depletion Approximation.

X. CONCLUSION

Hole Accumulation Diode[6] (HAD), with the P+ heavily doped surface hole accumulation layer, invented in 1975, is very important, because first of all it has the excellent short wave length blue light sensitivity feature producing the high picture quality of color reproduction in low level light illumination, which is realized by the photo electron and hole pair generation and separation in the built-in potential barrier[1] and the electric field at the surface heavily doped P+ hole accumulation HAD. No dark current is the second important feature. And no image lag is the third one since CCD was known to have the no image lag feature already. But CCD itself does NOT have the excellent blue light sensitivity and does NOT have the low dark current feature which the Pinned Photodiode[1,2,6,10] invented by Hagiwara has.

HAD is defined as the PNPN junction Photodiode with the VOD function. HAD is also by necessity the P+N-P junction Pinned Photodiode with no dark current feature. HAD is also by necessity the PN-P junction Depletion Photodiode defined as Buried Photodiode with no image lag feature. When Hagiwara invented HAD[1,2,6,10] in 1975, Hagiwara also invented (1) Pinned Photodiode[6], (2) Depletion Photodiode[1], (3) Buried Photodiode[10], (4) the in-pixel vertical overflow drain[6] (VOD) function and (5) the in-pixel Global Shutter function[1, 10]. The surface pinned potential[1, 6, 10] also serves as the hole collector terminal separating the holes from photo electrons which drift more than the distance estimated by Debye length until being collected into the Buried[10], Depletion[1] and Pinned[6] Photodiode (HAD), with the back light illumination scheme[1] which is the most important feature needed to build the super sensitive 3D CMOS image sensor with the high blue-light quantum efficiency and the excellent color reproduction at low light level for fast action pictures with no image lag.

Future AI traffic control system will need at least the high definition 8K image format of 7680H x 4320V, with 33 million pixels, to obtain the details of flash action images, with the in-pixel flash AD converters, and fast Cache SRAM chips in the 3D multichip CMOS image sensor with the more complex future digital circuit system implementations of the human friendly artificial intelligent partner system[17] (AIPS) to realize the smart AI image sensors for the smart AI robot vision system and home AI security and house cares..

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