

Pinned Photo Diode (PPD) and Hole Accumulation Diode (HAD)

PPD and HAD Story (2)

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Yoshiaki Hagiwara was invited in the following four international conferences because of his contributions to the image sensor community and related digital system LSI chip design works. See the four invited talks related to the Pinned Photo Diode which is also called as SONY original Hole Accumulation Diode (HAD) image sensor.

(1) International Conference CCD79 in Edinburgh, Scotland UK

See http://www.aiplab.com/0-CCD79_1979Hagiwara.pdf

(2) International Conference ESSCIRC2001 in Vilach, Austria.

See <http://www.aiplab.com/ESSCIRC2001.pdf>

(3) International Conference ESSCIRC2008 in Edinburgh, Scotland UK

See <http://www.aiplab.com/0-ESSCIRC2008Hagiwara.pdf>

(4) International Conference ISSCC2013 in San Francisco, California USA

See <http://www.aiplab.com/ISSCC2013PanelTalk.pdf>

(5) Pinned Photo Diode and SONY HAD are the same thing. Both were invented by Hagiwara at Sony in 1975 in the Japanese Patents (1975-127646, 1975-127647, 1975-134985).

See http://www.aiplab.com/Pinned_Photo_Diode_1975_invented_by_Hagiwara.pdf

(6) Hagiwara as a PhD student at CalTech designed a Fast 128 bit digital data stream parallel comparator chip, which was fabricated at Intel with the Intel 1101 PMOS process technology.

See http://www.aiplab.com/128_bit_Comparator.pdf

(7) Hagiwara designed a Fast 25 nanosecond access time 4 M bit Cache SRAM chip for digital camera applications. Intel used the SONY SRAM chips in the Intel boards. Sony enjoyed SRAM business while many companies in Japan were focusing on the 4 M bit DRAM chip business.

See http://www.aiplab.com/SONY_4MSRAM_1989.pdf

ヨーロッパ国際半導体電子電気集積回路総会での招待講演

@ESSCIRC2001 Villach, Austria, September 26, 2001

***Micro-Electronics
for Home Entertainment***

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Microelectronics for Home Entertainment

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Abstract

A brief historical overview of a first home entertainment consumer electronic gadget, called a portable transistor radio is given, and then some introductory comments on the basic semiconductor device concepts are explained. They are strongly related to the microelectronics of the present home entertainment LSI chips with regard to the product specifications and performance aspects of the home entertainment LSI chip sets, such as for digital cameras, home robotics and games.

1. Introduction

The history of home entertainment consumer electronics begins in May 7, 1946, with the founding of Tokyo Tsushin Kogyo (Tokyo Telecommunication Engineering) by Masaru Ibuka (36) and Akio Morita (25). Had these two bright young men not met and combined their considerable resolve and talents, the home electronics business would not have accelerated so much as we see it today, and our semiconductor business efforts would have been aimed only for military purpose for a while.

In the Founding Prospectus, Ibuka eloquently stated his dreams for the company. Morita, together with the company's first directors headed by Kazuo Iwama, led employees to realize these goals. Throughout their work, the young force was inspired by the free and dynamic atmosphere of the "ideal" factory they were striving to create. From the onset, Ibuka, Morita and Iwama endeavoured to develop unique and exciting products that fulfil their customers' dream.

Iwama was 35 when he visited Western Electric to study transistors in January 1954. Iwama was the first engineer in Japan who understood the concept of "electron fog" in the bipolar transistor device physics.

He worked as the leader of the bipolar transistor development project to realize the epoch-making portable bipolar transistor radio TR-55 introduced to the home entertainment electronics market in August 1955.

Seven years had passed since the invention of the bipolar transistor in Bell Lab in Dec 1947. I was only seven years old and had completely no idea about how a transistor works at that time.

I was a junior undergraduate at CalTech in Pasadena, California in 1969 when I learned how the bipolar transistor and MOS FET work with the classical textbook by Grove. My class instructor was Prof. James McCaldin who was known as the co-inventor of basic planar passivation technology in modern MOS transistor fabrications.

In the summer 1971, I visited Sony Atsugi plant right after I received BS from CalTech and worked as a reliability engineer in Bipolar IC production line for Sony's Trinitron colour TV sets.

In the fall 1971, I returned to CalTech to pursue further my graduate work and learned how to design MOS LSIs from Prof. Carver Mead. My PhD thesis was about the buried channel CCD imagers which can be applied to low light intensity solid state imagers. Prof. T.C. McGill was my PhD thesis advisor.

After defending my PhD, in February 1975, I joined Sony at the Central Research Center in Yokohama, Japan, and engaged with further research on high performance CCD imagers project headed by Iwama who was the pioneer engineer in the early bipolar technology development effort in Sony.

My first patent filed in Sony in Nov 1975 was about a simple pnp-sub structure used as the light sensing device for imagers. The sensor structure is now called the HAD sensor in Sony's current video cameras and digital still cameras.

Sony put most of its engineering sources in CCD imagers and its camera system in 1970s. We engineers had to design signal processing and camera control chips by ourselves. Those experience were useful to apply for other MOS LSI design applications which made possible the current home entertainment LSI chip sets such as digital cameras, home robots, and games.

In this paper, some basic semiconductor device concepts are first reviewed briefly. They are about the concept of "electron fog", the bipolar and MOSFET device model, the buried channel CCD imager structure and the pnp-sub structure which is used as the light sensing device, which is now universally adopted in most of high performance solid state imagers. Then, some general discussions on the product specifications and performance aspects of the home entertainment consumer LSI chip sets, such as for digital cameras, home robotics and games are presented in details

2. Basic Semiconductor Device Concepts

In this section some introductory comments on the basic semiconductor device concepts are explained. They are strongly related to the microelectronics of the present home entertainment LSI chips.

2.1 Concept of Electron Fog

Fig.1 shows the electron fog in metal and semiconductor. Electrons in metal are depicted in this picture as the moisture above the water surface in the container while the electrons in the semiconductor are depicted as the moisture on the top of a floating box in water. If the box is heavy, the water surface is very close to the top of the box and there are a lot of moistures.

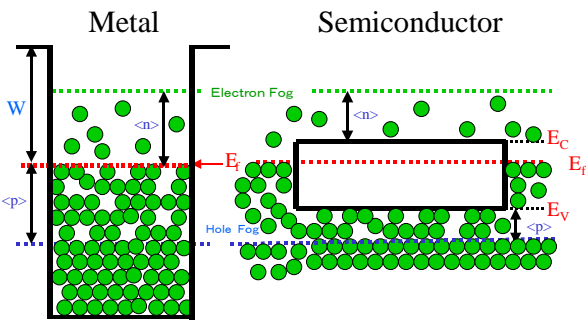


Fig 1 Electron Fog Model in Metal and Semiconductor

This corresponds to the n-type semiconductor band diagram. If the box is relatively light, only a small bottom portion of the box is emerged into the water and the top of the box can be quite dry and there will a lot of bubbles (holes) under the bottom of the box. This corresponds to the p-type semiconductor.

Applying these n-type and p-type semiconductor box models, a diode behaviour model can be constructed and the diode rectifying characteristics can be explained.

2.2. Bipolar Transistor Device Model

Fig.2 shows energetic boys (electron fog in the emitter region) trying to climb a hill (base region) to catch the girls on the hill (hole fog which is the majority carriers in the base region). Some of the boys can luckily catch girls on the hill, recombine, become happy and disappear as light or heat energy. But the hill width is very short and most of the boys will not have enough time to catch girls and fall down the cliff (the base-collector depletion region). The poor boys are now collected in the deep down the cliff in the collector region.

In the time interval Δt , there are $I_E \Delta t$ boys jumping to the hill to catch girls on the hill. Some boys are luckily enough to catch girls on the hill. The number of girls caught by the energetic boys in Δt is $I_B \Delta t$, which is

proportional to the number of the average boys on the hill Q_n . The girls are supplied as the base current I_B . Other salient physical parameters normally used in the bipolar transistor device modelling are also given in the figure.

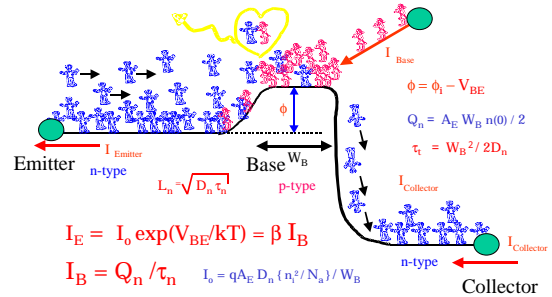


Fig. 2 Bipolar Transistor Action

2.3 MOS FET Model

Fig.3 shows a MOS FET structure. If you see how the electron fog moves from the left source n+ region to the right n+ region through the Si-SiO₂ surface under the MOS gate, you can see that it is also considered as an electron transportation along an npn structure. In this case however the potential in the p-region is controlled by the gate voltage isolated by the thin oxide.

The figure shows the electron fog moving from the source to the region under gate at the onset of strong inversion at the Si-SiO₂ surface. At this point the electron fog density at the channel is equal to the density of the majority "hole fog" in the p-type Si substrate, and the gate voltage at this point is defined to be the threshold voltage V_{th} of the MOS FET.

$$V_{th}(V_{BB}, V_S) = V_{FB} + \left\{ B + V_S - V_{BB} \right\} + \gamma \sqrt{\left\{ B + V_S - V_{BB} \right\}}$$

$$V_{FB} = V_{BB} - (kT/q) \ln(N_C N_A / n_i^2) - \left\{ \chi_{si} - \phi_m \right\} q / q_{ox} / C_{ox}$$

$$K = q \epsilon_{si} N_A / C_{ox}^2 \quad \gamma = \sqrt{2k} \quad B = 2 (kT/q) \ln(N_A / n_i)$$

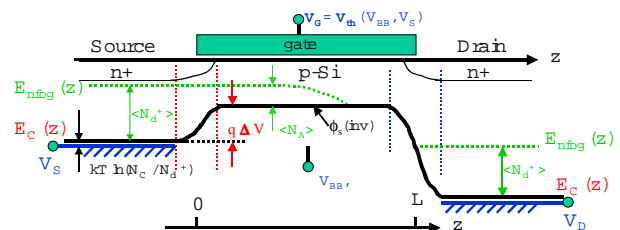


Fig. 3 MOS FET @ Onset $V_G = V_{th}$

Fig.4 shows water flowing from the right source region to the left drain region through the water gate. The depth of the channel V_{ch} is given as $(V_g - V_{th})$ where V_g is the applied gate voltage which induces the channel depth $V_{ch} = (V_g - V_{th})$. The amount of the water flow I is proportional to the mobility μ , the water amount Q

under the gate and the electric field E . That is, we can write $I = \mu Q E$ in this rough approximations..

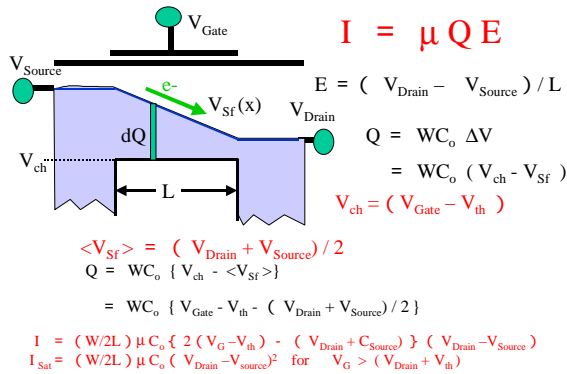


Fig. 4 MOS FET I-V Characteristics

In the first approximation, we take $E = (V_d - V_s)/L$ where V_d , V_s and L are the drain voltage, the source voltage and the gate channel length. The total charge can be approximated as $Q = W C_o \Delta V$ where W and C_o are the channel width and the oxide capacitance of the actual corresponding MOS FET transistor. Now ΔV corresponds to the voltage difference between the average water surface $(V_d + V_s)/2$ and the channel potential $V_{ch} = (V_g - V_{th})$.

That is, we have $\Delta V = \{ (V_d + V_s)/2 - V_{ch} \}$. Hence now since we have $Q = W C_o \Delta V$, the equivalent amount Q of the water (or charge) under the gate is given as $Q = W C_o \{ (V_d + V_s)/2 - V_{ch} \}$ where we have $V_{ch} = (V_g - V_{th})$, $E = (V_d - V_s)/L$.

Now if we put these relationships into the original equation $I = \mu Q E$, we get, without going through the calculations normally done in the classical gradual channel approximation, the finally the classical MOS I-V equation:

$$I = (W/2L) \mu C_o \{ V_d + V_s - 2V_{ch} \} (V_d - V_s)$$

$$= (W/2L) \mu C_o \{ V_d + V_s - 2(V_g - V_{th}) \} (V_d - V_s)$$

2.4 Buied Channel CCD Structure

Fig.5 shows the physical structure and the potential profile of a buried channel CCD. The signal charge is the electron fog in the lightly doped n-region at the surface. As you can see, these signal charges are isolated from the direct contact to the Si-SiO₂ interface and do not suffer the charge trapping. This structure gives a good CCD charge transfer efficiency of more than 99.9999 % along the buried channel CCD shift register along the direction of in&out of this paper. At very high light, excess charge can be drained into the substrate by lowering the well voltage V_{well} or making the substrate voltage very deep and inducing the punch through mode in the n-p-n(sub) structure.

High density and high performance solid state imagers became available applying this structure as the scanning

system. The surface n-layer is completely depleted when there is no signal charge. It is dynamically operated .

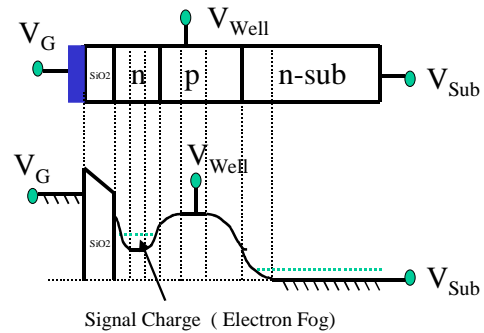


Fig. 5 Buried Channel CCD Structure

It is considered as one extended application of dynamic MOS device operations. The most well-know dynamic operation of a MOS device application is the DRAM data storage operation.

2.5. HAD sensor, a pnp-sub structure

The floating diode structure for image sensing unit was well known in early 1970s. I simply proposed to use a pnp-sub structure instead for the imaging element. Fig.6 shows the proposed structure.

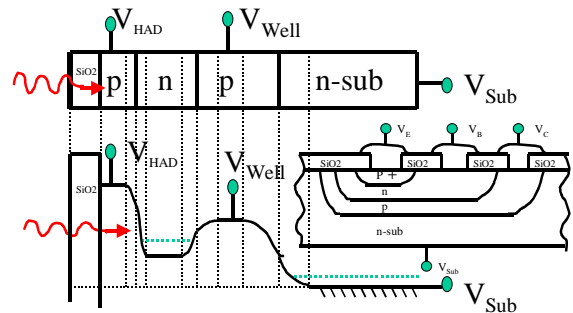


Fig. 6 a typical PNP Bip Tr Structure in early 1970s and a proposed application as an Image Sensing Element in 1975

It is a simple pnp bipolar transistor structure itself with a very lightly doped base region, operated in the strong cut-off mode with the base majority charge completely depleted.

It is the first practical application of the bipolar transistor in dynamic operation mode, which turned out to be the best structure and way to convert photons to electrons for imaging including the current MOS imagers applications. The sensor structure is now called the HAD sensor in Sony's current video cameras and digital still cameras.

3 LSI Chips for Home Entertainments

3.1 Digital Still Camera.

The picture in the Fig. 7 shows a 2/3 inch 190K pixel IT CCD Imager, ICX016/XC-37 which I designed when I was still a young CCD design engineer in early 1981. This model became the model of the world first consumer CCD video camera for mass production in 1983.

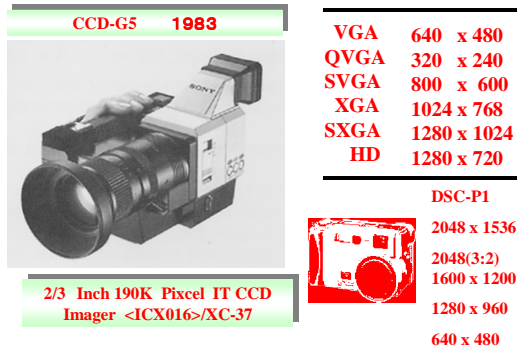


Fig. 7 The World First Consumer CCD Video Camera for Mass Production 1983

We are now striving to become “Imaging Device NO.1 !” There are many applications of CCD and LCD as seen in Fig. 8.



Fig. 8 Applications of CCD&LCD

3.2 AIBO, a home entertainment robot

Now, I will go through first the most popular product, the entertainment robot AIBO shown in Fig.9. When you buy a brand new AIBO. It is like a baby which does not have any knowledge. It has a certain intelligent level which is pre-programmed. You can play with the AIBO and gradually your AIBO will recognize your gestures and voices. AIBO will remember the wonderful time you spent together with it. Actually the experience and knowledge AIBO accumulates during these memorable

moments are stored in a chewing gum size NVRAM called a memory stick shown in Fig.9.

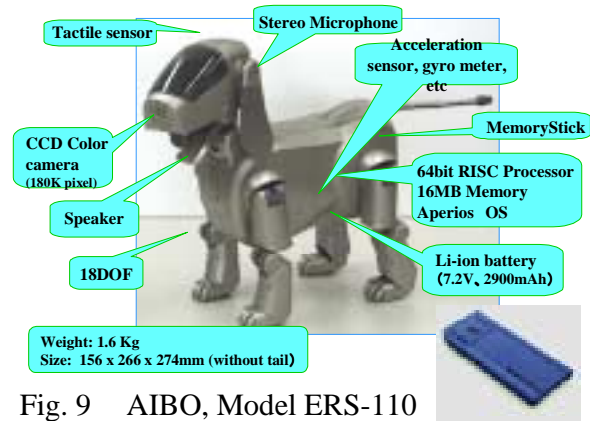


Fig. 9 AIBO, Model ERS-110

This memory stick can be also used in other products such as PCs, Digital Audios, and DSCs. Unfortunately it is not used in PS and PS2 for generation compatibility for now. But in one form or another we definitely need NVRAMs in PS,DSC,Digital Audio,PC and the future home entertainment robots.

The 21st century will become an era of autonomous robots which are partners of human beings. Autonomous robot will help and support people in the future. AIBO is designed to be the first product model of Robot Entertainment Systems. The main application of this robot is a pet-style robot, which must be in lifelike appearances. Although AIBO is not a nursing robot, the development of AIBO is the first step of the era of autonomous robots in the 21st century.

I will go through here some works done in Digital Creation Laboratory in our company. Most of the works were actually done by the pioneering engineers, Mr.Fujita,Mr.Kageyama, Mr.Kitano and Mr.Sabe.

The epoch making debut of AIBO, model ERS-110 in 1999, had the following features.

First of all it has a CCD color camera with 180K pixels. Of course it does not have a mechanical shutter. It does not have any eye-lid ! It has an audio sensor called microphones, a pair of them for stereo audio pick-up. It also has an acceleration sensor,

Gyro meter and also a tactile sensor. So if you pat it on the head gently, it will show some happy gesture. If you strike it on the head, it will interpret it as your sermon. The moving joints had 18 degrees of freedom in total.

Before introducing this first AIBO model, ERS-110, there was about five years of basic research period. Now we have the 2nd generation AIBO model, ERS-210 and also another type of robot, Sony Dream Robot, SDR-3 as seen in Fig.10.

AIBO 2nd Generation, ERS-210

Sony Dream Robot, SDR-3



Fig. 10 New AIBO Models, ERS-210 and SDR-3

The 2nd generation AIBO model, ERS-210 has the following features:

- Joint DOF: neck:3, mouth:1, ear:2,
- legs:3x4, tail:2, total:20
- Sensors : Color CMOS Image sensor (1100K pixel),
- Microphone x 2,
- Infrared sensor,
- Acceleration sensor x 3,
- Tactile Sensor x 7
- CPU : 64bit RISC Processor (192MHz)
- Memory: 32MB DRAM
- OS, Architecture: Aperios, OPEN-R.1.1
- IF: PCMCIA, MemoryStick

The model SDR-3 has the following features:

- Joint DOF: neck:2, body:2, arms:4x2, legs:6x2, total:24
- Sensors : Color CCD camera 1800K pixel, Microphone x 2,
- Infrared sensor, Acceleration sensor x 2
- Gyro meter x 2, Tactile Sensor x 8
- CPU : 64bit RISC Processor x 2
- Memory: 32MB DRAM x 2
- OS, Architecture: Aperios, OPEN-R

It weighs 5.0 Kg and its size is 500 x 220 x 140 mm.

It has an OPEN-R architecture: It is made of configurable physical components (CPCs). The CPU in the head recognizes the robot configuration automatically. The components are built for Plug&Play or Hot Plug-In use. The relevant information in each segment is memorized in each CPC.

Each CPS may have a different function such as Behavior Planning, Motion Detection, Color Detection, Walking and Camera Module. Each CPS is also provided the corresponding object oriented programming and software component.

With this OPEN-R architecture, the body can be decomposed or assembled anyway for Plug&Play or Hot Plug-In use. The diagram in Fig.11 shows the details of the logical hardware block diagrams which contain DMAC : FBK: CDT: IPE and HUB

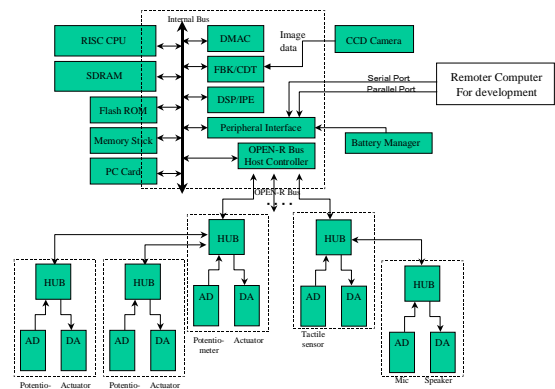


Fig. 11 Logical Hardware Block Diagram

In the following two figures, Fig.12 and Fig.13, the topology of Model ERS-110 and Model SDR-3x are shown respectively.

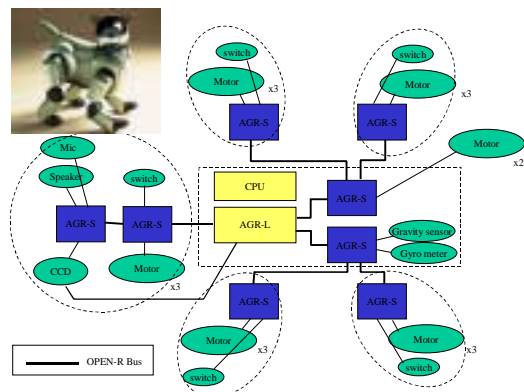


Fig. 12 Topology of ERS-110

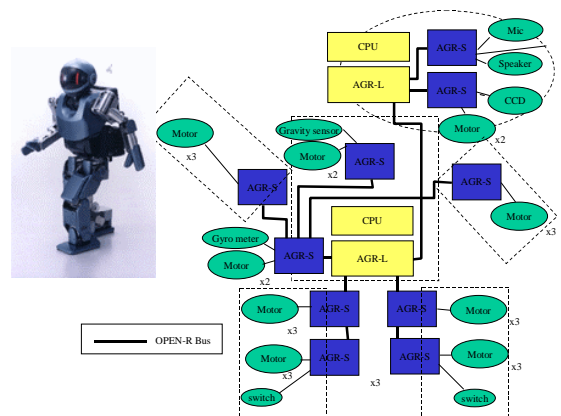


Fig. 13 Topology of SDR-3x

At the same time, it is very important to have a powerful software platform which covers from the top semantic layer to the deep bottom Device Driver Objects

Codings. Careful design considerations are very important to make the middleware software components.

3.3 Memory Stick

Now about our Memory Sticks. AIBO, VAIO PC and other audio and video products now use Memory Stick as the digital data recording media.

On July 1997, we had a technical announcement. Next year, Jan 1998, VAIO center was inaugurated. On July 1998, we had a product announcement. The 4Mbyte and 8Mbyte memory sticks were on sale in September 1998. In Feb 1999, we announced Magic Gate, that is, memory sticks with copyright-protection feature. Fig.14 shows the form comparison. Memory Stick is unique in its chewing gum-like shape, much taller in length than other media. The difference in appearance of Memory Stick from other media is clear in size and features.

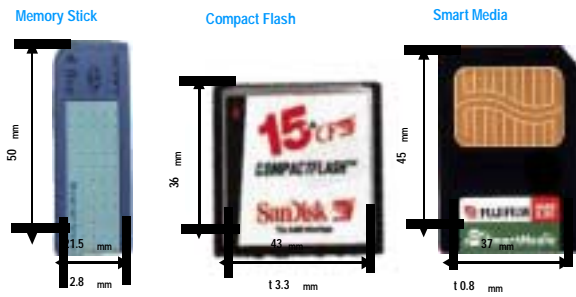


Fig. 14 Form Comparison

The Fig.15 shows the internal structure. It is fool proof. It features simple 10 pin connection and it is impossible to touch terminals directly.

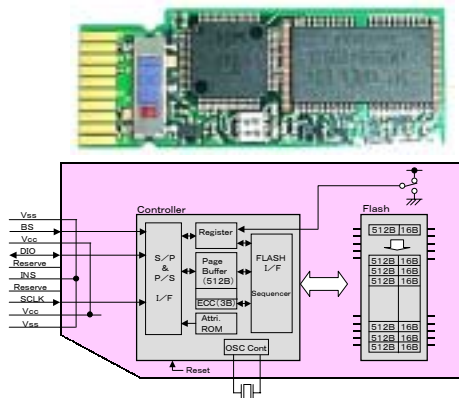


Fig. 15 Internal Structure

The shape was designed by intention to make exchanging of media to be easy without having to actually see them, and to guide the direction for easy and correct insertion. Much contrivance is made in the design.

In order to decrease the number of connector pins for ensuring reliability of the connectors, serial interface was adopted instead of parallel interface

used in conventional memory cards. As a result, connector pins were reduced to 10. And as the structure is such so that they do not touch the terminal directly, extremely high reliability is ensured. The length is same as AA size battery of 50 mm for further deployment to portable appliances. The width is 21.5 mm and 2.8 mm in thickness.

Memory Stick consists of FLASH EEPROM and a controller, controlling multiple Flash EEPROM, flexible to their variations, and capable of correcting errors unique to different Flash EEPROMs used. Memory Stick converts parallel to/from serial data with the controller designed in compliance to serial interface protocol, any kind of existing or future Flash EEPROM can be used for Memory Stick. The function load to the controller chip is not excessive, and its cost can be kept to a minimum.

It is light and the shape makes it easy to carry around and to handle. Also the write-protection switch enables easy protection of variable data.

For still-image format, DCF standardized by JEIDA is applied. DCF stands for design rule for camera file system and JEIDA stands for Japan Electronic Industry Development Association. For voice format, ITU-T Recommendation G.726 ADPCM is adopted. The format is regulated for applications which convert voice data to text data by inserting Memory Stick to a PC.

Memory Stick can handle multiple applications such as still image, moving image, voice and music on the same media. In order to do this, formats of respective application and directory management must be stipulated to realize compatibility among appliances.

Thus simply by specifying the “control information” format, we can have a new form of enjoyments through connecting AV appliances and PC. This format which links data handed in AV appliances enables relating multiple AV applications. For example, voice recorded on IC recorder can be dubbed on to a still image file recorded by a digital still camera.

At present, the music world is going digital from analog, and the copyright protection issue is becoming serious along with wide use of internet. Memory Stick can provide a solution to this problem by introducing “Magic Gates”, a new technology..

By Open MG, we mean 1 : allowing music download through multiple electronic music distribution platforms 2 : enabling to playback music files and CD extracting on PCs (OpenMG Jukebox) 3 : transferring contents securely from PCs to portable devices.

Fig.16 shows the stack technology applied to Memory Stick with 4 Stacked Chips.

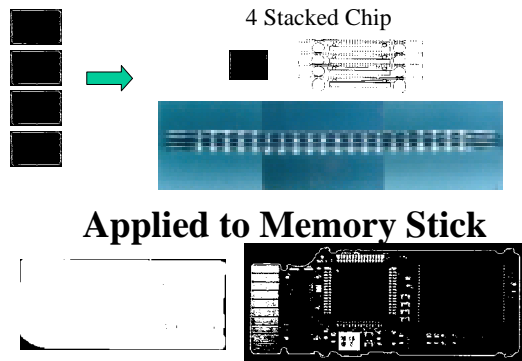


Fig. 16 Stack Technology

3.4 Play Station 2

Now some information on Playstaion2.

Playstation2 aimed as the fusion of graphics, audio/video and PC. The chipset includes a 128 bit CPU called “Emotion Engine” with 300 MHz clock frequency with direct RambusDRAM of 32Mbyte main memory. The chipset also includes a graphic synthesizer chip with 150 MHz clock frequency. It has 4Mbyte video RAM as an embedded cache.

As SPUs, the chipset also has an I/O processor for X24 speed CR-ROM drive and X4 speed DVD-ROM. Fig.17 shows PlayStation 2 (SCPH-10000) System Block Diagram.

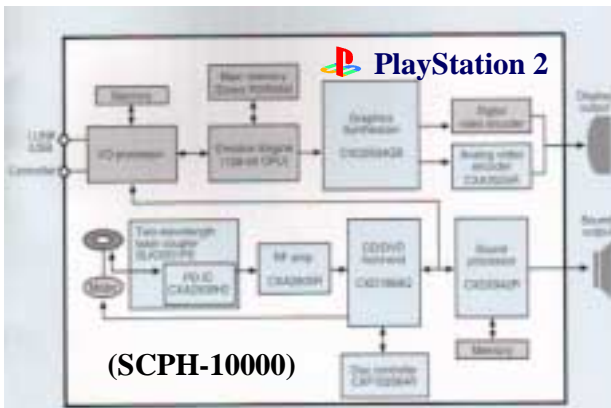


Fig. 17 PSX2 System Block Diagram

Playstation 2, which Sony Computer Entertainment Inc. released in March 2000, integrates games, music, and movies into a new dimension. It is designed to become the boarding gate for computer entertainment. PlayStation 2 uses an ultra-fast computer and 3D graphics technology to allow the creation of

video expressions that were not previously possible.

While supporting DVD, the latest media, it also features backwards compatibility with PlayStation CD-ROM so that users can enjoy the several thousand titles of PlayStation software. PlayStation 2 is designed as a new generation computer entertainment system that incorporates a wide range of future possibilities. The table shows the performance spec of the graphic synthesizer chip, CXD2934.

Clock Frequency	150 MHz
Number of pixel engines	16 parallel processors
Hybrid DRAM capacity	4MB@150MHz
Total memory bandwidth	48GB/sec
Maximum number of display colors	2560 bits
Z buffer	32 bits (RGBA: 8 bit each)
Process Technology	0.25 um
Total number of transistors	43 M Tr's
Package	384-pin BGA
Image Output Formats	NTSC/PAL, D-TV, VESA (upto 1280x1024 dots)

In Addition to the 128-bit CPU Emotion Engine™ and I/O processor, Playstation 2 adopts several advanced technologies. The Graphics Synthesizer graphic engine, CXD2934GB, takes full advantage of embedded DRAM system LSI technology.

The following Fig.18 shows the chip photograph of our 0.25 um CMOS 4MB Embedded DRAM which has 42.7 M Trs. The clock rate is 150 MHz, with 48 GBps band width. It can draw 75M polygons/sec. It has 384 pin in BGA. Its cross sectional view is also shown here.

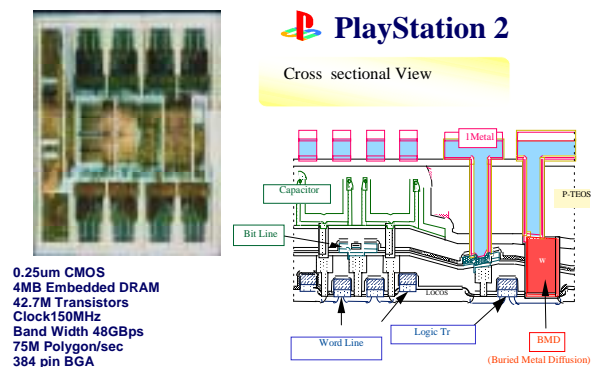


Fig. 18 4MB EmDRAM for PSX2

Semiconductor’s optical integrated device technology contributes significantly to miniaturization and high reliability in the optical pickups, SLK3201PE, a two-wavelength laser coupler chip. PlayStation 2 also adopts the optical disc system chip solution which has a solid track record, CXD2942R, a sound processor chip, and has earned the trust of the optical disc system market.

It also includes CXD1869 (CD/DVD signal Processor LSI), CXP102064R (Disk Controller), CXA2605R (Cd/DVD RD Matrix Amplifier) and CXA3525R (Analog Video Encoder).

First commercial product for use in consumer products is 0.5 μm LSI chips for 8 mm camcorders in 1995. Then we had 0.35 μm LSI chips for MD products with low voltage operation of 2.0 volt. Now 0.25 μm PlayStation 2 Graphics Synthesizer has eDRAM with 48 GB/sec bandwidth. Fig.19 shows the EmDRAM History.

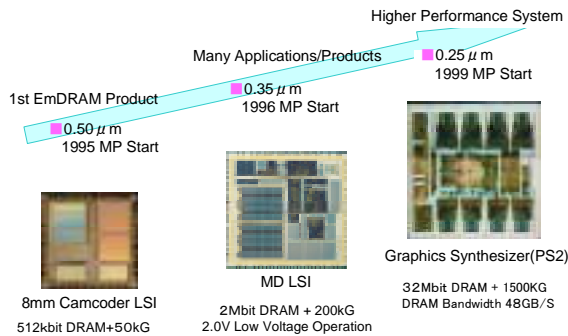


Fig. 19 Embedded DRAM History

Sony Em-DRAM has a high-band performance of 76.8 Gbyte/sec. See Fig.20.

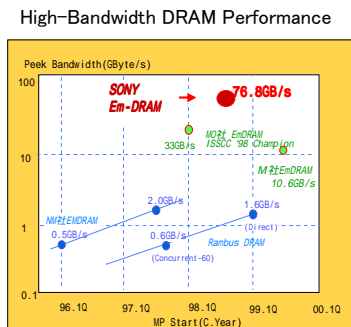


Fig. 20 Performance of Embedded DRAM

In the following three figures, Fig.21, Fig.22 and Fig.23, the memory cell size trend, some details of our embedded DRAM history and the vertical critical dimensions between 0.25 μm and 0.18 μm EmDRAM process are shown respectively.

Some words on the feature and critical issues of 130 nm Emb-DRAM LSI Process.

The most advanced design rule to achieve high performance T_r –

- Enhance resolution, and
- refine OPC system (speed, accuracy)
- Large variation in duty cycles
- Reduce isolation – dense bias

High global step → Enlarge D.O.F
High aspect hole process
→ Enhance etching durability

OPC=Optical Proximity Correction
 DOF=Depth of Focus

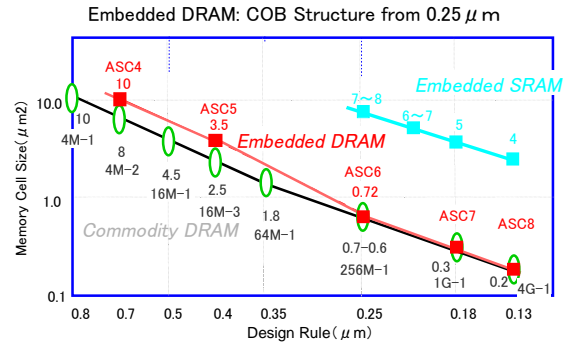


Fig. 21 CMOS Memory Cell Size

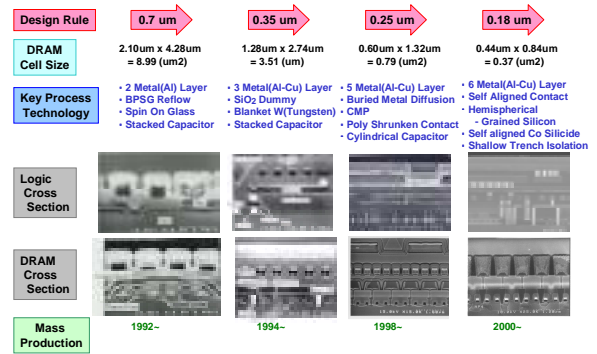


Fig. 22 Embedded DRAM History

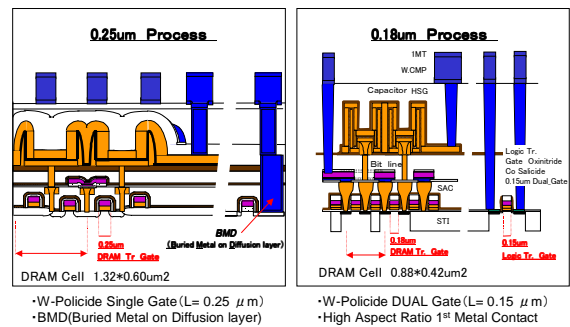


Fig. 23 Em-DRAM Process Technology

In the 0.18 μm EmDRAM process, the optical Proximity Correction (OPC) technology and the phase-shift mask technology (PSM) were very important. See Fig.24 and Fig.25. Many high performance manufacturing and measurement automatic machines such as shown in Fig.26 are necessary

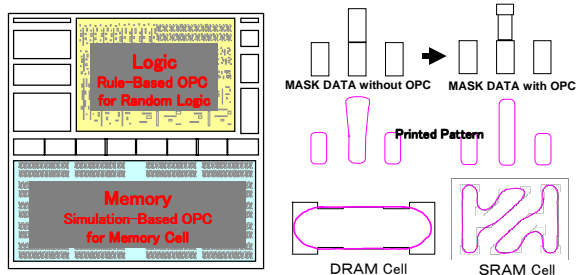


Fig. 24 Optical Proximity Correction

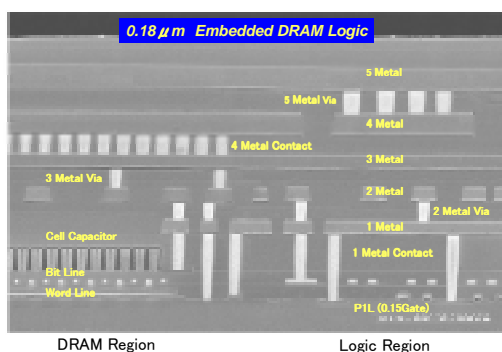


Fig. 27 Cross Sectional View

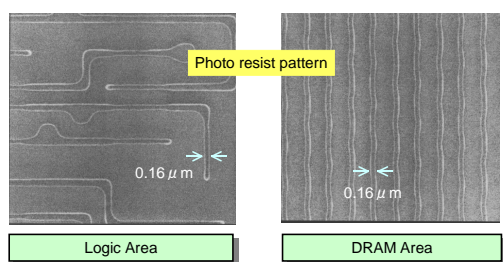


Fig. 25 Phase-Shift Mask(PSM) Technology

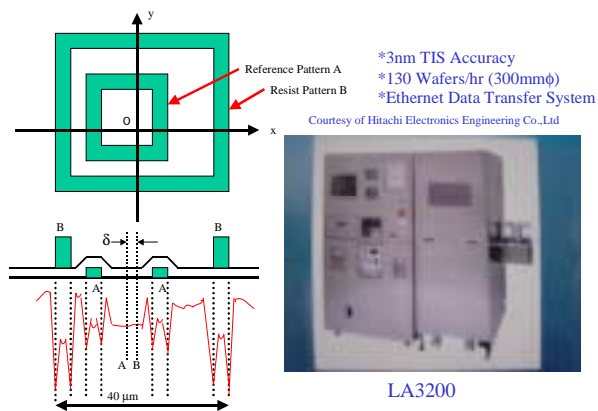


Fig. 26 Overlay Accuracy Measurement System

The Fig.27 shows the cross sectional view of 0.18 um EmDRAM which was realized by utilizing all of these technology and the high performance machines.

Now some comments on key factors: technology extension such as optical extension and full flat process technology. KrF lithography optical extension features high NA, Ultra-Resolution, thin photo resist and the OPC technology. Wirings are fully planarized interlayers Cu/Dual Damascene. The EmDRAM features Fully Planarized Capacitor with the Global step-less DRAM/Logic structure by self-align process.

4 Conclusion

Some introductory comments on the basic semiconductor device concepts were given. They are strongly related to the microelectronics of the present home entertainment LSI Chips. The talk covered some product specifications and performance aspects of the home entertainment LSI chip sets, such as for digital cameras, home robotics and games in details. Cost of EmDRAM and its solutions by using EmDRAM are strongly related with new market creation like PSX2. The EmDRAM technology for PS2/Computer and some other future home entertainment electronics gadgets has a potential to be the technology driver in years to come.

4 Reference

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