- (1) Historically we had P+N junction type photodiode which suffered the serious image lag problem.
- (2) When CCD was invented, we obtained image lag free fast action picture quality. However, the CCD type MOS capacitor structure had serious blue light sensitivity problem and surface dark current.
- (3) Hagiwara at SONY invented in 1975 the P+NPNsub junction type photodiode with the heavily doped P+ surface hole accumulation layer and the built-in vertical overflow drain (VOD) function with complete charge transfer operation mode with no image lag. See the Japanese Patent 1975-134985.
- (4) Hagiwara at Sony in 1975 also invented the back light illumination type Pinned Photodiode and with the MOS Capacitor type Buffer memory for the built-in Global Shutter Scheme in his Japanese Patent 1975-127649, which is useful specially for the modern CMOS image sensor applications.

There are basically four kinds of Photodiode.

- (1) The classical N+P junction type photodiode
- (2) The Buried Photodiode named by NEC in IEDM1982
- (3) which is also Depletion Photodiode with no image lag.
- (4) The Pinned Photodiode named by KODAK in IEDM 1983, which has low surface dark current.

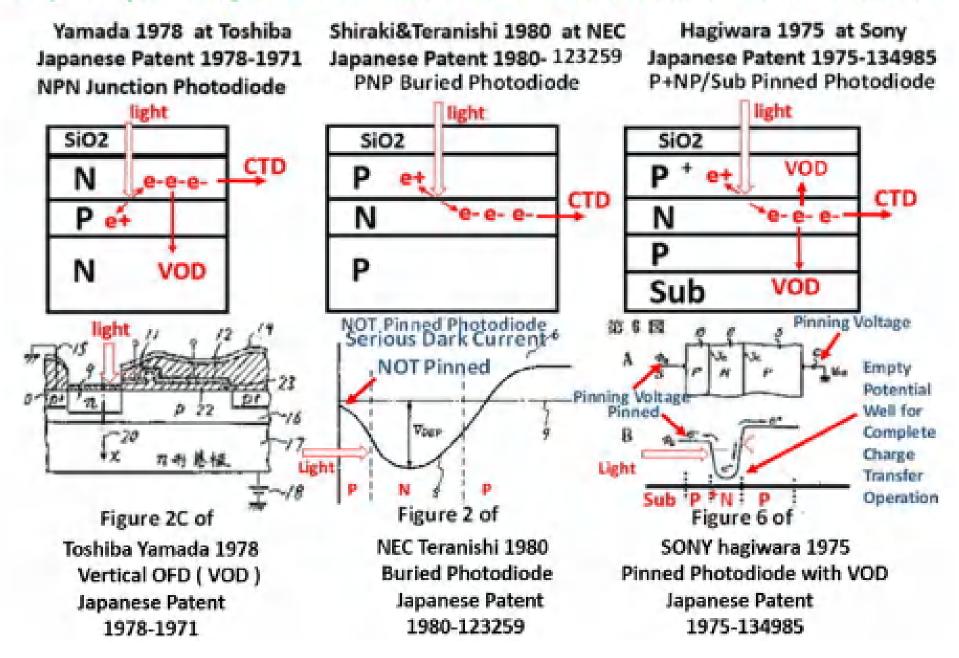
SONY developed the complete production quality of Hole Accumulation Diode Sensor with VOD function in 1984. Everyone thought that the invention of SONY HAD was after the NEC IEDM1982 and the KODAK 1983 IEDM papers. But that is not true. Hagiwara at SONY invented in 1975 the Buried Photodiode, Depletion Photodiode and Pinned Photodiode with the vertical overflow drain (VOD) Function and the in-pixel MOS capacitor type Buffer memory for the built-in Global Shutter operation and the Back Light Illumination Scheme.

Please look carefully at the original NEC patent 1980-123259 on the Buried Photodiode filed by Shirai-san and Teranishi-san at NEC.

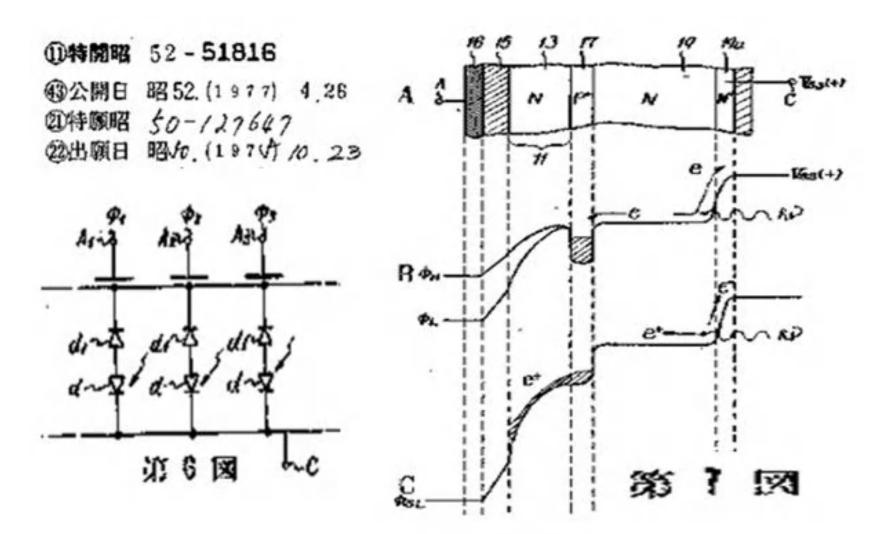
This patent describes about the Buried Photodiode and the Depletion Photodiode which were already Invented by Hagiwara at SONY in 1975. But this patent does not describe about Pinned Photodiode.

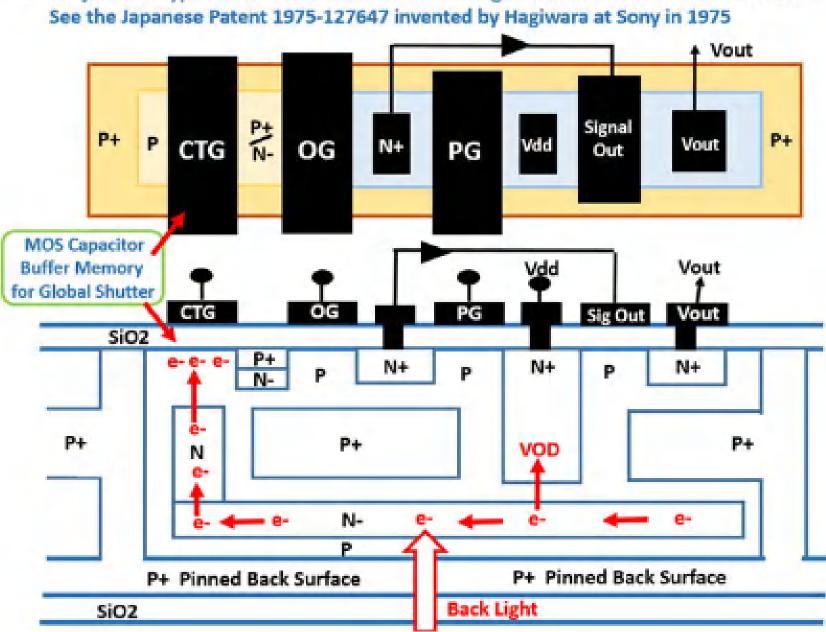
This is NOT Pinned Photodiode Patent ! Teranishi-san did not invent Pinned Photodiode !

The Toshiba 1978 VOD Patent and the NEC 1980 Buried Photodiode Patent are both invalid. They are copies of Hagiwara 1975 P+NP/Sub Pinned Photodiode with built-in VOD function.

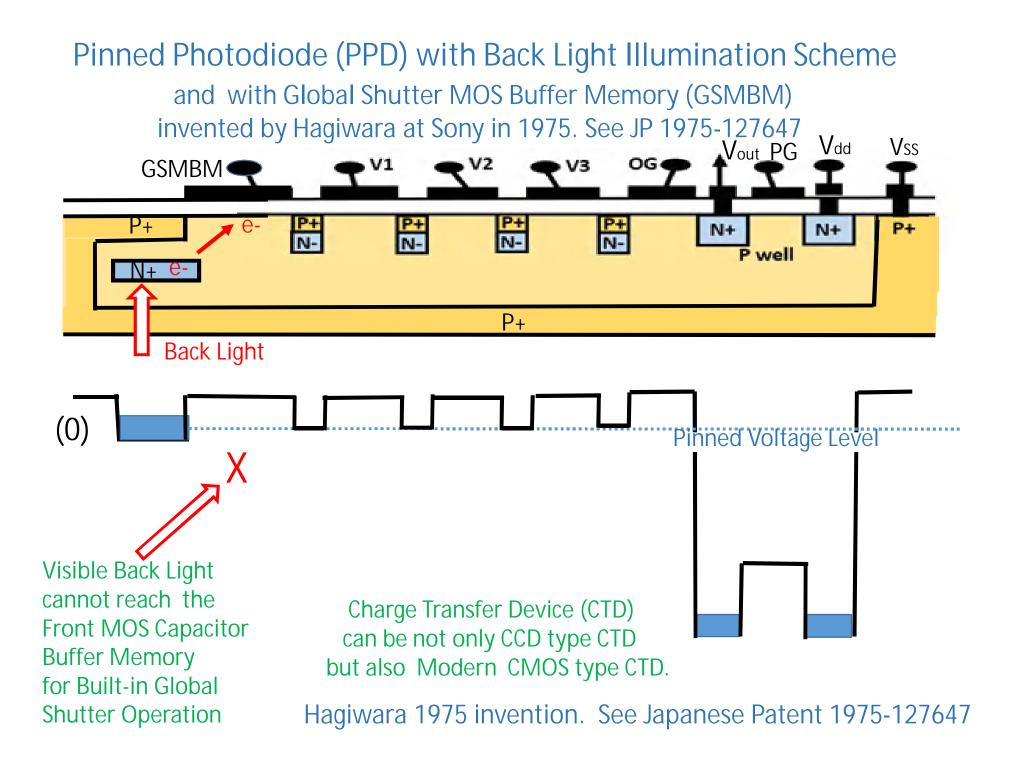


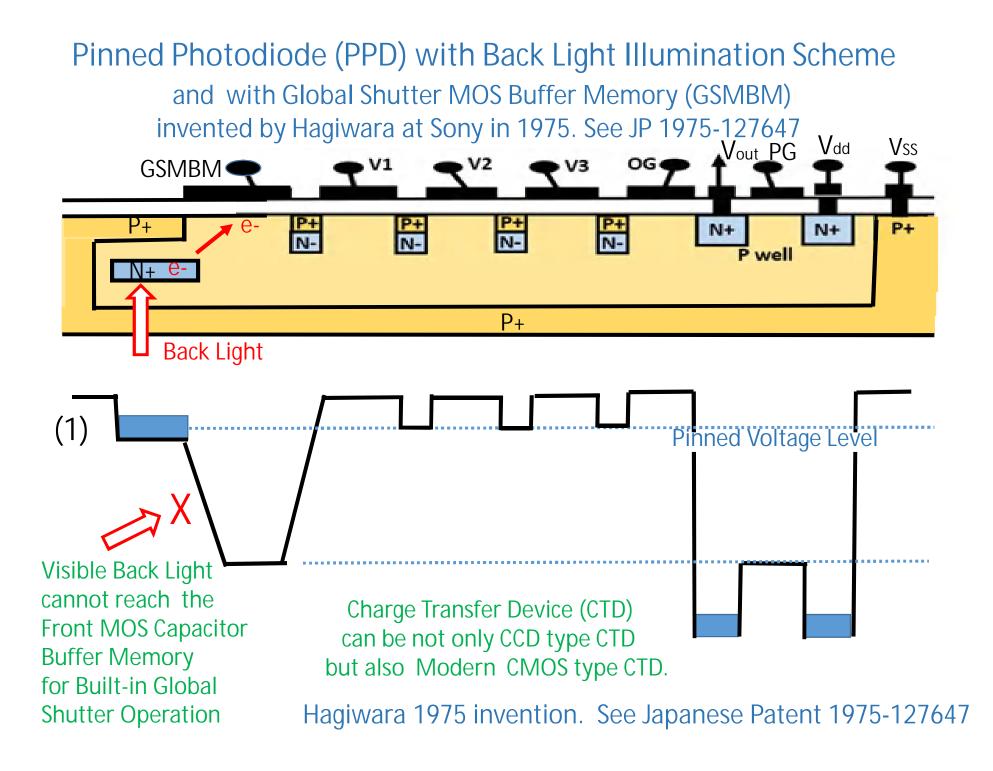
Pinned Photodiode (PPD) with Back Light Illumination Scheme with Complete Charge Transfer Operation (No Image Lag) and with Global Shutter MOS Buffer Memory (GSMBM) invented by Hagiwara at Sony in 1975. See JP 1975-127647

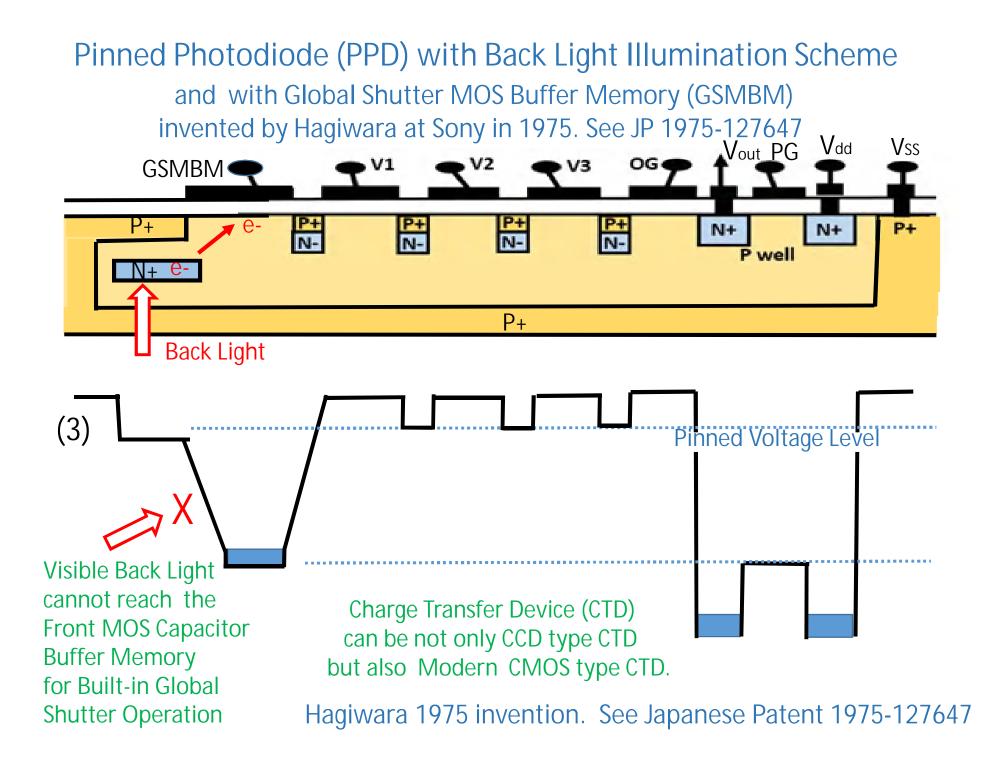


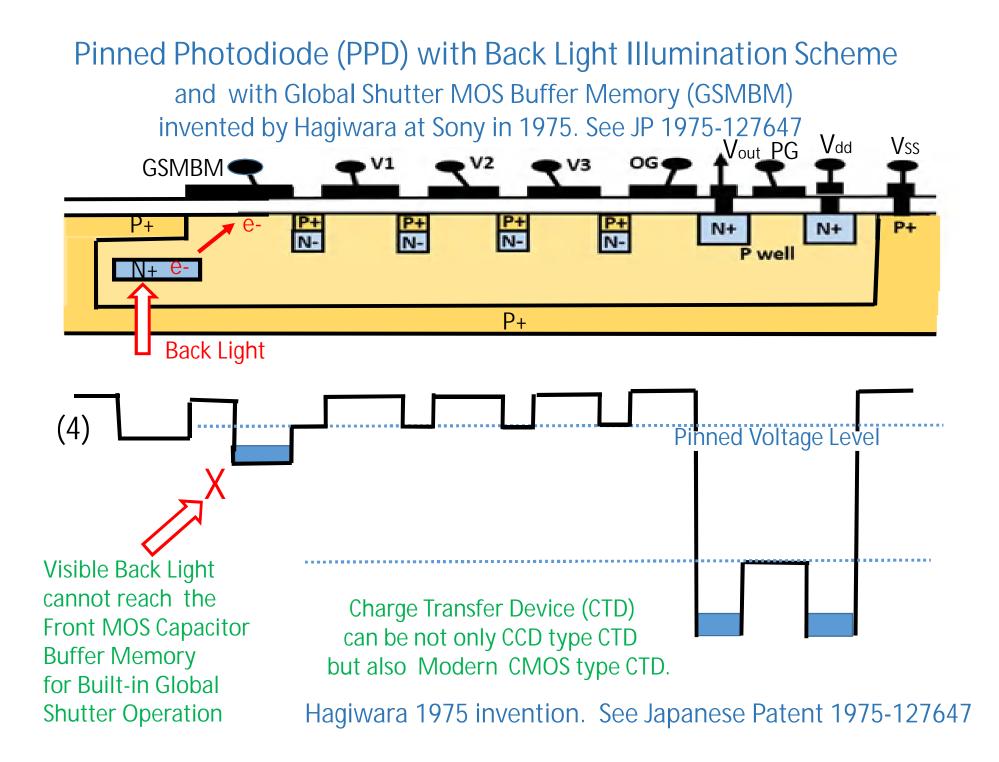


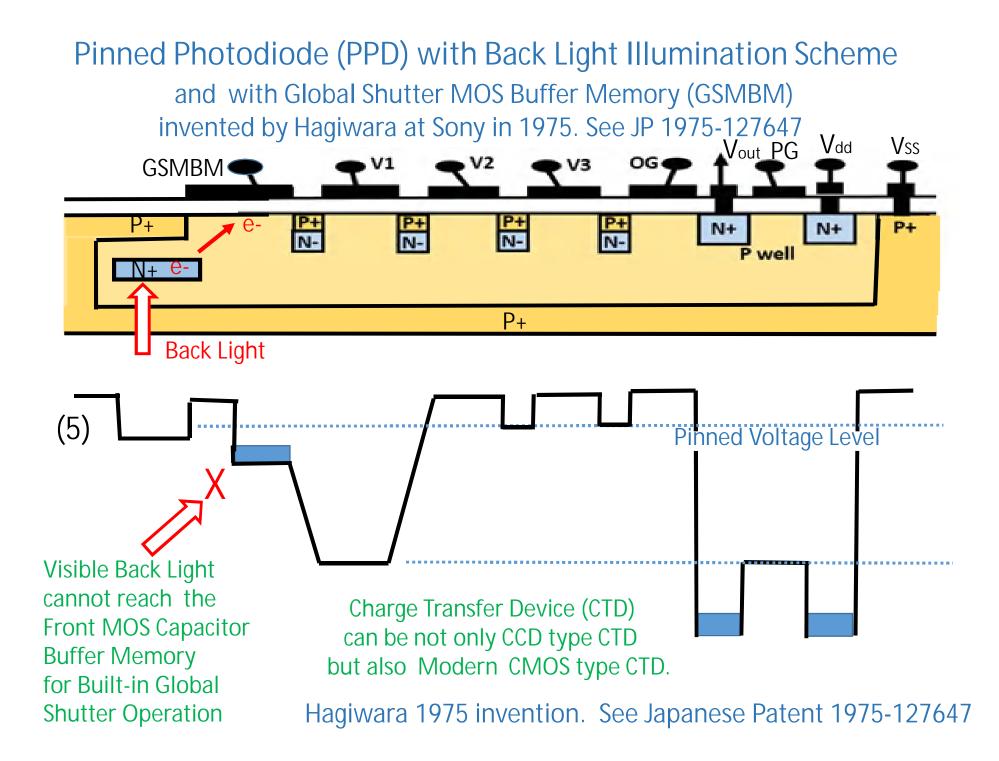
P+NP junction type Pinned Photodiode with Back Light Illumination and VOD function.

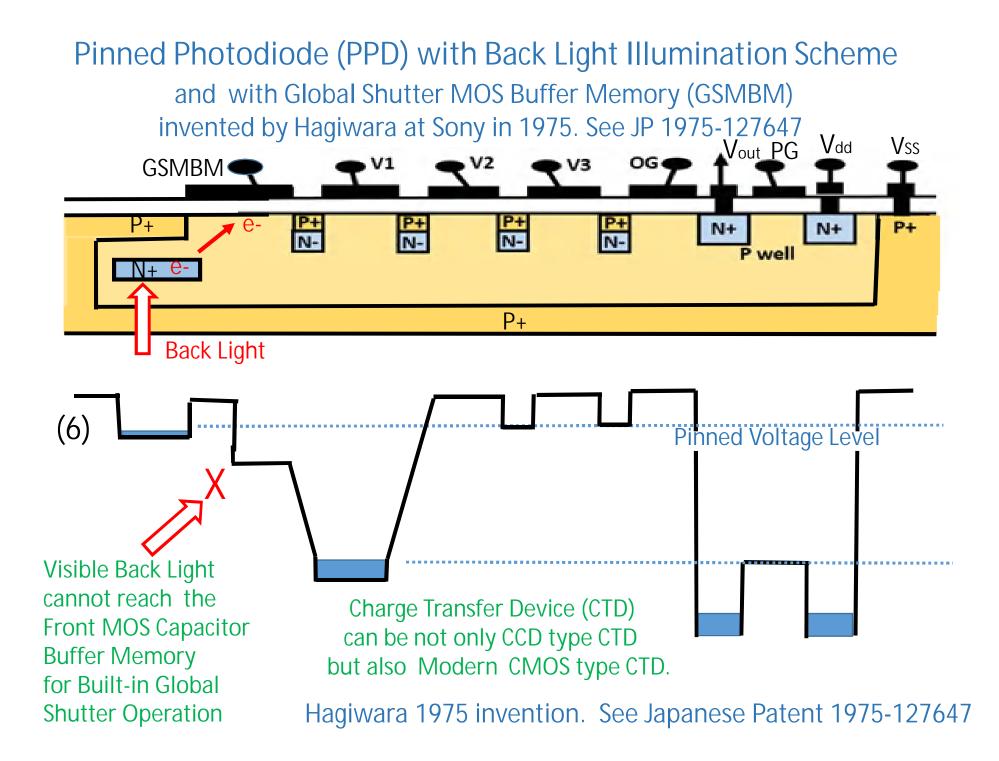


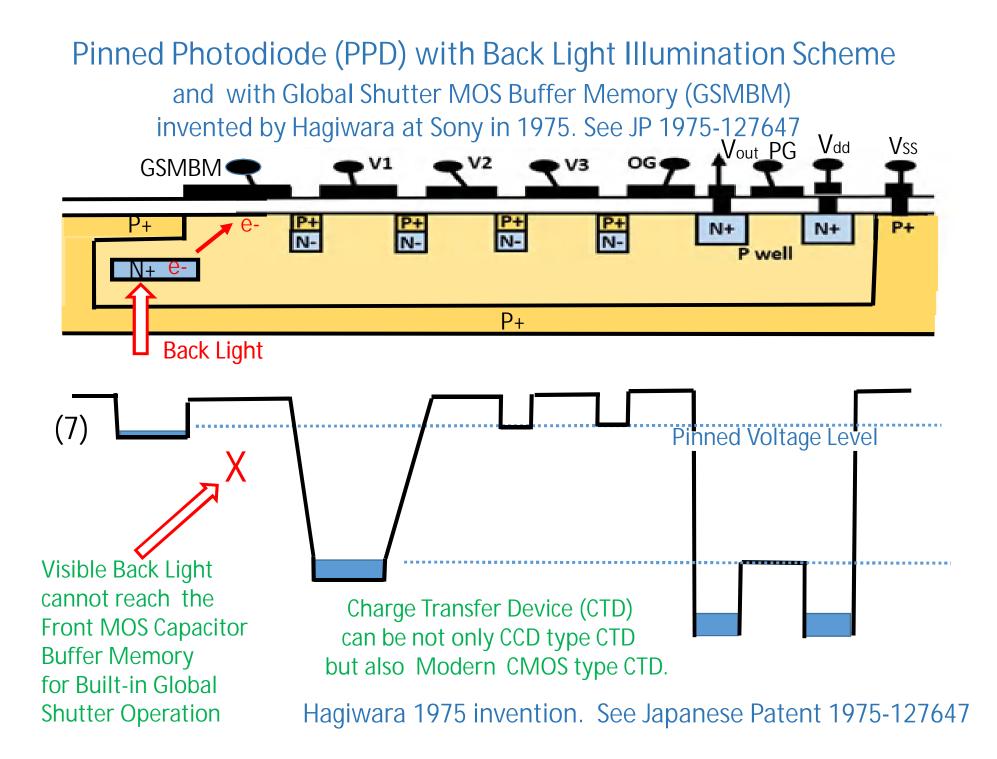


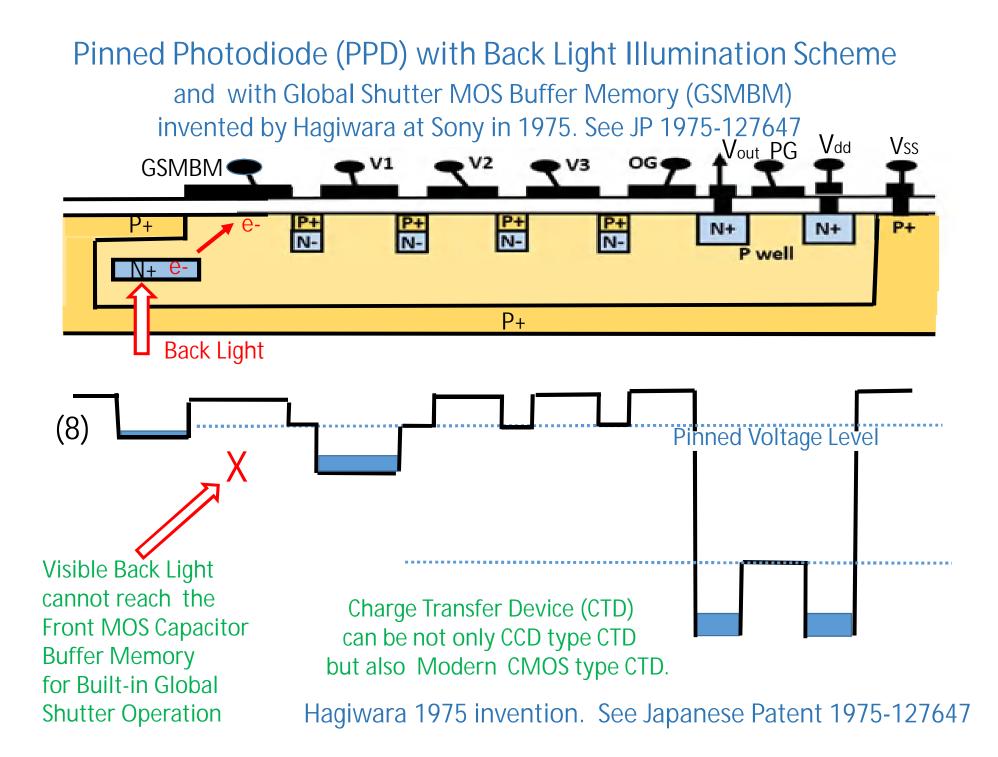


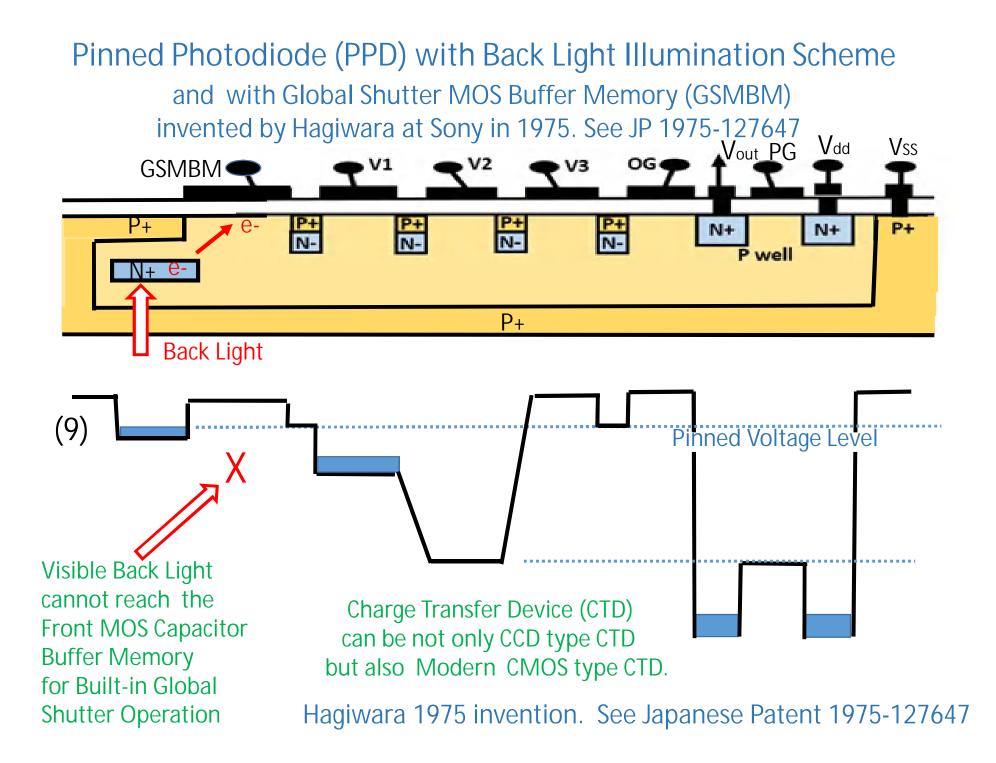


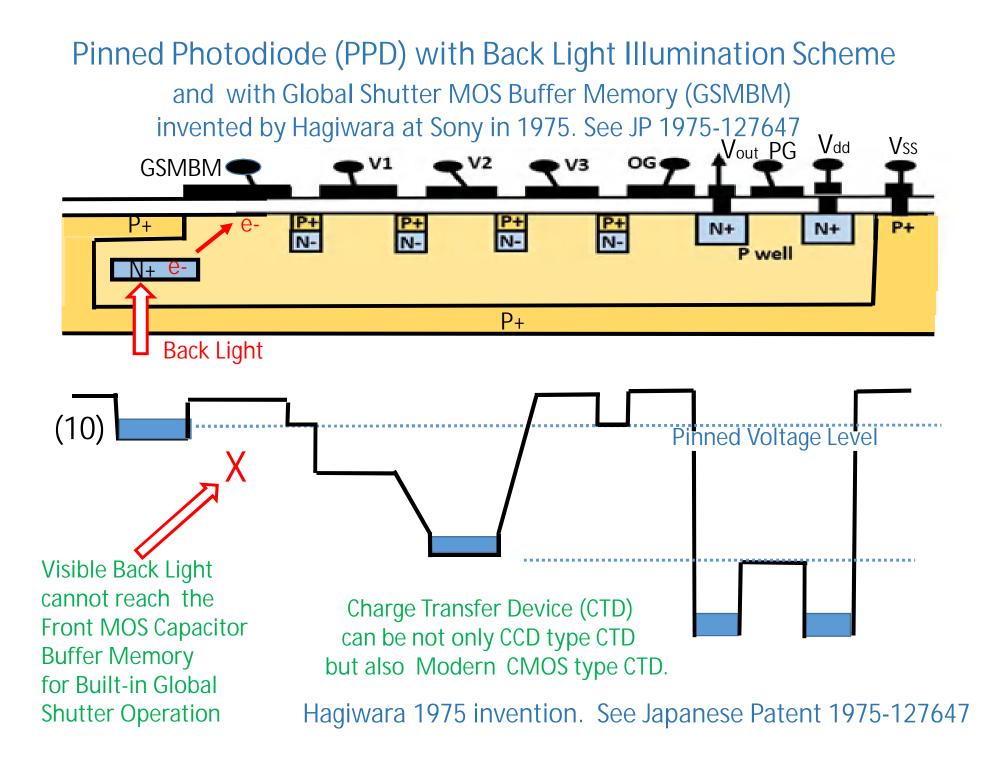


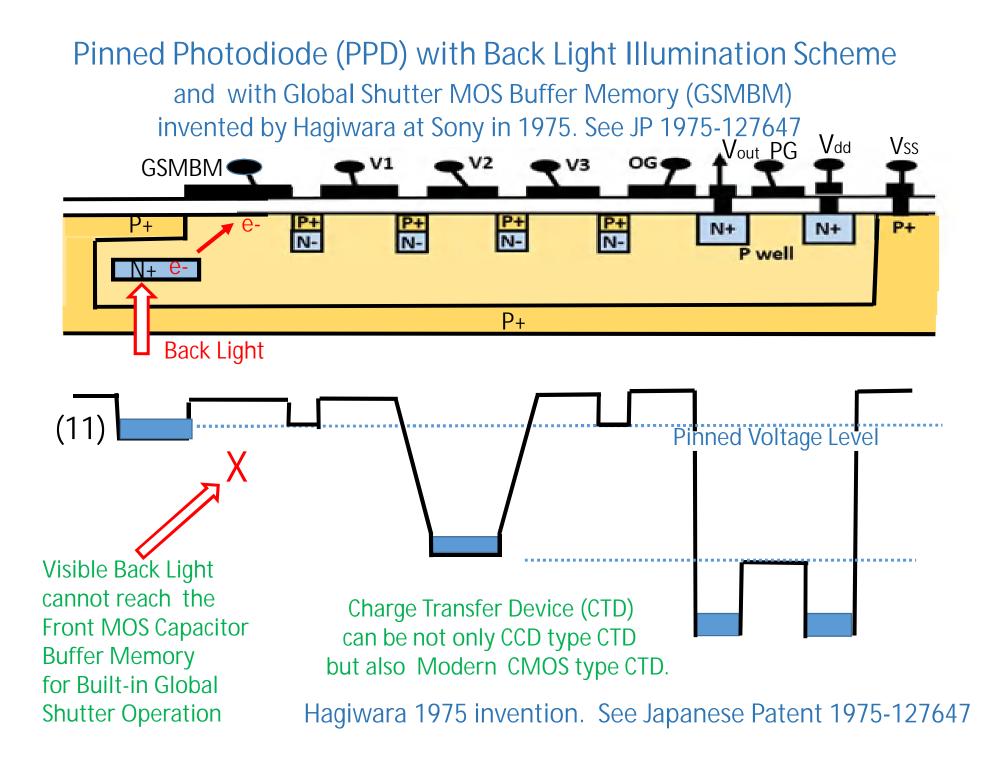


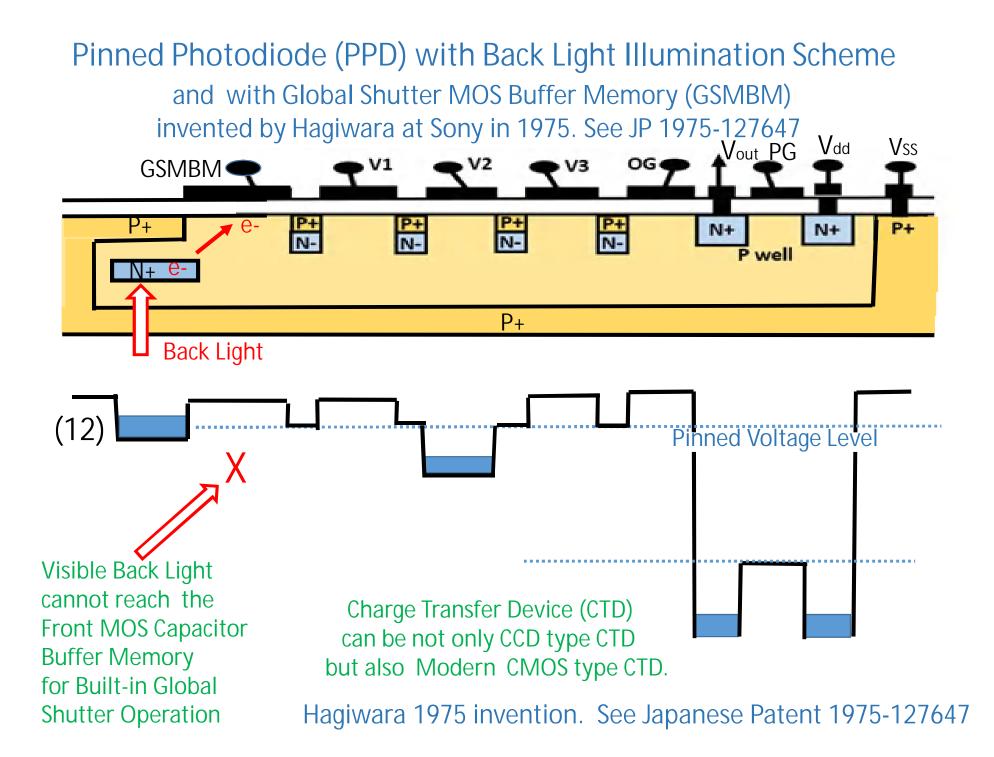


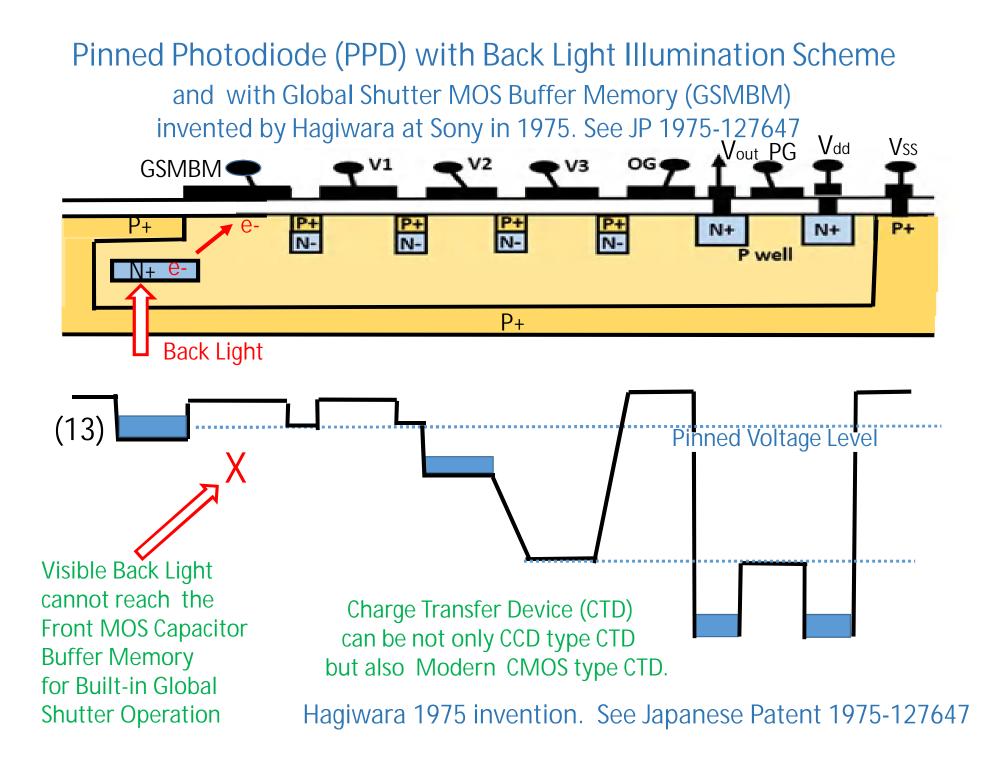


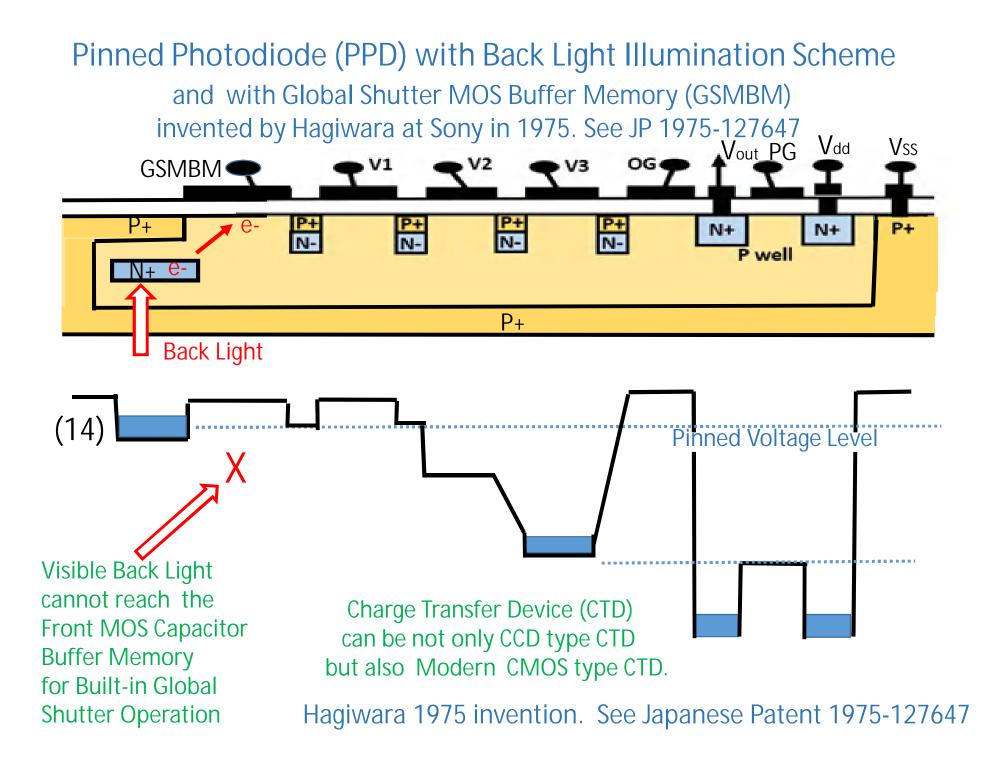


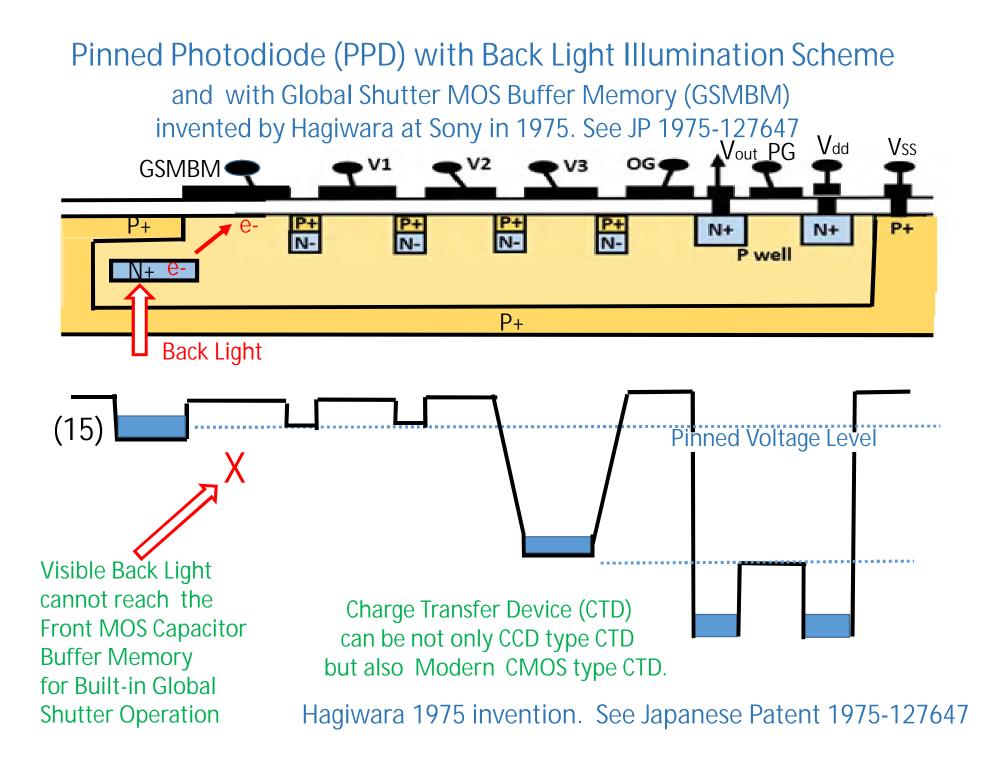


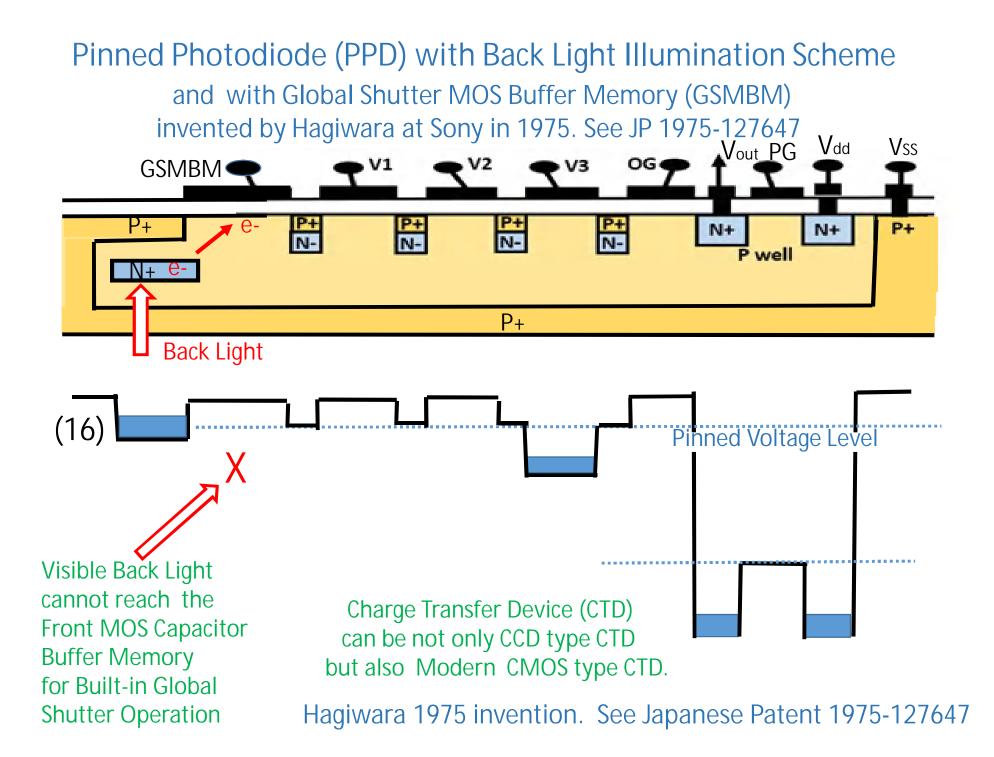


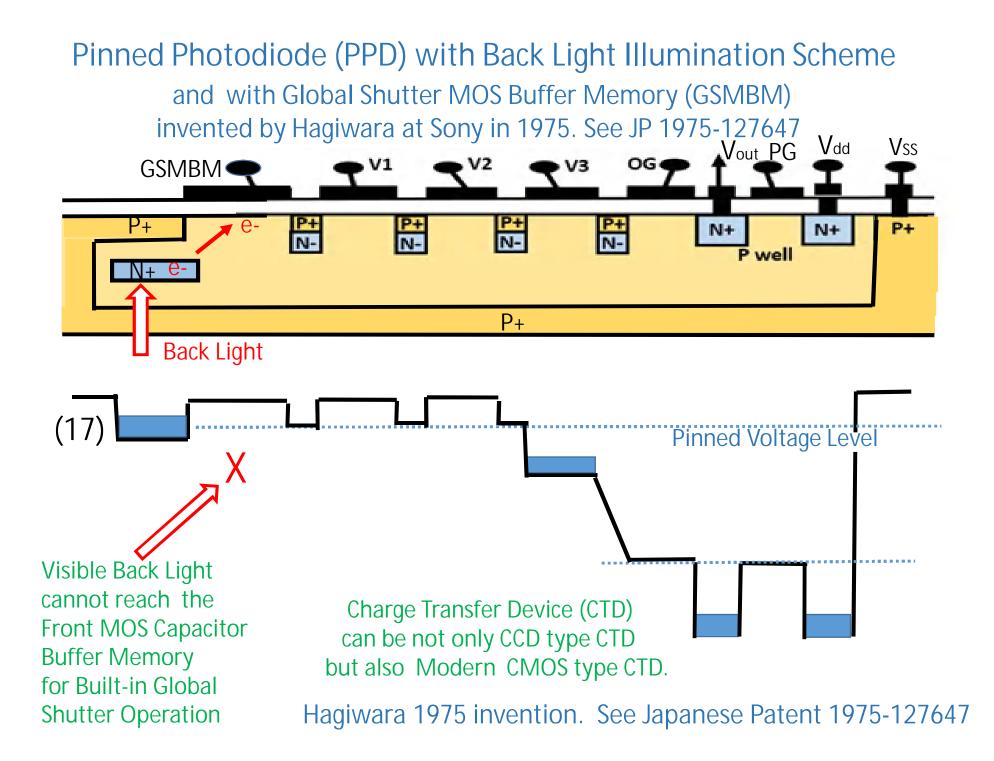


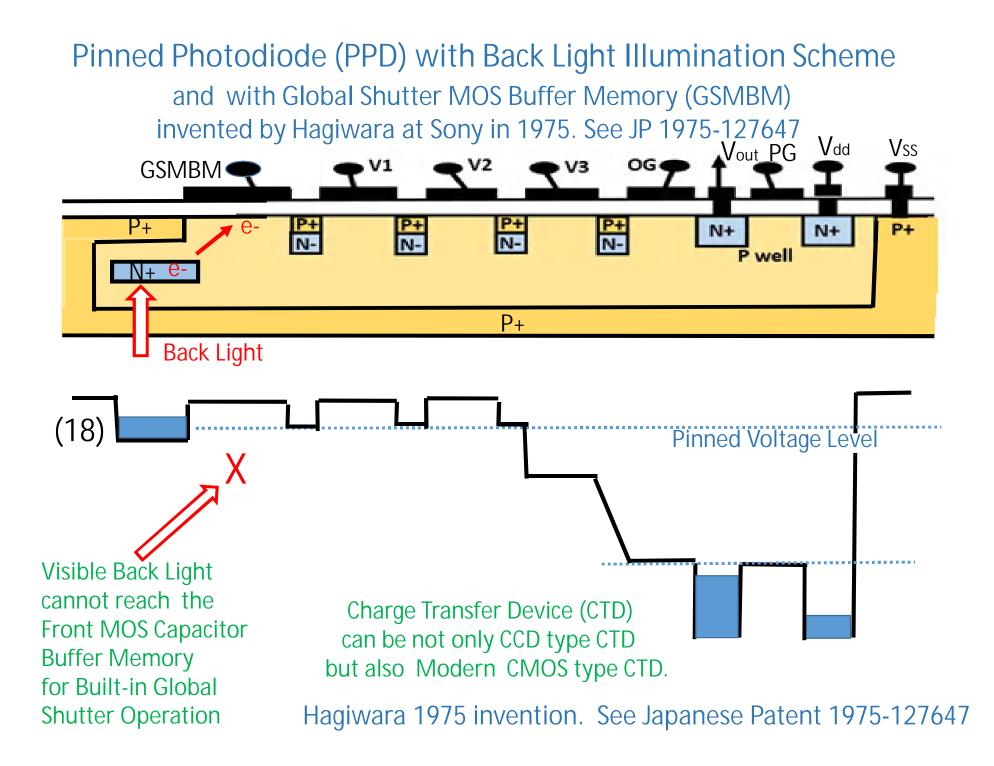


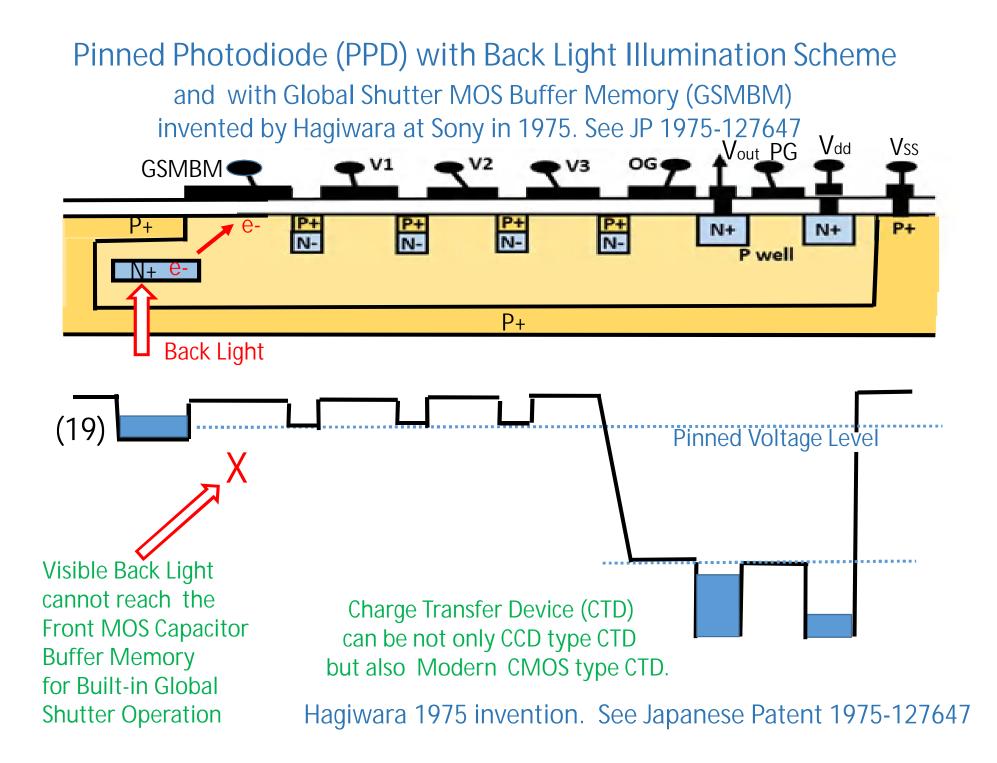


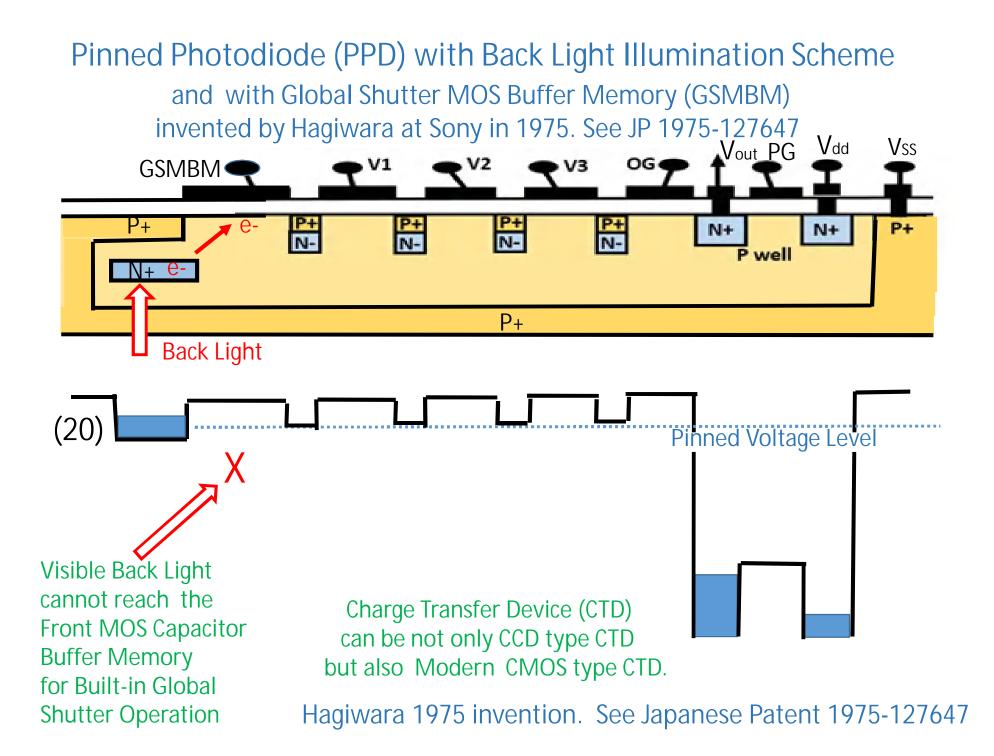


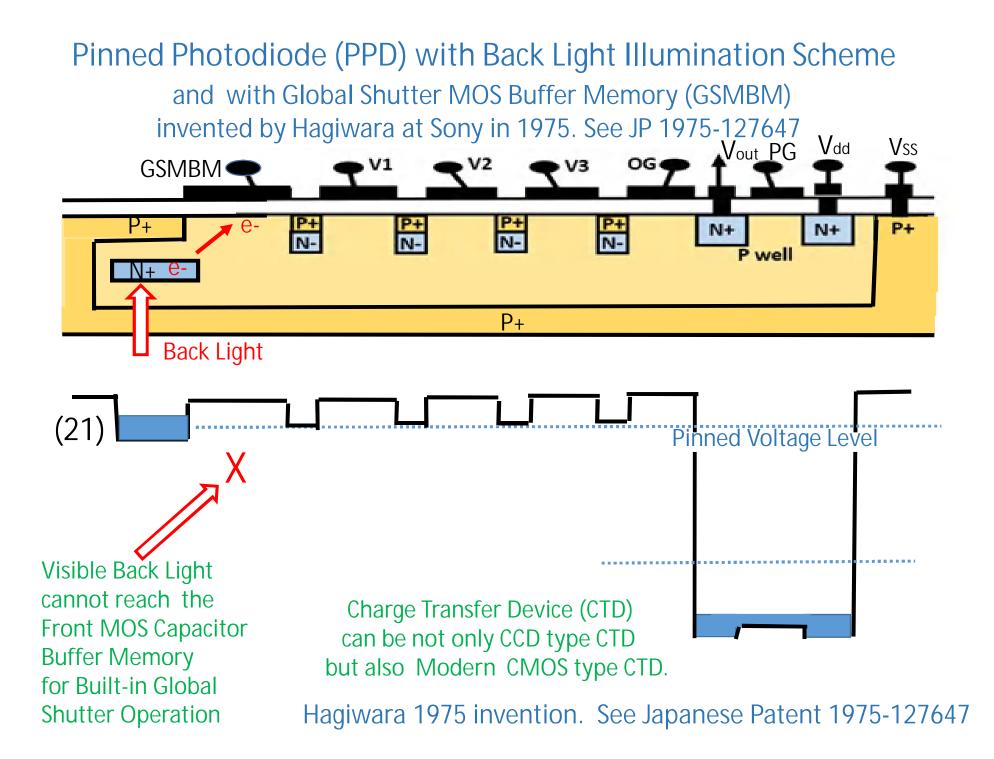


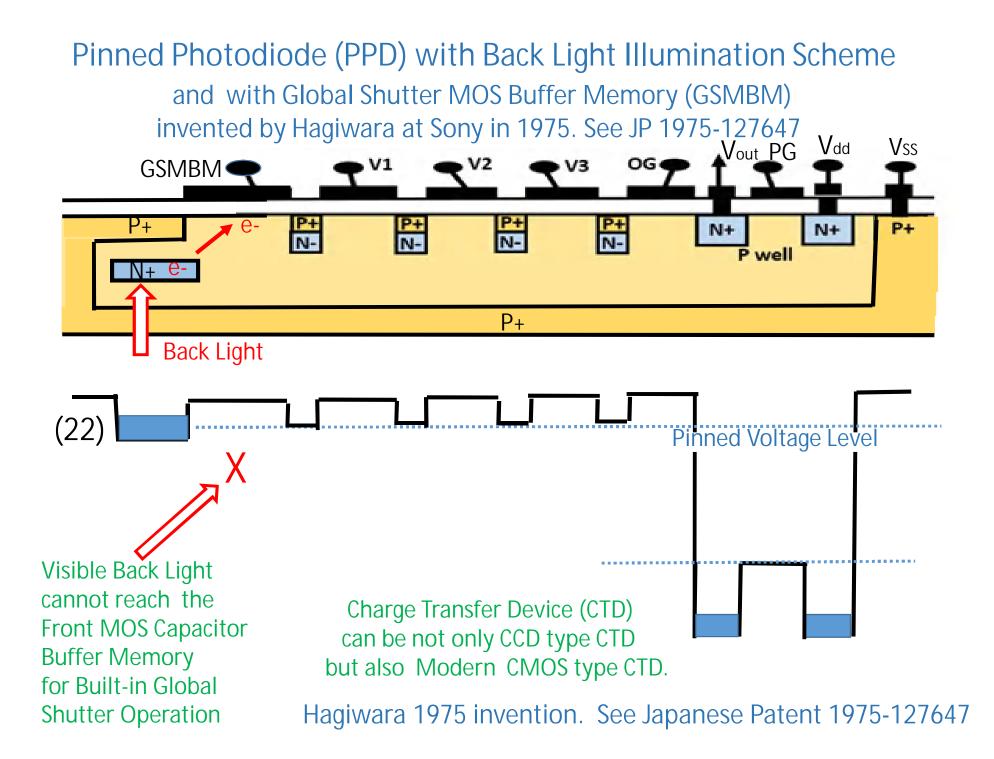












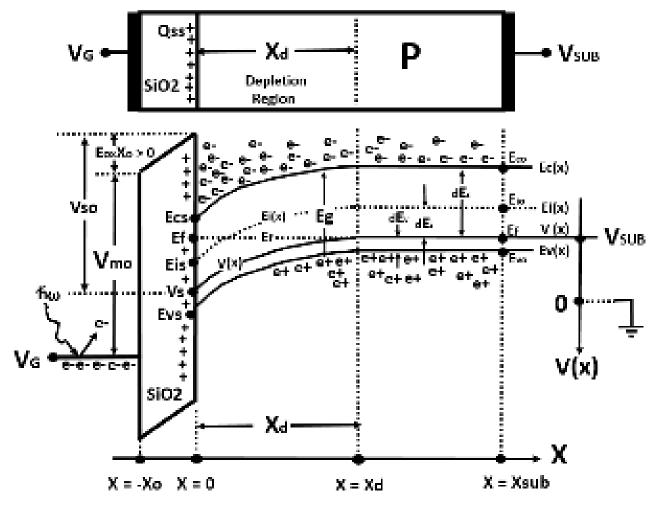


Figure 1

The band diagram of one Dimension MOS structure of P-type silicon wafer with a positive gate voltage

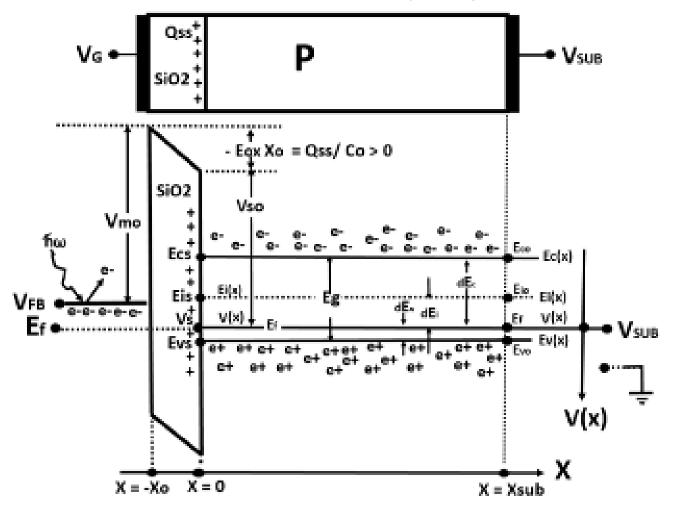


Figure 2

The band diagram of one Dimension MOS structure of P-type silicon wafer at the flat band gate voltage.

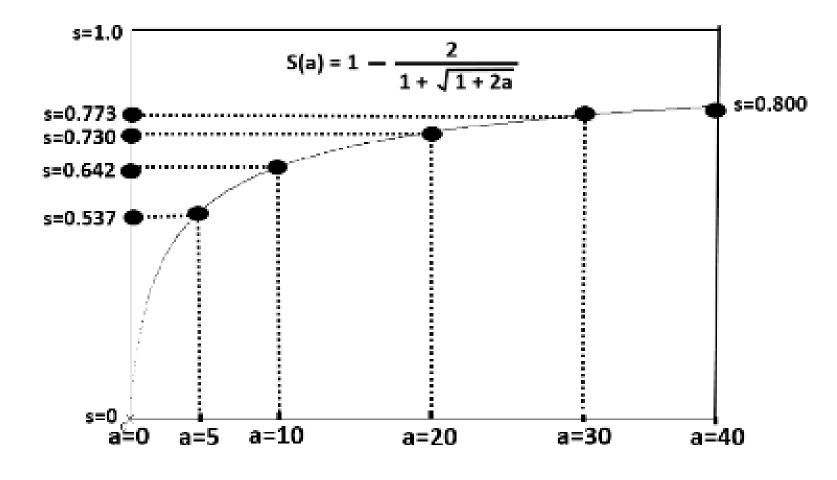


Figure 3

The values of the function S = S(a) plotted against the input physical parameter a = VGG/VA.

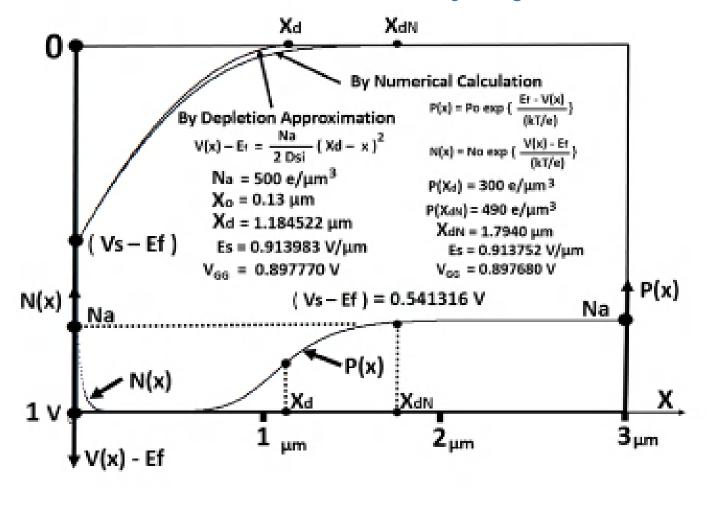


Figure 4

The internal potential V(x) and the mobile electron and hole densities P(x) and N(x) at the onset of the strong inversion condition.

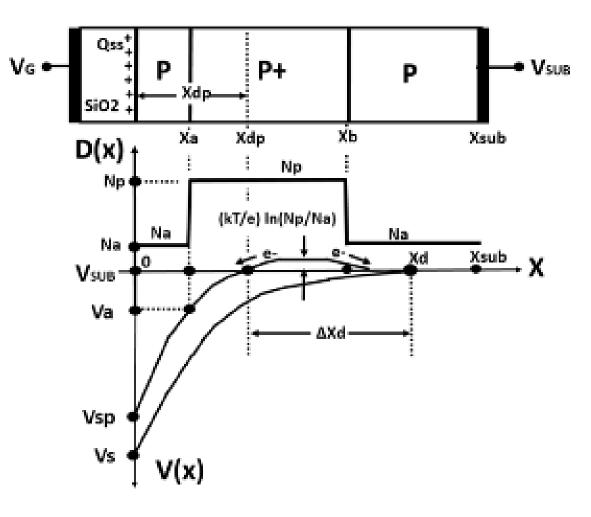


Figure 5

The impurity doping profile D(x) for the heavily doped buried P+ layer and the internal potential V(x)

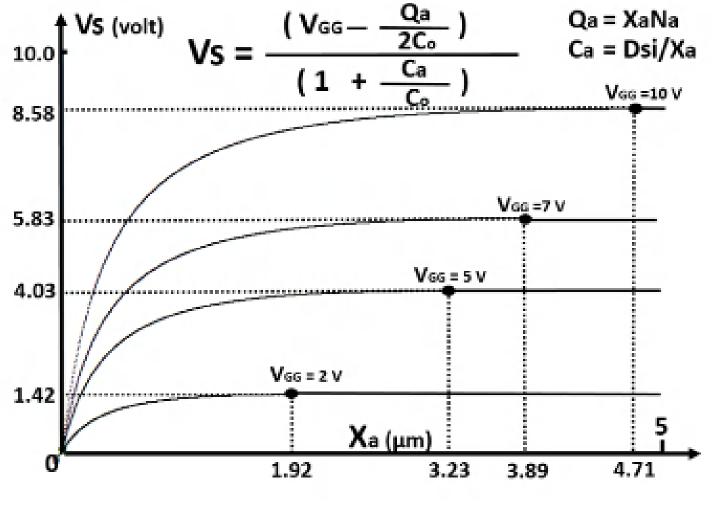


Figure 6

The surface potential plotted against the depth Xa of the buried P+ layer.

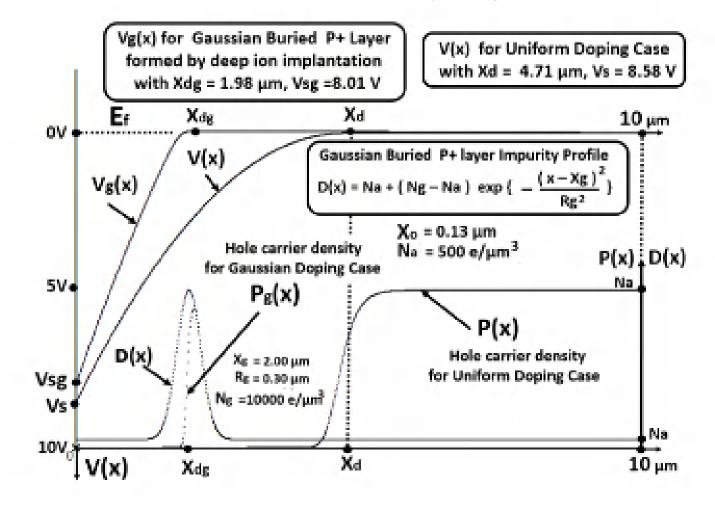


Figure 7

The internal potential profile Vg(x) and the majority carrier hole density Pg(x) for the case of Gaussian Buried P+ Layer are shown in comparison with the Uniform Doping Profile case

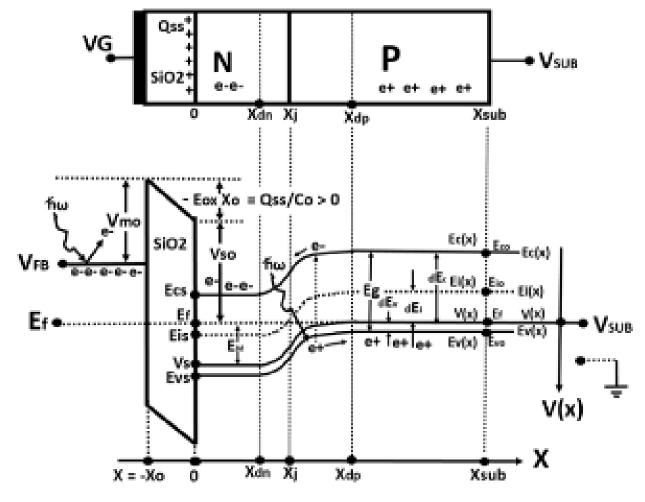


Figure 8

The NP junction type Buried Channel MOS Capacitor Structure with the flat band gate voltage

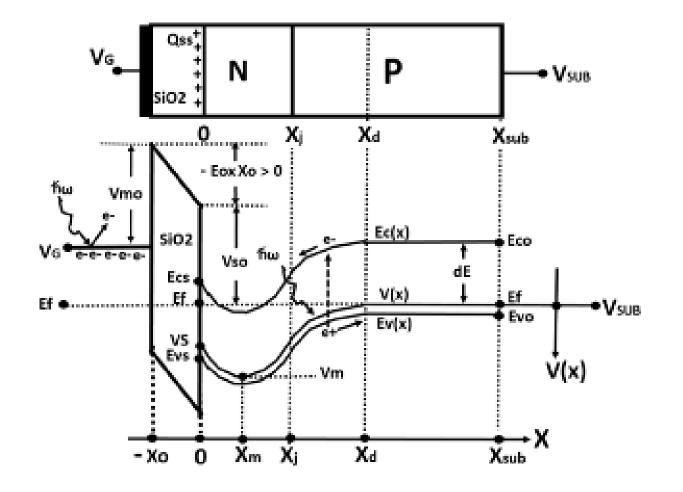
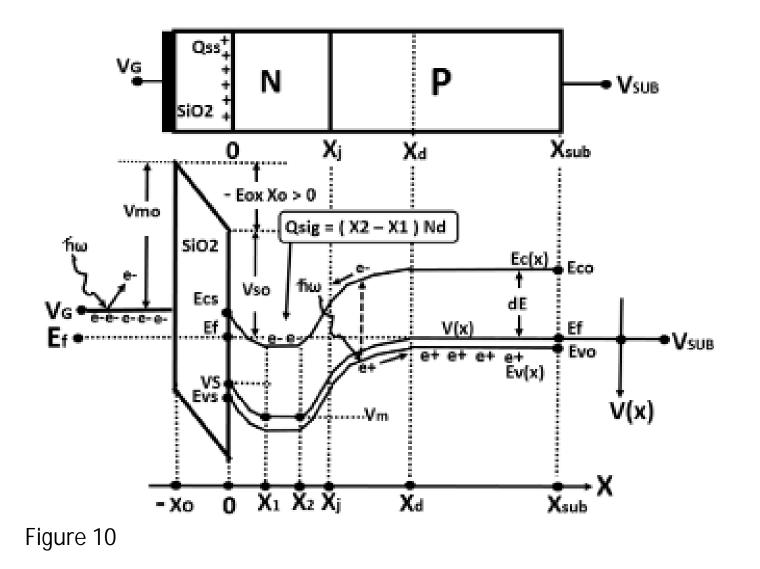


Figure 9

The NP junction type Buried Channel MOS Capacitor Structure at the dynamic operation mode when the buried channel layer is completely depleted of the majority carrier electrons.



The NP junction type Buried Channel MOS Capacitor Structure at the dynamic operation mode with the majority carrier mobile electrons present in the buried channel layer.

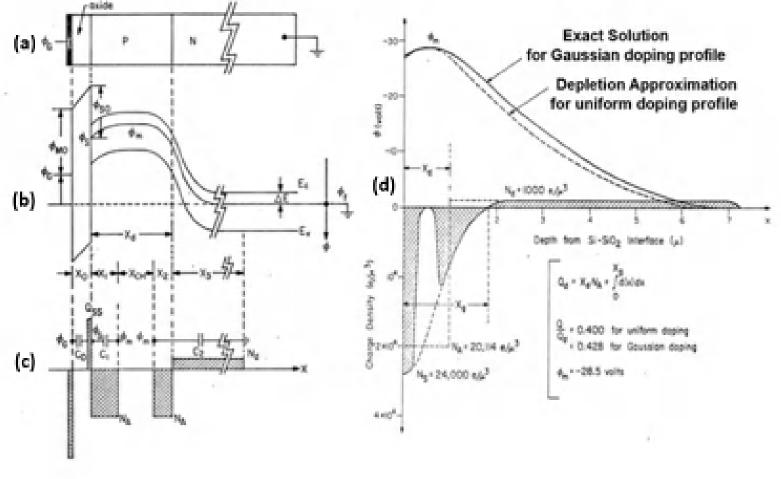


Figure 11

The electrostatic potential and the charge distribution in Buried Channel CCD with the Gaussian doping profile compared with the depletion approximation.

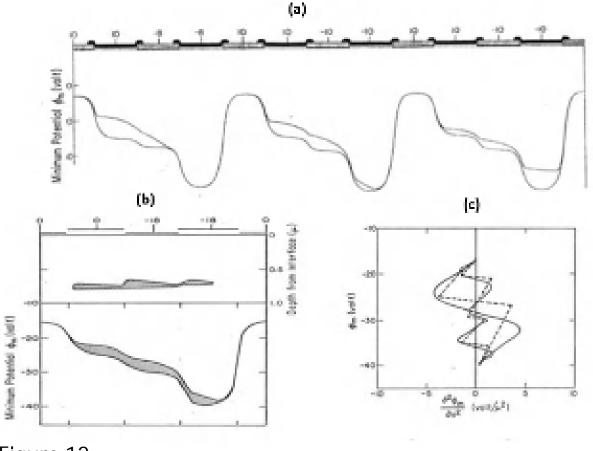


Figure 12

The electrostatic potential and the charge distribution in Buried Channel CCD obtained by time domain (t) and two dimensional (x, y) numerical computation solving simultaneously the Poisson Equation in the (x, y) domain and the continuity equation in the (t, x) domain.

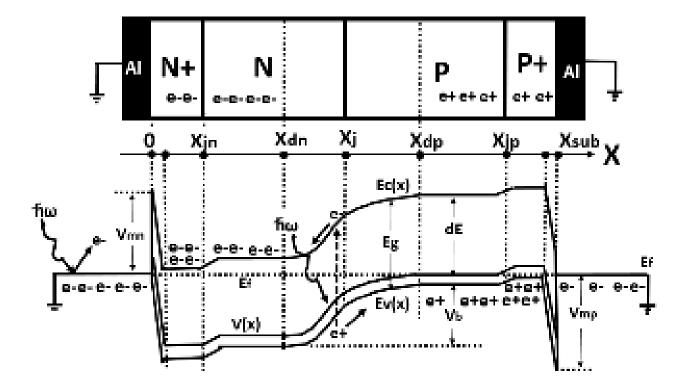
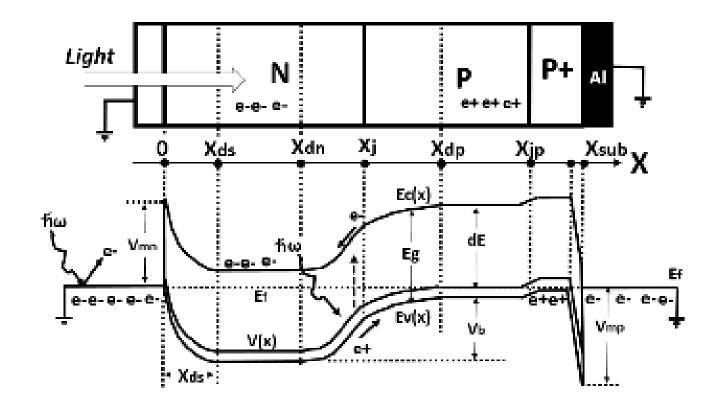


Figure 13

NP junction type photodiode at the thermal equilibrium with a heavily doped region in each side forming an Ohmic contact, pinned by the external aluminum metal terminal voltage. The charge carriers can pass thru the Schottky barrier by tunneling.





Schottky Barrier NP junction type photodiode with a transparent metal electrode with the N type buried channel charge collecting storage region at the thermal equilibrium

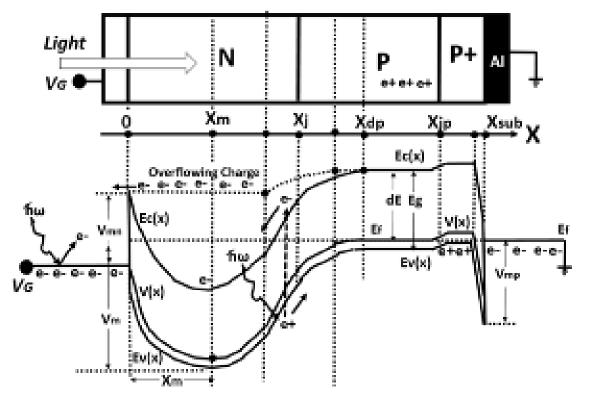


Figure 15

The NP junction type photodiode with the Schttky barrier with a transparent metal electrode, acting also as the overflow draining gate, and with the completely majority carrier depleted N type buried channel charge collecting storage region, by complete charge transfer with no image lag in the dynamic operation mode. When the N storage region is full, the excess charge can be drained by flowing over the Schottky barrier into the draining gate electrode.

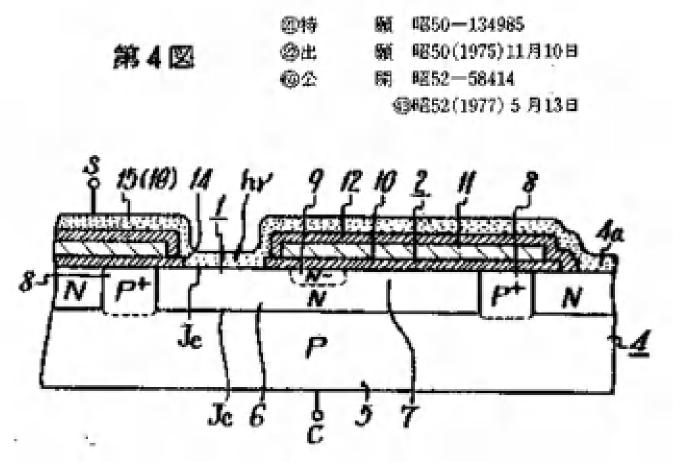


Figure 16

Schottky Barrier NP junction type Photodiode, drawn in Japanese Patent 1975-134985 by Hagiwara at Sony, used in Interline Transfer Buried Channel CCD image sensor.

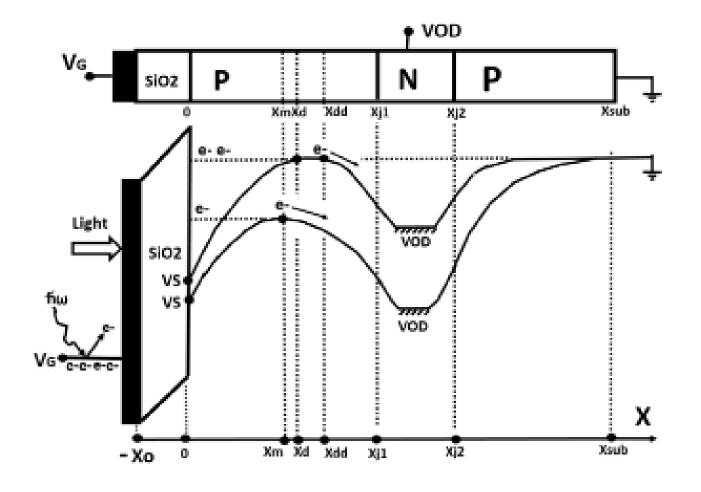


Figure 17

Surface Channel MOS Light Collecting Photo Capacitor with Buried Vertical Overflow Drain (VOD) protection

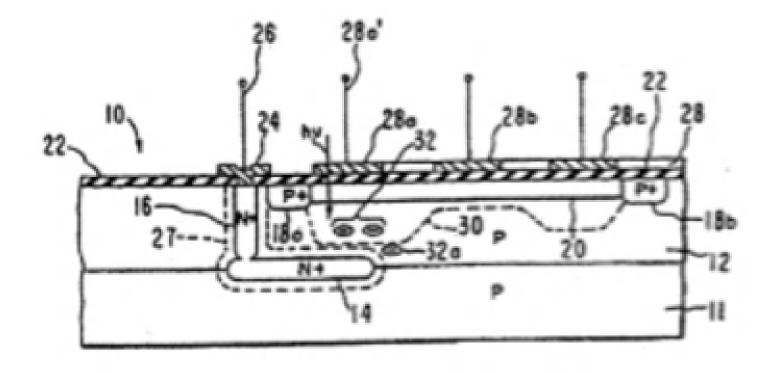


Figure 18

The Buried Vertical Overflow Drain (VOD) protection, drawn in the USA patent USP3896485 (July 22, 1975) by James M. Early at Fairchild, USA, applied in the Surface Channel CCD Image Sensor.

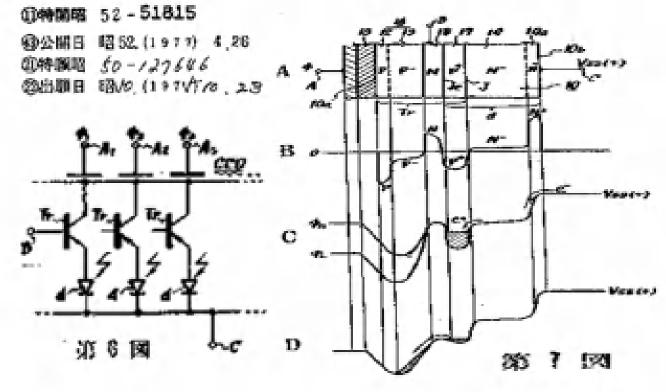


Figure 19

The N+N-P+ junction type Buried Photodiode, which has a charge collecting and storage buried P+ layer, drawn in Japanese Patent 1975-127646 (Oct 23, 1975) by Hagiwara at Sony, with a PNP bipolar transistor type Charge Transfer Gating (CTG) and with P-type Buried Channel MOS Capacitor used as the temporary storage buffer memory for Global Shutter operation in back light illumination scheme.

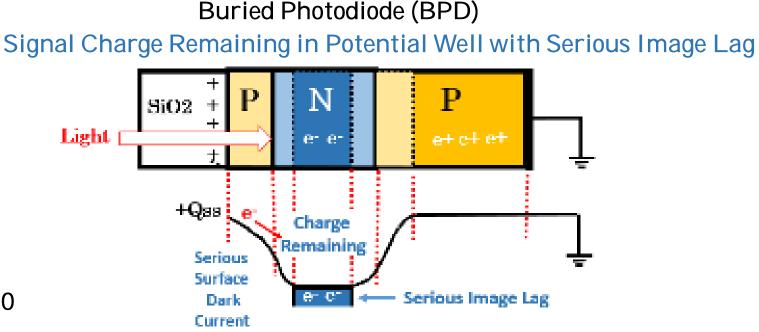


Figure 20

The original Buried Photodiode (BPD) invented by Hagiwara in Japanese Patent 1975-127646. The Buried Photodiode (BPD) is a simple PNP junction type photodiode that may still have the remaining electron charge in the charge collection region when reset, and also that the surface potential is not pinned. Therefore, the surface electric field and the surface fixed positive charge +Qss may generate the undesired serious dark current that degrades image output quality and also creates silicon chip yield problems. Buried Photodiode(BPD) is not by necessity Depletion Photodiode (DPD) that has no image lag. Moreover, Buried Photodiode (BPD) is not by necessity Pinned Photodiode (PPD) that has no dark current.

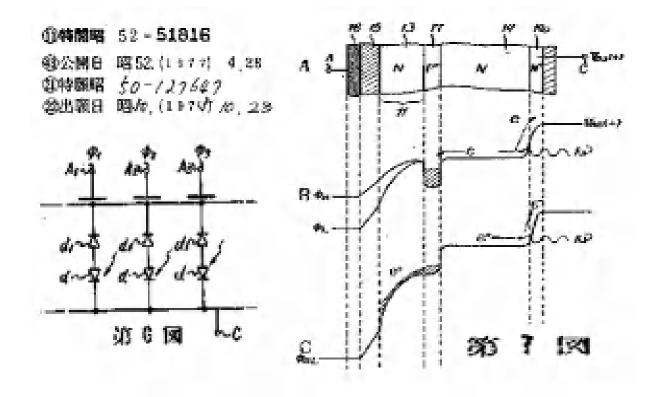
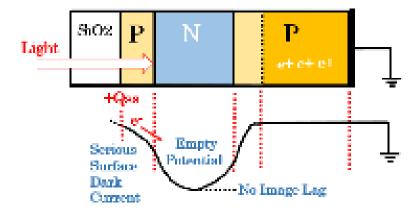


Figure 21

The N+NP+ junction type Depletion Photodiode, which is also a Buried Photodiode that has a charge collecting and storage buried P+ layer, drawn in Japanese Patent 1975-127647 (Oct 23, 1975) by Hagiwara at Sony, with N-type Surface Channel MOS Capacitor used as the temporary storage buffer memory for Global Shutter operation in back light illumination scheme.

Depletion Photodiode (DPD)

Completely Depleted Empty Potential Well with No Image Lag



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Figure 22
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The original Depletion Photodiode (DPD), drawn in Japanese Patent 1975-127647 by Hagiwara at Sony. Depletion Photodiode (DPD) is a Photodiode that has no remaining electron charge in the charge collection region when reset by the complete charge transfer operation. Hence there is no image lag in DPD. However the surface potential is by necessity not pinned. Therefore, the surface electric field and the surface fixed positive charge +Qss may generate the undesired serious dark current that degrades image output quality and also creates silicon chip yield problems. Depletion Photodiode (DPD) is by necessity Buried Photodiode (BPD). So, Depletion Photodiode (DPD) is not by necessity the Pinned Photodiode (PPD) that has no dark current.

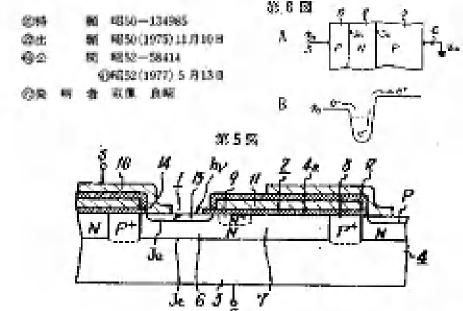


Figure 23

The Pinned photodiode with the heavily doped P+ surface layer, drawn in Japanese Patent 1975-134985 by Hagiwara at Sony, used for the Buried Channel Interline Transfer CCD image sensor. The surface hole accumulation layer is shown to have such a very heavily doped P+ region that can have a fixed or Pinned potential by the external metal Ohmic contact by option. The charge collecting region is a buried layer under the P+ surface layer. Hence, this is also a Buried Photodiode. The buried N type base region in the PNP junction type photodiode structure has the same doping level of the lightly doped buried channel CCD, and can be completely depleted of the signal charge to the adjacent buried channel CCD type readout charge transfer device (CTD) by the complete charge transfer so that we have no image lag picture. Hence this is also a Depletion Photodiode with complete charge transfer mode.

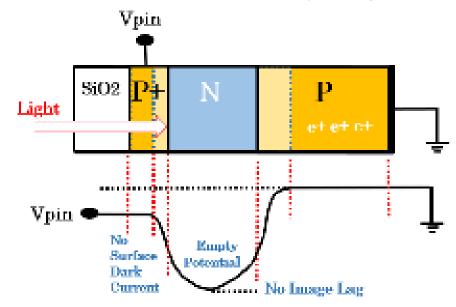


Figure 24

Pinned Photodiode (PPD), invented by Hagiwara in Japanese Patent 1975-134985, is a simple P+NP junction type Depletion Photodiode (DPD), which is also a Buried Photodiode (BPD) that has no remaining electron charge in the charge collection region by the complete charge transfer operation when reset. The surface potential is pinned by the heavily doped P+ hole accumulation surface layer. This is the original invention of SONY Hole Accumulation Diode (SONY HAD). There is no surface electric field and the surface fixed positive charge +Qss is quenched so that we do not suffer the undesired serious surface dark current that degrades the image output quality and also creates the serious chip yield problems. Pinned Photodiode (PPD) is by necessity Depletion Photodiode (DPD) and also by necessity Buried Photodiode (BPD).

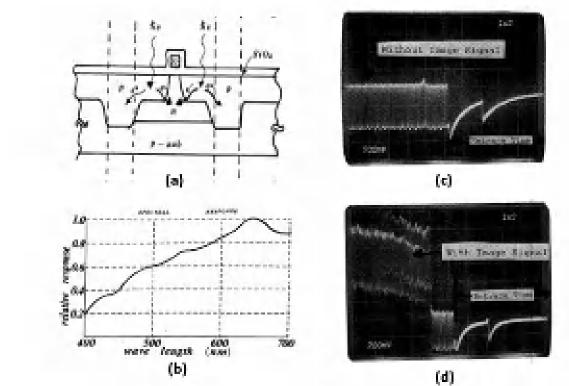


Figure 25

The original Pinned window (a) with the heavily doped P+ Pinned Surface potential connected to the substrate voltage by option with excellent blue light sensitivity (b). The P+NP junction type Pinned Photodiode with the self-aligned boron atom ion implantation, forming the P+ hole accumulation layer at the silicon surface to quench the surface dark current as shown in (c) and (d). See "A 380Hx488V CCD imager with narrow channel transfer gates," by Y. Daimon-Hagiwara, M. Abe, and C. Okada, Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Applied Physics , vol. 18, supplement 18–1, pp. 335–340, 1979

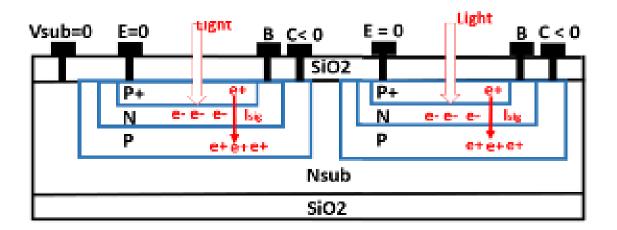


Figure 26a

Conventional Phototransistor in 1948. John Northrup Shive (February 22, 1913 – June 1, 1984) is best known for inventing this phototransistor in 1948 (a device that combines the sensitivity to light of a photodiode and the current gain of a transistor). But he also produced experimental evidence that holes could diffuse through bulk germanium, and not just along the surface as previously thought. This paved the way from Bardeen and Brattain's point-contact transistor to Shockley's more-robust junction transistor.

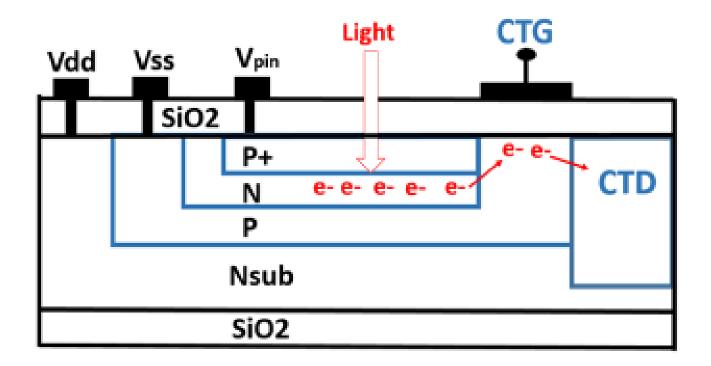


Figure 26b

Dynamic Phototransistor with Floating Base used as Signal Charge Storage Region, the original form of the P+NPNsub junction type Pinned Photodiode invented by Hagiwara at Sony in 1975. See Japanese Patent 1975-134985.

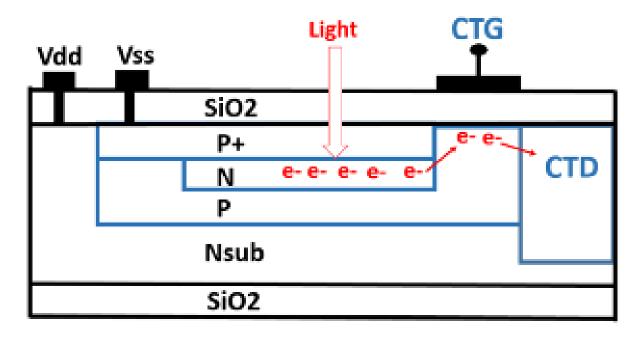


Figure 26c

Dynamic Phototransistor with Floating Base used as Signal Charge Storage Region, the P+NPNsub junction type Pinned Photodiode with the Pinned Window with the Pinned surface Ppotentail of the P+ hole accumulation layer pinned directly by the substrate voltage. This is the SONY original Hole Accumulation Diode (SONY HAD) invented by Hagiwara at Sony in 1975. See also the paper "A 380Hx488V CCD imager with narrow channel transfer gates," by Y. Daimon-Hagiwara, M. Abe, and C. Okada, Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Applied Physics, vol. 18, supplement 18–1, pp. 335–340, 1979

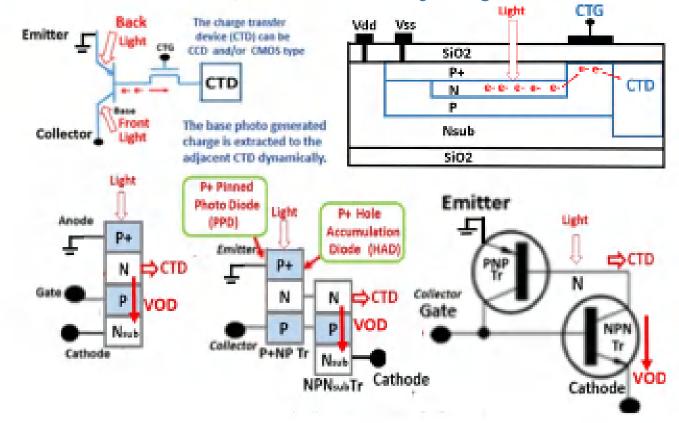


Figure 27

The P+NPNsub junction type Thyristor structure for the light collecting device, invented by Hagiwara in Japanese Patent 1975-134985, which is also the P+NP junction type Pinned Photodiode (PPD), Since this is a P+NPNsub junction type Thyristor structure which has a variety of device operation modes that includes the Thysistor punch thru action mode that can be applied for the vertical overflow drain (VOD) function controlling the overflowing signal charge at the high light beam.

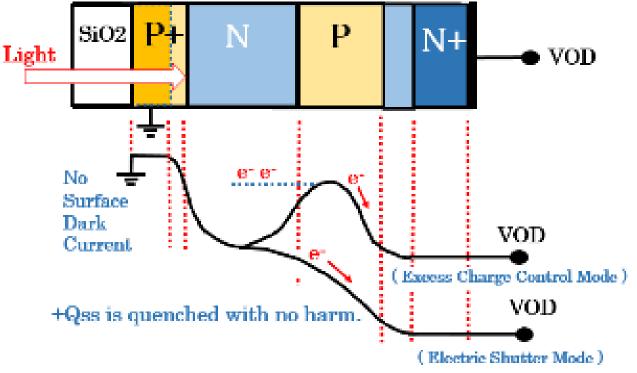


Figure 28

The P+NPwell/Nsub junction type Pinned Photodiode (PPD), invented by Hagiwara in Japanese Patent 1975-134985, is also by necessity a Depletion Photodiode (DPD) and also by necessity a Buried Photodiode (BPD). Since this is a P+NPwell/Nsub junction type Thyristor structure which has a variety of device operation modes that includes the Thysistor punch thru mode that can be applied for the vertical overflow drain (VOD).

Figure 29 P+NP/Sub junction type Pinned Photo Diode

invented by Hagiwara at Sony in Japanese Patent 1975-134985.

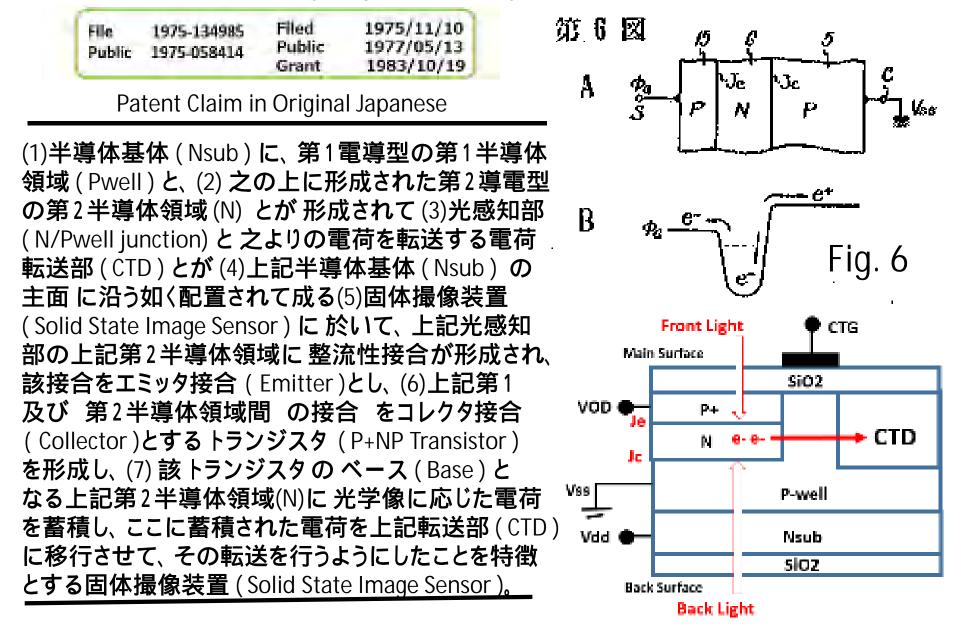


Figure 30 P+NP/Sub junction type Pinned Photo Diode

invented by Hagiwara at Sony in Japanese Patent 1975-134985.

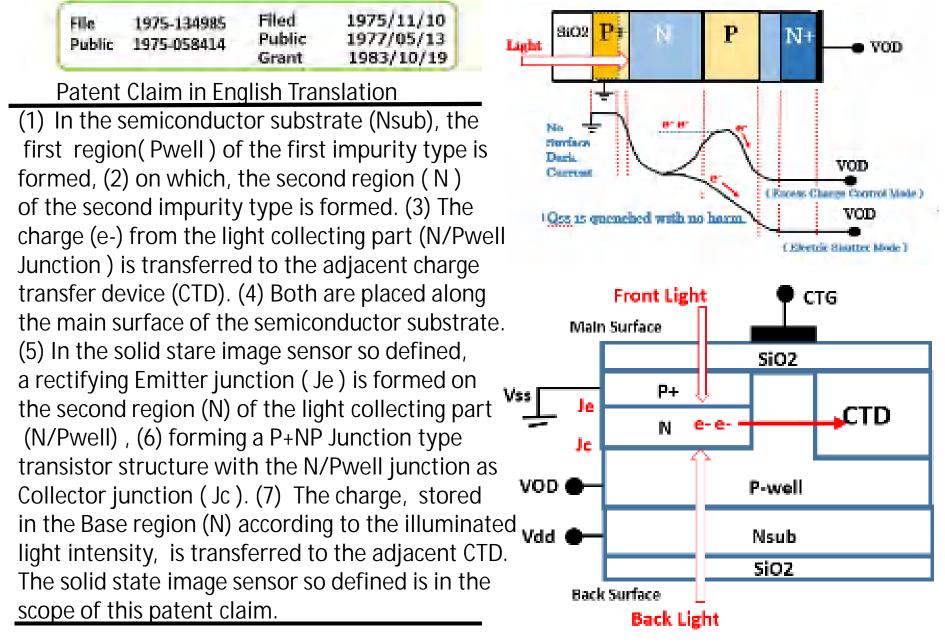
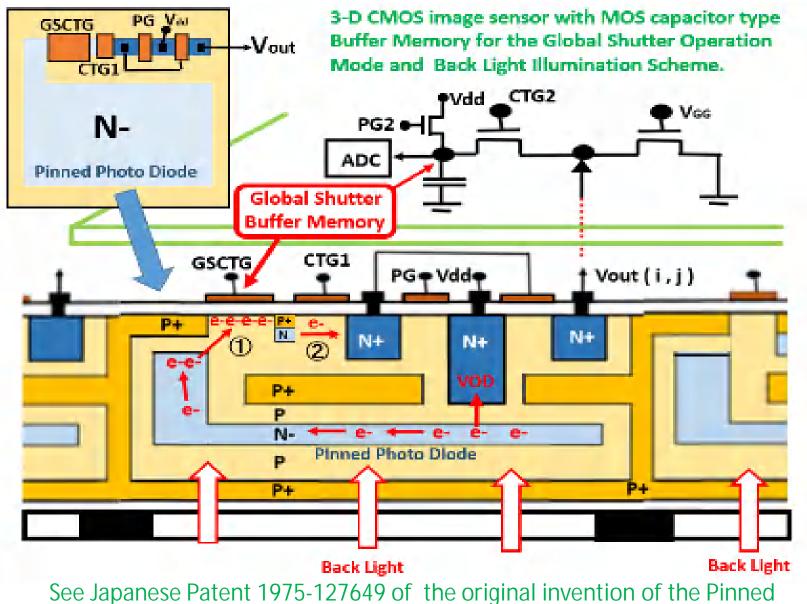


Figure 31



Photodiode by Yoshiaki Hagiwara at Sony in 1975. The visible light cannot penetrate more than $12 \,\mu m$ into the silicon crystal. We do not need blinds.

