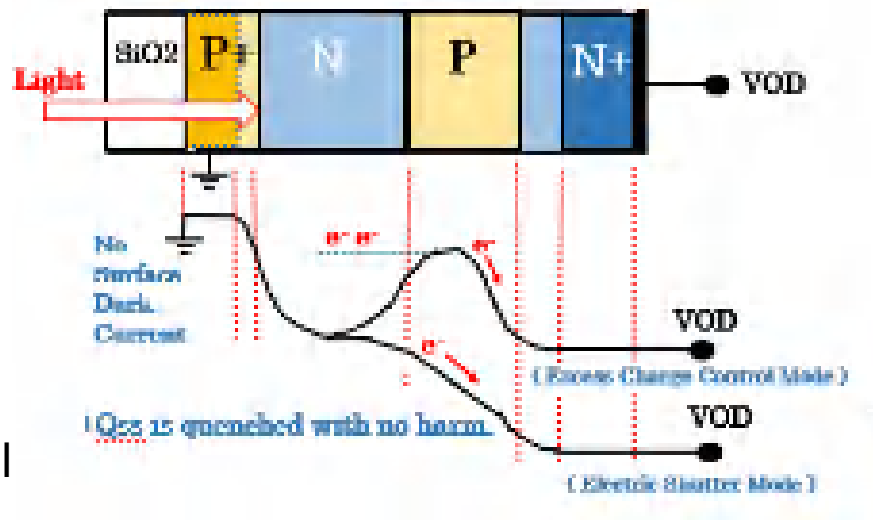
P+NP/Sub junction type Pinned Photo Diode

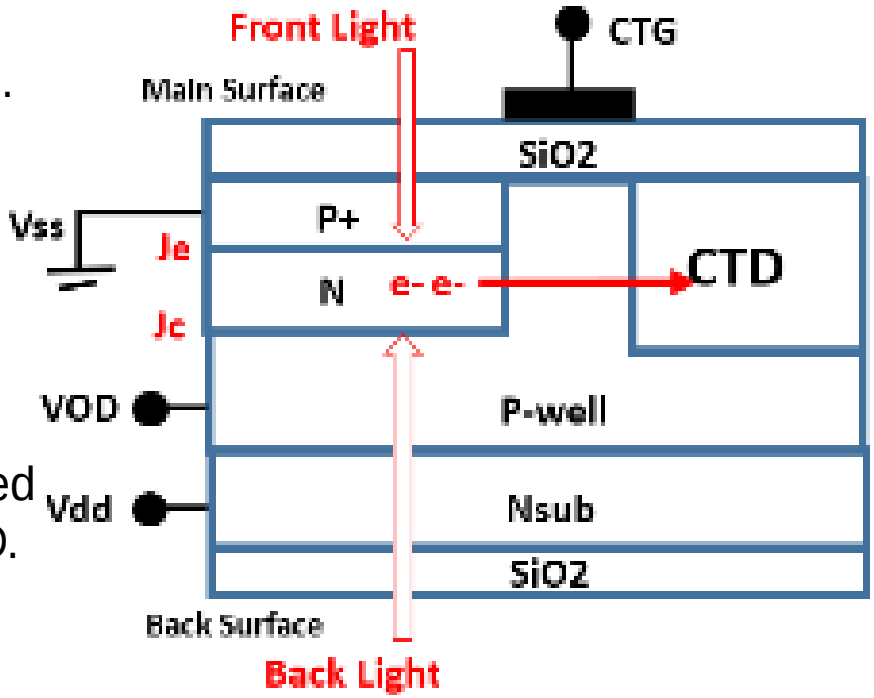
invented by Hagiwara at Sony in Japanese Patent 1975-134985.

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

Patent Claim in English Translation

(1) In the semiconductor substrate (Nsub), the first region(Pwell) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N/Pwell Junction) is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N/Pwell) , (6) forming a P+NP Junction type transistor structure with the N/Pwell junction as Collector junction (Jc). (7) The charge, stored in the Base region (N) according to the illuminated light intensity, is transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.





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Patent Claim in Original Japanese

(1)半導体基体 (Nsub) に、第1電導型の第1半導体領域 (Pwell) と、(2) 之の上に形成された第2導電型の第2半導体領域 (N) とが 形成されて (3)光感知部 (N/Pwell junction) と 之よりの電荷を転送する電荷転送部 (CTD) とが (4)上記半導体基体 (Nsub) の主面 に沿う如く配置されて成る(5)固体撮像装置 (Solid State Image Sensor) に 於いて、上記光感知部の上記第2半導体領域に 整流性接合が形成され、該接合をエミッタ接合（Emitter)とし、(6)上記第1及び 第2半導体領域間 の接合 をコレクタ接合（Collector)とするトランジスタ (P+NP Transistor) を形成し、(7) 該トランジスタ の ベース (Base) となる上記第2半導体領域(N)に 光学像に応じた電荷を蓄積し、ここに蓄積された電荷を上記転送部 (CTD) に移行させて、その転送を行うようにしたことを特徴とする固体撮像装置 (Solid State Image Sensor)。

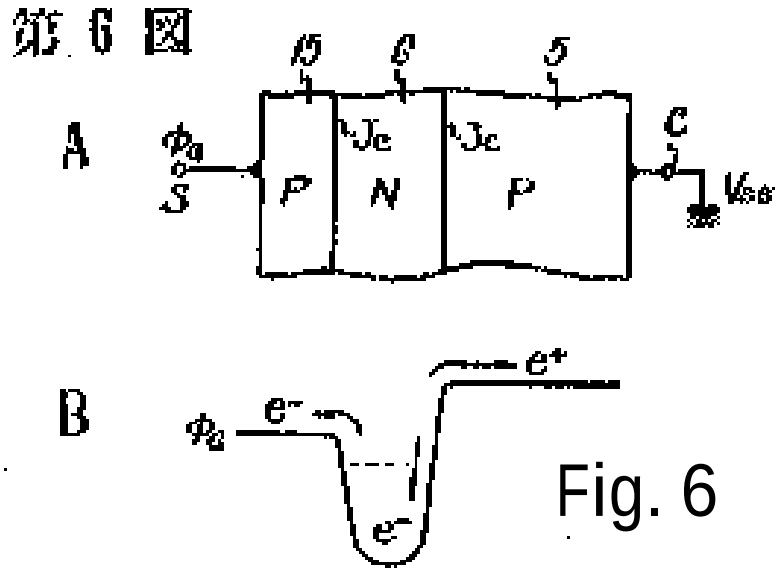

Fig. 6