Pinned Photo Diode

Yoshiaki Hagiwara at Sony invented the Pinned Photo Diode in 1975.
Pinned Photo Diode is identical to SONY HAD (Hole Accumulation Diode).
Please Visit http://www.aiplab.com/

For the original document, visit and search the Japanese Official Patent Web:
https://www4.j-platpat.inpit.go.jp/eng/tokujitsu/tkbs_en/TKBS_EN_GM101_Top.action
and put documentation numbers 1975-134985, 1975-127647 and 1975-127646.

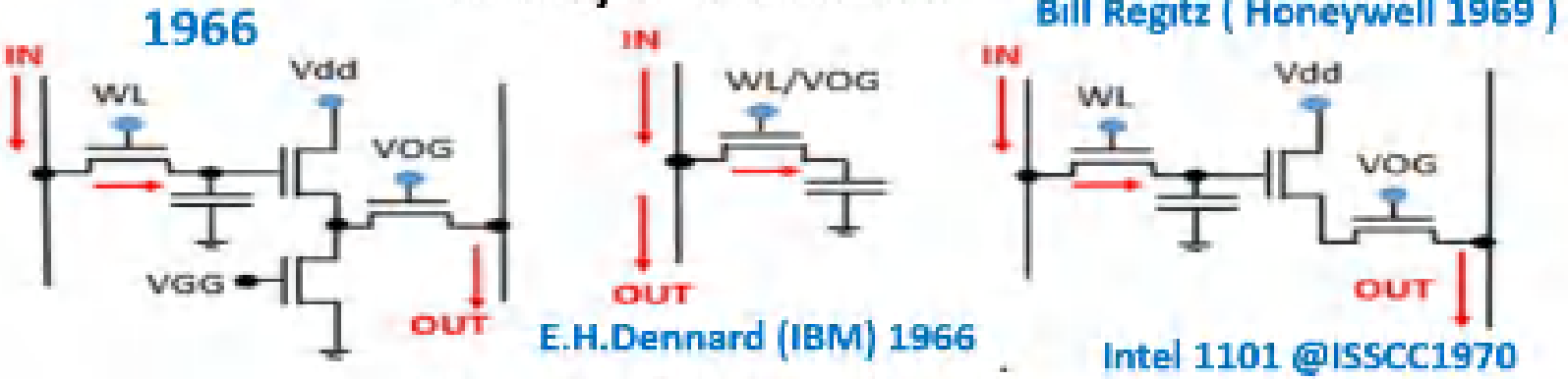
Multi-functionality of Image Sensors

Sony HAD (Sony Hole Accumulation Diode) is the Pinned Photo Diode (PPD) with VOD. See Hagiwara 1975 invention of Japanese Patent 1975-134985

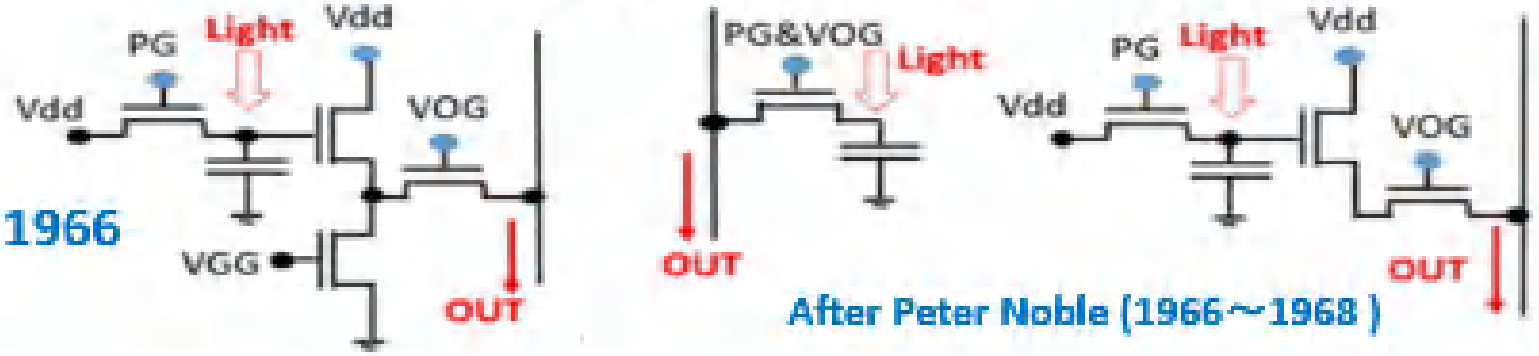
Comparison of Various Light Detecting Photo Sensor Structures

feature \ type	Classical N+Psub Diode Sensor	SCCD type MOS Sensor	BCCD type MOS Sensor	Yamada 1978 NPNsub Diode Sensor	Teranishi 1980 P+NP Diode Sensor	Hagiwara 1975 P+NPNsub Sony HAD Sensor
Blue Sensitivity	○	X	X	○	◎	◎
Low Image Lag	X	◎	◎	X	◎	◎
Surface Dark Current	X	X	X	X	◎	◎
Surface Trap Noise	X	X	◎	X	◎	◎
Vertical OFD (VOD)	X	X	X	◎	X	◎
Global Shutter Function with a buffer memory	○	◎	◎	○	○	○
		(CCD does not need extra buffer memory)			(PPD)	(PPD with VOD)

History of DRAM Cell



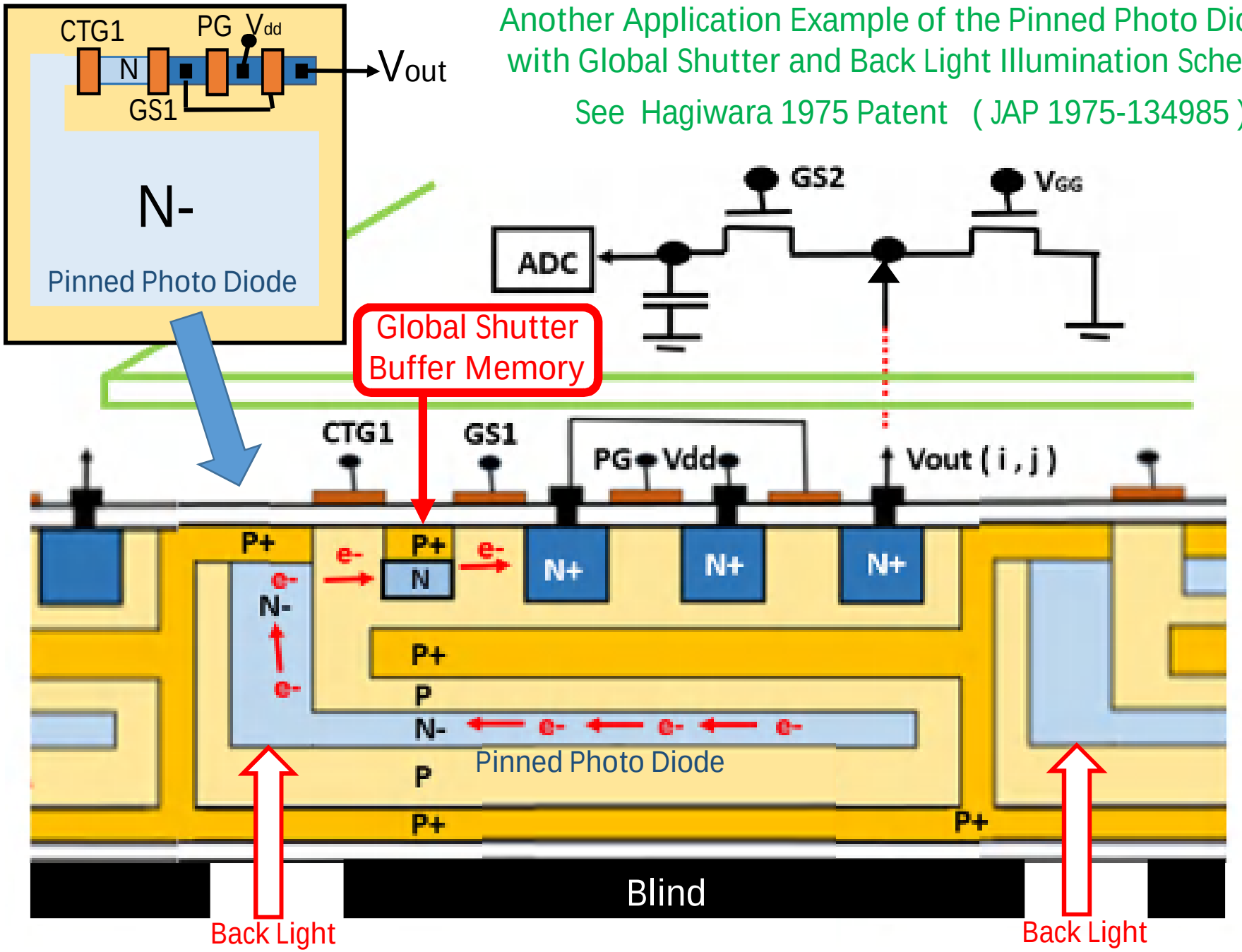
History of Photo Diode Cell



Engineers in 1960s working on the classical MOS image sensors, already knew the source follower type active pixel circuit photo diode by Peter Noble 's invention. From 1970 to 2000, CCD was a Super Star because CCD has a very low image lag feature , and does not need any extra buffer memory for the global shutter function, while MOS imagers needed an extra expensive buffer memory and this active source follower type amplifier circuit in each pixel. We all knew it !! Nothing is new about the CMOS image sensors with the active pixel circuit and the buffer memory for global shutter.

Another Application Example of the Pinned Photo Diode with Global Shutter and Back Light Illumination Scheme

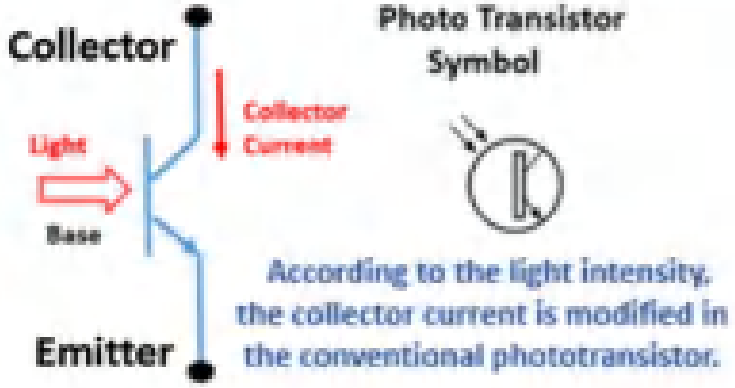
See Hagiwara 1975 Patent (JAP 1975-134985)



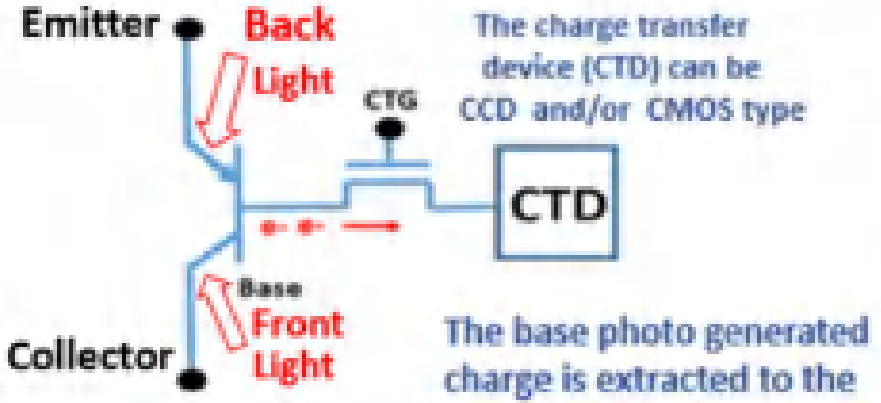
Pinned Photo Diode (PNP/Sub junction type)

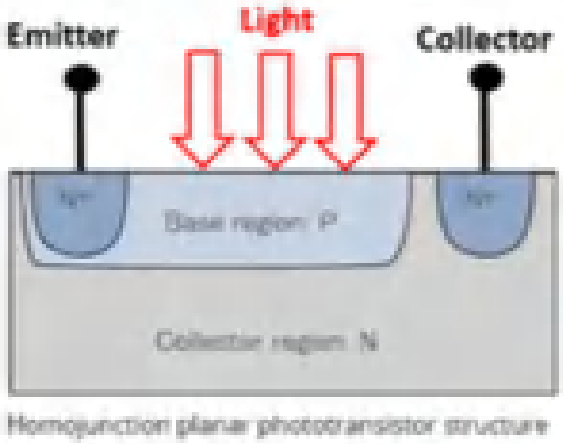
See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

Conventional Static Photo Transistor of PNP junction type



Dynamic Photo Transistor Operation proposed by Hagiwara Sony in 1975





Homojunction planar phototransistor structure

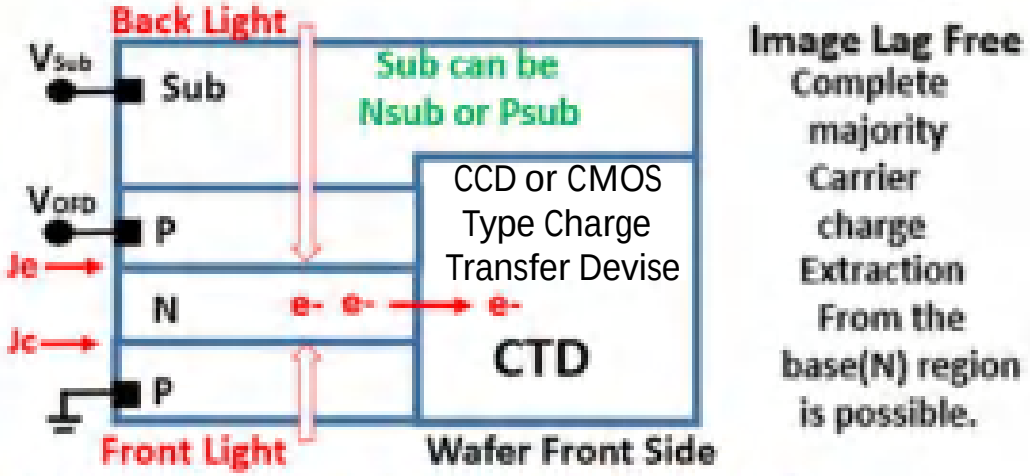


Image Lag Free Complete majority Carrier charge Extraction From the base(N) region is possible.

PNP/Sub junction type Pinned Photo Diode

Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

with vertical overflow drain (VOD) function
including back light illumination scheme

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

A Pinned Photo Diode defined in the Patent Claims

Basic Sensor Structure defined in this Patent

Fig. 6 A

第 6 図

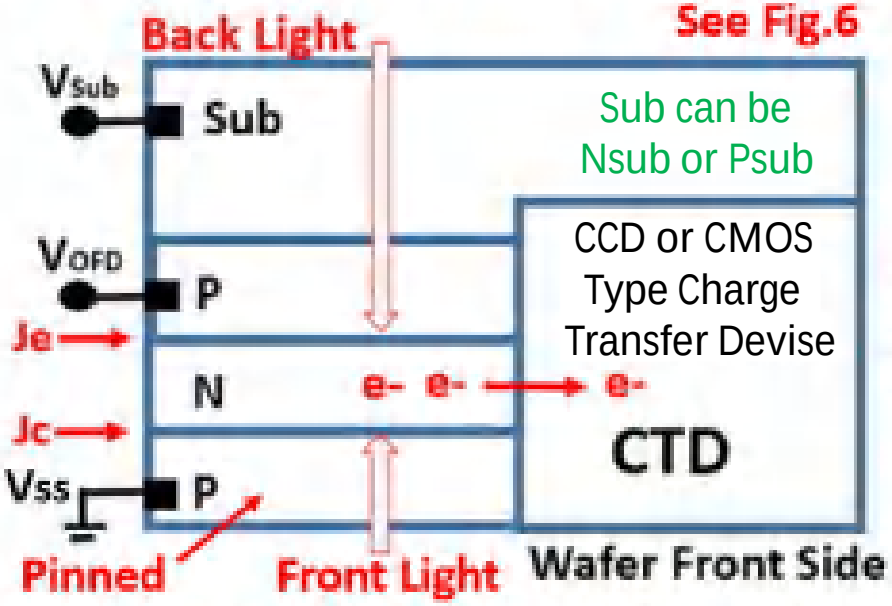
e- = electron e+ = hole

B

Empty Potential Well with completely majority-carrier depleted base signal charge storage area.

Structure defined for Upside-Down Wafer

See Fig.6



The basic P/N/P/Sub junction (thyristor) type Photo Sensor can have various kinds of Vertical Overflow Drain(VOD) functions.

Fig. 4

Example of VOD Schottky Barrier type Photo Diode in IT CCD sensor Application

第 4 図

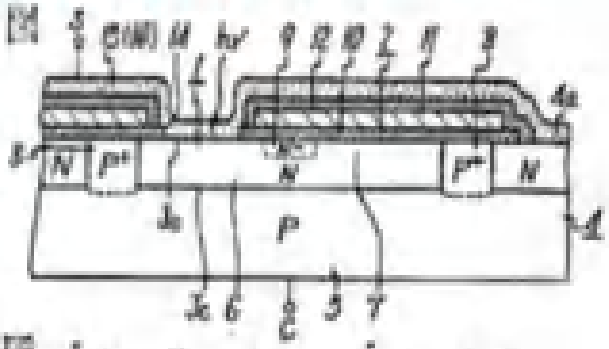
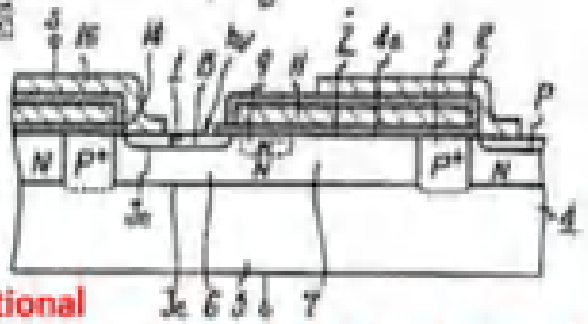


Fig. 5

Example of VOD P+NPsub Junction type Photo Diode in IT CCD sensor Application

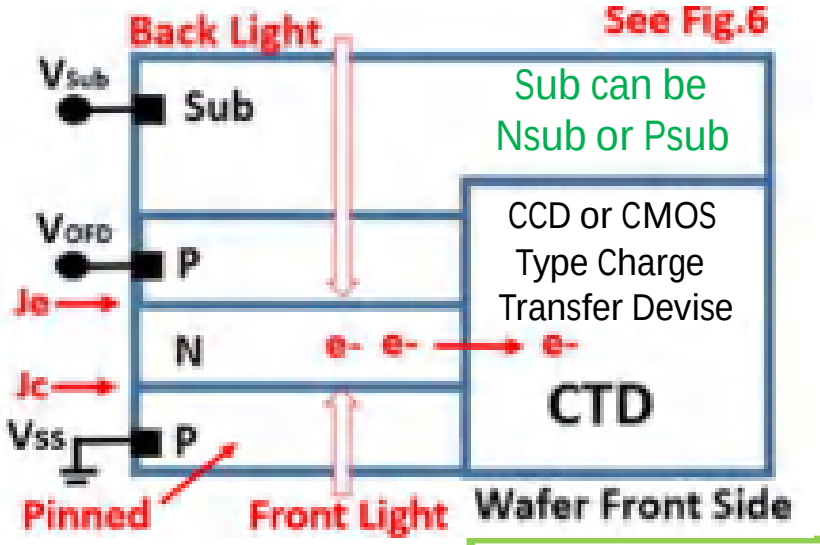
第 5 図

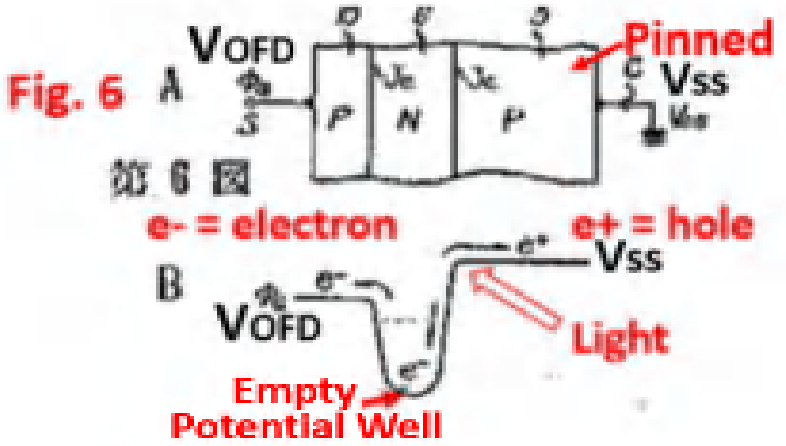


Metal Contact is optional

This patent structure can include both the back and front light illumination schemes.

PNP/Sub Junction type Pinned Photo Diode





English Translation of the Patent Clams

This Japanese Patent 1975-134985 shown here is the evidence to claim that the Pinned Photo Diode with the vertical overflow drain (VOD) function was invented by Yoshiaki Daimon Hagiwara at Sony in 1975.

(1) In the semiconductor substrate (Sub)
(2) the first region (P) is formed,
(3) and the second region (N) is formed upon on the first region (P),
(4) forming the photo sensing part (NP).
(5) The charge from this (NP) is transferred to the charge transfer device (CTD),
(6) which is formed along the front surface of the semiconductor substrate (Sub).
(7) In the so-defined image sensing device,
(8) on the second region (N) of the photo sensing part (NP),
(9) a rectifying junction (PN) is formed.
(10) Let this junction(PN) be called an emitter junction (Je).
(11) Let the junction between the first region(N) and the second region (P)
(12) be called as the collector junction (Jc) forming a transistor (PNP).
(13) In the second region (N) , which is the base of the said transistor (PNP),
(14) according to the optical image, the electronic charge (e-) is stored.
(15) The electronic charge (e-) , stored in here (N) , is transferred to the said CTD.
(16) the image sensor structure with such a charge transfer operation
(17) with the features explained above is in the scope of this patent claim.

Pinned Photo Diode (PNP/Sub junction type)

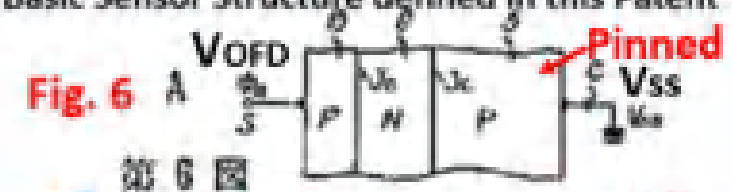
See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

with vertical overflow drain (VOD) function
including back light illumination scheme

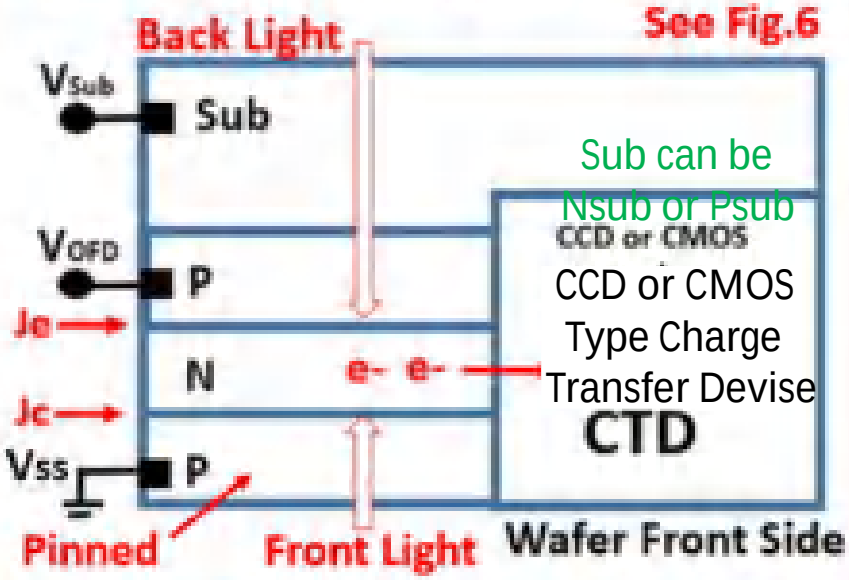
File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

A Pinned Photo Diode defined in the Patent Claims

Basic Sensor Structure defined in this Patent



Structure defined for Upside-Down Wafer



The basic P/N/P/Sub junction (thyristor) type Photo Sensor can have various kinds of Vertical Overflow Drain(VOD) functions.

This patent structure can include both the front and back light illumination schemes.

Patent Claims in Japanese 特許請求範囲

(1) 半導体基体(Sub)に
(2) 第1伝導型の第1半導体領域(P)と
(3) この上(P)に形成された第2伝導型の第2半導体領域(N)
(4) とが形成されて光感知部(NP)と
(5) これ(NP)よりの電荷を転送する電荷転送部(CTG)とが
(6) 上記半導体基体(Sub)の主面に沿う如く配置されて成る
(7) 固体撮像装置に於いて
(8) 上記光感知部(NP)の上記第2半導体領域(N)に
(9) 整流性接合(PN)が形成され、
(10) 該接合(PN)をエミッタ接合(Je)とし、
(11) 上記第1(P)及び第2半導体(N)間の接合を
(12) コレクター(Jc)とするトランジスタ(PNP)が形成し、
(13) 該トランジスタ(PNP)のベースとなる
上記第2半導体領域(N)に
(14) 光学像に応じた電荷を蓄積し、
(15) ここに蓄積された電荷を上記転送部(CTD)に移行させて、
(16) その転送を行うようにしたことを
(17) 特徴とする固体撮像装置

Pinned Photo Diode (PNP/Sub junction type)

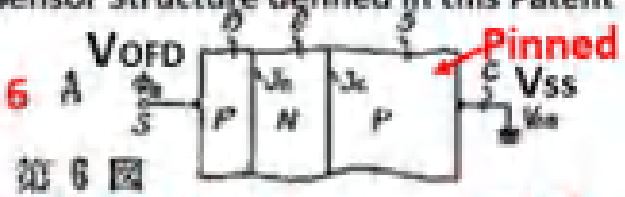
See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

with vertical overflow drain (VOD) function
including back light illumination scheme

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

A Pinned Photo Diode defined in the Patent Claims

Basic Sensor Structure defined in this Patent

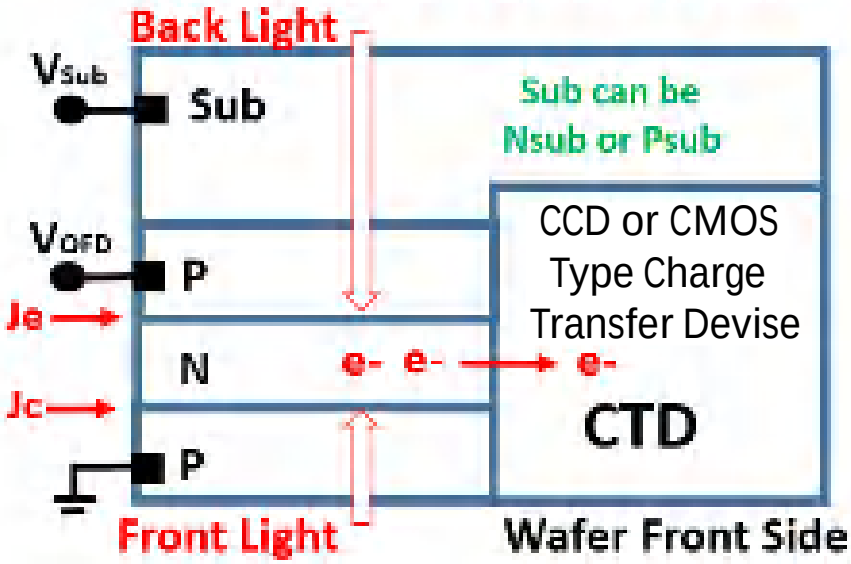


e- = electron e+ = hole

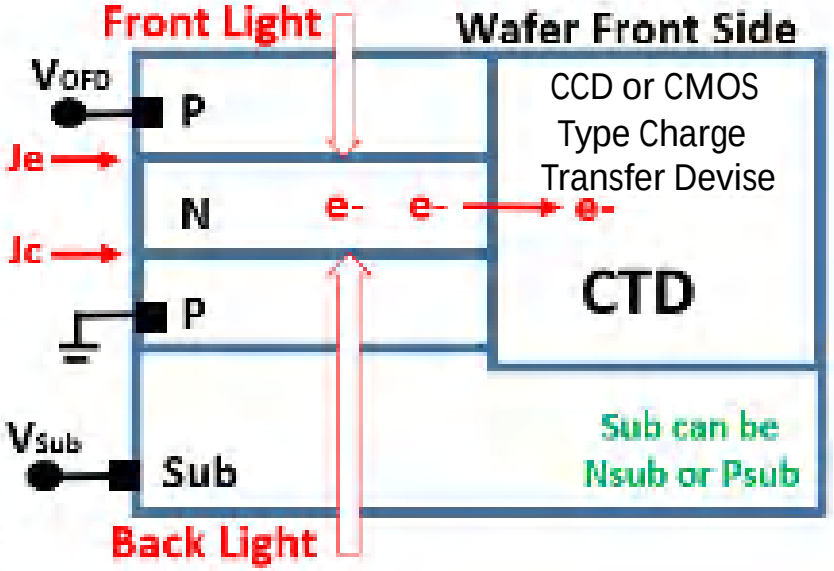
Empty Potential Well with completely majority-carrier depleted base signal charge storage area.

The basic P/N/P/Sub junction (thyristor) type Photo Sensor can have various kinds of Vertical Overflow Drain(VOD) functions.

(a) Structure define for Up-Side Down wafer



(b) Structure define for Up-Side Up wafer



This patent structure can include both the back and front light illumination schemes.

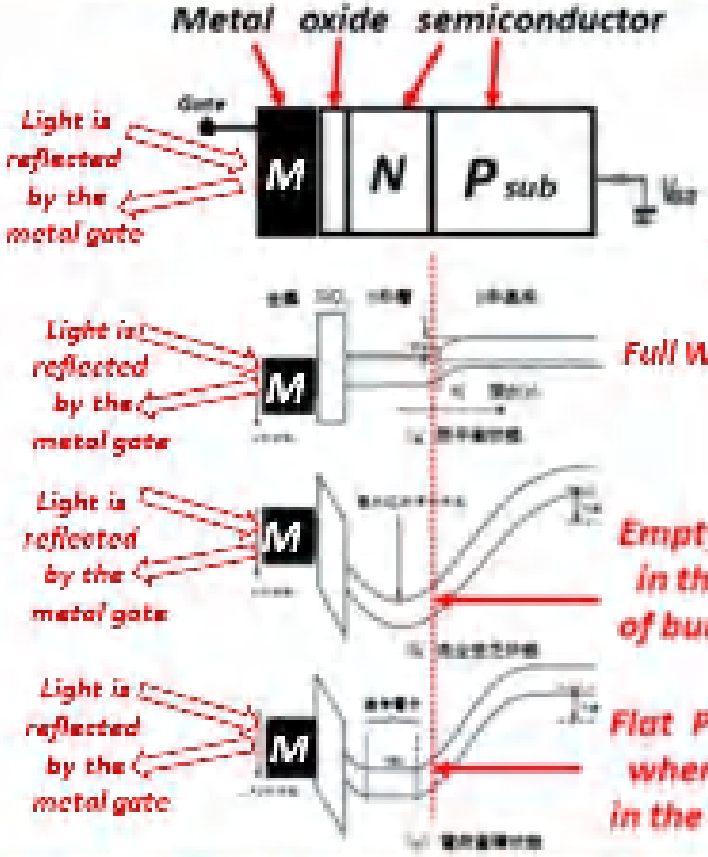
The evidence that Hagiwara at Sony is the inventor of the pinned photo diode.

See Fig.6 of Y. Hagiwara, Japanese Patent App 50 - 134985,

Conventional Buried Channel CCD

empty potential well

Buried Channel Type CCD MOS capacitance

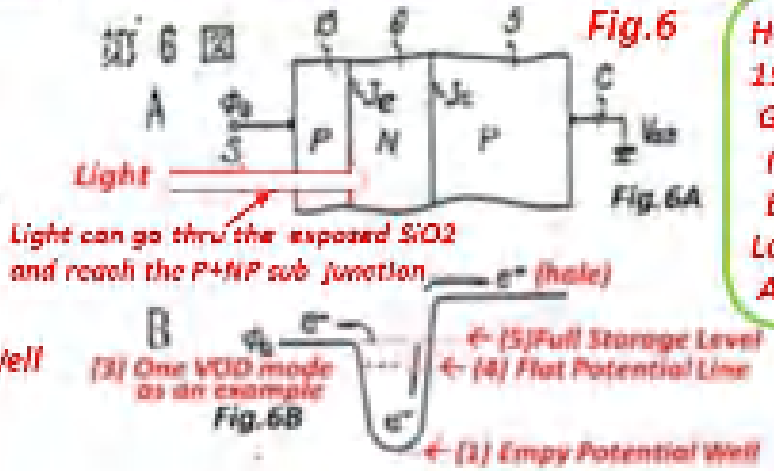


CCD type light sensing structure has poor light sensitivity

Pined Photo Diode (Hagiwara 1975 invention)

empty potential well

PNP junction transistor capacitance



Hagiwara Diode 1975 Photo Sensor, Good sensitivity, No Image Lag, Built-in VOD, Low dark current And Low Noise.

Hagiwara in 1975 drew an empty potential well in the empty base N storage layer of the dynamic PNP transistor capacitance for the first time in the world in 1975.

In 1975, Hagiwara drew for the first time in the world the empty potential well curve in Pinned Photo Diode.

Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

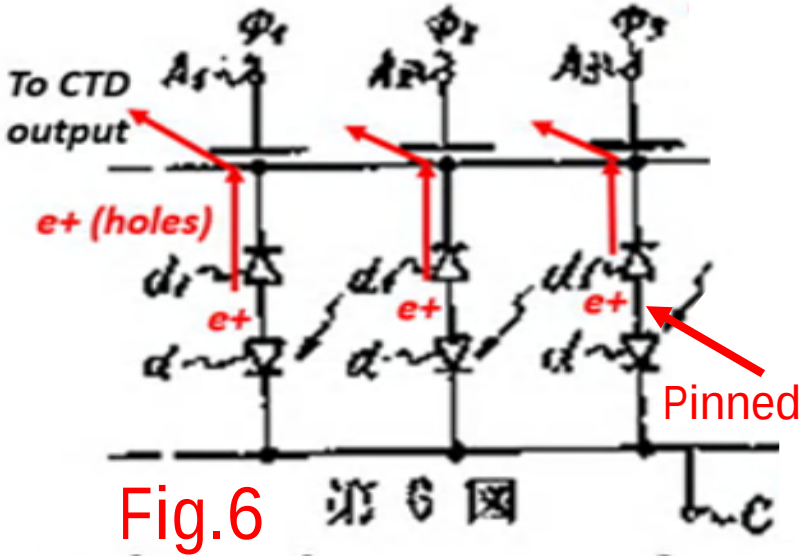


Fig.6 第 6 図

with Vertical Complete Charge Transfer Function.

File	1975-127647	Filed	1975/10/23
Public	1975-051816	Public	1977/04/26

NPN junction type Pinned Photo DIode

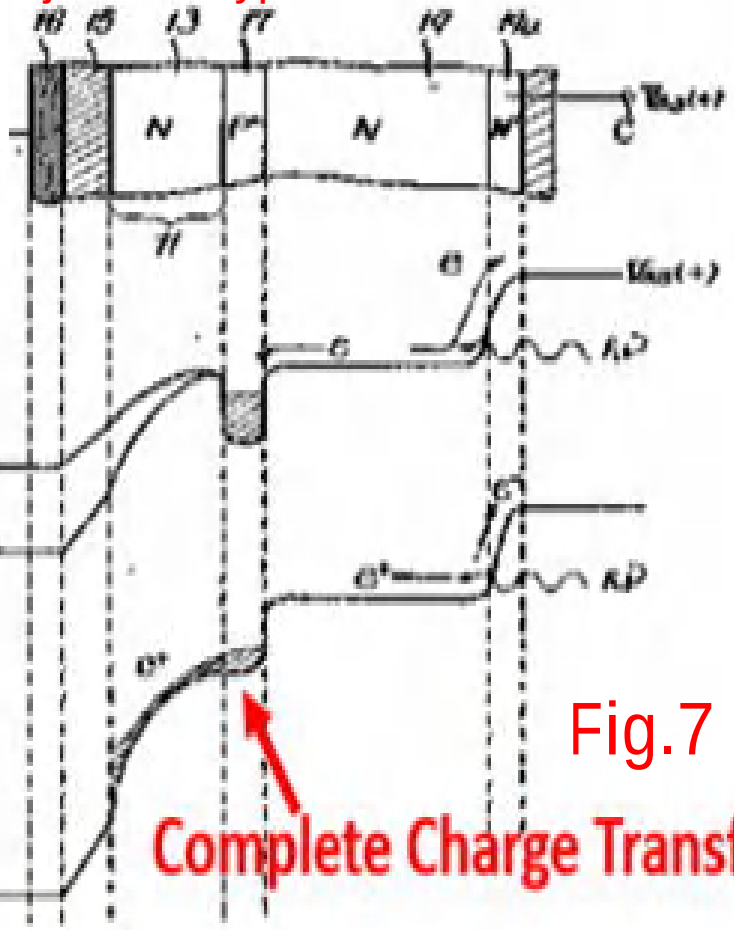
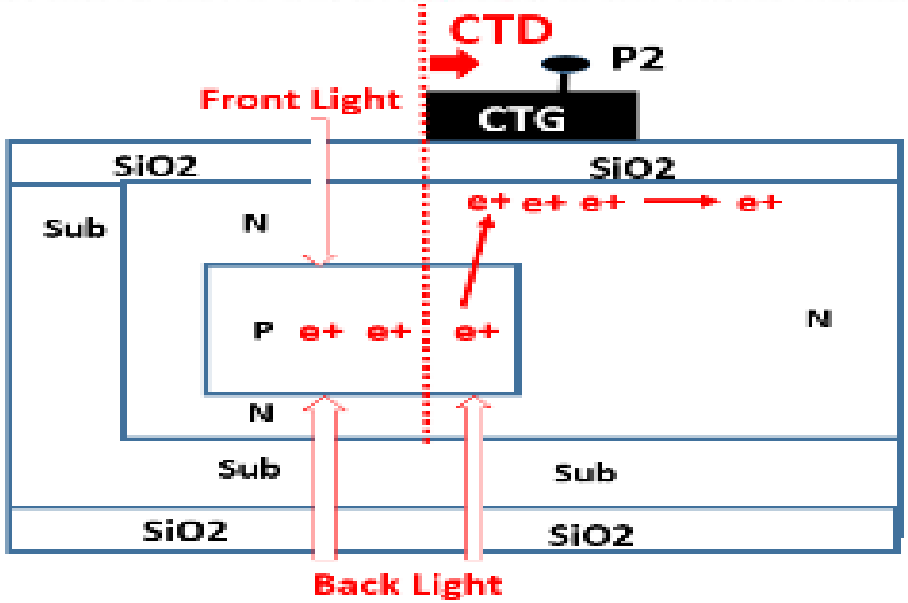


Fig.7

Complete Charge Transfer

A Pinned Photo Diode defined in the Patent Claim



Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

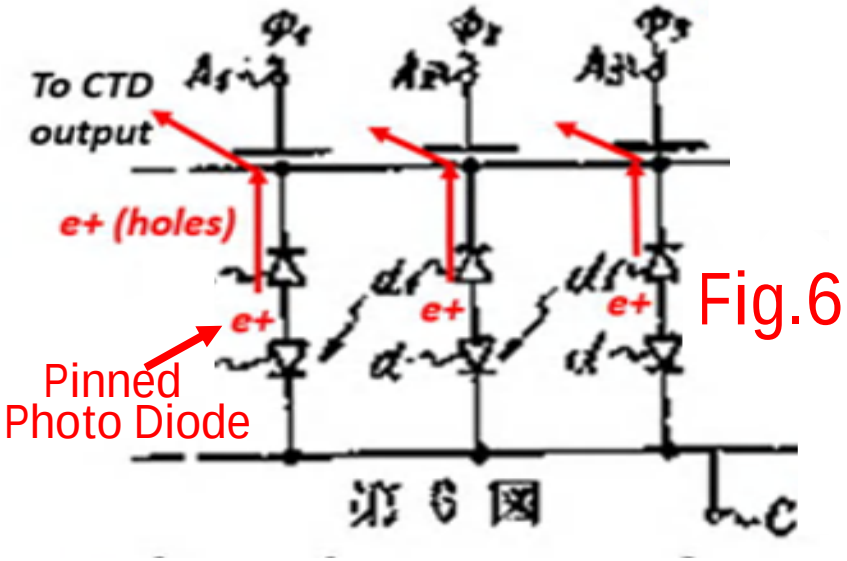
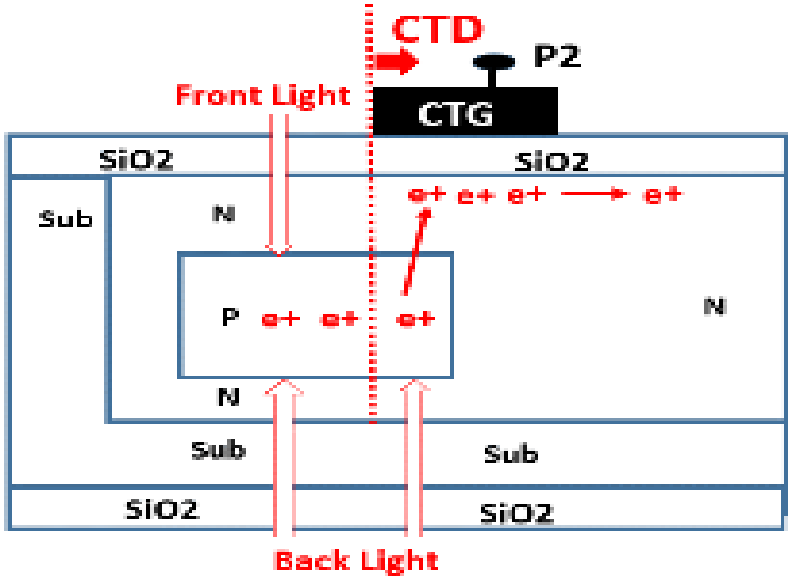


Fig.6

The Pinned Photo Diode Structure defined in this Patent Claim



Patent Claim in English Translation

(1) Along the main surface of the silicon substrate die (Sub),
(2) the charge transfer gate (CTG) is formed upon the oxide layer (SiO2).
(3) whereby the first region (N) is formed for charge transferring area (CTD).
(4) On the other side of the silicon substrate die (Sub),
(5) another region (P) is formed nearby the charge transferring area (CTD).
(6) The region (P) and the nearby first region (N) together
(7) form a photo sensing area (NPN junction).
(8) By applying a proper pulse (P1) onto the charge transfer gate (CTG),
(9) the charge (e+) stored in the photo sensing area (PNP junction) is transferred to the charge transfer area (CTD).
(10) And upon the said transfer gate (CTG),
(11) a different type of clock pulse (P2) is applied, which is different from the previous pulse (P1).
(12) Along the main surface of the silicon substrate die (Sub)
(13) the charge (e+) is transferred in this way.
(14) And so defined solid state image sensor is in the scope of this patent claim.

Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

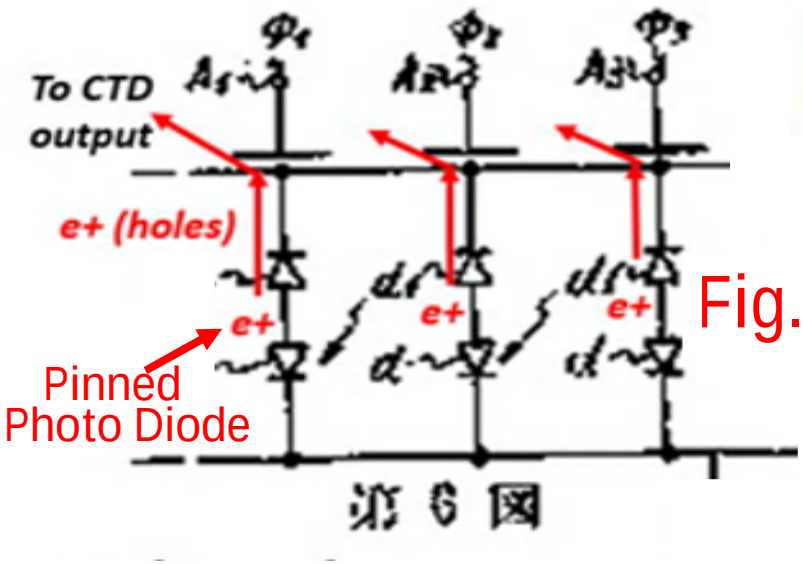
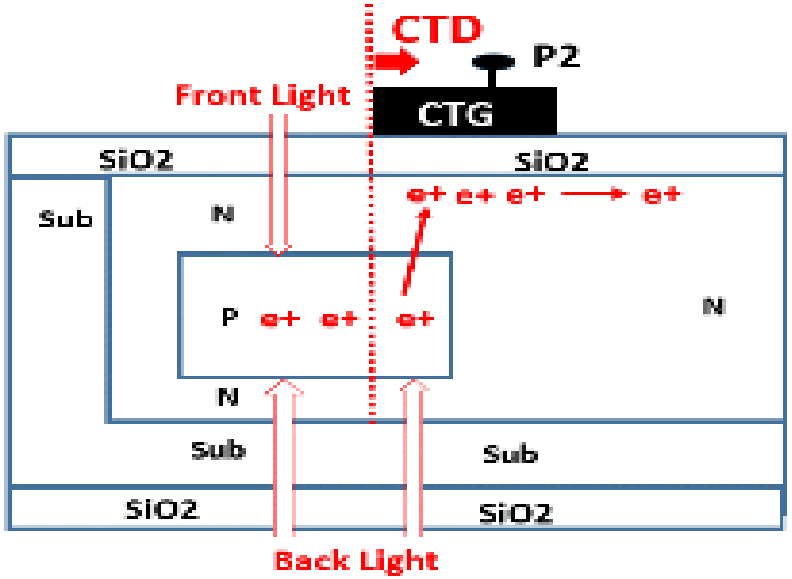


Fig.6

The Pinned Photo Diode Structure defined in this Patent Claim



File	1975-127647	Filed	1975/10/23
Public	1975-051816	Public	1977/04/26

Patent Claim in Japanese 特許請求範囲

(1)半導体基体の一方の主面側に、
(2)絶縁膜を介して電荷転送用電極が被着配列される
(3)1の導電型の転送領域が形成され、
(4)之より上記半導体基体の他方の主面側に
(5)上記転送領域に接する他の導電型の領域と
(6)該領域に接する1の導電型の領域とより成る
(7)受光領域が形成され、
(8)上記転送用電極に所要の電圧を印加することにより、
(9)上記受光領域に蓄積した電荷を上記転送領域に転送し、
(10)上記電荷転送用電極に
(11)上記所要の電圧とは異るクロック電圧を印加して
(12)上記基体の上記一方の主面に沿って
(13)電荷の転送を行うようにしたことを
(14)特徴とする固体撮像装置。

Pinned Photo Diode (NPN/Sub junction type)

English Translation of Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Patent Claim in English Translation

(1) Along the front surface of a semiconductor substrate (Nsub),
(2) the charge transfer gate (CTG) is placed upon the oxide,
(3) whereby a first region (P) is formed for charge transfer
(4) On the opposite side of this region (P),
(5) on the back side of the semiconductor substrate (Nsub),
(6) in between the region (P) for charge transfer,
(7) a base region (N) of another doping is formed.
(8) Nearby, a photo sensing region (P) is formed.
(9) By applying a proper voltage (Vbase) to the base region (N),
(10) The electronic charge (e+) ,which is stored in the photo sensing region (P),
(11) is transferred to the charge transfer region (P).
(12) By applying a proper clock pulse to the charge transfer gate (CTG),
(13) the charge is further transferred in the CTD.
(14) So defined solid state image sensor with the features described aboveis in the scope of the patent claim.

File 1975-127646 Filed 1975/10/23
Public 1975-051815 Public 1977/04/26

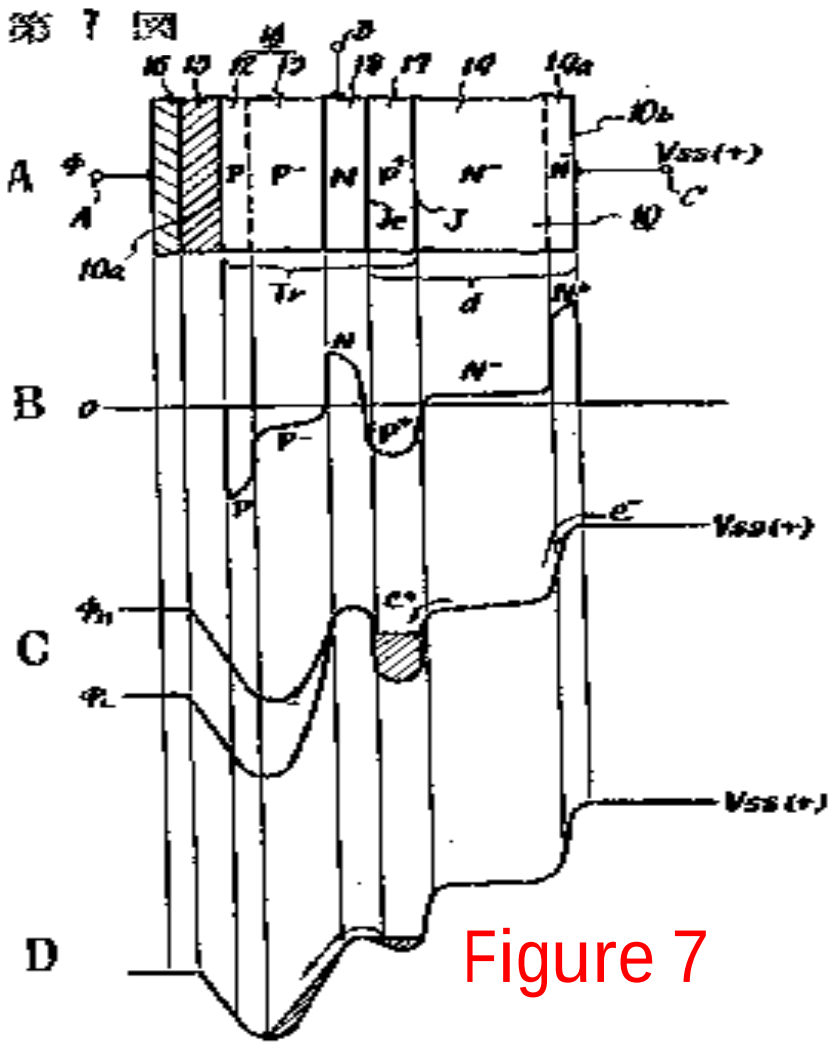


Figure 7

Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

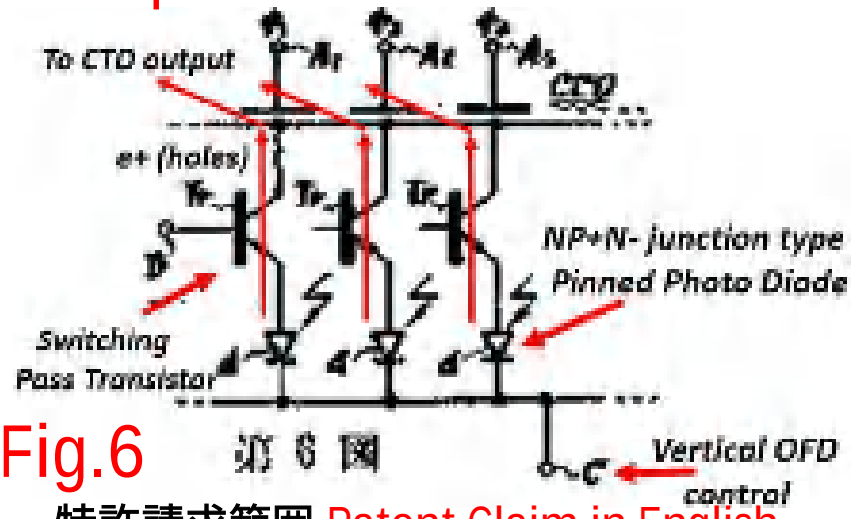
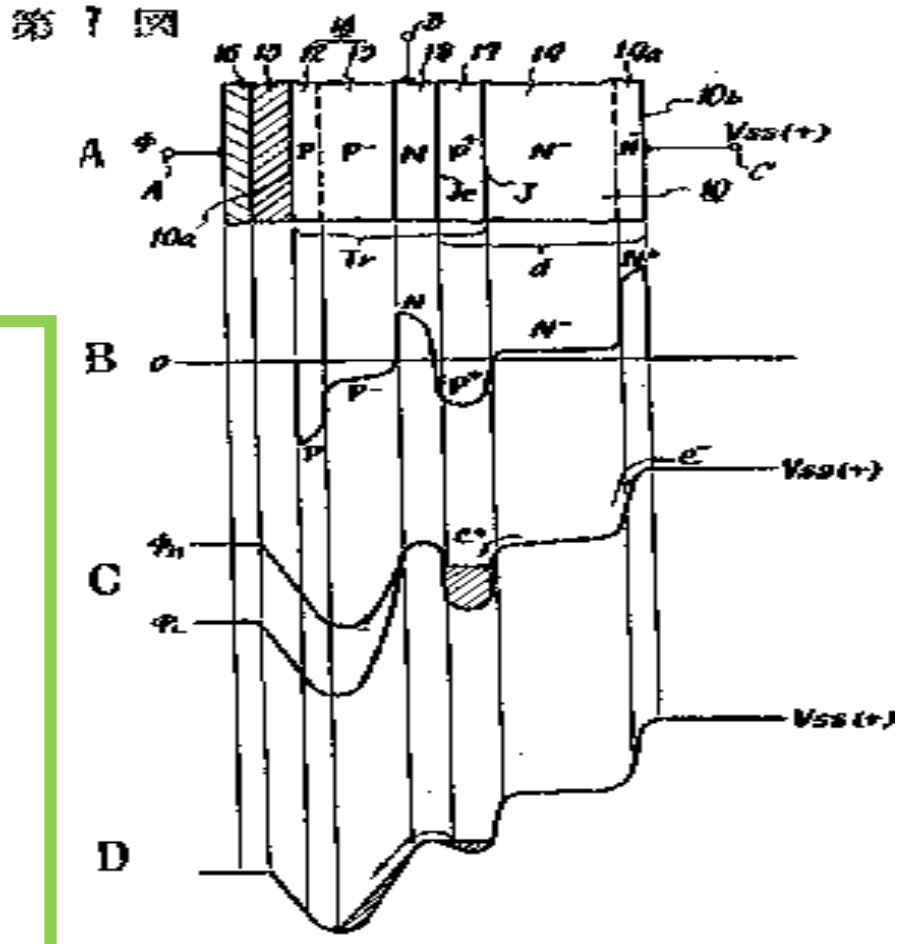


Fig.6 第 6 図

File 1975-127646 Filed 1975/10/23
Public 1975-051815 Public 1977/04/26



特許請求範囲 Patent Claim in English

(1) 半導体基体に一方の主面側に、
(2) 絶縁膜を介して電荷伝送用電極が配列される
(3) 1の導電型の転送領域が形成され、
(4) 之に対向し且つ之より
(5) 上記半導体基体の他方の主面側に
(6) 上記転送領域との間に
(7) 他の導電型のベース領域
(8) を介して受光領域が形成され、
(9) 上記ベース領域に所定電圧を印加することにより
(10) 上記受光領域に蓄積した電荷を
(11) 上記転送領域に転送し、
(12) 上記電荷転送用電極に所定のクロック電圧を印加して
(13) 電荷の転送を行うようにしたことを
(14) 特徴とする固体撮像装置

The Japanese Patent 1975-134985 shown above is the evidence to claim that the Pinned Photo Diode with the vertical overflow drain (VOD) function was invented by Yoshiaki Hagiwara. Moreover, the Japanese Patent 1975-127647 shown above is the evidence to claim also that the Pinned Photo Diode with the back light illumination scheme was also invented by Yoshiaki Hagiwara at Sony in 1975.

Yoshiaki Hagiwara, the inventor of Pinned Photo Diode