

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976

Prof. C. A. Mead and Yoshiaki Daimon Hagiwara working on the silicon chip design at Caltech in 1972

128-Bit Multicomparator

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Abstract—A 128-bit multicomparator was designed to perform the multibit function on arbitrary length data strings. Entries can be searched for longer than strings or parallel for independent, multiple operations. The circuit utilizes a 2-phase static CMOS shift register with the data handling and a unique parallel access logic circuit to accomplish the address function. The compare operation is performed by parallel between a "data" register and a "key" register with a shift "mask" register handling one's complement data decompaction. The multicomparator was fabricated using enhanced silicon-gate metal-insulator-semiconductor (MOS) technology on a $2\mu\text{m} \times 128\text{-bit}$ chip containing 2000 devices. With variable-frequency logic (VFL) logic, data rates in excess of 1.5 MHz have been achieved. The average power dissipation was 220 mW in the 0.5- μm mode and 300 mW in the 1- μm mode.

INTRODUCTION

OVER the past several years, there have been significant advances of energy devoted to the fabrication of large and faster semiconductor memories and conventional central processing units (CPU's) in silicon form. In the process, more vital applications of large-scale integration (LSI) to computer architecture have been neglected [1]. LSI has increased the technological distinction between logic and memory. It is now economically feasible to decentralize the CPU of a computer by replacing much of its traditional silicon with functional hardware to improve system efficiency. Presently, an increasing amount of processing time is spent on organizing and accessing data in programs. People who are usually controlled directly by the CPU and have little or no associated logic of their own. A good improvement in this situation can be made by developing peripheral logic units. This would allow each peripheral to accomplish its own internal processing and thus reduce CPU bus-wiring delays. This paper describes a 128-bit multicomparator that is designed to perform the search-sort function.

The block diagram of the multicomparator is shown in Fig. 1. The circuit consists of three independently clocked static CMOS shift registers with associated exclusive-or gates. In operation, the device indicates a match between the data word and the extended bits of the key word. The multicomparator is loaded with a key word by initially shifting the word into the top register and loading the register in static mode. While the key word is being loaded, the comparator is enabled by entering zero's in the appropriate locations of the

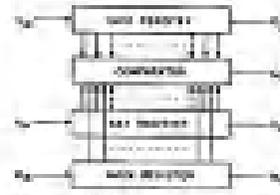


Fig. 1. Block diagram of multicomparator.

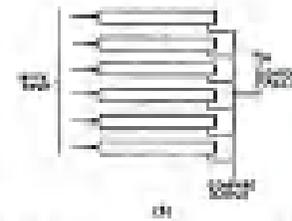


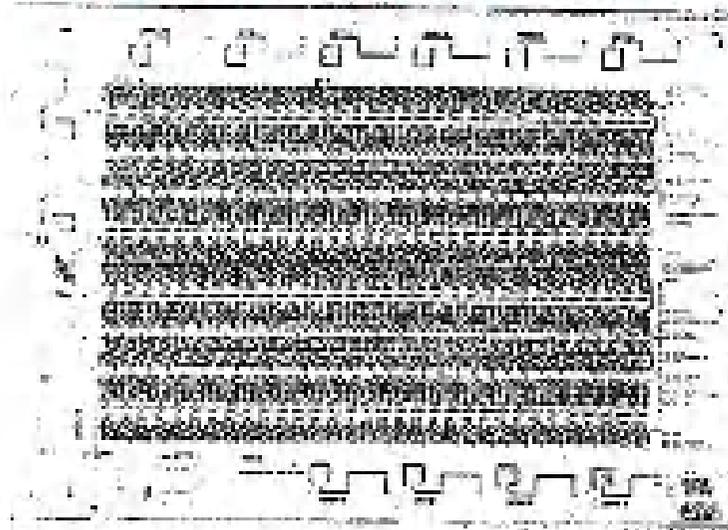
Fig. 2. Parallel structure of multicomparator: (a) Cascaded; (b) Bit-parallel, word-wide.

mask register. Loading (clears the multicomparator to search for the string of varying length and composition. For example, assume it is necessary to search for all words containing a specific 111-bit code. By entering the 111-bit code in the key register and masking out the rest of the comparator, the multicomparator is configured to search for that code wherever it occurs in the data file. Once the multicomparator is loaded with "key" and "mask" words, the file being searched is serially shifted through the data register. The data words are compared in bit parallel with the extended bits of the key word as they pass through the data register. When a match is found, the compare output goes high.

Logic multicomparators can be constructed of the 128-bit circuit. Cascaded [Fig. 2(a)], the comparator can be used to search for words longer than 128 bits. By implementing multicomparators in parallel [Fig. 2(b)], a word-wide, bit-parallel



128-bit Multicomparator chip, designed by Hagiwara in 1972-1973 and fabricated by Intel PMOS process.



Manuscript received July 17, 1976; revised July 18, 1976.
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*Formerly Associate (1972-73), Prof. (1973-74), and (1974-75) with the Intel Corp. It appears the p-channel MOS can provide for better multicomparator logic. 128-bit logic may be made and have greater yield by depending on the processing used.

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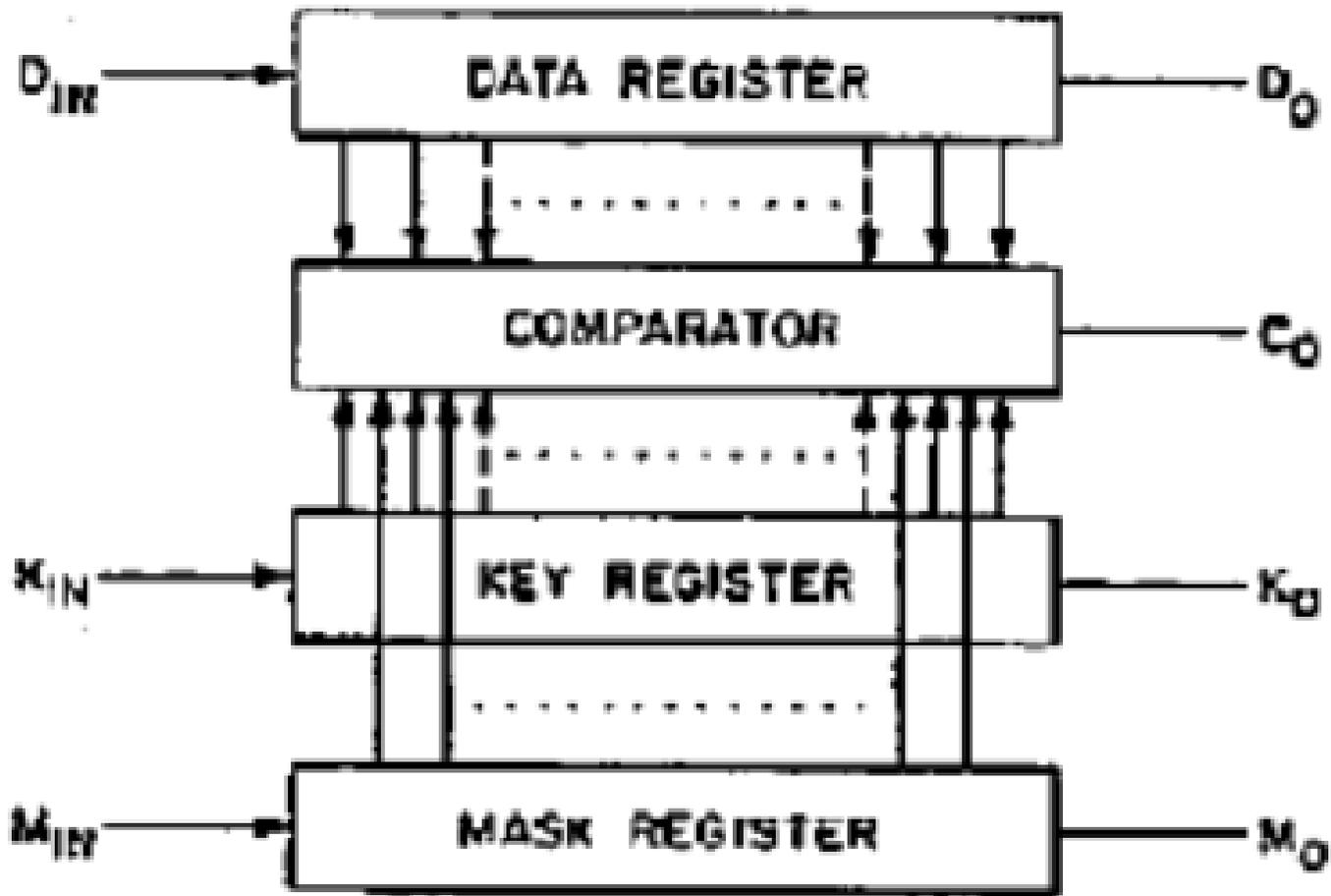
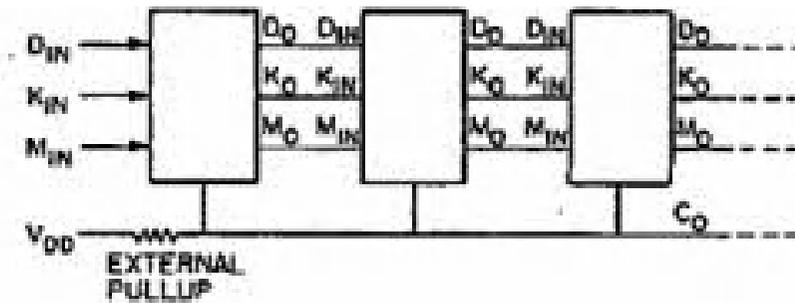


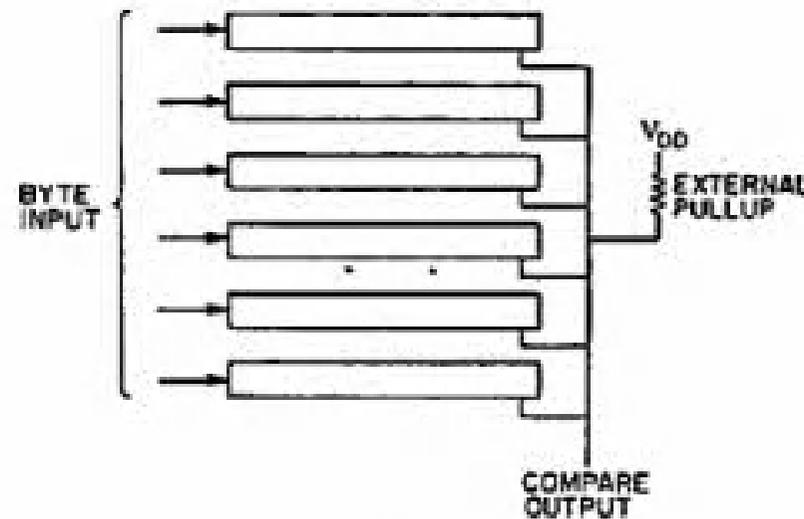
Fig. 1. Block diagram of multicomparator.

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(a)



(b)

Fig. 2. Possible connections of multicomparator. (a) Cascaded. (b) Bit-parallel, word-serial.

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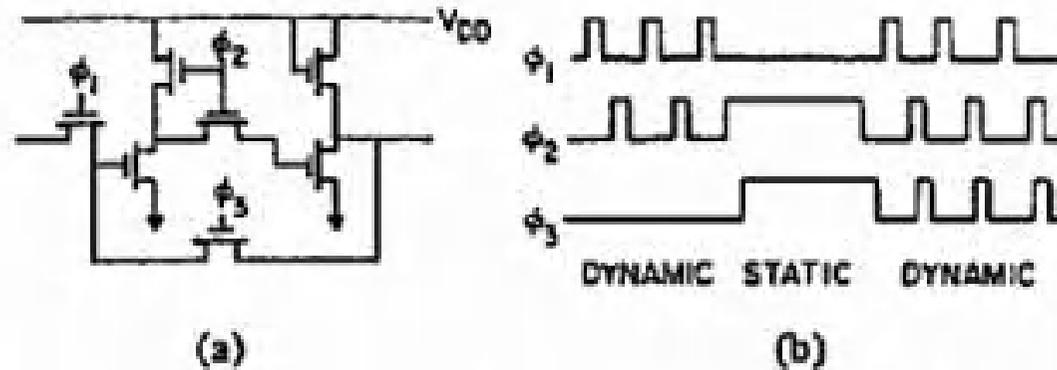


Fig. 3. Basic shift register cell. (a) Schematic. (b) Clock timing.

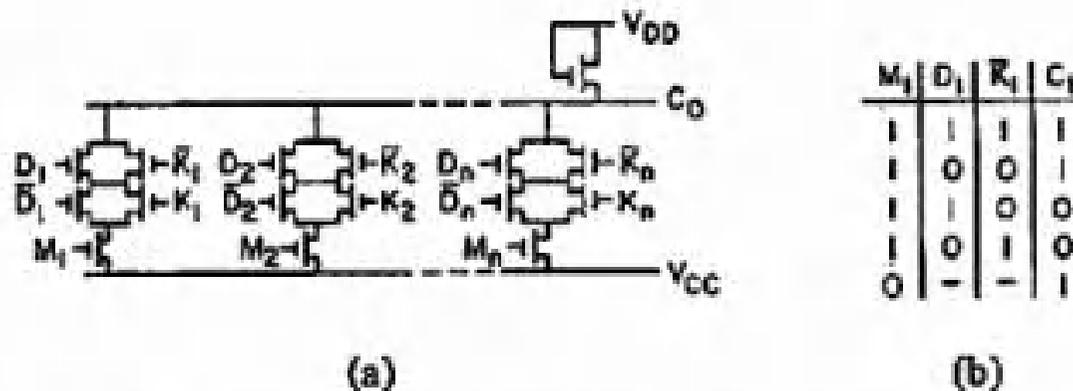


Fig. 4. Gated EXCLUSIVE-NOR gate. (a) Schematic. (b) Truth table.

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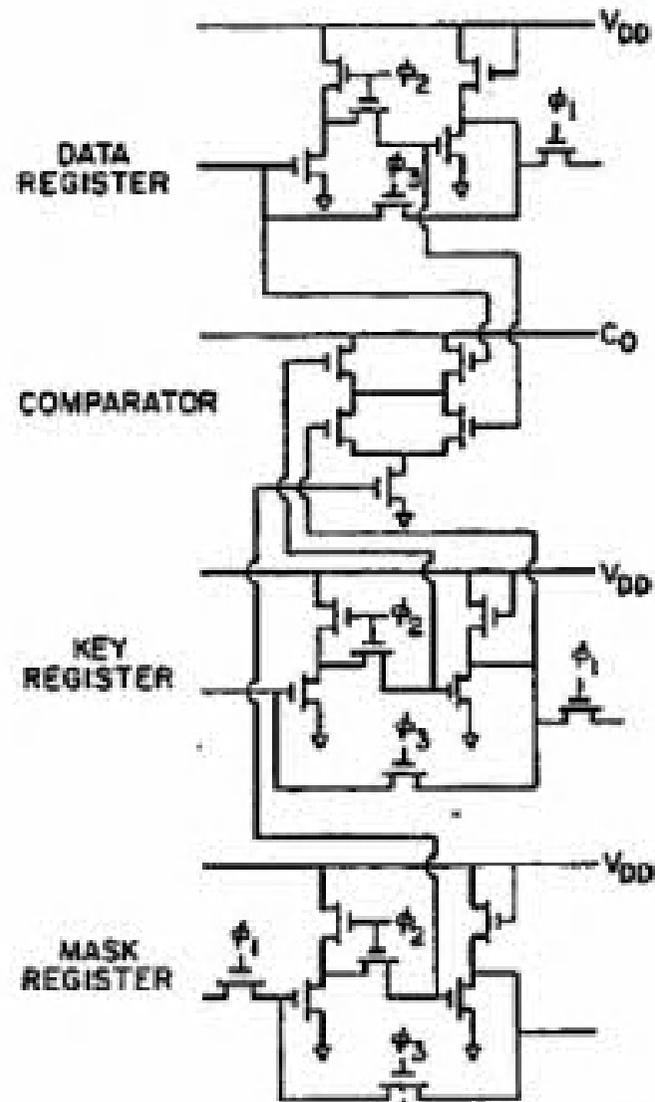


Fig. 5. Full schematic of one bit slice of the multicomparator.

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*serial-in/serial-out fast 128 bit parallel data comparator chip
fabricated by Intel corporation p-channel E/D MOS fabrication line*

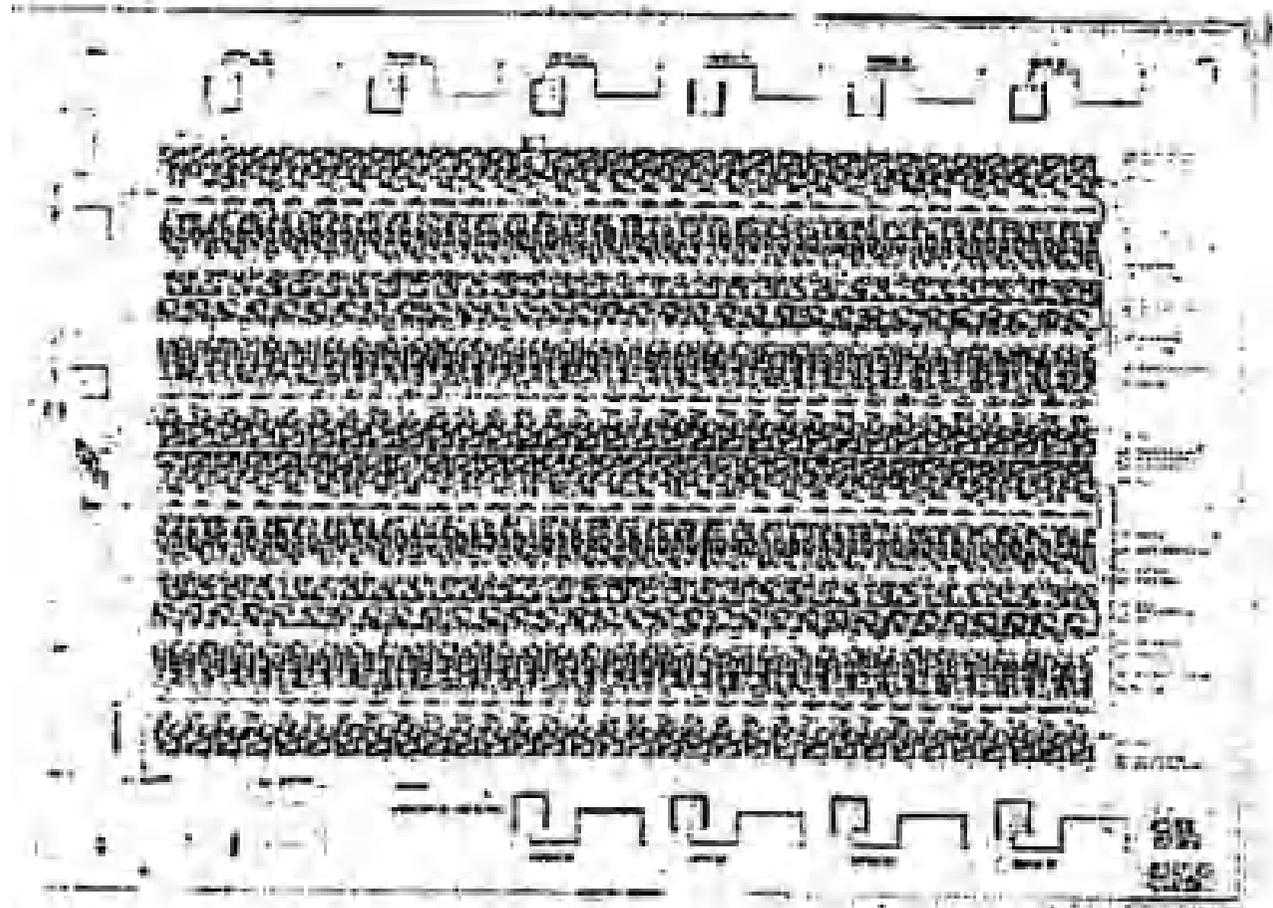


Fig. 6. Photomicrograph of multicomparator chip.

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TABLE I

Parameter	Performance ^a
Clock rate	0.0001-2 MHz
Dynamic supply current	25 mA
Static supply current	30 mA
Clock leakage current (ϕ_1)	120 nA
Clock leakage current (ϕ_2)	300 nA
Clock capacitance (ϕ_1)	40 pF
Clock capacitance (ϕ_2)	60 pF
Clock capacitance (ϕ_3)	40 pF
Interclock capacitance	7 pF
Input capacitance	10 pF
Output capacitance	10 pF

^aTest Conditions:

$$T = 23^\circ\text{C}, V_{CC} = 5\text{ V}, V_{DD} = -5\text{ V},$$

$$V_{\phi L} = +5\text{ V}, V_{\phi H} = -5\text{ V}, V_{\text{input}} = 0.5\text{ V}.$$

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Dr. Lee Barton at Hewlett-Packard
Caltech Graduate, 1973



Lee D. Barton received the B.S.E.E. degree from the California Institute of Technology, Pasadena, in 1973.

He then invented and marketed a computer-aided memory for theater lighting control, and now works for Hewlett-Packard Laboratories, Cupertino, CA, designing and testing LSI integrated circuits for mini-computers.

Dr. Yoshiaki Hagiwara at Sony
Caltech Graduate, 1975



Yoshiaki Hagiwara was born in Kyoto, Japan, on July 4, 1948. He received the B.S., M.S., and Ph.D. degrees from the California Institute of Technology, Pasadena, in 1971, 1972, and 1975, respectively.

Since 1967, he has served several research groups in the Institute. He worked as a Data Professor in hydrodynamics from 1967 to 1969, engaging in the analysis of the pressure distribution of solitary waves, the influence of the geological features of a harbor upon the forced standing-wave amplitude in the harbor, and the diffusion mechanism of polluted objects in moving fluids. From 1969 to 1971, he worked as an Experimentalist in the Material Science Department and studied the switching and other electronic properties of newly developed amorphous alloys from the low temperature of 4 K to room temperature. From 1971 to 1975 he was a Research and Teaching Assistant both in the Electrical Engineering and Physics Departments at the California Institute of Technology. In the summer of 1971 and 1973, he visited Sony Corporation, Tokyo, Japan, as a Product-Appraisal Engineer at the Asoji plant and engaged in developments and applications of bipolar technologies in video and power integrated circuits. He is presently with the Sony Corporation, Tokyo, Japan. His interests lie in the areas of digital and linear integrated circuit design, the physics of microelectronics, and artificial intelligence.



Prof. C.A.Mead at Caltech



Carver A. Mead received the B.S., M.S., and Ph.D. degrees from the California Institute of Technology, Pasadena, in 1959, 1961, and 1963, respectively.

He has been a member of the faculty of the California Institute of Technology, Pasadena, CA, since 1957. His research interests are in the understanding of current flow mechanisms in thin, metal-semiconductor films, metal-semiconductor junctions in amorphous materials, and the design and fabrication of a number of new solid-state electronic devices and integrated circuits.

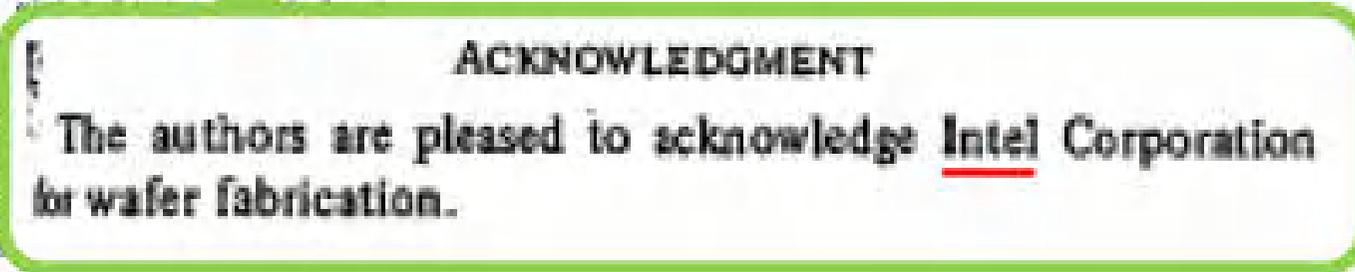
Dr. Mead is a Fellow of the American Physical Society and a member of the American Nuclear Society.

Dr. Richard Pashley at Intel
Caltech Graduate, 1974



Richard D. Pashley OM received the B.S. degree from the University of Virginia, VA, on September 1947. He is currently a member of the faculty of the California Institute of Technology, Pasadena, CA.

Dr. Pashley is a member of the American Physical Society and the American Nuclear Society.



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