# ２入力１出力論理ゲート　in2GateG( )回路の動作説明


特別なGate名

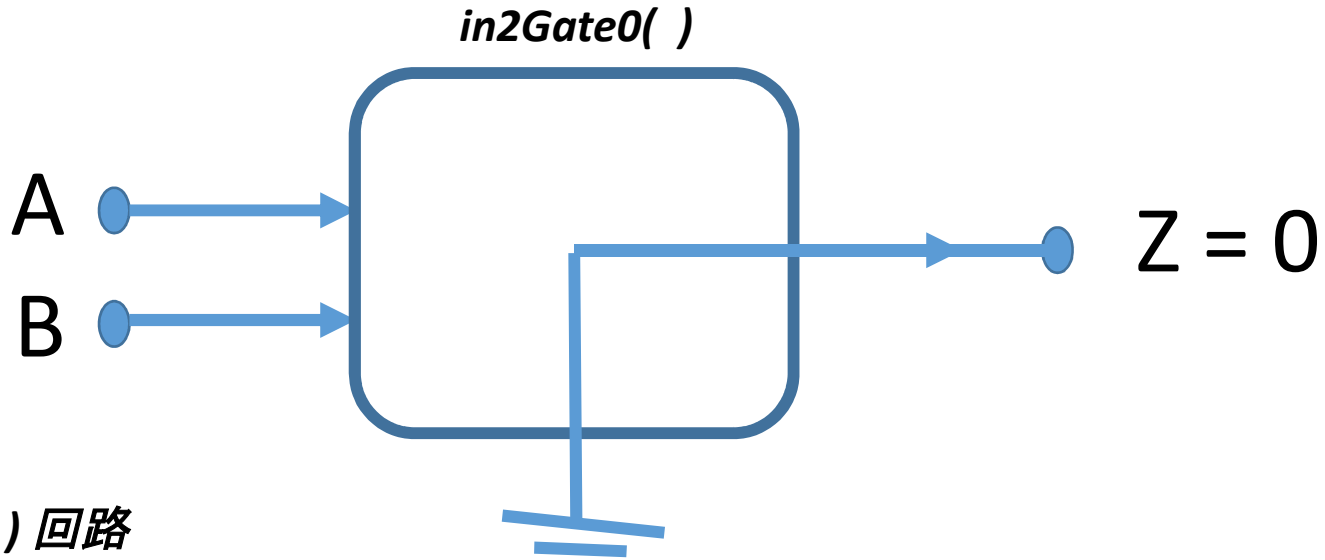
in2Gate1 ( ) = AND( ) ;
in2Gate6( ) = EXOR( ) ;
in2Gate7( ) = OR( ) ;
in2Gate8( ) = NOR( ) ;
in2Gate9( ) = EXNOR( ) ;
in2GateE( ) = NAND( ) ;

**( G = 0 to F )**

16個ある　in2GateG ( ) 回路　の番号と出力値　Z ( A, B )

| A | B | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

# ２入力１出力論理ゲート　in2Gate0( )回路の動作説明




*in2Gate0( ) 回路*

| A | B | Z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

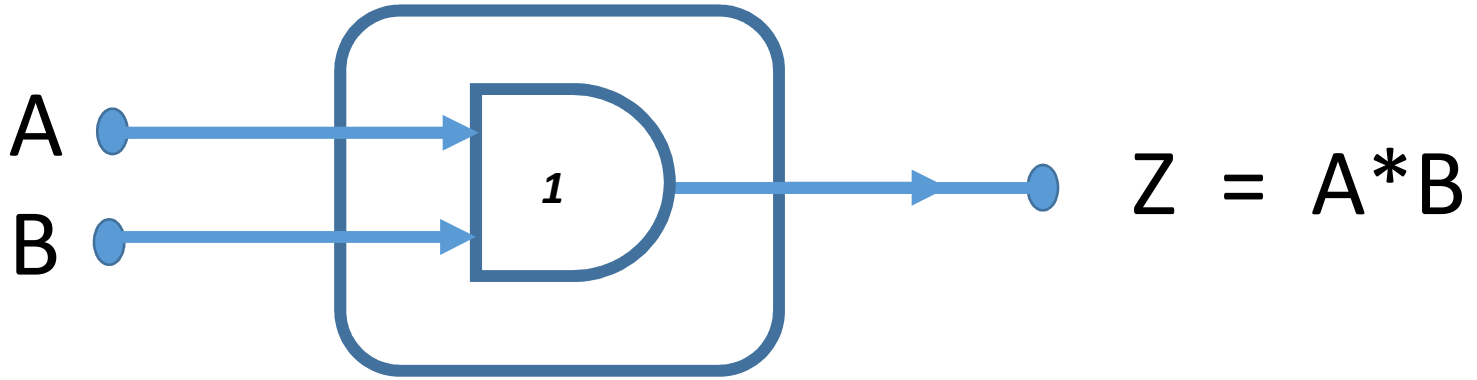
*DCDL Code for in2Gate0( ) 回路*

```
define  in2Gate0( )  {  input  A, B ;  output  Z ;
                        Z = 0 ;  }
```

$(0)_{10} = (0000)_2 = (0)_{16}$

# ２入力１出力論理ゲート　in2Gate1( )回路の動作説明

*in2Gate1( ) = AND( )*




*in2Gate1( ) 回路*

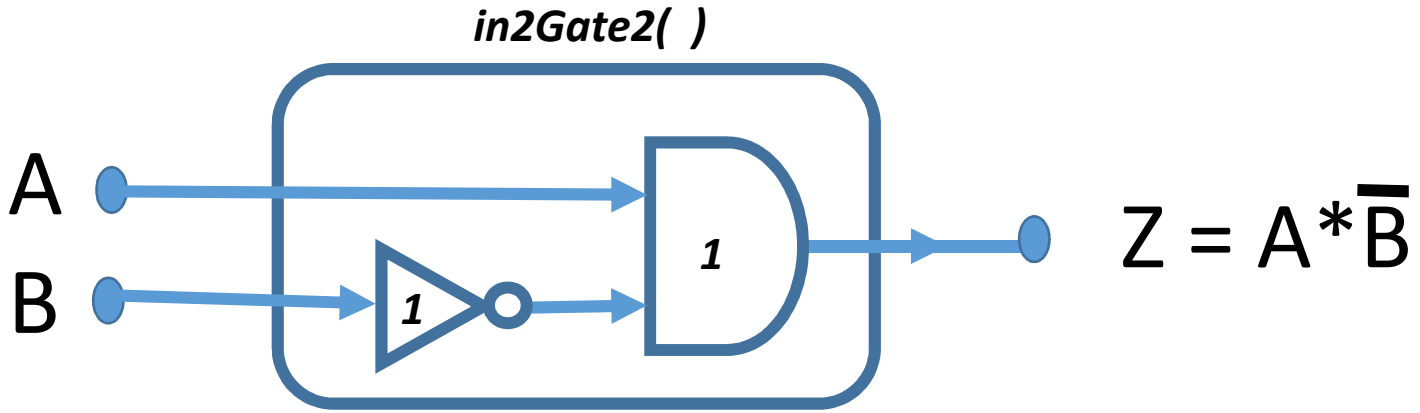
| A | B | Z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

*DCDL Code for in2Gate1( ) 回路*

```
define  in2Gate1( ) { input A, B ; output Z ;
                      memory ZZ ;
                      Z = ZZ ;
                      ZZ= A*B ; }
```

$(1)_{10} = (0001)_2 = (1)_{16}$

# ２入力１出力論理ゲート　in2Gate2( )回路の動作説明




*in2Gate2( ) 回路*

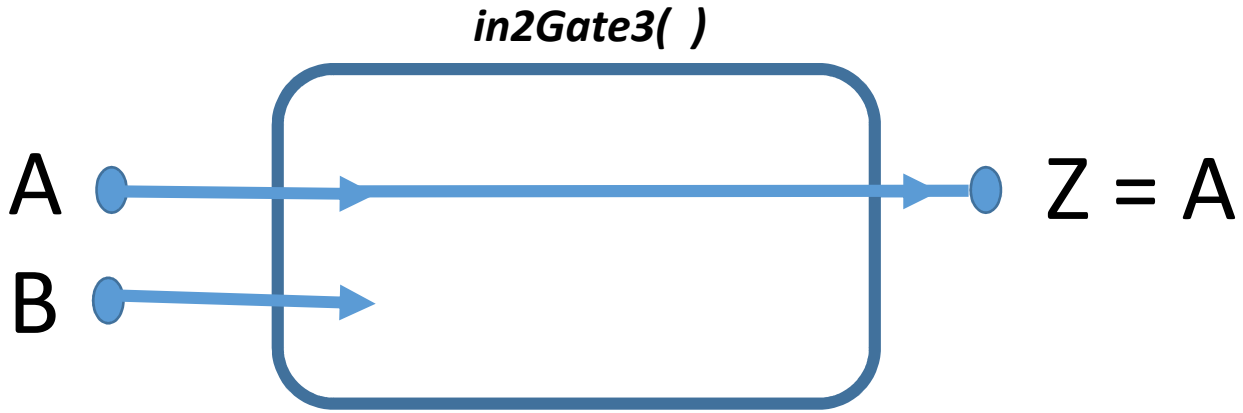
| A | B | Z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

*DCDL Code for in2Gate2( ) 回路*

```
define  in2Gate2( ) { input A, B ; output Z ;
                      memory ZZ ;
                      Z = ZZ ;
                      ZZ= A*(1 – B ) ; }
```

$(2)_{10} = (0010)_2 = (2)_{16}$

# ２入力１出力論理ゲート　in2Gate3( )回路の動作説明




*in2Gate3( ) 回路*

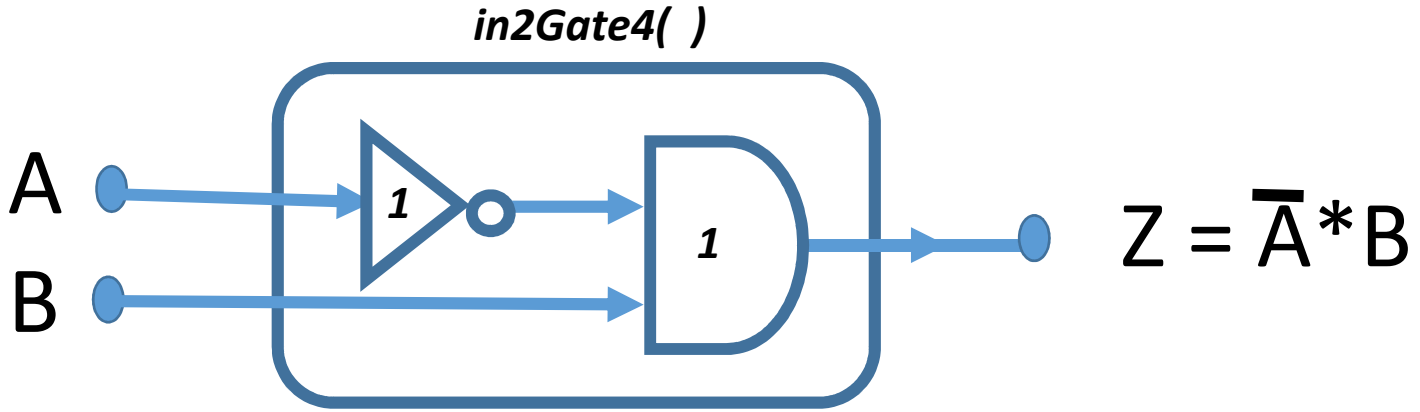
| A | B | Z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

*DCDL Code for in2Gate3( ) 回路*

```
define  in2Gate3( ) { input A, B ; output Z ;
                      memory ZZ ;
                      Z = ZZ ;    ZZ= A ; }
```

$$(3)_{10} = (0011)_2 = (3)_{16}$$

# ２入力１出力論理ゲート　in2Gate4( )回路の動作説明




*in2Gate4( ) 回路*

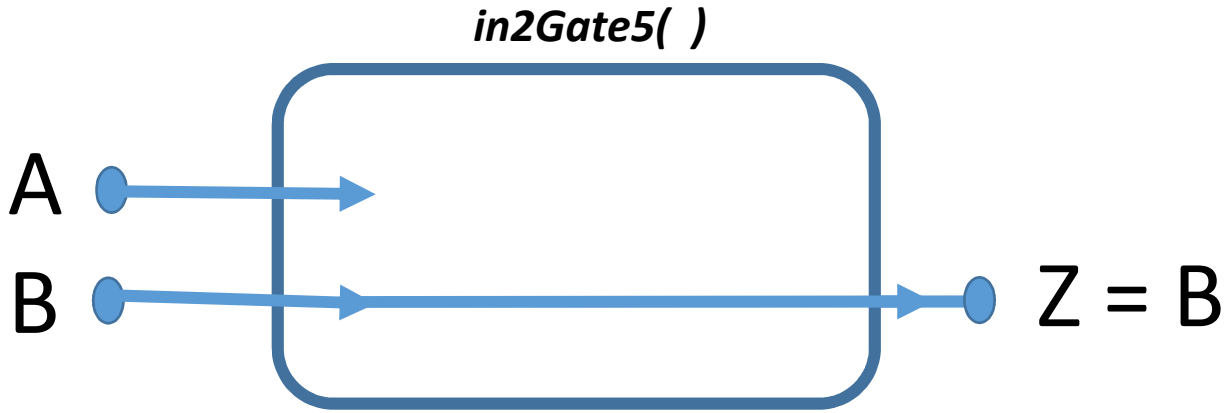
| A | B | Z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

*DCDL Code for in2Gate4( ) 回路*

```
define   in2Gate4( )  { input  A, B ;  output  Z  ;

                        memory  ZZ  ;

                        Z = ZZ ;

                        ZZ= (1 – A ) *B   ;  }
```

$(4)_{10} = (0100)_2 = (4)_{16}$

# ２入力１出力論理ゲート　in2Gate5( )回路の動作説明




*in2Gate5( ) 回路*

| A | B | Z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

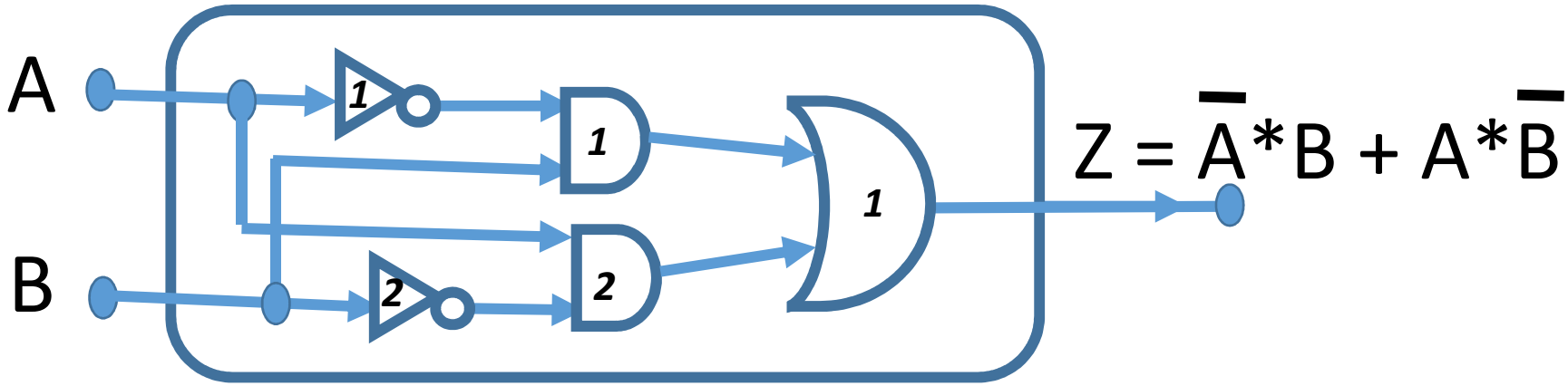
*DCDL Code for in2Gate5( ) 回路*

```
define  in2Gate5( ) { input A, B ; output Z ;
                      memory ZZ ;
                      Z = ZZ ;
                      ZZ= B ; }
```

$(5)_{10} = (0101)_2 = (5)_{16}$

# 2入力1出力論理ゲート　in2Gate6( )回路の動作説明

*in2Gate6( )=EXOR( )*




*in2Gate6( ) 回路*

| A | B | Z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

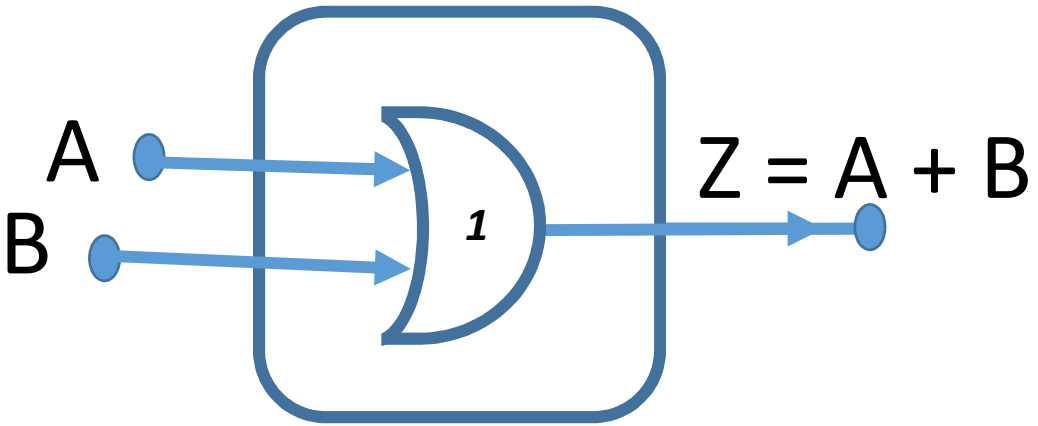
*DCDL Code for in2Gate6( ) 回路*

```
define  in2Gate6( )  { input  A, B ;  output  Z  ;
                       memory  ZZ  ;
                       Z = ZZ ;
                       ZZ=( 1 – A) *B + A*(1 – B) ;  }
```

$(6)_{10} = (0110)_2 = (6)_{16}$

# ２入力１出力論理ゲート　in2Gate7( )回路の動作説明

*in2Gate7( )=OR( )*




*in2Gate7( ) 回路*

| A | B | Z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

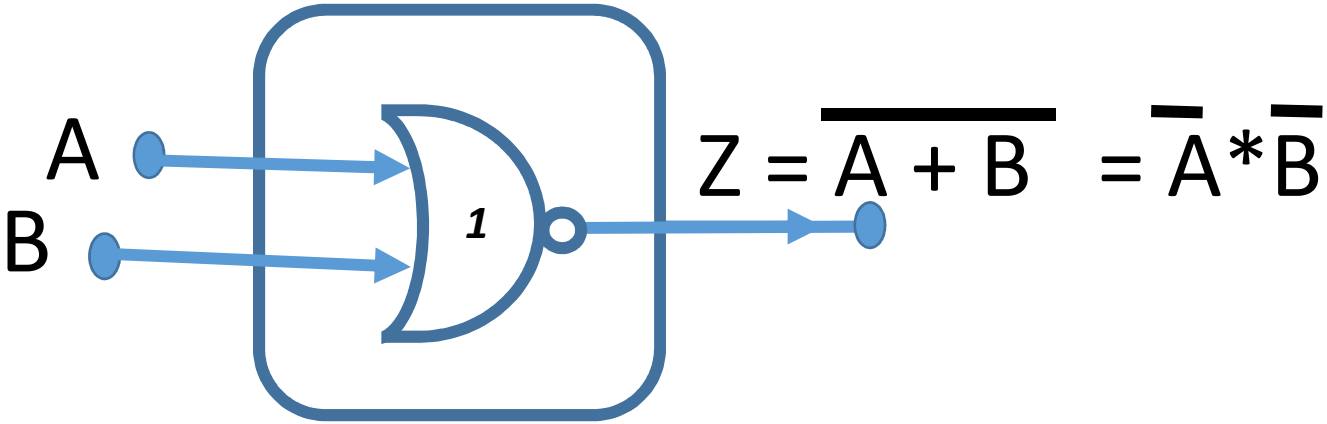
*DCDL Code for in2Gate7( ) 回路*

```
define  in2Gate7( )  { input  A, B ;  output  Z  ;

                       memory  ZZ  ;

                       Z = ZZ ;

                       ZZ= A + B – A*B  ;  }
```

$(7)_{10} = (0111)_2 = (7)_{16}$

# ２入力１出力論理ゲート　in2Gate8( )回路の動作説明

*in2Gate8( )=NOR( )*




*in2Gate8( ) 回路*

| A | B | Z |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

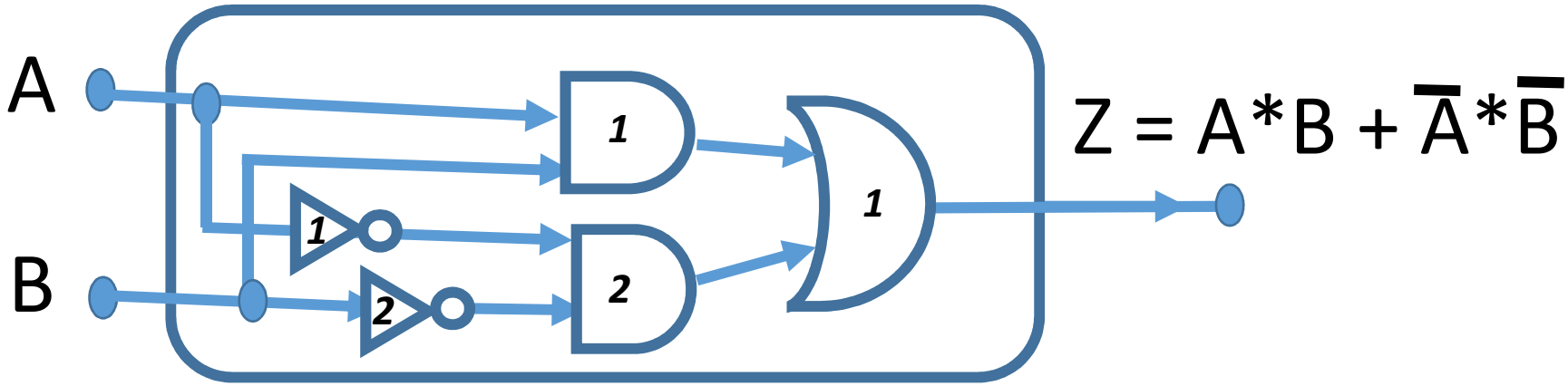
*DCDL Code for in2Gate8( ) 回路*

```
define  in2Gate8( )  { input  A, B ;  output  Z  ;
                       memory  ZZ  ;
                       Z = ZZ ;
                       ZZ= (1 – A )*(1 – B ) ;  }
```

$(8)_{10} = (1000)_2 = (8)_{16}$

# ２入力１出力論理ゲート　in2Gate9( )回路の動作説明

*in2Gate9( )=EXNOR( )*




*in2Gate9( ) 回路*

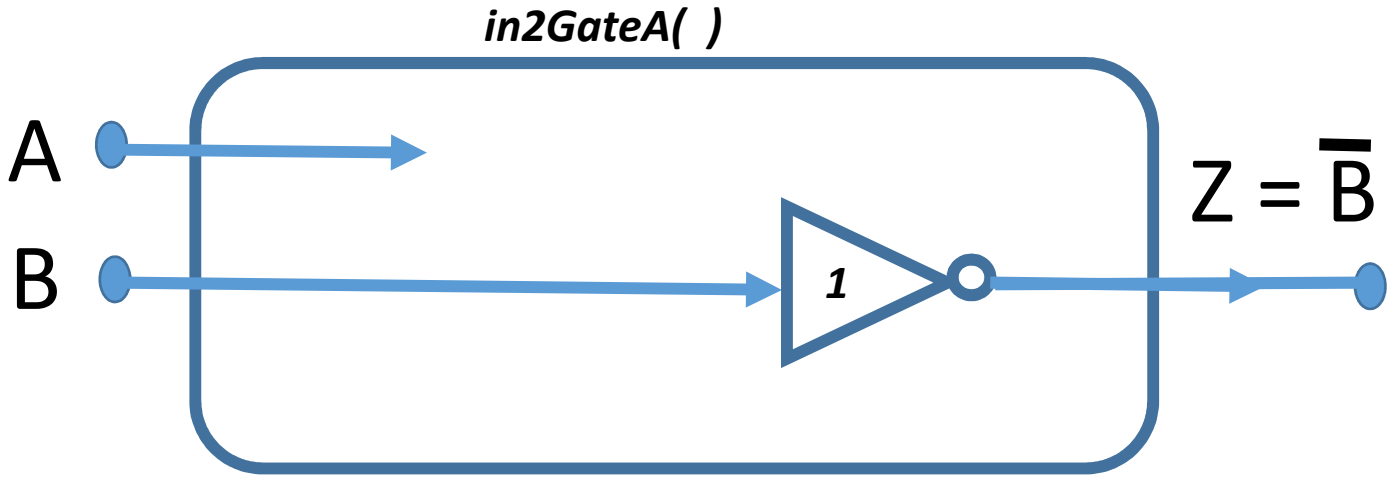
| A | B | Z |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

*DCDL Code for in2Gate9( ) 回路*

```
define  in2Gate9( )  { input  A, B ;  output  Z  ;
                       memory  ZZ  ;
                       Z = ZZ ;
                       ZZ= A*B + ( 1 – A)*(1 – B ) ;  }
```

$(9)_{10} = (1001)_2 = (9)_{16}$

# ２入力１出力論理ゲート　in2GateA( )回路の動作説明




in2GateA( ) 回路

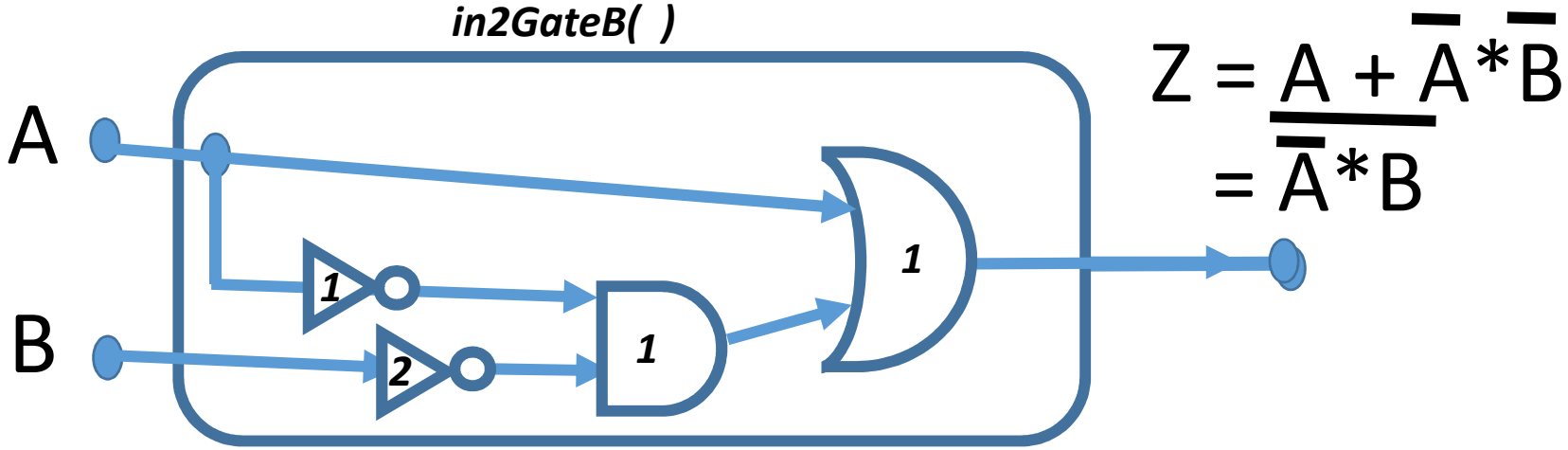
| A | B | Z |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

DCDL Code for in2GateA( ) 回路

```
define  in2GateA( ) { input A, B ; output Z ;
                      memory ZZ ;
                      Z = ZZ ;
                      ZZ= 1 – B ; }
```

$(10)_{10} = (1010)_2 = (A)_{16}$

# ２入力１出力論理ゲート　in2GateB( )回路の動作説明




in2GateB( ) 回路

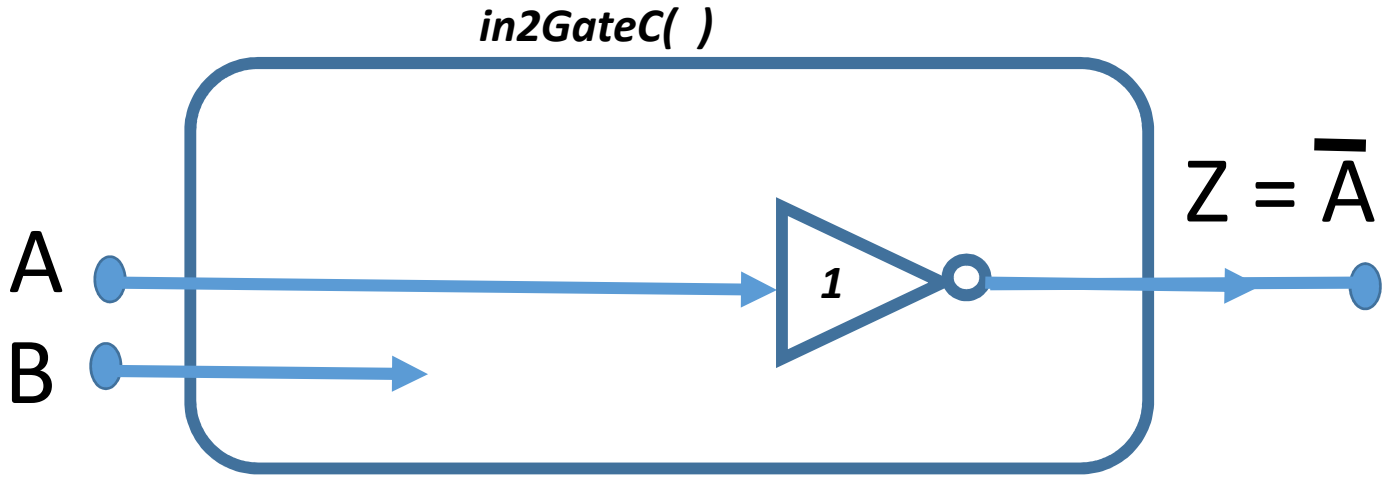
| A | B | Z |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

DCDL Code for in2GateB( ) 回路

```
define  in2GateB( ) { input A, B ; output Z ;
                      memory ZZ ;
                      Z = ZZ ;
                      ZZ= A + (1 – A) *(1 – B) ; }
```

$(11)_{10} = (1011)_2 = (B)_{16}$

# ２入力１出力論理ゲート　in2GateC( )回路の動作説明




in2GateC( ) 回路

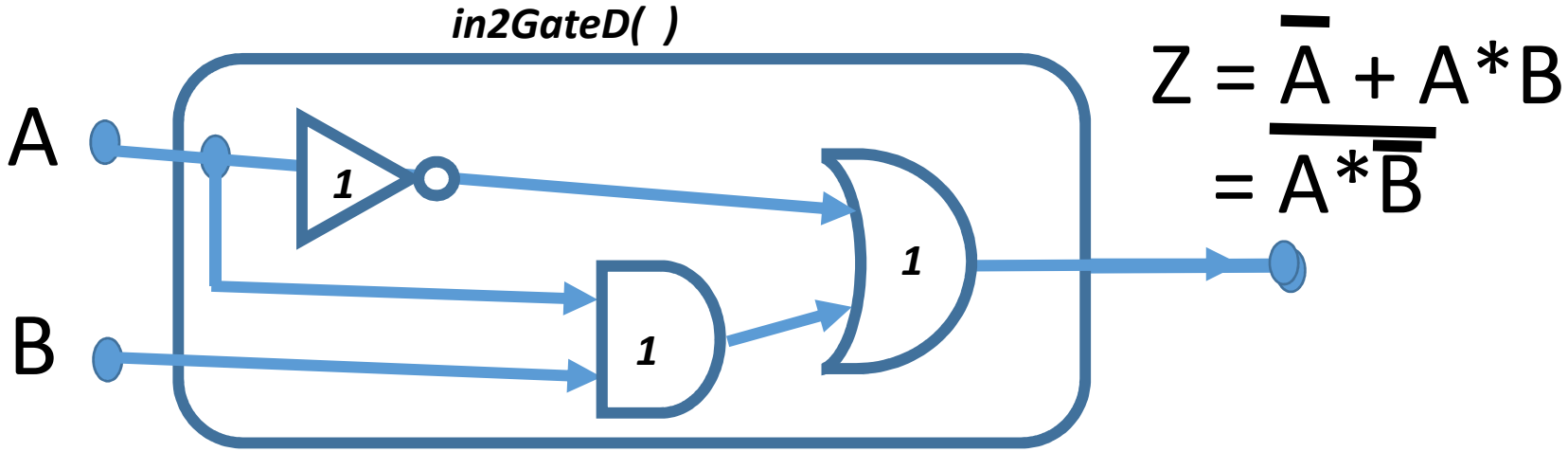
| A | B | Z |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

DCDL Code for in2GateC( ) 回路

```
define  in2GateC( ) { input A, B ; output Z ;
                      memory ZZ ;
                      Z = ZZ ;
                      ZZ= 1 – A ; }
```

$(12)_{10} = (1010)_2 = (C)_{16}$

# ２入力１出力論理ゲート　in2GateD( )回路の動作説明




in2GateD( ) 回路

| A | B | Z |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

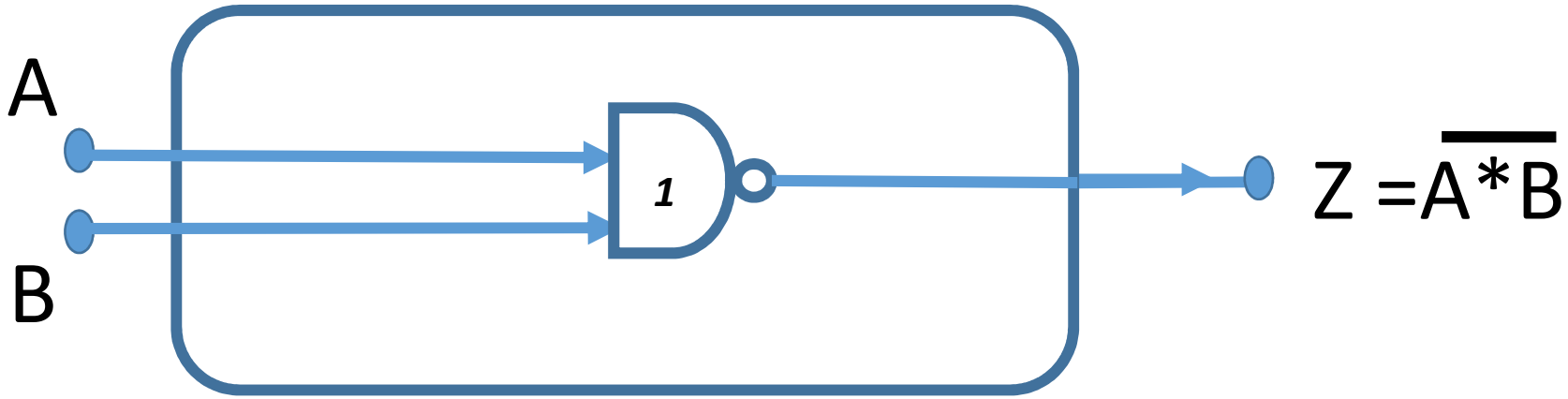
DCDL Code for in2GateD( ) 回路

```
define  in2GateD( ) { input A, B ; output Z ;
                      memory ZZ ;
                      Z = ZZ ;
                      ZZ=(1 – A) + A*B ; }
```

$(13)_{10} = (1101)_2 = (D)_{16}$

# ２入力１出力論理ゲート　in2GateE( )回路の動作説明

*in2GateE( )=NAND( )*




*in2GateE( ) 回路*

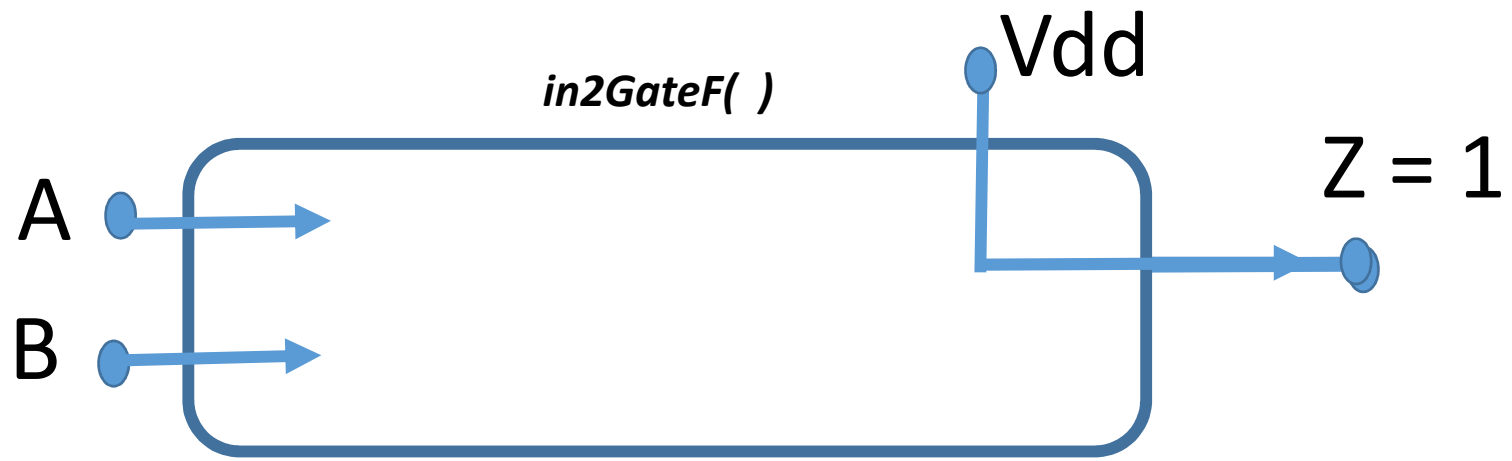
| A | B | Z |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

*DCDL Code for in2GateE( ) 回路*

```
define  in2GateE( ) { input A, B ; output Z ;
                      memory ZZ ;
                      Z = ZZ ;
                      ZZ=(1 – A*B) ; }
```

$(14)_{10} = (1110)_2 = (E)_{16}$

# ２入力１出力論理ゲート　in2GateF( )回路の動作説明




*in2GateF( ) 回路*

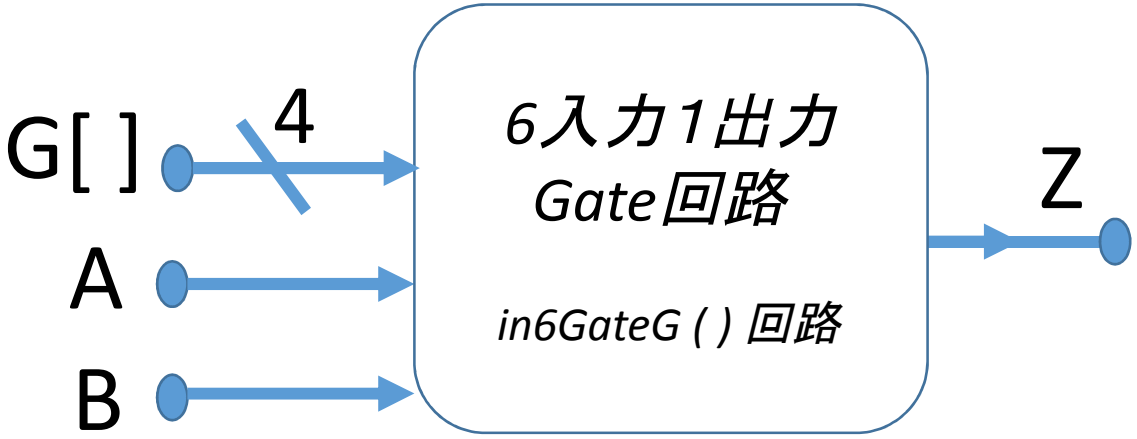
| A | B | Z |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

*DCDL Code for in2GateF( ) 回路*

```
define  in2GateE( )  {  input  A, B ;  output Z;
                         Z = 1;   }
```

$(15)_{10} = (1111)_2 = (F)_{16}$

# 6入力1出力論理ゲート　in4GateG( )回路の動作説明




```
in2Gate1 ( ) = AND(  ) ;
in2Gate6( ) = EXOR( ) ;
in2Gate7( ) = OR( ) ;
in2Gate8( ) = NOR( ) ;
in2Gate9( ) = EXNOR( ) ;
in2GateE( ) = NAND( ) ;
```

| G[ ] | G[3] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | G[2] | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| | G[1] | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| | G[0] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| A | B | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |